LCD Segment Driver series

For 200 Segment type LCD
LCD Segment Driver
BU9794KV, BU9799KV

● Outline

This is LCD segment driver for 200 segment type display. There is a lineup which is suitable for multi function display and is integrated display RAM and power supply circuit for LCD driving with 4 common output type: BU9794KV and BU9799KV.

○ 200Segment (50SEG×4COM) Driver BU9794KV ·····P.1
○ 200Segment (50SEG×4COM) Driver BU9799KV ·····P.11

BU9794KV 200Segment (50SEG×4COM) Driver

● Feature (BU9794KV)

1) 3wire serial interface (CSB, SD, SCL)
2) Integrated RAM for display data (DDRAM) : 50 × 4bit (Max 200 Segment)
3) LCD driving port: 4 Common output, 50 Segment output
4) Display duty: 1/4 duty
5) Integrated Buffer AMP for LCD driving power supply
6) 1/2bias, 1/3bias selectable
7) No external components
8) Low power/ Ultra low power consumption design: +2.5～5.5V
9) Independent power supply circuit for LCD driving

● Uses (BU9794KV)

Telephone, FAX, Portable equipment (POS, ECR, PDA etc.),
DSC, DVC, Car audio, Home electrical appliance, Meter equipment etc.

● Absolute Maximum Ratings (Ta=25degree, VSS=0V) (BU9794KV)

Parameter	Symbol	Limits	Unit	Remarks
Power Supply Voltage1	VDD	-0.5 ～ +7.0	V	Power supply
Power Supply Voltage2	VLCD	-0.5 ～ +7.0	V	LCD drive voltage
Allowable loss	Pd	0.75	W	When use more than Ta=25°C, subtract 7.5mW per degree.
Input voltage range	VIN	-0.5 ～ VDD+0.5	V	
Operational temperature range	Topr	-40 ～ +85	degree	
Storage temperature range	Tstg	-55 ～ +125	degree	

*This product is not designed against radioactive ray.

● Recommend operating conditions (Ta=25degree, VSS=0V) (BU9794KV)

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Power Supply Voltage1	VDD	2.5	-	5.5	V	Power supply
Power Supply Voltage2	VLCD	2.5	-	5.5	V	LCD drive voltage

● Electrical Characteristics (BU9794KV)

DC Characteristics (VDD=2.5～5.5V, VLCD=2.5～5.5V, VSS=0V, Ta=-40～85degree, unless otherwise specified)

Parameter		Symbol	Limit			Unit	Condition
			MIN	TYP	MAX		
"H" level input voltage		VIH	0.8VDD	-	VDD	V	SD,SCL,CSB
"L" level input voltage		VIL	VSS	-	0.2VDD	V	SD,SCL,CSB
"H" level input current		IIH	-	-	1	uA	SD,SCL,CSB
"L" level input current		IIL	-1	-	-	uA	SD,SCL,CSB
LCD Driver on resistance	SEG	RON	-	3.5	-	kΩ	Iload=±10uA
	COM	RON	-	3.5	-	kΩ	
Standby current		Ist	-	-	5	uA	Display off, Oscillation off
Power consumption 1		IDD	-	5	15	uA	VDD=3.3V, VLCD=5V, Ta=25degree Power save mode1, FR=70Hz 1/3 bias, Frame inverse
Power consumption 2		ILCD	-	10	20	uA	VDD=3.3V, VLCD=5V, Ta=25degree Power save mode1, FR=70Hz 1/3 bias, Frame inverse

Oscillation Characteristics (VDD=2.5～5.5V, VLCD=2.5～5.5V, VSS=0V, Ta=-40～85degree, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Frame frequency	fCLK	68	80	92	Hz	FR = 80Hz setting VDD=3.3V

MPU interface Characteristics (VDD=2.5～5.5V, VLCD=2.5～5.5V, VSS=0V, Ta=-40～85degree, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN.	TYP.	MAX.		
Input rise time	tr	-	-	80	ns	
Input fall time	tf	-	-	80	ns	
SCL cycle time	tSCYC	400	-	-	ns	
"H" SCL pulse width	tSHW	100	-	-	ns	
"L" SCL pulse width	tSLW	100	-	-	ns	
SD setup time	tSDS	20	-	-	ns	
SD hold time	tSDH	50	-	-	ns	
CSB setup time	tCSS	50	-	-	ns	
CSB hold time	tCSH	50	-	-	ns	
"H" CSB pulse time	tCHW	50	-	-	ns	

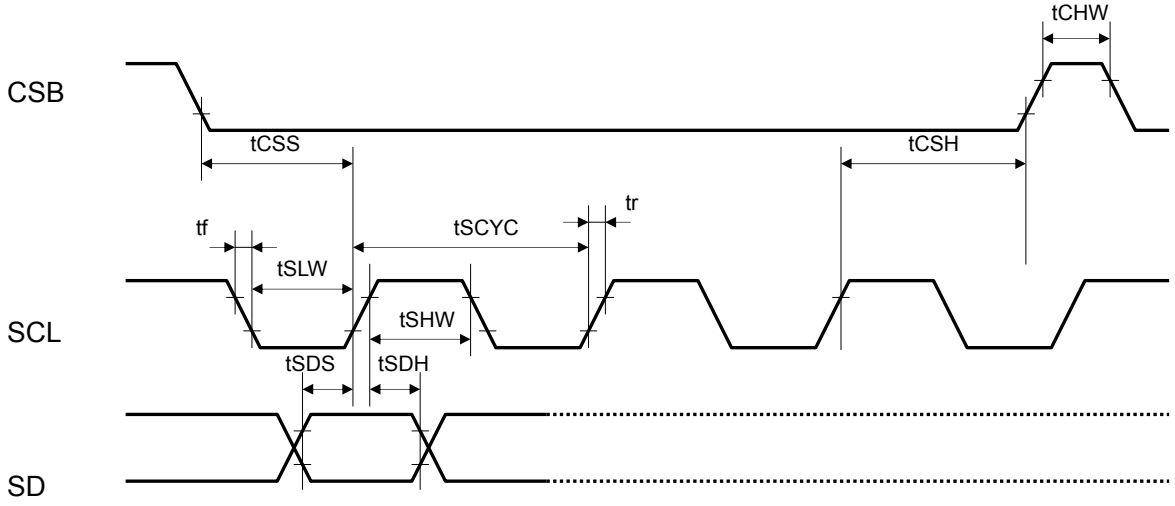


Fig. BU9794KV-1 Interface Timing

● Block Diagram （BU9794KV）

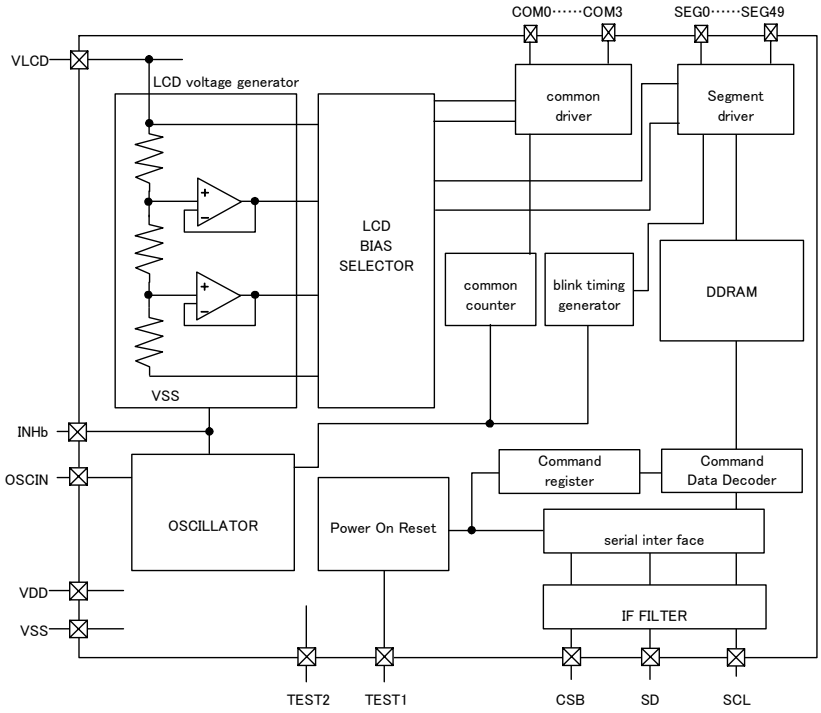


Fig. BU9794KV-2 Block diagram

●Pin Arrangement （BU9794KV）

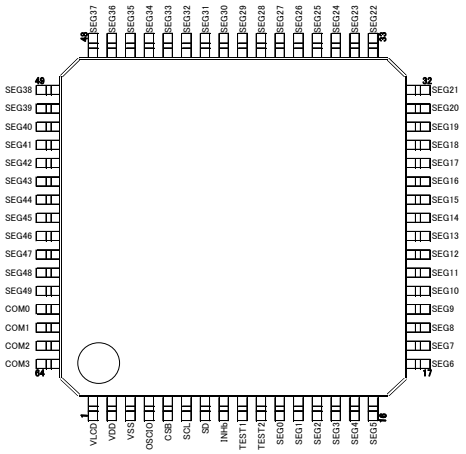


Fig. BU9794KV-3 Pin arrangement

● Terminal description （BU9794KV）

Terminal	Terminal No.	I/O	Function
INHb	8	I	Input terminal for turn off display H: turn on display　L: turn off display
TEST1	9	I	Test input (ROHM use only) Must be connect to VSS
TEST2	10	I	Test input (ROHM use only) Must be connect to VSS
OSCIO	4	I	External clock input Ex clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SD	7	I	serial data input
SCL	6	I	serial data transfer clock
CSB	5	I	Chip select ： “L” active
VSS	3		GND
VDD	2		Power supply
VLCD	1		Power supply for LCD driving
SEG0-49	11-60	O	SEGMENT output for LCD driving
COM0-3	61-64	O	COMMON output for LCD driving

●Command Description （BU9794KV）

D7 (MSB) is bit for command or data judgment.
Refer to Command and data transfer method.

C：0：Next byte is RAM write data.
1：Next byte is command.

○ Mode Set (MODE SET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	0	P3	P2	P1	P0

Set display ON and OFF

Setting	P3	Reset initialize condition
Display OFF	0	○
Display ON	1	

Set LCD drive waveform

Setup	P2	Reset initialize condition
Line inversion	0	○
Frame inversion	1	

Set Power save mode

Setup	P1	P0	Reset initialize condition
Power save mode 1	0	0	
Power save mode 2	0	1	
Normal mode	1	0	○
High power mode	1	1	

＊ Please use in VLCD≧3.0V condition in High power mode.

○ Address set (ADSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	P5	P4	P3	P2	P1	P0

The range of address can be set as 00h to 31h.
Don’t set out of range address, otherwise address will be set 00h.
In reset condition, it will be set 00h.

○ Display control (DISCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	1	P3	P2	P1	P0

Set bias level

setup	P3	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	

Set oscillator mode

setup	P2	Reset initialize condition
Internal oscillation	0	○
External clock input	1	

Set Frame frequency

setup	P1	P0	Reset initialize condition
80Hz	0	0	○
71Hz	0	1	
64Hz	1	0	
53Hz	1	1	

○ Software Reset(SWRST)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	0	1	1

This command will be set initialize condition.

○ Blink control (BLKCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	*	P1	P0

(Don't care)

Set blink mode

Blink mode (Hz)	P1	P0	Reset initialize condition
OFF	0	0	○
0.5	0	1	
1	1	0	
2	1	1	

○ All Pixel control (APCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

All display set ON, OFF

APON	P1	Reset initialize condition
Normal	0	○
All pixel ON	1	

APOFF	P0	Reset initialize condition
Normal	0	○
All pixel OFF	1	

●Function description （BU9794KV）

○SPI (3wire Serial Interface)

This device is controlled by 3-wire signal (CSB, SCL, and SD).
First, Interface counter is initialized with CSB=“H", and CSB=”L” makes SD and SCL input enable.
The protocol of 3-SPI transfer is as follows.
Each command starts with Command or Data judgment bit (D/C) as MSB data, and continuously in order of D6 – D0 are followed after CSB =”L”. (Internal data is latched at the rising edge of SCL, it converted to 8bits parallel data at the rising edge of 8th CLK.)

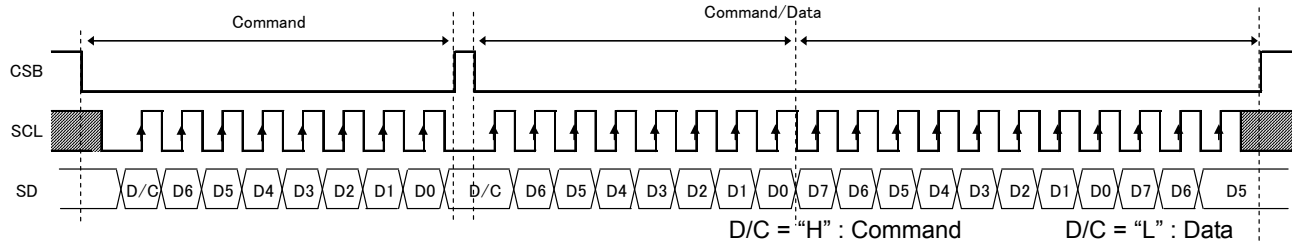
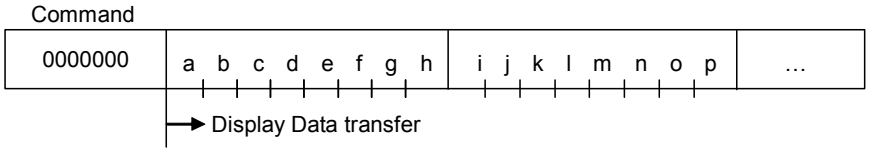


Fig. BU9794KV-4 3-SPI Command/Data Transfer format

○ Write display data and transfer method

This device has Display Data RAM (DDRAM) of 50×4=200bit.
The relationship between data input and display data, DDRAM data and address are as follows;



8 bit data will be stored in DDRAM. The address to be written is specified by Address set command, and the address is automatically incremented in every 4bit data.
Data can be continuously written in DDRAM by transmitting Data continuously.
(When RAM data is written successively after writing RAM data to 31h (SEG49), the address is returned to 00h (SEG0) by the auto-increment function

DDRAM address

BIT	00	01	02	03	04	05	06	07	・・・	2Fh	30h	31h	
0	a	e	i	m									COM0
1	b	f	j	n									COM1
2	c	g	k	o									COM2
3	d	h	l	p									COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7		SEG47	SEG48	SEG49	

As data transfer to DDRAM is done every 4bit data,
it will be cancelled if it changes CSB=”L”→”H” before 4bits data transfer.

○ Reset initialize condition

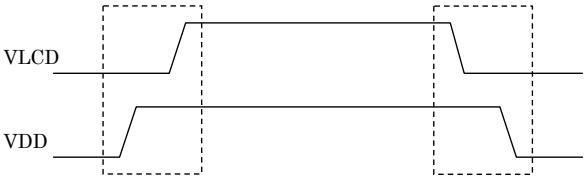
Initial condition after execute Software Reset is as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).
- Refer to Command Description about initialize value of register.

● Cautions in Power ON/OFF (BU9794KV)

○ Power supply sequence

Please keep Power ON/OFF sequence as below waveform.

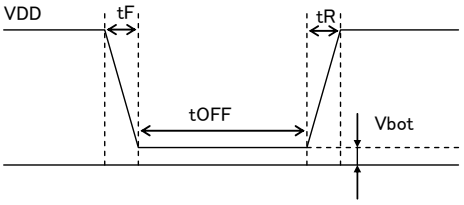


FigBU9794KV-5 Power supply sequence

○ Caution in P.O.R circuit use

This device has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Please keep the following recommended Power-On conditions in order to power up properly.

Please set power up conditions to meet the recommended tR, tF, tOFF, and Vbot spec below in order to ensure P.O.R operation



Recommendation condition of tR, tF, tOFF, Vbot (Ta=25℃)

tR	tF	tOFF	Vbot
Less than 5ms	Less than 5ms	More than 20ms	Less than 0.3V

Fig. BU9794KV-6 Power ON/OFF waveform

If it is difficult to meet above conditions, execute the following sequence after Power-On.
But it is not able to accept Command input in Power off status, it has to take care that software reset is not perfectly alternative method of POR function.

(1) CSB “L”→ “H”

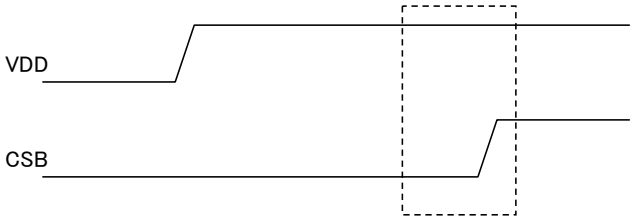


Fig. BU9794KV-7 CSB timing

(2) CSB→ “L” , execute Software Reset command.

● IO Equivalent Circuit (BU9794KV)

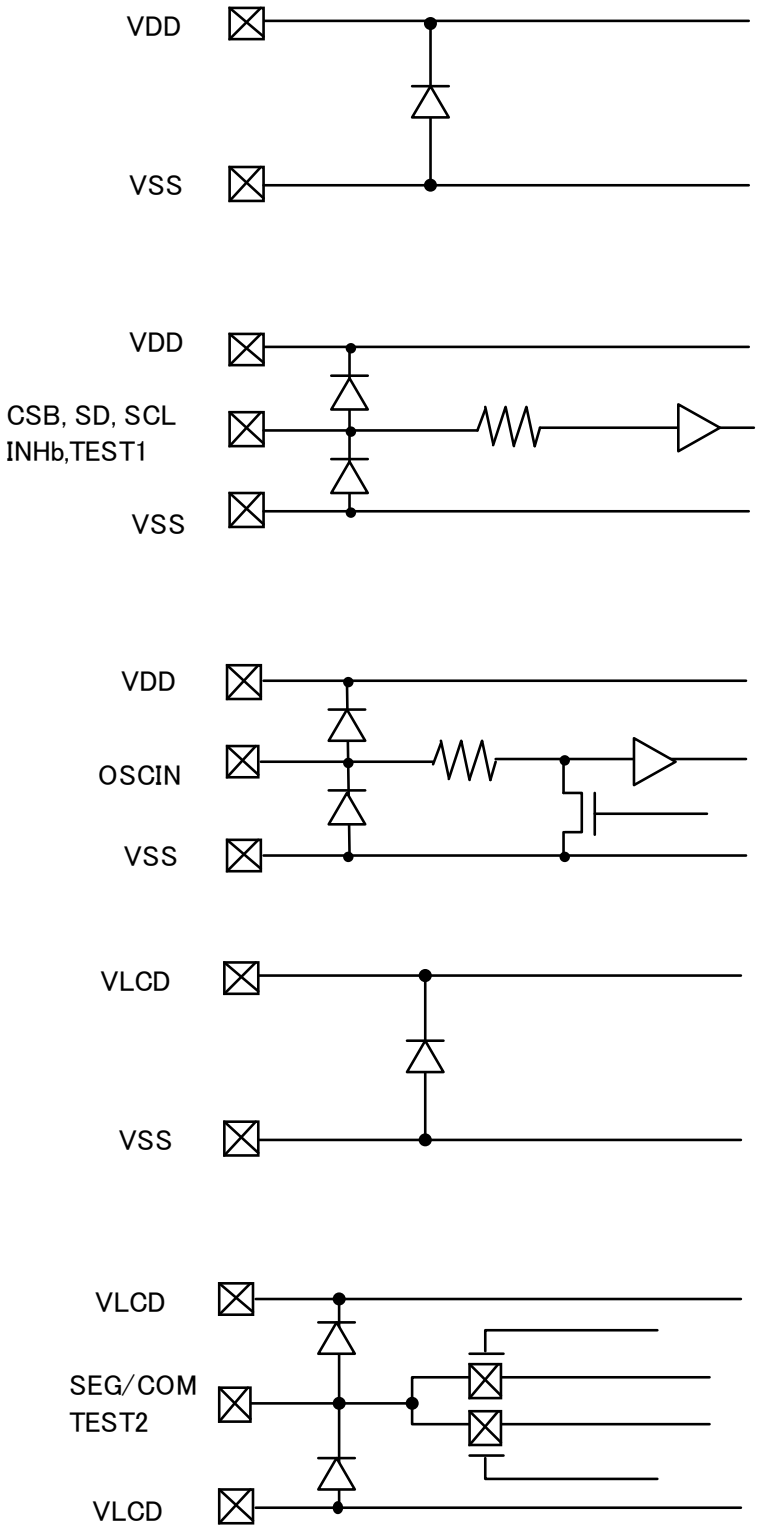


Fig. BU9794KV-8 I/O equivalent circuit

● Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

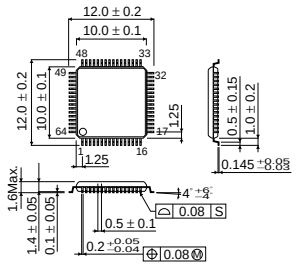
● Order form name selection

B	U	9	7	9	4	K	V	−	E	2

ROHM form name　Part No.　Package type KV=VQFP　Packaging and forming specification E2 =Reel-shaped emboss taping

VOFP64

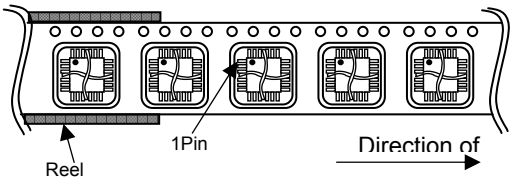
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（Unit:mm)

<Packing information>

Tape	Embossed carrier tape(with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

BU9799KV 200Segment (50SEG×4COM) Driver

● Feature (BU9799KV)

1) LCD driving port: 4 Common output, 50 Segment output
2) Integrated RAM for display data (DDRAM) : 50 × 4bit (Max 200 Segment)
3) 2wire serial interface (SCL,SDA)
4) Integrated Oscillation circuit
5) Integrated Power supply circuit for LCD driving
   1/2 ,1/3 Bias 1/4 Duty
   Integrated Buffer AMP
6) No external components
7) Low power consumption design
8) Support standby mode (Controlled by INHb terminal or command)
9) Integrated Power-on Reset circuit
10) Integrated Electrical volume register (EVR) function
11) Support Blink function
12) Operation power supply: 2.5～5.5V
13) Power supply for LCD driving: 2.5～5.5V

● Uses (BU9799KV)

Telephone, FAX, Portable equipments (POS, ECR, PDA etc.),
DSC, DVC, Car audio, Home electrical appliance, Meter equipment etc.

● Absolute Maximum Ratings (Ta=25degree, VSS=0V) (BU9799KV)

Parameter	Symbol	Limits	Unit	Remarks
Power Supply Voltage1	VDD	-0.5 ～ +7.0	V	Power supply
Power Supply Voltage2	VLCD	-0.5 ～ +7.0	V	LCD drive voltage
Allowable loss	Pd	0.75	W	When use more than Ta=25°C, subtract 7.5mW per degree.
Input voltage range	VIN	-0.5 ～ VDD+0.5	V	
Operational temperature range	Topr	-40 ～ +85	degree	
Storage temperature range	Tstg	-55 ～ +125	degree	

*This product is not designed against radioactive ray.

● Recommend operating conditions (Ta=25degree, VSS=0V) (BU9799KV)

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Power Supply Voltage1	VDD	2.5	-	5.5	V	Power supply
Power Supply Voltage2	VLCD	2.5	-	5.5	V	LCD drive voltage

● Electrical Characteristics (BU9799KV)

DC Characteristics (VDD=2.5～5.5V, VLCD=2.5～5.5V, VSS=0V, Ta=-40～85degree, unless otherwise specified)

Parameter		Symbol	Limit			Unit	Condition
			MIN	TYP	MAX		
"H" level input voltage		VIH	0.8VDD	-	VDD	V	SDA,SCL
"L" level input voltage		VIL	VSS	-	0.2VDD	V	SDA,SCL
"H" level input current		IIH	-	-	1	uA	SDA,SCL
"L" level input current		IIL	-1	-	-	uA	SDA,SCL
LCD Driver on resistance	SEG	RON	-	3.5	-	kΩ	Iload=±10uA
	COM	RON	-	3.5	-	kΩ	
Standby current		Ist	-	-	5	uA	Display off, Oscillation off
Power consumption 1		IDD	-	2.5	15	uA	VDD=3.3V, VLCD=5V, Ta=25degree Power save mode1, FR=70Hz 1/3 bias, Frame inverse
Power consumption 2		ILCD	-	10	20	uA	VDD=3.3V, VLCD=5V, Ta=25degree Power save mode1, FR=70Hz 1/3 bias, Frame inverse

Oscillation Characteristics (VDD=2.5～5.5V, VLCD=2.5～5.5V, VSS=0V, Ta=-40～85degree, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Frame frequency	fCLK	56	80	104	Hz	FR = 80Hz setting VDD=3.3V

MPU interface Characteristics (VDD=2.5～5.5V, VLCD=2.5～5.5V, VSS=0V, Ta=-40～85degree, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN.	TYP.	MAX.		
Input rise time	tr	-	-	0.3	us	
Input fall time	tf	-	-	0.3	us	
SCL cycle time	tSCYC	2.5	-	-	us	
"H" SCL pulse width	tSHW	0.6	-	-	us	
"L" SCL pulse width	tSLW	1.3	-	-	us	
SDA setup time	tSDS	100	-	-	ns	
SDA hold time	tSDH	100	-	-	ns	
Buss free time	tBUF	1.3	-	-	us	
START condition hold time	tHD;STA	0.6	-	-	us	
START condition setup time	tSU;STA	0.6	-	-	us	
STOP condition setup time	tSU;STO	0.6	-	-	us	
Noise cancel width	tsp	-	-	50	us	

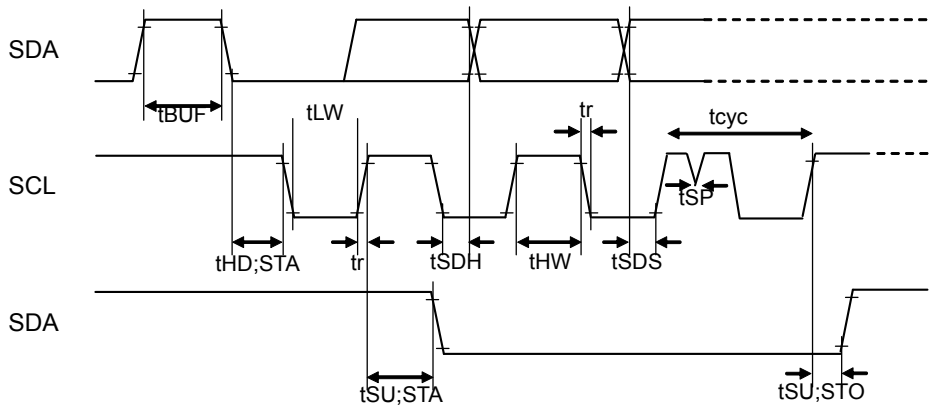


Fig. BU9799KV-1 interface timing

●Block Diagram（BU9799KV）

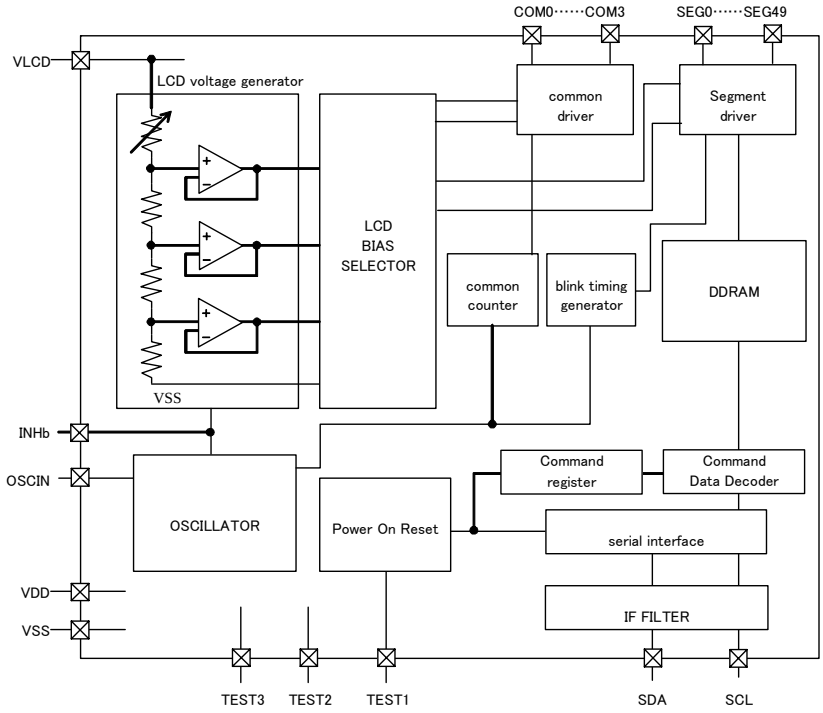


Fig. BU9799KV-2 block diagram

● Pin Arrangement （BU9799KV）

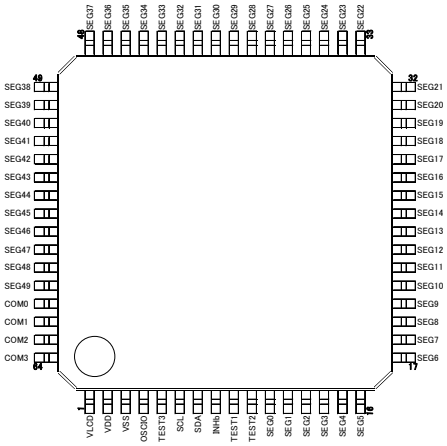


Fig. BU9799KV-3 Pin arrangement

●Terminal description （BU9799KV）

Terminal	Terminal No.	I/O	Function
INHb	8	I	Input terminal for turn off display H: turn on display L: turn off display
TEST1	9	I	Test input (ROHM use only) TEST1=”L”: POR circuit enable TEST1=”H”: POR circuit disenable, refer to “Cautions in Power ON/OFF”
TEST2	10	I	Test input (ROHM use only) Must be connect to VSS
TEST3	5	I	Test input (ROHM use only) Must be connect to VSS
OSCIO	4	I	External clock input Ex clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SDA	7	I	serial data input
SCL	6	I	serial data transfer clock
VSS	3		GND
VDD	2		Power supply
VLCD	1		Power supply for LCD driving
SEG0-49	11-60	O	SEGMENT output for LCD driving
COM0-3	61-64	O	COMMON output for LCD driving

● Command Description （BU9799KV）

D7 (MSB) is bit for command or data judgment.
Refer to Command and data transfer method.

C：0：Next byte is RAM write data.
1：Next byte is command.

○ Mode Set (MODE SET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	0	P3	P2	*	*

Set display ON and OFF

Setting	P3	Reset initialize condition
Display OFF	0	○
Display ON	1	

Set bias level

setup	P3	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	

○ Address set (ADSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

It is set address as follows;

	MSB			LSB
Internal register	Address [5]	Address [4]	・・・	Address [0]
command	ICSET [P2]	ADSET [P4]	・・・	ADSET [P0]

The range of address can be set as 00000 to 10001(2).
Don't set out of range address, otherwise address will be set 00000.
ICSET command is only define MSB bit of address, not set the address of DDRAM.
If want to set the address of DDRAM, it has to be input ADSET command.

○ Display control (DISCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Set Power save mode FR

Power save mode FR	P4	P3	Reset initialize condition
Normal mode	0	0	○
Power save mode1	0	1	
Power save mode2	1	0	
Power save mode3	1	1	

Set LCD drive waveform

Setup	P2	Reset initialize condition
Line inversion	0	○
Frame inversion	1	

Set Power save mode SR

Setup	P1	P0	Reset initialize condition
Power save mode1	0	0	
Power save mode2	0	1	
Normal mode	1	0	○
High power mode	1	1	

○ Set IC Operation (ICSET)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	P2	P1	P0

P2: Define the MSB bit of address of DDRAM. Refer to ADSET command.

Set software reset execution

Setup	P1
No operation	0
Software Reset execute	1

This command will be set initialize condition.
When executed Software reset, P1 and P0 will be ignored.

Set oscillator mode

setup	P0	Reset initialize condition
Internal oscillation	0	○
External clock input	1	

○ Blink control (BLKCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	*	P1	P0

Set blink mode

Blink mode (Hz)	P1	P0	Reset initialize condition
OFF	0	0	○
0.5	0	1	
1	1	0	
2	1	1	

○ All Pixel control (APCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

All display set ON, OFF

APON	P1	Reset initialize condition
Normal	0	○
All pixel ON	1	

APOFF	P0	Reset initialize condition
Normal	0	○
All pixel OFF	1	

○ EVR Set 1(EVRSET1)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	0	P2	P1	P0

It is able to control 32-step electrical volume register (EVR).
It is able to set V0 voltage level (the max level voltage of LCD driving voltage).
It is set electrical volume register as follows;

MSB EVR4	EVR3	EVR2	EVR1	LSB EVR0	
EVRSET1 P2	EVRSET1 P1	EVRSET1 P0	EVRSET2 P1	EVRSET2 P0	
0	0	0	0	0	Reset initialize condition

Electrical volume register (EVR) is set “00000” in reset initialize condition
In “00000” condition, V0 voltage output VLCD voltage.
Please refer to next page about V0 output voltage.
It is prohibited the EVR setting that V0 voltage will be under 2.5V.

EVRSET1 is defined the upper 3bit of electrical volume register.
It will be set the electrical volume register by this command (EVRSET1) input.

○ EVR Set 2(EVRSET2)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	0	P1	P0

EVRSET2 is defined the lower 2bit of electrical volume register.
It will be set the electrical volume register by this command (EVRSET2) input.

○ The relationship of electrical volume register(EVR) setting and V0 voltage

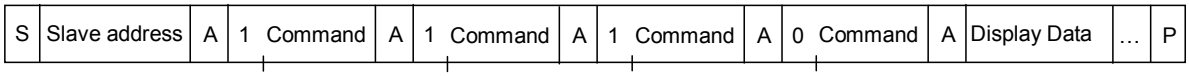
EVR	Calculation formula	VLCD= 5.500	VLCD= 5.000	VLCD= 4.000	VLCD= 3.500	VLCD= 3.000	VLCD= 2.500	[V]
0	VLCD	V0= 5.500	V0= 5.000	V0= 4.000	V0= 3.500	V0= 3.000	V0= 2.500	[V]
1	0.967*VLCD	V0= 5.323	V0= 4.839	V0= 3.871	V0= 3.387	V0= 2.903	V0= 2.419	[V]
2	0.937*VLCD	V0= 5.156	V0= 4.688	V0= 3.750	V0= 3.281	V0= 2.813	V0= 2.344	[V]
3	0.909*VLCD	V0= 5.000	V0= 4.545	V0= 3.636	V0= 3.182	V0= 2.727	V0= 2.273	[V]
4	0.882*VLCD	V0= 4.853	V0= 4.412	V0= 3.529	V0= 3.088	V0= 2.647	V0= 2.206	[V]
5	0.857*VLCD	V0= 4.714	V0= 4.286	V0= 3.429	V0= 3.000	V0= 2.571	V0= 2.143	[V]
6	0.833*VLCD	V0= 4.583	V0= 4.167	V0= 3.333	V0= 2.917	V0= 2.500	V0= 2.083	[V]
7	0.810*VLCD	V0= 4.459	V0= 4.054	V0= 3.243	V0= 2.838	V0= 2.432	V0= 2.027	[V]
8	0.789*VLCD	V0= 4.342	V0= 3.947	V0= 3.158	V0= 2.763	V0= 2.368	V0= 1.974	[V]
9	0.769*VLCD	V0= 4.231	V0= 3.846	V0= 3.077	V0= 2.692	V0= 2.308	V0= 1.923	[V]
10	0.750*VLCD	V0= 4.125	V0= 3.750	V0= 3.000	V0= 2.625	V0= 2.250	V0= 1.875	[V]
11	0.731*VLCD	V0= 4.024	V0= 3.659	V0= 2.927	V0= 2.561	V0= 2.195	V0= 1.829	[V]
12	0.714*VLCD	V0= 3.929	V0= 3.571	V0= 2.857	V0= 2.500	V0= 2.143	V0= 1.786	[V]
13	0.697*VLCD	V0= 3.837	V0= 3.488	V0= 2.791	V0= 2.442	V0= 2.093	V0= 1.744	[V]
14	0.681*VLCD	V0= 3.750	V0= 3.409	V0= 2.727	V0= 2.386	V0= 2.045	V0= 1.705	[V]
15	0.666*VLCD	V0= 3.667	V0= 3.333	V0= 2.667	V0= 2.333	V0= 2.000	V0= 1.667	[V]
16	0.652*VLCD	V0= 3.587	V0= 3.261	V0= 2.609	V0= 2.283	V0= 1.957	V0= 1.630	[V]
17	0.638*VLCD	V0= 3.511	V0= 3.191	V0= 2.553	V0= 2.234	V0= 1.915	V0= 1.596	[V]
18	0.625*VLCD	V0= 3.438	V0= 3.125	V0= 2.500	V0= 2.188	V0= 1.875	V0= 1.563	[V]
19	0.612*VLCD	V0= 3.367	V0= 3.061	V0= 2.449	V0= 2.143	V0= 1.837	V0= 1.531	[V]
20	0.600*VLCD	V0= 3.300	V0= 3.000	V0= 2.400	V0= 2.100	V0= 1.800	V0= 1.500	[V]
21	0.588*VLCD	V0= 3.235	V0= 2.941	V0= 2.353	V0= 2.059	V0= 1.765	V0= 1.471	[V]
22	0.576*VLCD	V0= 3.173	V0= 2.885	V0= 2.308	V0= 2.019	V0= 1.731	V0= 1.442	[V]
23	0.566*VLCD	V0= 3.113	V0= 2.830	V0= 2.264	V0= 1.981	V0= 1.698	V0= 1.415	[V]
24	0.555*VLCD	V0= 3.056	V0= 2.778	V0= 2.222	V0= 1.944	V0= 1.667	V0= 1.389	[V]
25	0.545*VLCD	V0= 3.000	V0= 2.727	V0= 2.182	V0= 1.909	V0= 1.636	V0= 1.364	[V]
26	0.535*VLCD	V0= 2.946	V0= 2.679	V0= 2.143	V0= 1.875	V0= 1.607	V0= 1.339	[V]
27	0.526*VLCD	V0= 2.895	V0= 2.632	V0= 2.105	V0= 1.842	V0= 1.579	V0= 1.316	[V]
28	0.517*VLCD	V0= 2.845	V0= 2.586	V0= 2.069	V0= 1.810	V0= 1.552	V0= 1.293	[V]
29	0.508*VLCD	V0= 2.797	V0= 2.542	V0= 2.034	V0= 1.780	V0= 1.525	V0= 1.271	[V]
30	0.500*VLCD	V0= 2.750	V0= 2.500	V0= 2.000	V0= 1.750	V0= 1.500	V0= 1.250	[V]
31	0.491*VLCD	V0= 2.705	V0= 2.459	V0= 1.967	V0= 1.721	V0= 1.475	V0= 1.230	[V]

Prohibit setting

● Function description（BU9799KV）

○ Command transfer method

Issue Slave Address (“01111100”) after generate “START condition”.
1byte after Slave Address always becomes command input.
MSB (“command or data judge bit”) of command decide to next data is command or display data.
When set “command or data judge bit”=‘1’, next byte will be command.
When set “command or data judge bit”=‘0’, next byte data is display data.



Once it becomes display data transfer condition, it cannot input command.
When want to input command again, please generate “START condition” once.

○ Write display and transfer method

This device has Display Data RAM (DDRAM) of 50×4=200bit.

The relationship between data input and display data, DDRAM data and address are as follows;



DDRAM address

BIT	00	01	02	03	04	05	06	07	・・・	2Fh	30h	31h	
0	a	e	i	m									COM0
1	b	f	j	n									COM1
2	c	g	k	o									COM2
3	d	h	l	p									COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7		SEG47	SEG48	SEG49	

Data transfer to DDRAM happens every 4bit data.
So It will be finished to transfer with no need to wait ACK.

○ Reset initialize condition

Initial condition after execute Software Reset is as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).
- Refer to Command Description about initialize value of register.

● Cautions in Power ON/OFF (BU9799KV)

○ Power supply sequence

Please keep Power ON/OFF sequence as below waveform.

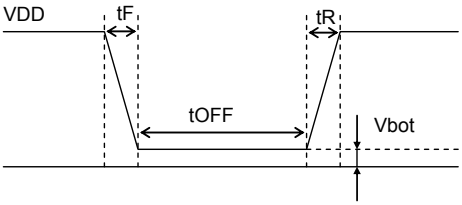


Fig. BU9799KV-4 Power supply sequence

○ Caution in P.O.R circuit use

This device has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Please keep the following recommended Power-On conditions in order to power up properly.

Please set power up conditions to meet the recommended tR, tF, tOFF, and Vbot spec below in order to ensure P.O.R operation
* It has to set TEST1=”L” to be valid in POR circuit.



Recommendation condition of tR, tF, tOFF, Vbot (Ta=25℃)

tR	tF	tOFF	Vbot
Less than 5ms	Less than 5ms	More than 20ms	Less than 0.3V

Fig. BU9799KV-5 Power ON/OFF waveform

If it is difficult to meet above conditions, execute the following sequence after Power-On.
* It has to keep the following sequence in the case of TEST1=”H”. As POR circuit is invalid status.

(1) TEST1 =”H”

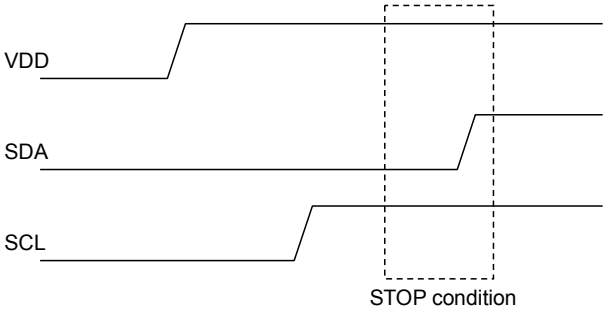


Fig. BU9799KV-6 Stop condition

(2) After send STOP condition, execute Software Reset (ICSET) command.

● IO Equivalent Circuit (BU9799KV)

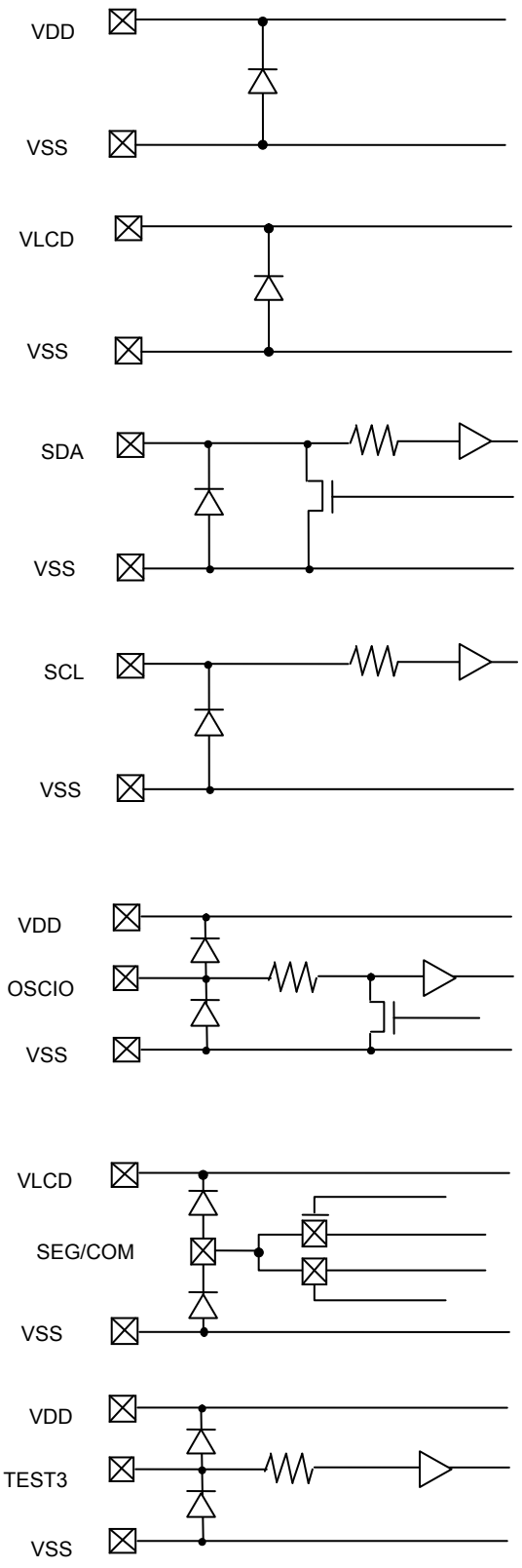


Fig. BU9799KV-7 I/O equivalent circuit

● Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

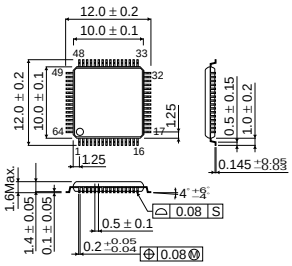
● Order form name selection

B	U	9	7	9	9	K	V	–	E	2

ROHM form name　Part No.　Package type KV=VQFP　Packaging and forming specification E2 =Reel-shaped emboss taping

VOFP64

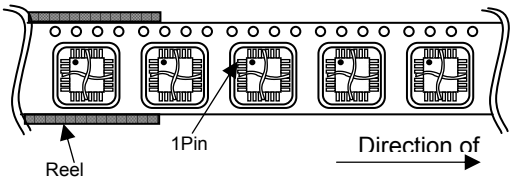
<Dimension>



(Unit:mm)

<Packing information>

Tape	Embossed carrier tape(with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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