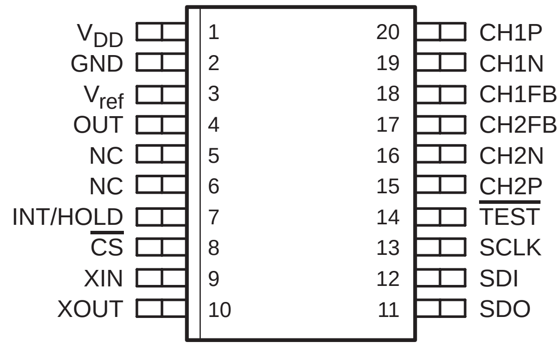
features

- **Dual-Channel Knock Sensor Interface**
- **Programmable Input Frequency Prescaler (OSC_{IN})**
- **Serial Interface With Microprocessor (SPI)**
- **Programmable Gain**
- **Programmable Band-Pass Filter Center Frequency**
- **External Clock Frequencies up to 24 MHz − 4, 5, 6, 8, 10, 12, 16, 20, and 24 MHz**
- **Programmable Integrator Time Constants**
- **Operating Temperature Range −40°C to 125°C**

DW PACKAGE
(TOP VIEW)



applications

- **Engine Knock Detector Signal Processing**
- **Analog Signal Processing With Filter Characteristics**

description

The TPIC8101 is a dual-channel signal processing IC for detection of premature detonation in combustion engine. The two sensor channels are selectable through the SPI bus. The knock sensor typically provides an electrical signal to the amplifier inputs. The sensed signal is processed through a programmable band-pass filter to extract the frequency of interest (engine knock or ping signals). The band-pass filter eliminates any engine background noise associated with combustion. The engine background noise is typically low in amplitude compared to the predetonation noise.

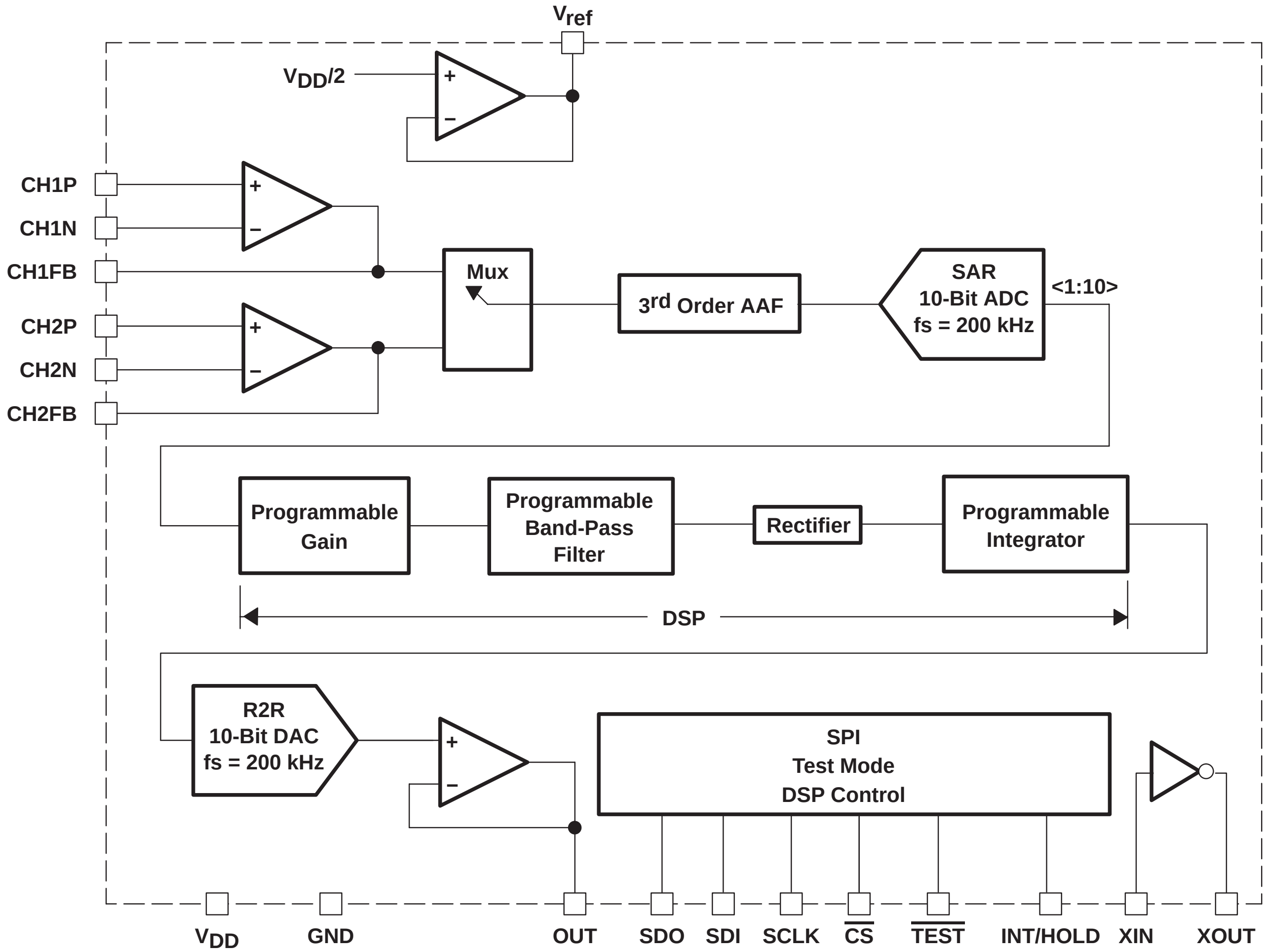
The detected signal is full-wave rectified and integrated by use of the INT/HOLD signal. The digital output from the integration stage is either converted to an analog signal, passed through an output buffer, or be read directly by the SPI.

This analog buffered output may be interfaced to an A/D converter and read by the microprocessor. The digital output may be directly interfaced to the microprocessor.

The data from the A/D enables the system to analyze the amount of retard timing for the next spark ignition timing cycle.

With the microprocessor closed-loop system, advancing and retarding the spark timing optimize the load/RPM conditions for a particular engine (data stored in RAM).

functional block diagram



Terminal Functions

TERMINAL			DESCRIPTION
NAME	**NO.**	**TERMINAL TYPE (PULLUP/PULLDOWN)**	
V_{DD}	1	I	5-V input supply
GND	2	I	Ground connection
Vref	3	O	Supply reference generator with external bypass capacitor
OUT	4	O	Buffered integrator output
NC†	5, 6		No connection
INT/HOLD	7	I / Pulldown	Selectable for integrate (high) or hold (low) mode (with internal pulldown)
$\overline{CS}$	8	I / Pullup	Chip select for SPI communications (active low with internal pullup)
XIN	9	I	Inverter input for oscillator
XOUT	10	O	Inverter output for oscillator
SDO	11	O	Serial data output for SPI bus
SDI	12	I / Pullup	Serial data input line
SCLK	13	I / Pullup	SPI clock
$\overline{TEST}$	14	I / Pullup	Test mode (active low), open for normal operation
CH2P	15	I	Positive input for amplifier #2
CH2N	16	I	Negative input for amplifier #2
CH2FB	17	O	Output of amplifier #2, for feedback connection
CH1FB	18	O	Output of amplifier #1, for feedback connection
CH1N	19	I	Negative input for amplifier #1
CH1P	20	I	Positive input for amplifier #1

† These terminals are to be used for test purposes only and are no connected in the system application. No signal traces should be connected to the NC terminals.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Regulated input voltage (see Notes 1 and 2), V_{DD} .... −0.3 V to 7 V
Output voltage (see Notes 1 and 2), V_O .... −0.3 V to 7 V
Input voltage (see Notes 1 and 2), V_{IN} .... −0.3 V to 7 V
DC input current on terminals CH1P, CH1N, CH2P, and CH2N (see Notes 1 and 2), I_{IN} .... 2 mA
DC input voltage on terminals CH1P, CH1N, CH2P and CH2N (see Notes 1 and 2), V_{DCIN} .... 14 V
Thermal impedance junction to ambient, θ_{JA} .... 120°C/W
Continuous power dissipation, P_D .... 200 mW
Electrostatic discharge susceptibility (see Note 3), $V_{(HBMESD)}$ .... 2 kV
Operating ambient temperature range, T_A .... −40°C to 125°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature (soldering, 10 sec), T_{LEAD} .... 265°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Absolute negative voltage on these terminals is not to go below –0.5 V.
3. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.

recommended operating conditions

	MIN	MAX	UNITS
Regulated input voltage, V_{DD}	−0.3	5.5	V
Output voltage, V_O	−0.3	5.5	V
Input voltage, V_{IN}	0.05	V_{DD} − 0.05	V
DC input current on terminals CH1P, CH1N, CH2P, and CH2N, I_{IN}	−1	1	µA
DC input voltage on terminals CH1P, CH1N, CH2P, and CH2N, V_{DCIN}		Vref, (V_{DD}/2)	V
Continuous power dissipation, P_D		100	mW

dc electrical characteristics, V_{DD} = 5 V ±5%, input frequency before prescaler = 4 MHz to 20 MHz (±0.5%), T_A = −40°C to 125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{DD(Q)}$	Quiescent current	V_{DD} = 5 V		7.5		mA
$I_{DD(OP)}$	Operating current	V_{DD} = 5 V, XIN = 8 MHz			20	mA
V_{mid0}	Midpoint voltage	V_{DD} = 5 V, I_{Source} = 2 mA	2.3	2.5	2.55	V
V_{mid1}	Midpoint voltage	V_{DD} = 5 V, I_{Sink} = 2 mA	2.4	2.5	2.7	V
V_{mid2}	Midpoint voltage	V_{DD} = 5 V, I_L = 0 mA	2.4	2.5	2.6	V
Rpull0	Internal pullup resistor $\overline{CS}$, SDI, SCLK, $\overline{TEST}$	V_{IN} = GND	30			kΩ
Rpull1	Internal pulldown resistor INT/HOLD	V_{IN} = V_{DD}	20			kΩ
I_{lkg}	Input leakage current $\overline{CS}$, SDI, SCLK, INT/HOLD, $\overline{TEST}$	Measured at GND and V_{DD}, V_{DD} = 5.5 V = V_{IN}			±3	µA
V_{IL}	Low-level input voltage INT/HOLD, $\overline{CS}$, $\overline{TEST}$, SDI, SCLK				30% of V_{DD}	
V_{IH}	High-level input voltage INT/HOLD, $\overline{CS}$, $\overline{TEST}$, SDI, SCLK		70% of V_{DD}			
V_{OL}	Low-level output voltage SDO	I_{Sink} = 4 mA, V_{DD} = 5 V			0.7	V
V_{OH}	High-level output voltage SDO	I_{Source} = 100 µA, V_{DD} = 5 V	4.4			V
$I_{lkg(OL)}$	Low-level leakage current SDO	Measured at GND and V_{DD} = 5 V, SDO in high impedance	−10		10	µA
$V_{OL(XOUT)}$	Low-level output voltage	I_{Sink} = 500 µA, V_{DD} = 4.5 V			1.5	V
$V_{OH(XOUT)}$	High-level output voltage	I_{Source} = 500 µA, V_{DD} = 5 V	4.4			V
V_{hyst}	Hysteresis voltage INT/HOLD, $\overline{CS}$, XIN, SDI, SCLK, $\overline{TEST}$		0.4			V
Input Amplifiers						
$V_{OH(1)}$	CH1FB and CH2FB high-level output voltage	V_{DD} = 5 V, I_{Source} = 100 µA	V_{DD} − 0.05	V_{DD} − 0.02		V
		V_{DD} = 5 V, I_{Source} = 2 mA	V_{DD} − 0.5			
$V_{OL(1)}$	CH1FB and CH2FB low-level output voltage	I_{Sink} = 100 µA		15	50	mV
		I_{Sink} = 2 mA			500	
C_{ATTEN}	Cross-coupling attenuation CH1FB and CH2FB	f_{in} $max_{(ch1)}$ = 20 kHz, measured on channel 2	40			dB
Av	Open-loop gain		60	100		dB
G_{BW}	Gain bandwidth product	Input range 0.5 V to 4.5 V	1	2.6		MHz
V_{IN}	Input voltage range		0.05		V_{DD} − 0.05	V
$V_{(offset)}$	Offset voltage at input		−10		10	mV
CMRR	Common-mode rejection ratio	Inputs at V_{mid} f_{in} = 0 to 20 kHz	60	80		dB
PM	Phase margin	Gain = 1, C_L = 200 pF, R_L = 100 kΩ	45			deg
Prescaler, XIN						
V_{OSC}	Minimum input peak amplitude	V_{DD} = V_{min}, oscillator inverter biased feedback resistor 1 MΩ, f_{osc} = 24 MHz	150			mV
C_{IN}	Input capacitance	Assured by design			7	pF
$I_{lkg(XIN)}$	Leakage current		−1		1	µA

dc electrical characteristics, V_{DD} = 5 V ±5%, input frequency before prescaler = 4 MHz to 20 MHz (±0.5%), T_A = −40°C to 125°C (unless otherwise specified) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Multiplexer						
C_{ATTEN}	Cross-coupling attenuation (assured by design)	f_{in} $max_{(ch1)}$ = 20 kHz, measured on channel 2	40			dB
Anti-Aliasing Filter						
f_c‡	Cut-off frequency at –3 dB		35	45	55	kHz
BW	Response 1 kHz to 20 kHz referenced to 1 kHz	70-mV RMS, input: CH1FB or CH2FB, output: OUT	−1	−0.5	1	dB
ATTEN	Attenuation at 100 kHz referenced to 1 kHz	70-mV RMS, input: CH1FB or CH2FB, output: OUT	−10	−15		dB
Analog-to-Digital Converter						
f_S	Sampling frequency	For all frequencies stated	198	200	202	kHz
AR	Analog resolution		10			Bit
ADNL	Differential linearity error (DNL)			1		Bit
AINL	Linearity error (INL)			1		Bit
Digital-to-Analog Converter						
$f_{S(DA)}$	Sampling frequency		198	200	202	kHz
DR	Resolution at 200 kHz		10			Bit
DDNL	Differential linearity error (DNL)	(Vreset < DACout < 0.98 V_{DD})	−1		1	LSB
DINL	Linearity error (INL)	(Vreset < DACout < 0.98 V_{DD})	−2.5		2.5	LSB
DRNIL	Repeatability (for characterization purposes only)		−1		1	LSB
Output Buffer						
V_{OH}	High-level output voltage	V_{DD} = 5 V, I_{Source} = 2 mA	V_{DD} − 0.2	V_{DD} − 0.15		V
V_{OL}	Low-level output voltage	V_{DD} = 5 V, I_{Sink} = 2 mA		120	175	mV
Av	Open-loop gain	I_O = ±2 mA	60	100		dB
G	Output gain	I_O = ±2 mA		1		
V_{ripple}	Ripple voltage	C_L = 0 to 22 nF, max slew rate, 12 mV/µs from Vreset to 4 V			10	mV
t_S	Settling time	C_L = 0 to 22 nF, max slew rate, 12 mV/µs from Vreset to 4 V, output: ±0.5 LSB			20	µs

‡ f_c is programmable (see Table 1).

ac electrical characteristics, V_{DD} = 5 V ±5%, T_A = −40°C to 125°C (unless otherwise specified)

	DESCRIPTION	MIN	TYP	MAX	UNITS
f_{SPI}	SPI frequency			5	MHz
t1	Time from $\overline{CS}$ falling edge to SCLK rising edge	10			ns
t2	Time from $\overline{CS}$ falling edge to SCLK falling edge	80			ns
t3	Time for SCLK to go high	60			ns
t4	Time for SCLK to go low	60			ns
t5	Time from last SCLK falling edge to $\overline{CS}$ rising edge	80			ns
t6	Time from SDI valid to falling edge of SCLK	60			ns
t7	Time for SDI valid after falling edge of SCLK	10			ns
t8	Time after $\overline{CS}$ rises until INT/HOLD to go high	8			ns
t9	Time between two words for transmitting	170			ns
t10	Time for SDO valid after SDI on bus, at V_{DD} = 5 V and load = 20 pF			40	ns

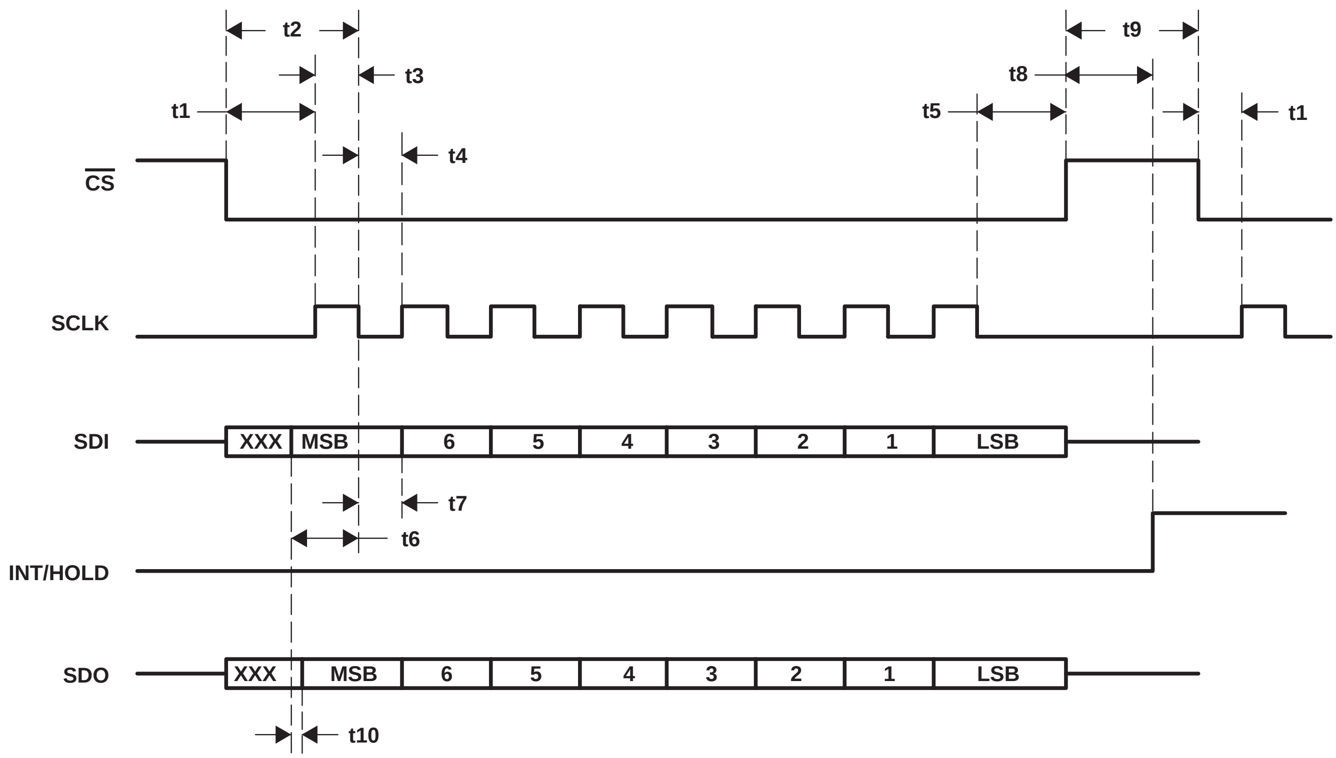


Figure 1. Serial Peripherial Interface (SPI)

This is an 8-bit SPI protocol used to communicate with the microcontroller in the system for setting various operating parameters.

When $\overline{CS}$ is held high, the signals on the SCLK and SDI lines are ignored and SDO is forced into a high-impedance state. SCLK must be low when $\overline{CS}$ is asserted low.

On each falling edge of the SCLK pulse after $\overline{CS}$ is asserted low, the new byte is serially shifted into the register. The most significant bit (MSB) is shifted first. Only eight bits in a frame are acceptable. When a number of bits shifted is different than the value eight, the information is ignored and the register retains the old setting.

The shift register transfers the data into a latch register after the eighth SCLK clock pulse and when $\overline{CS}$ transitions from low to high (see Figure 1).

The function of the integration mode is to ignore any SPI frame transmission when the INT/HOLD bit = 1. In the hold mode with INT/HOLD = 0, all necessary bytes may be transmitted.

function principle

The TPIC8101 is designed for knock sensor signal conditioning in automotive applications. The device is an analog interface between the engine acoustical sensors or accelerometers and the fuel management systems of a gasoline engine. The two wide-band amplifiers process signals from the piezoelectric sensors. Outputs of the amplifiers feed a channel select mux switch and then a 3^{rd} order antialiasing filter. This signal is converted using an analog-to-digital conversion (10 bits with a sampling frequency of 200 kHz) prior to the gain stage.

The gain stage is adjustable via the SPI to compensate for the knock energies. The gain setting is selectable up to 64 values ranging from 0.111 to 2.0.

The output of the gain stage feeds a band-pass filter circuit to process the particular frequency component associated with the engine and transducer.

The band-pass filter has a gain of two and a center frequency range between 1.22 kHz and 19.98 kHz (64-bit selection). The output from this stage is internally clamped.

The output from the band-pass filter is full-wave rectified with its output clamped below V_{DD}.

The full-wave rectified signals are integrated using an integrator time constant set by the SPI and integration time window set by the pulse width of INT/HOLD. At the start of each knock window, the integrator output is reset. The output of the integrator is internally clamped and the digital output may be directly interfaced to the microprocessor.

The integrated signal is converted to an analog format by a 10-bit DAC. The microprocessor may interface to this signal, reads this data, and adjusts the spark ignition timing to optimize fuel efficiency related to load versus engine RPM.

description of the functional terminals

supply voltage (V_{DD})

The V_{DD} terminal is the input supply for the IC, typically 5 V ±5% tolerant. A noise filter capacitor of 4.7 µF (typ) is required on this terminal to ensure stability of the internal circuits.

ground (GND)

The GND terminal is connected to the system ground rail.

reference supply (V_{ref})

The V_{ref} is an internally generated supply reference voltage for biasing the amplifier inputs. The terminal is used to decouple any noise in the system by placing an external capacitor of 22 nF (typ).

buffered integrator output (OUT)

The OUT terminal is the output of the integrated signal. This is an analog signal interfaced to the microprocessor A/D channel for data acquisition. A capacitor of 2.2 nF is used to stabilize the signal output.

integration/hold mode selection (INT/HOLD)

The INT/HOLD is an input control signal from the microprocessor to select either to integrate the sensed signal or to hold the data for acquisition. There is an internal pulldown on this terminal (default HOLD mode).

chip select for SPI ($\overline{CS}$)

The $\overline{CS}$ terminal allows serial communication to the IC through the SPI from a master controller. The chip select is active low with an internal pullup (default inactive).

description of the functional terminals (continued)

oscillator input (XIN)

The XIN terminal is the input to the inverter used for the oscillator circuit. An external clock signal from the MCU, crystal, or ceramic resonator is configured with resistors and capacitors. To bias the inverter, a resistor (1 MΩ typ) is placed across XIN and XOUT.

This clock signal is prescaled to set the internal sampling frequency of the A/D converter.

oscillator output (XOUT)

The XOUT terminal is the output of the inverter used for the oscillator circuit.

data output (SDO)

The SDO output is the SPI data bus reporting information back to the microprocessor. This is a 3-state output with the output set to high-impedance mode when $\overline{CS}$ is pulled to V_{DD}. The high-impedance state can also be programmed by setting a bit in the prescale word which takes precedence over the $\overline{CS}$ setting. The output is disabled when the $\overline{CS}$ terminal is pulled high (V_{DD}).

data input (SDI)

The SDI terminal is the communication interface for data transfer between the master and slave components. The SDI has an internal pullup to V_{DD}; the data stream is in 8-bit word format.

serial clock (SCLK)

The SCLK output signal is used for synchronous communication of data. Typically, the output from the master clock is low with the IC having an internal pullup resistor to V_{DD}. The data is clocked to the internal shift register on the falling clock edge.

test ($\overline{TEST}$)

The $\overline{TEST}$ terminal, when pulled low, allows the IC to enter the test mode. During normal operation, this terminal is left open or tied high (V_{DD}). There is an internal pullup to V_{DD} (default).

feedback output for amplifiers (CH1FB and CH2FB)

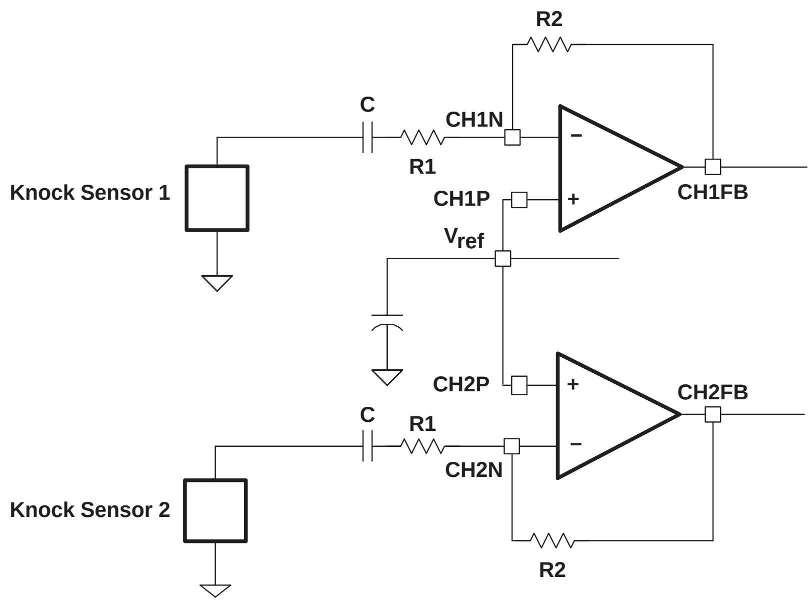
The CHXFB are amplifier outputs for the sensor signals. The gain of the respective amplifiers is set using the CHXFB and CHX input terminals (see Figure 1).

input amplifiers (CH1P, CH1N, CH2P, and CH2N)

CH1P, CH1N, CH2P, and CH2N are the inputs for the two amplifiers which interface to the external knock sensors.

The gain is set by external resistors R1 and R2. The inputs and outputs of the amplifier are rail-to-rail compatible to the supply V_{DD}.

An internal multiplexer selects the desired sensor signal to process programmable through the SPI.



NOTE: The series capacitor C is not mandatory and may be removed in some application circuits.

Figure 2. Input Signal Configuration

Table 1. Integrator Programming

DECIMAL VALUE (D4…D0)	INTEGRATOR TIME CONSTANT (µSEC)	BAND-PASS FREQUENCY (kHz)	GAIN	DECIMAL VALUE (D5…D0)	BAND-PASS FREQUENCY (kHz)	GAIN
0	40	1.22	2	32	4.95	0.421
1	45	1.26	1.882	33	5.12	0.4
2	50	1.31	1.778	34	5.29	0.381
3	55	1.35	1.684	35	5.48	0.364
4	60	1.4	1.6	36	5.68	0.348
5	65	1.45	1.523	37	5.9	0.333
6	70	1.51	1.455	38	6.12	0.32
7	75	1.57	1.391	39	6.37	0.308
8	80	1.63	1.333	40	6.64	0.296
9	90	1.71	1.28	41	6.94	0.286
10	100	1.78	1.231	42	7.27	0.276
11	110	1.87	1.185	43	7.63	0.267
12	120	1.96	1.143	44	8.02	0.258
13	130	2.07	1.063	45	8.46	0.25
14	140	2.18	1	46	8.95	0.236
15	150	2.31	0.944	47	9.5	0.222
16	160	2.46	0.895	48	10.12	0.211
17	180	2.54	0.85	49	10.46	0.2
18	200	2.62	0.81	50	10.83	0.19
19	220	2.71	0.773	51	11.22	0.182
20	240	2.81	0.739	52	11.65	0.174
21	260	2.92	0.708	53	12.1	0.167
22	280	3.03	0.68	54	12.6	0.16
23	300	3.15	0.654	55	13.14	0.154

Table 1. Integrator Programming (Continued)

DECIMAL VALUE (D4…D0)	INTEGRATOR TIME CONSTANT (μSEC)	BAND-PASS FREQUENCY (kHz)	GAIN	DECIMAL VALUE (D5…D0)	BAND-PASS FREQUENCY (kHz)	GAIN
24	320	3.28	0.63	56	13.72	0.148
25	360	3.43	0.607	57	14.36	0.143
26	400	3.59	0.586	58	15.07	0.138
27	440	3.76	0.567	59	15.84	0.133
28	480	3.95	0.548	60	16.71	0.129
29	520	4.16	0.5	61	17.67	0.125
30	560	4.39	0.471	62	18.76	0.118
31	600	4.66	0.444	63	19.98	0.111

PRINCIPLES OF OPERATION

system transfer equation

The output voltage may be derived from:

$$V_O = V_{IN} \times A_{IN} \times A_P \times A_{BP} \times A_{INT} \times \frac{t_{INT}}{\tau_C} \times A_O + V_{RESET}$$

where:

- V_{IN} = Input voltage peak (amplitude)
- V_O = Output voltage
- A_{IN} = Input amplifier gain setting
- A_P = Programmable gain setting
- A_{BP} = Gain of band-pass filter
- A_{INT} = Gain of integrator
- t_{INT} = Integration time from 0.5 ms to 10 ms
- A_O = Output buffer gain
- τ_C = Programmable integrator time constant
- V_{RESET} = Reset voltage from which the integration operation starts

If $A_{BP} = A_{INT} = 2$ and $A_{IN} = A_O = 1$,

then

$$V_O = V_{IN} \times A_P \times \frac{8}{\Pi} \times \frac{t_{INT}}{\tau_C} + V_{RESET}$$

programming in normal mode ($\overline{\text{TEST}}$ = 1)

To enable programming in the normal mode, the $\overline{\text{TEST}}$ terminal must be high. Communication is through the SPI and the $\overline{\text{CS}}$ terminal is used to enable the IC. The information on the SDI line consists of two parts: address and data.

After power up, the SPI is in default mode (see Table 2).

default SPI mode

The SPI is in the default mode on the power up sequence. In this case, the SDO directly equals the SDI (echo function). In this mode, five commands can be transmitted by the master controller to configure the IC (see Table 2).

PRINCIPLES OF OPERATION

Table 2. Default SPI Mode

NO.	CODE	COMMAND (t)	DATA	RESPONSE (t)
1	010 D[4:0]	Set the prescaler and SDO status	OSC_{IN} frequency D[4:1]=0000=> 4 MHz D[4:1]=0001=> 5 MHz D[4:1]=0010=> 6 MHz D[4:1]=0011=> 8 MHz D[4:1]=0100=> 10 MHz D[4:1]=0101=> 12 MHz D[4:1]=0110=> 16 MHz D[4:1]=0111=> 20 MHz D[4:1]=1000=> 24 MHz D[0]=0 => SDO active D[1]=1=> SDO high impedance	SDI (010 D[4:0])
2	1110 000 D[0]	Select the channel	D[0]=0 => Channel 1 selected D[1]=1=> Channel 2 selected	SDI (1110 000 D[0])
3	00 D[5:0]	Set the band-pass center frequency	D[5:0] (see Table 1)	SDI (00 D[5:0])
4	10 D[5:0]	Set the gain	D[5:0] (see Table 1)	SDI (10 D[5:0])
5	110 D[4:0]	Set the integration time constant	D[4:0] (see Table 1)	SDI (100 D[4:0])
6	0111 0001	Set SPI configuration to the advanced mode	None	SDI (0111 0001)

NOTE: Command #6 is to enter into the advanced mode.

advanced SPI mode

The advanced SPI mode has additional features to the default SPI mode. A control byte is written to the SDI and shifted with the MSB first. The response byte on the SDO is shifted out with the MSB first. The response byte corresponds to the previous command. Therefore, the SDI shifts in a control byte *n* and shifts out a response command byte n−1. Each control/response pair of commands requires two full 8-bit shift cycles to complete a transmission. The control bytes with the expected response are shown in Table 3.

In the advanced SPI mode, only a power-down condition may reset the SPI mode to the default state on the subsequent power-up cycle.

PRINCIPLES OF OPERATION

Table 3. Advanced SPI Mode

NO.	CODE	COMMAND (t)	DATA	RESPONSE (t)
1	010 D[4:0]	Set the prescaler and SDO status	OSC_{IN} frequency D[4:1]=0000=> 4 MHz D[4:1]=0001=> 5 MHz D[4:1]=0010=> 6 MHz D[4:1]=0011=> 8 MHz D[4:1]=0100=> 10 MHz D[4:1]=0101=> 12 MHz D[4:1]=0110=> 16 MHz D[4:1]=0111=> 20 MHz D[4:1]=1000=> 24 MHz D[0]=0 => SDO active D[1]=1=> SDO high impedance	Byte 1 (D7 to D0) of the digital integrator output
2	1110 000 D[0]	Select the channel	D[0]=0 => Channel 1 selected D[1]=1=> Channel 2 selected	D9 to D8 of digital integrator output followed by six zeros
3	00 D[5:0]	Set the band-pass center frequency	D[5:0] (see Table 1)	Byte 1 (MSB) of the 00000001
4	10 D[5:0]	Set the gain	D[5:0] (see Table 1)	Byte 2 (LSB) 11100000
5	110 D[4:0]	Set the integration time constant	D[4:0] (see Table 1)	SPI configuration (MSB)01110001(LSB)
6	0111 0001	Set SPI configuration to the advanced mode	None	Inverted SPI configuration (MSB)10001110(LSB)

digital data output from the TPIC8101

digital output

- Digital integrator output (10 bits, D[9:0])
- First response byte (MSB): 8 bits for D7 to D0 of the integrator output
- Second response byte (LSB): 2 bits for D9 to D8 of the integrator output followed by six zeros

programming examples

prescaler/SDO status

- 01000101 programs an input frequency of 6 MHz with SDO terminal in high impedance.

channel selection

- 1110001 selects channel 2.

band-pass frequency

- 00100111 programs a band-pass filter with center frequency of 6.37 kHz.

gain control

- 10010100 programs the gain with attenuation of 0.739.

integrator time constant

- 11000011 programs integrator time constant of 55 µs. The binary values are in Table 1 through Table 3.

programming in TEST mode ($\overline{\text{TEST}}$ = 0)

To enter test mode, the $\overline{\text{TEST}}$ terminal must be low. See Table 4 for the signal that may be accessed in this mode.

Table 4. Programming in TEST Mode

NO.	TEST DESCRIPTION	SDI COMMAND MSB…….LSB	RESPONSE	NOTE
T1	AAF individual test	1111 0000	ADC clock	Deactivates the input and output op amps AAF input connected to CH1FB terminal AAF output connected to OUT terminal
T2	In-line test to AAF output	1111 0000	None	Deactivates the output op amp AAF output connected to OUT terminal
T3	Output buffer individual test	1111 0010	None	Opens the feedback loop of the output buffer and deactivates the input op amp and AAF CH1FB connected to positive input terminal of op amp CH2FB connected to negative input terminal of op amp
T4	ADC/DAC individual test (with the output buffer)	1111 0011	ADC data	Deactivates the input op amps and AAF INT/HOLD = ADC_Sync OSC_{IN} = ADC_SCLK DAC shifted in from SDI terminal
T5	ADC/DAC individual test (without the output buffer)	1111 0100	ADC data	Deactivates the input op amps, AAF, and output buffer INT/HOLD = ADC_Sync OSC_{IN} = ADC_SCLK DAC is shifted in from SDI terminal
T6	In-line test to ADC output	1111 0011	ADC data	INT/HOLD = ADC_Sync OSC_{IN} = ADC_SCLK DAC shifted in from SDI terminal
T7	Reading of digital clamp flag	1111 1000	Clamp flag D[2:0]	Implies command 6 (advanced SPI mode) D[0]: Gain stage clamp status D[1]: BPF stage clamp status D[2]: INT stage clamp status D=0 => No clamp activated D=1 => Clamp activated

TYPICAL CHARACTERISTICS

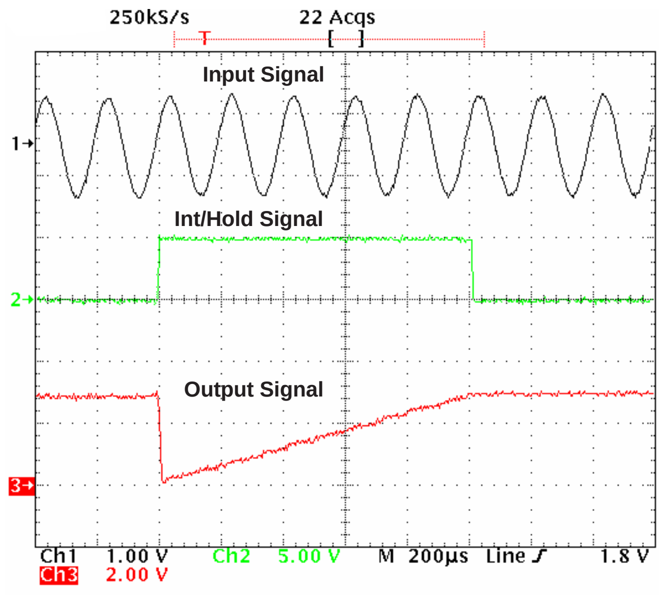


Figure 3. Amplified Input Signal Process

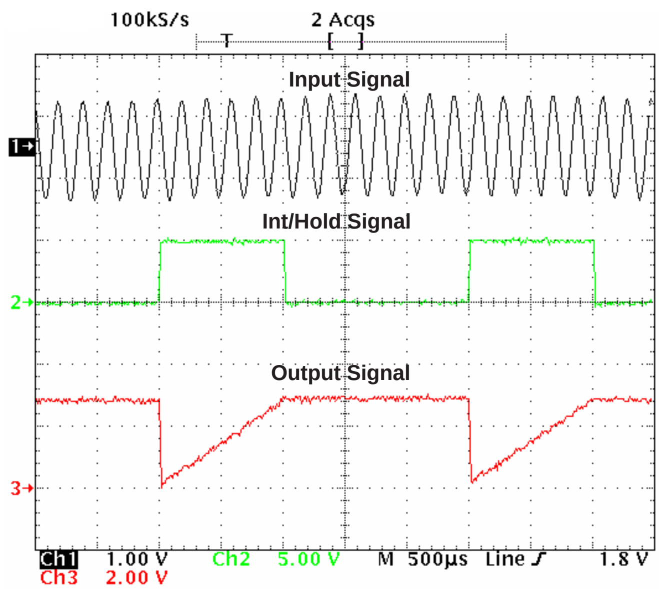
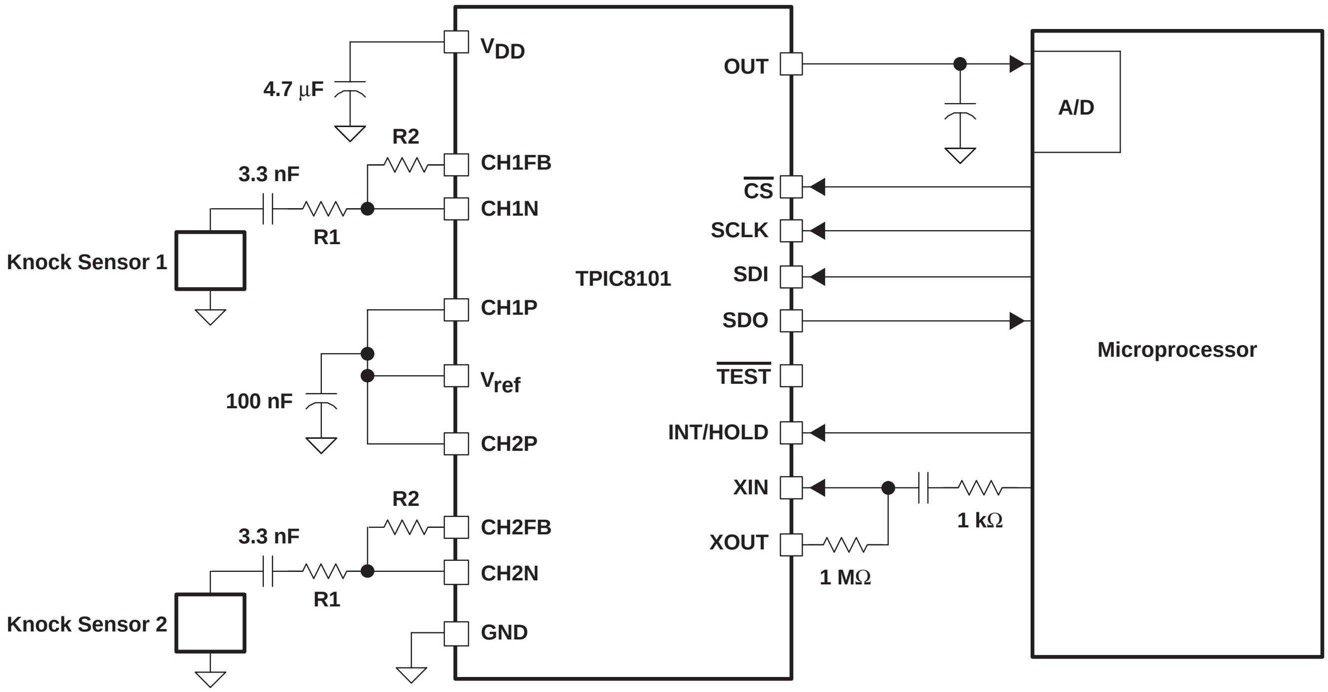


Figure 4. Input Signal Processing

application schematic



NOTE: R1 is greater than 25 kΩ.

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