Continuous Rate 10 Mbps to 2.7 Gbps Clock and Data Recovery ICs

Data Sheet

ADN2817/ADN2818

FEATURES

- Serial data input: 10 Mbps to 2.7 Gbps
- Exceeds ITU-T jitter specifications
- Integrated limiting amplifier
  - 5 mV p-p sensitivity (ADN2817 only)
- Adjustable slice level: ±100 mV (ADN2817 only)
- Patented dual-loop clock recovery architecture
- Programmable LOS detect (ADN2817 only)
- Integrated PRBS generator and detector
- No reference clock required
- Loss of lock indicator
- Supports double data rate
- Bit error rate monitor (BERMON) or sample phase adjust options
- Rate selectivity without the use of a reference clock
- I²C interface to access optional features
- Single-supply operation: 3.3 V
- Low power
  - 650 mW (ADN2817)
  - 600 mW (ADN2818)
- 5 mm × 5 mm 32-lead LFCSP

APPLICATIONS

- SONET OC-1, OC-3, OC-12, OC-48, and all associated FEC rates
- Fibre Channel, 2× Fibre Channel, GbE, HDTV
- WDM transponders
- Regenerators/repeaters
- Test equipment

GENERAL DESCRIPTION

The ADN2817/ADN2818 provide the receiver functions of quantization, signal level detect, and clock and data recovery for continuous data rates from 10 Mbps to 2.7 Gbps. The ADN2817/ADN2818 automatically lock to all data rates without the need for an external reference clock or programming. All SONET jitter requirements are exceeded, including jitter transfer, jitter generation, and jitter tolerance. All specifications are quoted for −40°C to +85°C ambient temperature, unless otherwise noted.

This device, together with a PIN diode and a TIA preamplifier, can implement a highly integrated, low cost, and low power fiber optic receiver.

The ADN2817/ADN2818 have many optional features available through an I²C interface. For example, the user can read back the data rate onto which the ADN2817 or ADN2818 is locked, or the user can set the device to lock only to one particular data rate if provisioning of data rates is required. A BERMON circuit provides an estimate of the received bit error rate (BER) without interruption of the data. Alternatively, the user can adjust the data sampling phase to optimize the received BER.

The ADN2817/ADN2818 are available in a compact 5 mm × 5 mm, 32-lead, lead frame chip scale package.

FUNCTIONAL BLOCK DIAGRAM

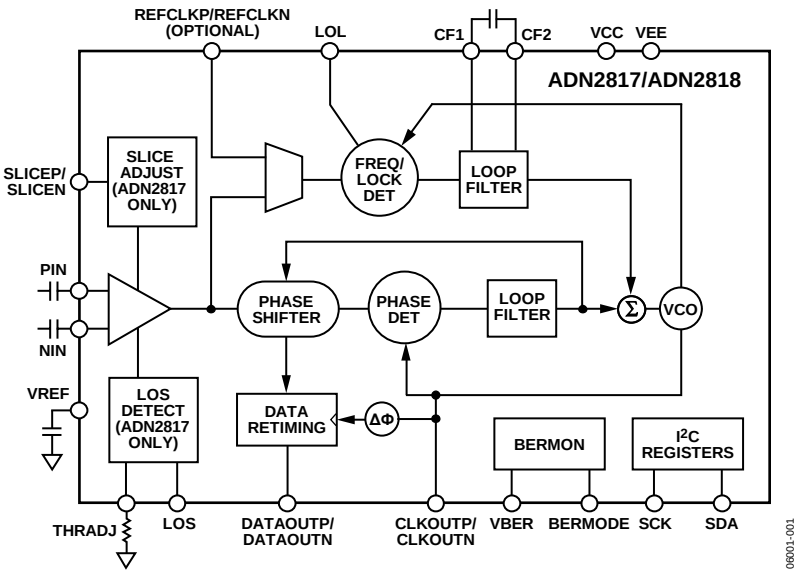


Figure 1.

Rev. E Document Feedback

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REVISION HISTORY

1/13 Rev. D to Rev. E

Moved Revision History Section 3
Change to Table 8 15
Changes to Table 15 17
Changes to Rate Selectivity Section 28

1/12—Rev. C to Rev. D

Changes to Figure 14 12
Updated Outline Dimensions 37

3/10—Rev. B to Rev. C

Changes to Features Section and Applications Section 1
Changes to Thermal Resistance Section 9
Added Table 6; Renumbered Sequentially 9
Changes to Table 7 10
Changes to Table 8 14
Changes to Table 14 15
Deleted Table 16; Renumbered Sequentially 16
Changes to Table 16 16
Changes to I^2C Interface Section 24
Changed f_{REF} Ratio to DIV_FREF Ratio 25
Changes to Initiate Frequency Acquisition, Rate Selectivity, Double Data Rate Mode, and PRBS Generator/Detector Sections 27
Changes to Table 19 32
Changes to Table 20 34

2/09—Rev. A to Rev. B

Updated Outline Dimensions 37
Changes to Ordering Guide 37

8/08—Rev. 0 to Rev. A

Changes to Features Section, General Description Section, and Figure 1 1
Added Bit Rate Monitor Specifications Section and Table 4; Renumbered Sequentially 7
Changes to Figure 5 and Table 6 10
Changes to Table 7 and Table 8 14
Changes to Table 14 15
Added Table 15 15
Added Table 16 16
Added Sample Phase Adjust Section and Bit Error Rate (BER) Monitor Section 23
Added Figure 32; Renumbered Sequentially 24
Changes to Figure 36 29
Added Exposed Pad Notation to Outline Dimensions 37

7/07—Revision 0: Initial Version

SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, SLICEP = SLICEN = VEE, input data pattern: PRBS $2^{23} - 1$, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
QUANTIZER—DC CHARACTERISTICS					
Input Voltage Range	At PIN or NIN, dc-coupled	1.8		2.8	V
Peak-to-Peak Differential Input	PIN − NIN			2.0	V
Input Common-Mode Level	DC-coupled (see Figure 40, Figure 41, and Figure 42)	2.3	2.5	2.8	V
Differential Input Sensitivity	$2^{23} - 1$ PRBS, ac-coupled,[1] BER = 1×10^{-10}				
	ADN2817	10	5		mV p-p
	ADN2818	200			mV p-p
QUANTIZER—AC CHARACTERISTICS					
Data Rate		10		2700	Mbps
S11	At 2.5 GHz		−15		dB
Input Resistance	Differential		100		Ω
Input Capacitance			0.65		pF
QUANTIZER—SLICE ADJUSTMENT	ADN2817 only				
Gain	SLICEP − SLICEN = ±0.5 V	0.10	0.11	0.13	V/V
Differential Control Voltage Input	SLICEP − SLICEN	−0.95		+0.95	V
Control Voltage Range	DC level @ SLICEP or SLICEN	VEE		0.95	V
Slice Threshold Offset			±1		mV
LOSS OF SIGNAL DETECT (LOS)	ADN2817 only				
Loss of Signal Detect Range (See Figure 6)	R_{Thresh} = 0 Ω	14.2		20.0	mV
	R_{Thresh} = 100 kΩ	2.1		5.0	mV
Hysteresis (Electrical)					
OC-48	R_{Thresh} = 0 Ω	6.2		8.2	dB
	R_{Thresh} = 100 kΩ	4.7		7.7	dB
OC-1	R_{Thresh} = 0 Ω	4.9		7.5	dB
	R_{Thresh} = 10 kΩ	3.0		7.3	dB
LOS Assert Time	DC-coupled[2]		450		ns
LOS Deassert Time	DC-coupled[2]		500		ns
LOSS OF LOCK DETECT (LOL)					
VCO Frequency Error for LOL Assert	With respect to nominal		1000		ppm
VCO Frequency Error for LOL Deassert	With respect to nominal		250		ppm
LOL Response Time					
OC-48			1.0		µs
OC-12			1.0		µs
10 Mbps			500		µs
ACQUISITION TIME					
Lock to Data Mode					
OC-48			1.3		ms
OC-12			2.0		ms
OC-3			3.4		ms
OC-1			9.8		ms
10 Mbps			40.0		ms
Optional Lock to REFCLK Mode			10.0		ms
DATA RATE READBACK ACCURACY					
Coarse Readback	See Table 19		10		%
Fine Readback	In addition to REFCLK accuracy			100	ppm

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Voltage		3.0	3.3	3.6	V
Current					
ADN2817			210	247	mA
ADN2818			180	217	mA
OPERATING TEMPERATURE RANGE		−40		+85	°C

[1] PIN and NIN should be differentially driven and ac-coupled for optimum sensitivity.
[2] When ac-coupled, the LOS assert and deassert time is dominated by the RC time constant of the ac coupling capacitor and the 50 Ω input termination of the ADN2817 input stage.

JITTER SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, SLICEP = SLICEN = VEE, input data pattern: PRBS $2^{23} - 1$, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
PHASE-LOCKED LOOP CHARACTERISTICS					
Jitter Transfer Bandwidth					
OC-48			548	839	kHz
OC-12			93	137	kHz
OC-3			30	40	kHz
Jitter Peaking					
OC-48			0	0.03	dB
OC-12			0	0.03	dB
OC-3			0	0.03	dB
Jitter Generation					
OC-48	12 kHz to 20 MHz		0.001	0.003	UI rms
			0.02	0.046	UI p-p
OC-12	12 kHz to 5 MHz		0.001	0.004	UI rms
			0.01	0.036	UI p-p
OC-3	12 kHz to 1.3 MHz		0.001	0.004	UI rms
			0.01	0.023	UI p-p
Jitter Tolerance	$2^{23} - 1$ PRBS				
OC-48	600 Hz[1]	92.0			UI p-p
	6 kHz[1]	20.0			UI p-p
	100 kHz	7.0			UI p-p
	1 MHz[1]	1.00			UI p-p
	20 MHz	0.53			UI p-p
OC-12	30 Hz[1]	100.0			UI p-p
	300 Hz[1]	44.0			UI p-p
	25 kHz	7.35			UI p-p
	250 kHz[1]	1.00			UI p-p
	5 MHz	0.52			UI p-p
OC-3	30 Hz[1]	50.0			UI p-p
	300 Hz[1]	23.5			UI p-p
	6500 Hz	6.71			UI p-p
	65 kHz[1]	1.00			UI p-p
	130 kHz	0.54			UI p-p

[1] Jitter tolerance of the ADN2817/ADN2818 at these jitter frequencies is better than what the test equipment is able to measure.

OUTPUT AND TIMING SPECIFICATIONS

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
CML OUPUT CHARACTERISTICS (CLKOUTP/CLKOUTN, DATAOUTP/DATAOUTN)					
Single-Ended Output Swing, V_{SE}	See Figure 3	300	350	600	mV
Differential Output Swing, V_{DIFF}	See Figure 3	600	700	1200	mV
Output Voltage					
High, V_{OH}				VCC	V
Low, V_{OL}		VCC − 0.6	VCC − 0.35	VCC − 0.3	V
CML Outputs Timing					
Rise Time	20% to 80%		80	112	ps
Fall Time	80% to 20%		80	123	ps
Setup Time, t_S	See Figure 2, OC-48	150	200	250	ps
Hold Time, t_H	See Figure 2, OC-48	150	200	250	ps
Setup Time, t_{DDRS}	See Figure 4, OC-48	140	170	200	ps
Hold Time, t_{DDRH}	See Figure 4, OC-48	200	230	260	ps
I^2C INTERFACE DC CHARACTERISTICS	LVCMOS				
Input Voltage					
High, V_{IH}		0.7 VCC			V
Low, V_{IL}				0.3 VCC	V
Input Current	V_{IN} = 0.1 VCC or V_{IN} = 0.9 VCC	−10.0		+10.0	µA
Output Low Voltage	V_{OL}, I_{OL} = 3.0 mA			0.4	V
I^2C INTERFACE TIMING	See Figure 22				
SCK Clock Frequency				400	kHz
SCK Pulse Width High					
High, t_{HIGH}		600			ns
Low, t_{LOW}		1300			ns
Start Condition					
Hold Time, $t_{HD;STA}$		600			ns
Setup Time, $t_{SU;STA}$		600			ns
Data					
Setup Time, $t_{SU;DAT}$		100			ns
Hold Time, $t_{HD;DAT}$		300			ns
SCK/SDA Rise/Fall Time, t_R/t_F		20 + 0.1 Cb		300	ns
Stop Condition Setup Time, $t_{SU;STO}$		600			ns
Bus Free Time Between a Stop and a Start, t_{BUF}		1300			ns
REFCLK CHARACTERISTICS	Optional lock to REFCLK mode				
Input Voltage Range	At REFCLKP or REFCLKN				
V_{IL}			0		V
V_{IH}			VCC		V
Minimum Differential Input Drive			100		mV p-p
Reference Frequency		10		200	MHz
Required Accuracy			100		ppm

Parameter	Conditions	Min	Typ	Max	Unit
LVTTL DC INPUT CHARACTERISTICS					
Input Voltage					
High, V_{IH}		2.0			V
Low, V_{IL}				0.8	V
Input Current					
High	I_{IH}, V_{IN} = 2.4 V			+5	μA
Low	I_{IL}, V_{IN} = 0.4 V	−5			μA
LVTTL DC OUTPUT CHARACTERISTICS					
Output Voltage					
High	V_{OH}, I_{OH} = −2.0 mA	2.4			V
Low	V_{OL}, I_{OL} = +2.0 mA			0.4	V

BIT ERROR RATE MONITOR SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, SLICEP = SLICEN = VEE, input data pattern: PRBS $2^{23} - 1$, unless otherwise noted.

Table 4.

Parameter	Conditions	Min	Typ	Max	Unit
BERMON Extrapolation Mode	I^2C-controlled eye profiling				
Final Computed BER Accuracy	Input BER range 1×10^{-3} to 1×10^{-12}, input deterministic jitter (DJ) < 0.4 UI, DJ ceiling > 1×10^{-2}; asymmetry < 0.1 UI; requires external data processing algorithms to implement Q factor extrapolation		±1		Decades
Number of Bits (NUMBITS)	Number of data bits to collect pseudo errors; user programmable in increment factors of 2^3 over the range 2^{18} to 2^{39}	2^{18}		2^{39}	UI
Pseudo BER (PBER) Measurement Time			NUMBITS/ data rate		sec
BER Range				5×10^{-2}	BER
Sample Phase Adjust Resolution			6		Degrees
Sample Phase Adjust Accuracy			<6		Degrees
Sample Phase Adjust Range	With respect to normal sampling instant	−0.5		+0.5	UI
Minimum Input Signal Level	Differential peak to peak	4			mV
Power Increase	BER enabled		160		mW
	BER standby		77		mW
BERMON Voltage Output Mode	Analog voltage output				
BER Accuracy	Input BER range 1×10^{-3} to 1×10^{-9}, input DJ = 0 UI, DJ ceiling > 1×10^{-2}; asymmetry = 0 UI; BER is read as a voltage on the VBER pin, when the BER mode pin = VEE		±1		Decades
	Input BER range 1×10^{-3} to 1×10^{-9}, input DJ = 0.2 UI, DJ ceiling > 1×10^{-2}; asymmetry = 0 UI; BER is read as a voltage on the VBER pin, when the BER mode pin = VEE		+1/−2		Decades
NUMBITS	Number of data bits to collect pseudo errors		2^{27}		UI
Measurement Time	2.5 Gbps		0.054		sec
	1 Gbps		0.134		sec
	155 Mbps		0.865		sec
	10 Mbps		1.34		sec
VBER Voltage Range	Via 3 kΩ resistor to VEE	0.1		0.9	V
Minimum Input Signal Level	Differential peak to peak	4			mV
Power Increase	BER voltage mode		160		mW
Sample Phase Adjust Mode					
Sample Phase Adjust Step Size	Monotonic		6		Degrees
Sample Phase Adjust Accuracy			<6		Degrees
Sample Phase Adjust Range	With respect to normal sampling instant	−0.5		+0.5	UI
Power Increase			160		mW

TIMING CHARACTERISTICS

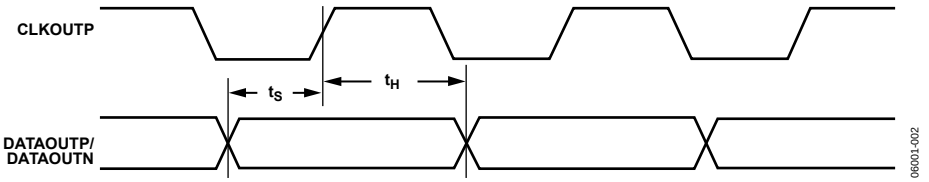


Figure 2. Default Mode Output Timing

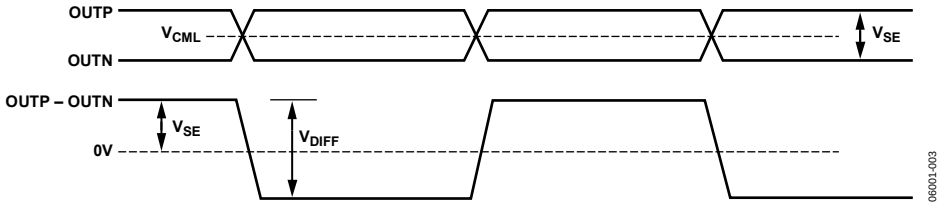


Figure 3. Single-Ended vs. Differential Output Specifications

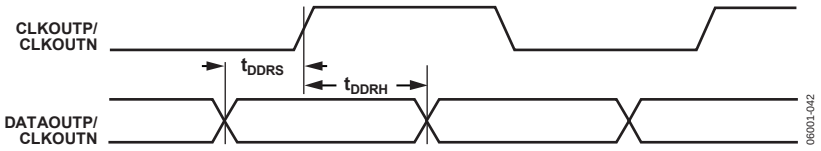


Figure 4. Double Data Rate Mode Output Timing

ABSOLUTE MAXIMUM RATINGS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, SLICEP = SLICEN = VEE, unless otherwise noted.

Table 5.

Parameter	Rating
Supply Voltage (VCC)	4.2 V
Input Voltage (All Inputs)	
Minimum	VEE − 0.4 V
Maximum	VCC + 0.4 V
Junction Temperature, Maximum	125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages, on a 4-layer board with the exposed paddle soldered to VEE.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
32-Lead LFCSP	28	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

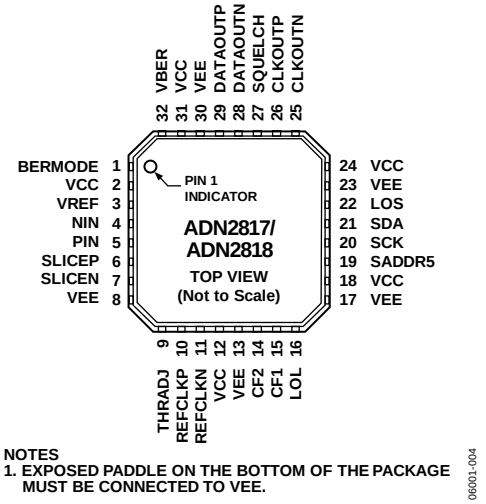


Figure 5. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	BERMODE	DI	Set this pin to logic low to enable analog voltage output mode for BER monitor.
2	VCC	P	Power for Input Stage, LOS.
3	VREF	AO	Internal VREF Voltage. Decouple to ground with a 0.1 µF capacitor.
4	NIN	AI	Differential Data Input. CML.
5	PIN	AI	Differential Data Input. CML.
6	SLICEP	AI	Differential Slice Level Adjust Input.
7	SLICEN	AI	Differential Slice Level Adjust Input.
8	VEE	P	GND for the Limiting Amplifier, LOS.
9	THRADJ	AI	LOS Threshold Setting Resistor.
10	REFCLKP	DI	Differential REFCLK Input. 10 MHz to 200 MHz.
11	REFCLKN	DI	Differential REFCLK Input. 10 MHz to 200 MHz.
12	VCC	P	VCO Power.
13	VEE	P	VCO Ground.
14	CF2	AO	Frequency Loop Capacitor.
15	CF1	AO	Frequency Loop Capacitor.
16	LOL	DO	Loss of Lock Indicator. Active high, LVTTL.
17	VEE	P	FLL Detector Ground.
18	VCC	P	FLL Detector Power.
19	SADDR5	DI	Slave Address Bit 5.
20	SCK	DI	I^2C Clock Input.
21	SDA	DI	I^2C Data Input.
22	LOS	DO	Loss of Signal Detect Output. Active high, LVTTL.
23	VEE	P	Output Buffer, I^2C Ground.
24	VCC	P	Output Buffer, I^2C Power.
25	CLKOUTN	DO	Differential Recovered Clock Output. CML.
26	CLKOUTP	DO	Differential Recovered Clock Output. CML.
27	SQUELCH	DI	Disable Clock and Data Outputs. Active high, LVTTL.
28	DATAOUTN	DO	Differential Recovered Data Output. CML.
29	DATAOUTP	DO	Differential Recovered Data Output. CML.
30	VEE	P	Phase Detector, Phase Shifter Ground.
31	VCC	P	Phase Detector, Phase Shifter Power.
32	VBER	AO	This pin represents BER when analog BERMON is enabled with 3 kΩ to VEE.
EP	EPAD	P	Exposed Paddle. The Exposed paddle on the bottom of the package must be connected to VEE.

[1] P = power, AI = analog input, AO = analog output, DI = digital input, DO = digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

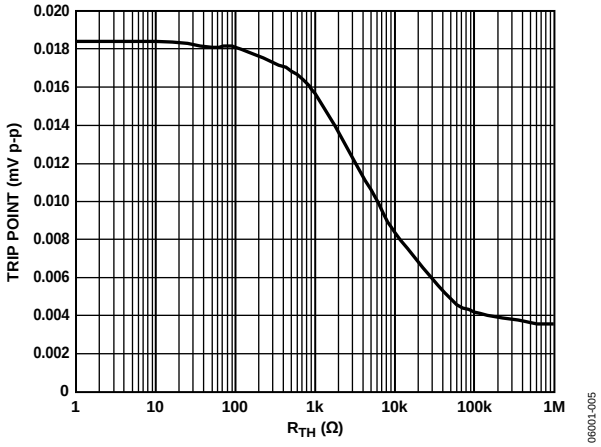


Figure 6. LOS Comparator Trip Point Programming

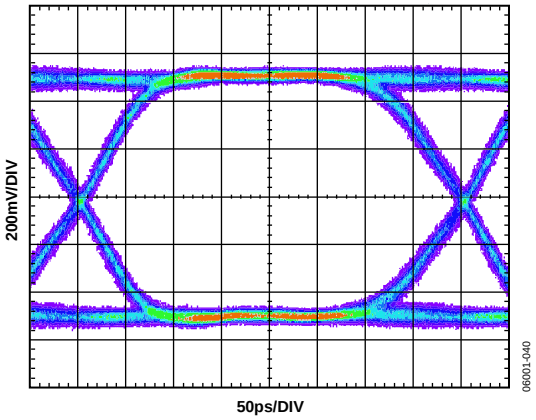


Figure 9. Output Eye, OC-48

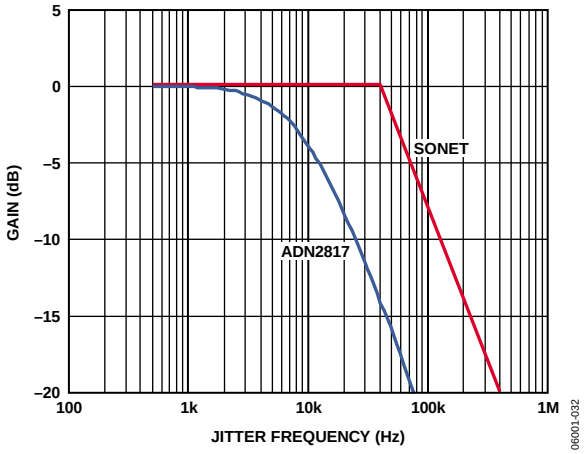


Figure 7. Jitter Transfer, OC-1

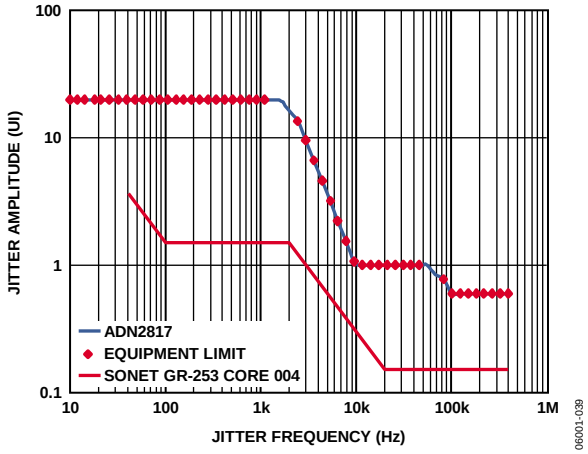


Figure 10. Jitter Tolerance, OC-1

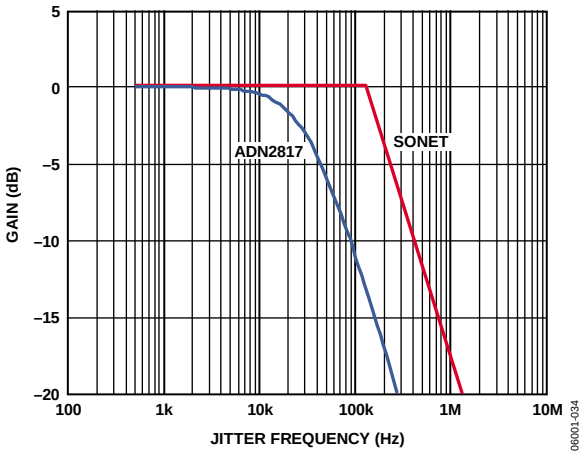


Figure 8. Jitter Transfer, OC-3

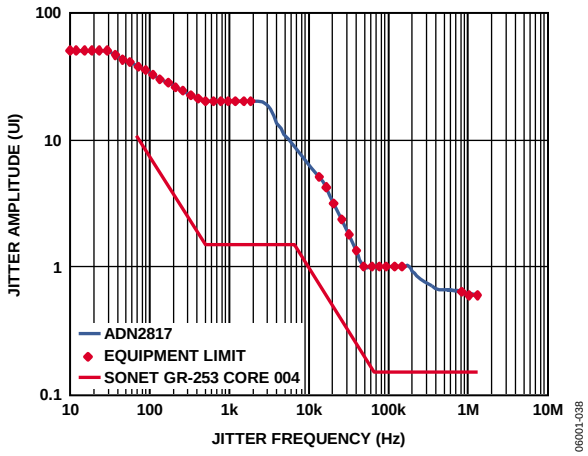


Figure 11. Jitter Tolerance, OC-3

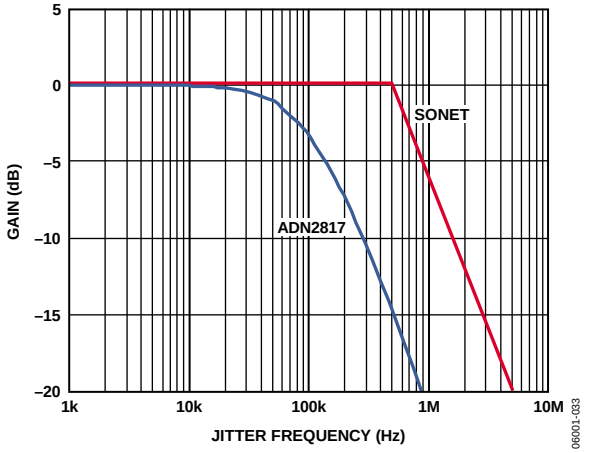


Figure 12. Jitter Transfer, OC-12

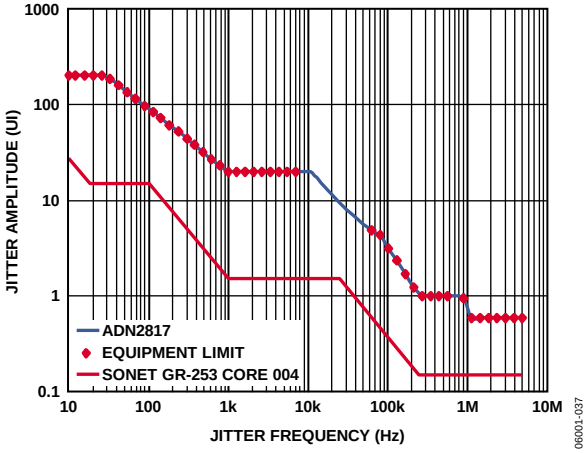


Figure 15. Jitter Tolerance, OC-12

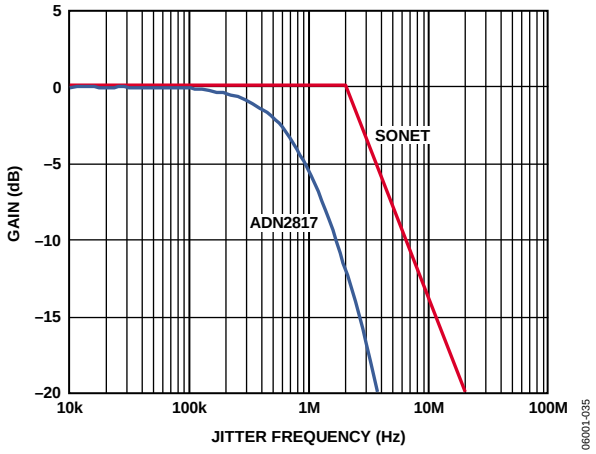


Figure 13. Jitter Transfer, OC-48

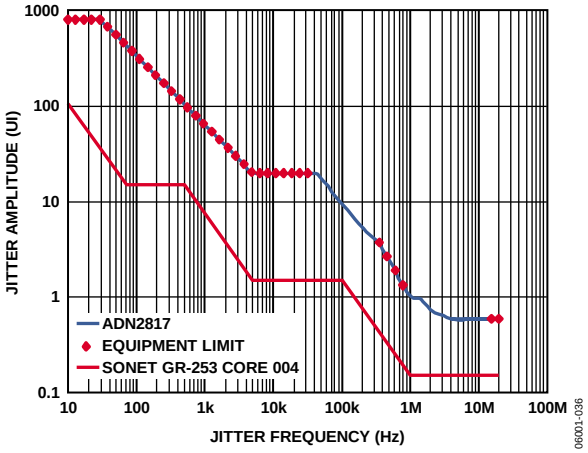


Figure 16. Jitter Tolerance, OC-48

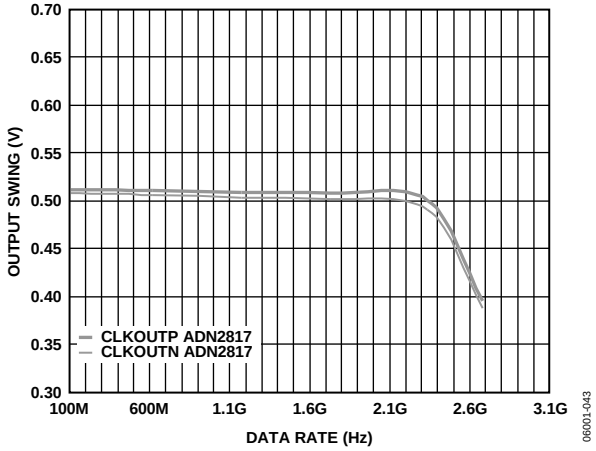


Figure 14. Output Swing vs. Data Rate

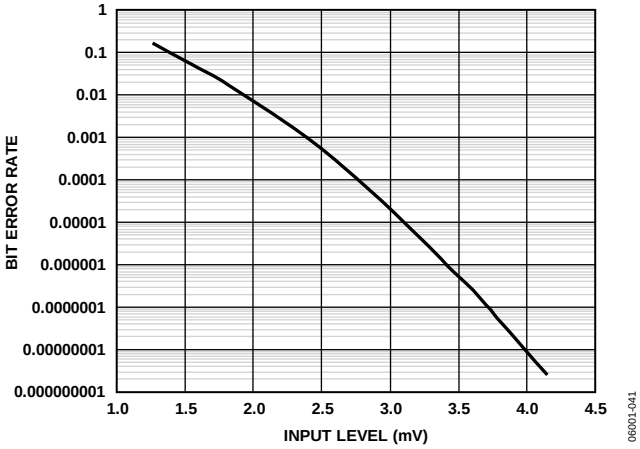


Figure 17. Bit Error Rate vs. Input Level

I²C-INTERFACE TIMING AND INTERNAL REGISTER DESCRIPTION

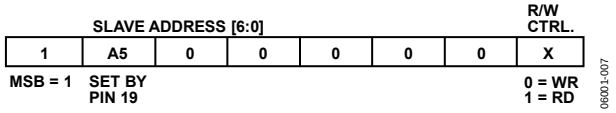


Figure 18. Slave Address Configuration

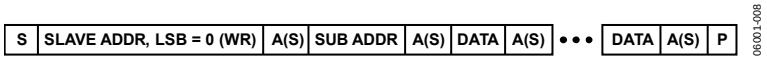


Figure 19. I²C Write Data Transfer

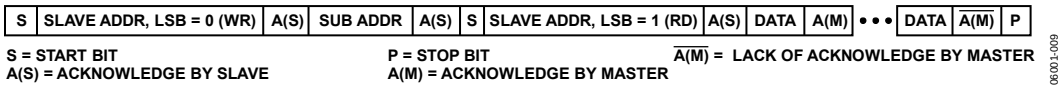


Figure 20. I²C Read Data Transfer

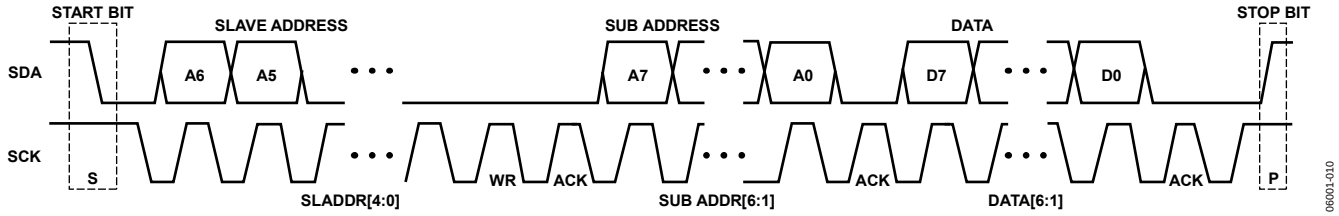


Figure 21. I²C Data Transfer Timing

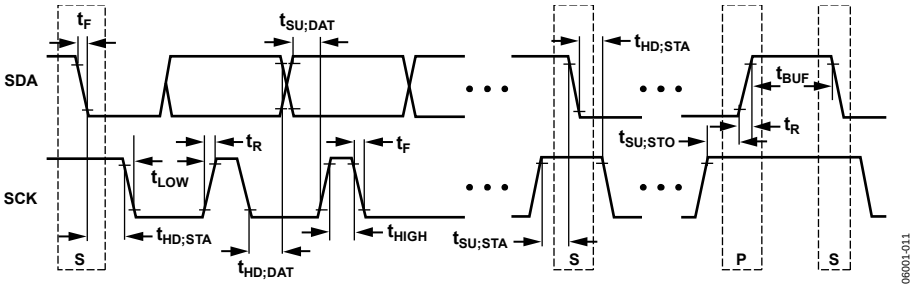


Figure 22. I²C Port Timing Diagram

Table 8. Internal Register Map[1]

Reg Name	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0
FREQ0	R	0x00	MSB							LSB
FREQ1	R	0x01	MSB							LSB
FREQ2	R	0x02	0	MSB						LSB
Rate	R	0x03	COARSE_RD[8:1]							
MISC	R	0x04	X	X	LOS status	Static LOL	LOL status	Data rate measurement complete	X	COARSE_RD[0] (LSB)
CTRLA	W	0x08	f_{REF} range		Data rate/DIV_FREF ratio				Measure data rate	Lock to REFCLK
CTRLA_RD	R	0x05	Readback CTRLA							
CTRLB	W	0x09	Config LOL	Reset MISC[4]	Initiate freq acquisition	0	Reset MISC[2]	0	0	0
CTRLB_RD	R	0x06	Readback CTRLB							
CTRLC	W	0x11	0	0	0	0	0	Config LOS	Squelch mode	0
CTRLD	W	0x22	CDR bypass	Disable DATAOUT buffer	Disable CLKOUT buffer	0	Initiate PRBS sequence	PRBS mode		
CTRLE/BERCTLB[2]	W	0x1F	0	0	Enable BERMON	BER stdby mode	0	PRBS/DDR enable and output mode		
SEL_MODE	W	0x34	0	0	0	0	Limited rate mode	0	CLK holdover mode	0
HI_CODE	W	0x35	HI_CODE[8:1]							
LO_CODE	W	0x36	LO_CODE[8:1]							
CODE_LSB	W	0x39	0	0	0	0	0	0	HI_CODE[0] (LSB)	LO_CODE[0] (LSB)
BERCTLA	W	0x1E	BER timer (NUMBITS)			0	BER start pulse	Error count byte select, for example, 011 = Byte 3 of 5 (NUMERRORS[39:0])		
BERSTS	R	0x20	X	X	X	X	X	X	X	End of BER measurement (EOBM)
BER_RES	R	0x21	BER_RES[7:0], one byte of pseudo BER measurement result (NUMERRORS[39:0])							
BER_DAC	R	0x24	X	X	BER_DAC[5:0], input to BER DAC in analog BERMON mode					
Phase	W	0x37	0	0	Phase[5:0], twos complement sample phase adjustment, phase code range is from −30 decimal to +30 decimal, which gives a sampling phase offset range from −0.5 UI to +0.5 UI; for example, phase = 111010 is−6 decimal, which gives a sampling phase offset of −6/+60 = −0.1 UI					

[1] X = don't care.
[2] Both CTRLE and BERCTLB registers are used, depending on the application.

Table 9. Miscellaneous Register, MISC

		LOS Status	Static LOL	LOL Status	Data Rate Measurement Complete		COARSE_RD[0] (LSB)
D7	D6	D5	D4	D3	D2	D1	D0
X	X	0 = no loss of signal 1 = loss of signal	0 = waiting for next LOL 1 = static LOL until reset	0 = locked 1 = acquiring	0 = measuring data rate 1 = measurement complete	X	COARSE_RD[0]

Table 10. Control Register, CTRLA

f_{REF} Range			Data Rate/DIV_FREF Ratio					Measure Data Rate	Lock to REFCLK
D7	D6	Range	D5	D4	D3	D2	Ratio	D1	D0
Set to 0	Set to 0	10 MHz to 25 MHz	0	0	0	0	1	Set to 1 to measure data rate	0 = lock to input data
Set to 0	Set to 1	25 MHz to 50 MHz	0	0	0	1	2		1 = lock to reference clock
Set to 1	Set to 0	50 MHz to 100 MHz	0	0	1	0	4		
Set to 1	Set to 1	100 MHz to 200 MHz			n		2^n		
			1	0	0	0	256		

Table 11. Control Register, CTRLB

Config LOL	Reset MISC[4]	Initiate Freq Acquisition		Reset MISC[2]			
D7	D6	D5	D4	D3	D2	D1	D0
0 = LOL pin normal operation 1 = LOL pin is static LOL	Write a 1 followed by 0 to reset MISC[4]	Write a 1 followed by 0 to initiate a frequency acquisition	Set to 0	Write a 1 followed by 0 to reset MISC[2]	Set to 0	Set to 0	Set to 0

Table 12. Control Register, CTRLC

					Configure LOS	Squelch Mode	
D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	0 = active high LOS 1 = active low LOS	0 = squelch CLK and DATA 1 = squelch CLK or DATA	Set to 0

Table 13. Control Register, CTRLD

CDR Bypass	Disable DATAOUT Buffer	Disable CLKOUT Buffer		Initiate PRBS Sequence	PRBS Mode			
D7	D6	D5	D4	D3	D2	D1	D0	Function
0 = CDR enabled 1 = CDR disabled	0 = data buffer enabled 1 = data buffer disabled	0 = CLK buffer enabled 1 = CLK buffer disabled	Set to 0	Write a 1 followed by 0 to initiate a PRBS generate sequence	0	0	0	Power-down PRBS
					0	0	1	Generate mode
					1	0	0	Detect mode

Table 14. Control Registers, CTRLE/BERCTLB

		Enable BERMON	BER Stdby Mode		PRBS/DDR Enable and Output Mode			
D7	D6	D5	D4	D3	D2	D1	D0	Function
Set to 0	Set to 0	1 = BERMON enabled 0 = BERMON disabled	1 = place BERMON in low power standby mode 0 = BERMON ready	Set to 0	0	0	0	Normal data rate output mode
					0	0	1	Offset decision circuit (ODC) output mode[1]
					0	1	0	Enable DDR mode (double data rate mode)
					0	1	1	Offset decision circuit (ODC) output in DDR mode[1]
					1	0	1	Enable PRBS detector/generator
					All other combinations reserved			

[1] See AN-941 Application Note, *BER Monitor User Guide*.

Table 15. Mode Select Register, SEL_MODE

						CLK Holdover Mode	
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Set to 0	Set to 0	Set to 0	Set to 0	Default 0 Limited rate enable = 1	Set to 0	Set to 1 for clock holdover mode	Set to 0

Table 16. BER Control Register, BERCTLA

BER Timer (NUMBITS)					BER Start Pulse	Error Count Byte Select (NUMERRORS[39:0])			
D7	**D6**	**D5**	**No. of Bits**	**D4**	**D3**	**D2**	**D1**	**D0**	**Byte Selection**
0	0	0	2^{18} bits	Set to 0	Write a 1 followed by a 0 to initiate BER measurement	0	0	0	Byte 0
0	0	1	2^{21} bits			0	0	1	Byte 1
0	1	0	2^{24} bits			0	1	0	Byte 2
0	1	1	2^{27} bits			0	1	1	Byte 3
1	0	0	2^{30} bits			1	0	0	Byte 4
1	0	1	2^{33} bits						
1	1	0	2^{36} bits						
1	1	1	2^{39} bits						

TERMINOLOGY

INPUT SENSITIVITY AND INPUT OVERDRIVE

Sensitivity and overdrive specifications for the quantizer involve offset voltage, gain, and noise. The relationship between the logic output of the quantizer and the analog voltage input is shown in Figure 23. For sufficiently large positive input voltages, the output is always Logic 1 and, similarly for negative inputs, the output is always Logic 0. However, the transitions between Output Logic Level 1 and Output Logic Level 0 are not at precisely defined input voltage levels but occur over a range of input voltages. Within this range of input voltages, the output may be either 1 or 0, or it may even fail to attain a valid logic state. The width of this zone is determined by the input voltage noise of the quantizer. The center of the zone is the quantizer input offset voltage. Input overdrive is the magnitude of signal required to guarantee the correct logic level with 1×10^{-10} confidence level.

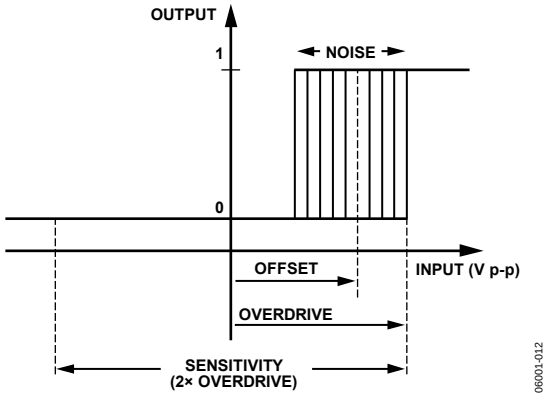


Figure 23. Input Sensitivity and Input Overdrive

SINGLE-ENDED vs. DIFFERENTIAL

AC coupling is typically used to drive the inputs to the quantizer. The inputs are internally dc biased to a common-mode potential of ~2.5 V. Driving the ADN2817/ADN2818 single-ended and observing the quantizer input with an oscilloscope probe at the point indicated in Figure 24 shows a binary signal with an average value equal to the common-mode potential and instantaneous values both above and below the average value. It is convenient to measure the peak-to-peak amplitude of this signal and call the minimum required value the quantizer sensitivity. Referring to Figure 24, because both positive and negative offsets need to be accommodated, the sensitivity is twice the overdrive. The ADN2817 quantizer typically has 5 mV p-p sensitivity. The ADN2818 does not have a limiting amplifier at its input. The input sensitivity for the ADN2818 is 200 mV p-p.

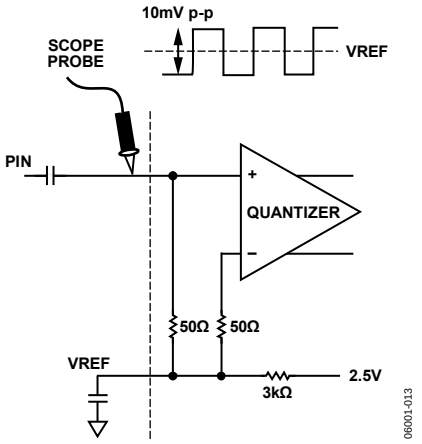


Figure 24. Single-Ended Sensitivity Measurement

Differentially driving the ADN2817 (see Figure 25), sensitivity seems to improve from observing the quantizer input with an oscilloscope probe. This is an illusion caused by the use of a single-ended probe. A 5 mV p-p signal appears to drive the ADN2817 quantizer. However, the single-ended probe measures only half the signal. The true quantizer input signal is twice this value because the other quantizer input is a complementary signal to the signal being observed.

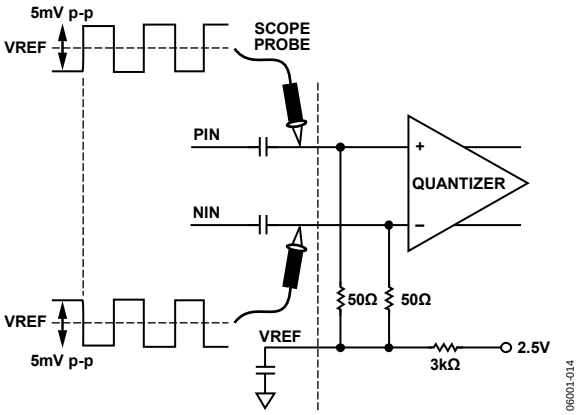


Figure 25. Differential Sensitivity Measurement

LOS RESPONSE TIME

The LOS response time is the delay between the removal of the input signal and the indication of the loss of signal at the LOS output, Pin 22. When the inputs are dc-coupled, the LOS assert time of the ADN2817 is 450 ns typically and the deassert time is 500 ns typically. In practice, the time constant produced by the ac coupling at the quantizer input and the 50 Ω on-chip input termination determine the LOS response time.

JITTER SPECIFICATIONS

The ADN2817/ADN2818 CDR is designed to achieve the best bit error rate (BER) performance and exceeds the jitter transfer, generation, and tolerance specifications proposed for SONET/SDH equipment defined in the Telcordia® Technologies specification.

Jitter is the dynamic displacement of digital signal edges from their long-term average positions, measured in unit intervals (UI), where 1 UI = 1 bit period. Jitter on the input data can cause dynamic phase errors on the recovered clock sampling edge. Jitter on the recovered clock causes jitter on the retimed data.

The following sections briefly summarize the specifications of jitter generation, transfer, and tolerance in accordance with the Telcordia document (*GR-253-CORE*, Issue 3, September 2000) for the optical interface at the equipment level and the ADN2817/ADN2818 performance with respect to those specifications.

JITTER GENERATION

The jitter generation specification limits the amount of jitter that can be generated by the device with no jitter and wander applied at the input. For OC-48 devices, the band-pass filter has a 12 kHz high-pass cutoff frequency with a roll-off of 20 dB/decade and a low-pass cutoff frequency of at least 20 MHz. The jitter generated must be less than 0.01 UI rms and must be less than 0.1 UI p-p.

JITTER TRANSFER

The jitter transfer function is the ratio of the jitter on the output signal to the jitter applied on the input signal vs. the frequency. This parameter measures the limited amount of the jitter on an input signal that can be transferred to the output signal (see Figure 26).

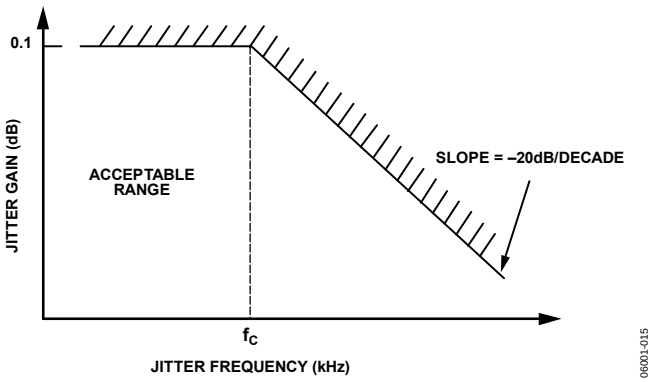


Figure 26. Jitter Transfer Curve

JITTER TOLERANCE

The jitter tolerance is defined as the peak-to-peak amplitude of the sinusoidal jitter applied on the input signal, which causes a 1 dB power penalty. This is a stress test intended to ensure that no additional penalty is incurred under the operating conditions (see Figure 27).

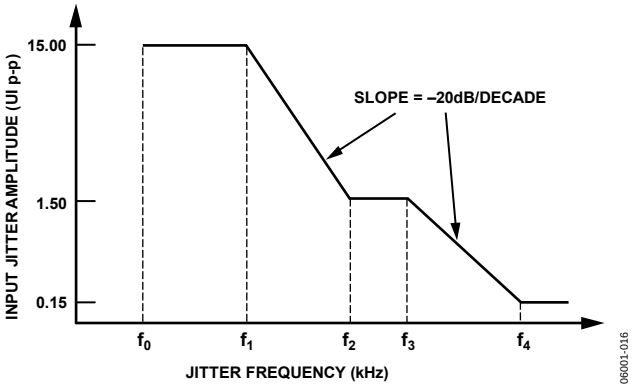


Figure 27. SONET Jitter Tolerance Mask

THEORY OF OPERATION

The ADN2817/ADN2818 are delay- and phase-locked loop circuits for clock recovery and data retiming from an NRZ encoded data stream. The phase of the input data signal is tracked by two separate feedback loops that share a common control voltage. A high speed delay-locked loop path uses a voltage controlled phase shifter to track the high frequency components of input jitter. A separate phase control loop, composed of the VCO, tracks the low frequency components of input jitter. The initial frequency of the VCO is set by a third loop, which compares the VCO frequency with the input data frequency and sets the coarse tuning voltage. The jitter tracking phase-locked loop controls the VCO by the fine-tuning control.

The delay- and phase-locked loops together track the phase of the input data signal. For example, when the clock lags input data, the phase detector drives the VCO to a higher frequency and increases the delay through the phase shifter; both of these actions serve to reduce the phase error between the clock and data. The faster clock picks up phase, while, simultaneously, the delayed data loses phase. Because the loop filter is an integrator, the static phase error is driven to zero.

Another view of the circuit is that the phase shifter implements the zero required for frequency compensation of a second-order phase-locked loop, and this zero is placed in the feedback path and, thus, does not appear in the closed-loop transfer function. Jitter peaking in a conventional second-order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Because this circuit has no zero in the closed-loop transfer, jitter peaking is minimized.

The delay- and phase-locked loops together simultaneously provide wideband jitter accommodation and narrow-band jitter filtering. The linearized block diagram in Figure 28 shows that the jitter transfer function, Z(s)/X(s), is second-order low-pass, providing excellent filtering. Note that the jitter transfer has no zero, unlike an ordinary second-order phase-locked loop. This means that the main PLL loop has virtually zero jitter peaking (see Figure 29). This makes this circuit ideal for signal regenerator applications, where jitter peaking in a cascade of regenerators can contribute to hazardous jitter accumulation.

The error transfer, e(s)/X(s), has the same high-pass form as an ordinary phase-locked loop. This transfer function is free to be optimized to give excellent wideband jitter accommodation, because the jitter transfer function, Z(s)/X(s), provides the narrow-band jitter filtering.

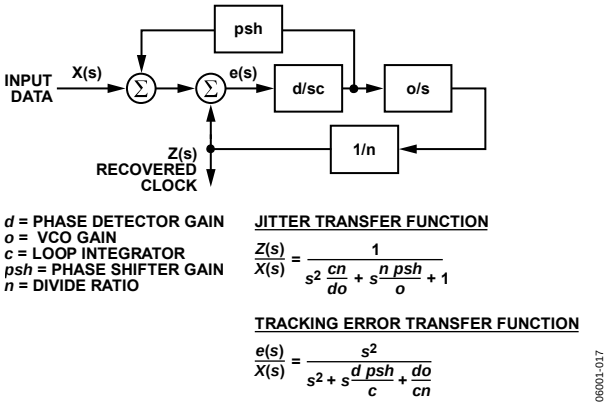


Figure 28. ADN2817/ADN2818 PLL/DLL Architecture

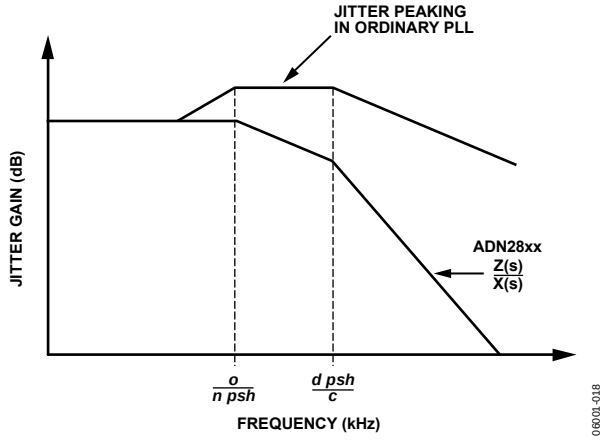


Figure 29. ADN2817/ADN2818 Jitter Response vs. Conventional PLL

The delay- and phase-locked loops contribute to overall jitter accommodation. At low frequencies of input jitter on the data signal, the integrator in the loop filter provides high gain to track large jitter amplitudes with small phase error. In this case, the VCO is frequency modulated and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the VCO tuning range. A wider tuning range gives larger accommodation of low frequency jitter. The internal loop control voltage remains small for small phase errors, so the phase shifter remains close to the center of its range and thus contributes little to the low frequency jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the VCO are not large enough to track input jitter. In this case, the VCO control voltage becomes large and saturates, and the VCO frequency dwells at one extreme of its tuning range or the other. The size of the VCO tuning range, therefore, has only a small effect on the jitter accommodation. The delay-locked loop control voltage is now larger, and so the phase shifter takes on the burden of tracking the input jitter. The phase shifter range, in UI, can be seen as a broad plateau on the jitter tolerance curve. The phase shifter has a minimum range of 2 UI at all data rates.

The gain of the loop integrator is small for high jitter frequencies, so that larger phase differences are needed to make the loop control voltage big enough to tune the range of the phase shifter. Large phase errors at high jitter frequencies cannot be tolerated. In this region, the gain of the integrator determines the jitter accommodation. Because the gain of the loop integrator declines linearly with frequency, jitter accommodation is lower with higher jitter frequency. At the highest frequencies, the loop gain is very small, and little tuning of the phase shifter can be expected. In this case, jitter accommodation is determined by the eye opening of the input data, the static phase error, and the residual loop jitter generation. The jitter accommodation is roughly 0.5 UI in this region. The corner frequency between the declining slope and the flat region is the closed-loop bandwidth of the delay-locked loop, which is roughly 3 MHz at OC-48.

FUNCTIONAL DESCRIPTION

FREQUENCY ACQUISITION

The ADN2817/ADN2818 acquire frequency from the data over a range of data frequencies from 10 Mbps to 2.7 Gbps. The lock detector circuit compares the frequency of the VCO and the frequency of the incoming data. When these frequencies differ by more than 1000 ppm, LOL is asserted. This initiates a frequency acquisition cycle. The VCO frequency is reset to the bottom of its range, which is 10 MHz. The frequency detector compares this VCO frequency and the incoming data frequency and increments the VCO frequency, if necessary. Initially, the VCO frequency is incremented in large steps to aid fast acquisition. As the VCO frequency approaches the data frequency, the step size is reduced until the VCO frequency is within 250 ppm of the data frequency, at which point LOL is deasserted.

Once LOL is deasserted, the frequency-locked loop is turned off. The phase- and delay-locked loop (PLL/DLL) pulls in the VCO frequency until the VCO frequency equals the data frequency.

The frequency loop requires a single external capacitor between CF1 and CF2, Pin 14 and Pin 15. A 0.47 µF ± 20%, X7R ceramic chip capacitor with <10 nA leakage current is recommended. Leakage current of the capacitor can be calculated by dividing the maximum voltage across the 0.47 µF capacitor, ~3 V, by the insulation resistance of the capacitor. The insulation resistance of the 0.47 µF capacitor should be greater than 300 MΩ.

LOCK DETECTOR OPERATION

The lock detector on the ADN2817/ADN2818 has three modes of operation: normal mode, REFCLK mode, and static LOL mode.

Normal Mode

In normal mode, the ADN2817/ADN2818 function as continuous rate CDRs that lock onto any data rate from 10 Mbps to 2.7 Gbps without the use of a reference clock as an acquisition aid. In this mode, the lock detector monitors the frequency difference between the VCO and the input data frequency, and deasserts the loss of lock signal that appears on LOL (Pin 16) when the VCO is within 250 ppm of the data frequency. This enables the delay- and phase-locked loop (DLL/PLL), which pulls the VCO frequency in the remaining amount and acquires phase lock. When locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss of lock signal is reasserted and control returns to the frequency loop, which begins a new frequency acquisition starting at the lowest point in the VCO operating range, 10 MHz. The LOL pin remains asserted until the VCO locks onto a valid input data stream to within 250 ppm frequency error. This hysteresis is shown in Figure 30.

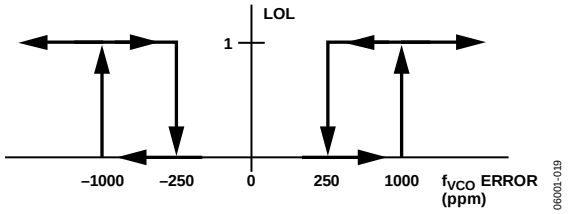


Figure 30. Transfer Function of LOL

LOL Detector Operation Using a Reference Clock

In this mode, a reference clock is used as an acquisition aid to lock the ADN2817/ADN2818 VCO. Lock to reference mode is enabled by setting CTRLA[0] to 1. The user also needs to write to the CTRLA[7:6] and CTRLA[5:2] bits to set the reference frequency range and the divide ratio of the data rate with respect to the reference frequency. For more details, see the Reference Clock (Optional) section. In this mode, the lock detector monitors the difference in frequency between the divided down VCO and the divided down reference clock. The loss of lock signal, which appears on LOL (Pin 16), is deasserted when the VCO is within 250 ppm of the desired frequency. This enables the DLL/ PLL, which pulls the VCO frequency in the remaining amount with respect to the input data and acquires phase lock. Once locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss of lock signal is reasserted and control returns to the frequency loop, which reacquires with respect to the reference clock. The LOL pin remains asserted until the VCO frequency is within 250 ppm of the desired frequency. This hysteresis is shown in Figure 30.

Static LOL Mode

The ADN2817/ADN2818 implement a static LOL feature, which indicates if a loss of lock condition has ever occurred and remains asserted, even if the ADN2817/ADN2818 regain lock, until the static LOL bit is manually reset. I^2C Register Bit MISC[4] is the static LOL bit. If there is ever an occurrence of a loss of lock condition, this bit is internally asserted to logic high. The MISC[4] bit remains high even after the ADN2817/ADN2818 reacquire lock to a new data rate. This bit can be reset by writing a 1 followed by 0 to I^2C Register Bit CTRLB[6]. When reset, the MISC[4] bit remains deasserted until another loss of lock condition occurs.

Writing a 1 to I^2C Register Bit CTRLB[7] causes the LOL pin, Pin 16, to become a static LOL indicator. In this mode, the LOL pin mirrors the contents of the MISC[4] bit and has the functionality described previously. The CTRLB[7] bit defaults to 0. In this mode, the LOL pin operates in the normal operating mode, that is, it is asserted only when the ADN2817/ ADN2818 are in acquisition mode and deasserts when the ADN2817/ADN2818 reacquire lock.

HARMONIC DETECTOR

The ADN2817/ADN2818 provide a harmonic detector, which detects whether the input data has changed to a lower harmonic of the data rate onto which the VCO is currently locked. For example, if the input data instantaneously changes from an OC-48, 2.488 Gbps to an OC-12, 622.080 Mbps bit stream, this could be perceived as a valid OC-48 bit stream, because the OC-12 data pattern is exactly 4× slower than the OC-48 pattern. Therefore, if the change in data rate is instantaneous, a 101 pattern at OC-12 is perceived by the ADN2817/ADN2818 as a 111100001111 pattern at OC-48. If the change to a lower harmonic is instantaneous, a typical CDR could remain locked at the higher data rate.

The ADN2817/ADN2818 implement a harmonic detector that automatically identifies whether the input data has switched to a lower harmonic of the data rate onto which the VCO is currently locked. When a harmonic is identified, the LOL pin is asserted and a new frequency acquisition is initiated. The ADN2817/ADN2818 automatically lock onto the new data rate, and the LOL pin is deasserted.

However, the harmonic detector does not detect higher harmonics of the data rate. If the input data rate switches to a higher harmonic of the data rate onto which the VCO is currently locked, the VCO loses lock, the LOL pin is asserted, and a new frequency acquisition is initiated. The ADN2817/ADN2818 automatically lock onto the new data rate.

The time to detect lock to harmonic is

$$16{,}384 \times (T_d/\rho)$$

where:
$1/T_d$ is the new data rate. For example, if the data rate is switched from OC-48 to OC-12, then T_d = 1/622 MHz.
ρ is the data transition density. Most coding schemes seek to ensure that ρ = 0.5, for example, PRBS or 8b/10b encoding.
When the ADN2817/ADN2818 is placed in lock to reference mode, the harmonic detector is disabled.

LIMITING AMPLIFIER (ADN2817 ONLY)

The limiting amplifier on the ADN2817 has differential inputs (PIN/NIN) that internally terminate with 50 Ω to an on-chip voltage reference (VREF = 2.5 V typically). The inputs are typically ac-coupled externally, although dc coupling is possible as long as the input common-mode voltage remains above 2.5 V (see Figure 40, Figure 41, and Figure 42). Input offset is factory trimmed to achieve better than 6 mV typical sensitivity with minimal drift. The limiting amplifier can be driven differentially or single-ended.

SLICE LEVEL ADJUST (ADN2817 ONLY)

The quantizer slicing level can be offset by ±100 mV to mitigate the effect of amplified spontaneous emission (ASE) noise or duty cycle distortion by applying a differential voltage input of up to ±0.95 V to SLICEP/SLICEN inputs. If no adjustment of the slice level is needed, SLICEP/SLICEN should be tied to VEE. The gain of the slice adjustment is ~0.1 V/V.

LOSS OF SIGNAL (LOS) DETECTOR (ADN2817 ONLY)

The receiver front-end LOS detector circuit detects when the input signal level has fallen below a user-adjustable threshold. The threshold is set with a single external resistor from Pin 9, THRADJ, to VEE. The LOS comparator trip point vs. resistor value is shown in Figure 6. If the input level to the ADN2817 drops below the programmed LOS threshold, the output of the LOS detector, Pin 22 (LOS), is asserted to a Logic 1. The LOS detector response time is 450 ns by design but is dominated by the RC time constant in ac-coupled applications. The LOS pin defaults to active high. However, by setting Bit CTRLC[2] to 1, the LOS pin is configured as active low.

There is typically 6 dB of electrical hysteresis designed into the LOS detector to prevent chatter on the LOS pin. This means that, if the input level drops below the programmed LOS threshold causing the LOS pin to assert, the LOS pin is not deasserted until the input level has increased to 6 dB (2×) above the LOS threshold (see Figure 31).

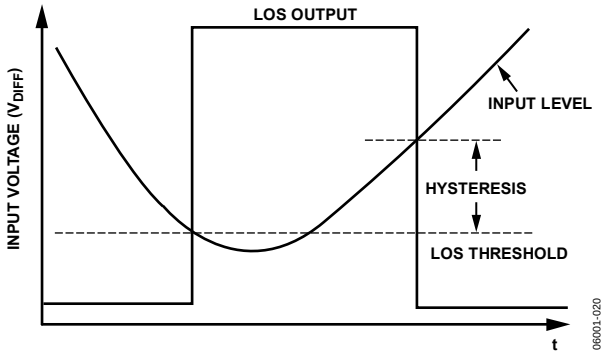


Figure 31. ADN2817 LOS Detector Hysteresis

The LOS detector and the slice level adjust can be used simultaneously on the ADN2817. This means that any offset added to the input signal by the slice adjust pins does not affect the LOS detector measurement of the absolute input level.

SAMPLE PHASE ADJUST

If the user is not using the BER monitoring function, sample phase adjustment can be used to optimize the horizontal sampling point of the incoming data eye. The ADN2817 automatically centers the sampling point to the best of its ability. However, sample phase adjustment can be used to compensate for any static phase offset of the CDR and data eye jitter profile asymmetry. Sample phase adjustment is applied to the incoming eye via the phase register. The sampling phase can be adjusted by ±0.5 UI, in 6 degree steps, relative to the normal CDR data sampling instant. Using the sample phase adjustment capability uses an additional 160 mW of power. The AN-941 application note gives additional information on the use of this feature.

BIT ERROR RATE (BER) MONITOR

The ADN2817 has a BER measurement feature that estimates the actual bit error rate of the IC. This feature also allows data eye jitter profiling and Q-factor estimation.

By knowing the BER at a sampling phase offset from the ideal sampling phase (known as pseudo BER [PBER] values), it is possible to extrapolate to obtain an estimate of the BER at the actual sampling instant. This extrapolation relies on the assumption that the input jitter is composed of deterministic and random (Gaussian) components. The implementation requires off-chip control and data processing to estimate the actual BER. A lower accuracy voltage output mode is also supported that requires no data processing or I²C control.

Brief Overview of Modes of Operation

The following two modes of operation are available for the BER feature: the BER extrapolation mode and the voltage output mode. Only one mode can be operational at a time. The BER extrapolation mode scans the input eye in the range of ±0.5 UI of the data center and reads the measured PBER over the I²C. The user then applies a data processing algorithm to determine the BER. Using the BER feature in this way provides for the greatest accuracy in BER estimation as the magnitude of both random (Gaussian) jitter and deterministic jitter can be estimated and used to predict the actual BER.

In the voltage output mode, the part autonomously samples the PBER at 0.1 UI offset and decodes this value to provide an estimate of the input BER. This estimate is output via a DAC as an analog current output. The AN-941 application note gives detailed information on the use of the BER monitor features.

BER Extrapolation Mode

Power Saving

The following three power settings are available in BER extrapolation mode: BER off, BER on, and BER standby.

In BER off mode (BERCTLB[5] = 0), the BER circuitry is powered down with the ADN2817 providing normal CDR operation.

In BER on mode (BERCTLB[5] = 1), the internal BER circuitry is powered up. The user can perform pseudo BER measurements through the I²C.

In BER standby mode (BERCTLB[5:4] = 11b), the BER is placed into a lower power mode. This setting can only be set after applying the BER on setting.

These modes are defined to allow optimal power saving opportunities. It is not possible to switch between the BER off setting and the BER on setting without losing lock. Switching between the BER standby setting and the BER on setting is achieved without interrupting data recovery. The incremental power between the BER off setting and the BER standby setting is 77 mW and between the BER off setting and the BER on setting it is 160 mW.

BER On Mode

The BER on mode allows the user to scan the incoming data eye in the time dimension and build up a profile of the BER statistics.

The following is a brief overview of user protocol:

- The user powers up BER circuitry through the I²C.
- The user initiates the PBER measurement. Sample phase offset and number of data bits to be counted (NUMBITS is a choice among 2^{18}, 2^{21}, 2^{24}, 2^{27}, 2^{30}, 2^{33}, 2^{36}, and 2^{39}) are supplied by the user through the I²C.
- The user initiates the pseudo BER measurement by writing a 1-to-0 transition on BERCTLA[3].
- BER logic indicates the end of the BER measurement with an EOBM signal and updates the number of counted errors on NUMERRORS[39:0]. The user must poll the I²C to determine if the EOBM bit, BERSTS[0], has been asserted.
- The user reads back NUMERRORS[39:0] through the I²C. NUMERRORS[39:0] is read back through the 8-bit register BER_RES at Address 0x21. The user sets BERCTLA[2:0] to address one of the five NUMERRORS bytes and then reads the selected byte from BER_RES.
- PBER for programmed sample phase is calculated as NUMERRORS/NUMBITS.
- The user initiates another PBER measurement.
- The user sweeps the phase over −0.5 UI to +0.5 UI with respect to the normal sampling instant to obtain the BER profile required.

The ADN2817 does not output the BER at the normal decision instant. It outputs PBER measurements to the left and right of the normal decision instants from which the user must calculate what the BER is at the normal decision instant. A microprocessor is required to parse the data and to use the remaining data for BER estimation. Suitable algorithms are suggested in the AN-941 Application Note, *BER Monitor User Guide*.

Voltage Output Mode of Operation

A second mode of operation is the voltage output mode. This mode is to give easy access to a coarse estimate of the BER. The functionality is similar to that already described in the Brief Overview of Modes of Operation section except that the measurement is performed autonomously by the ADN2817, and the result is output as a voltage on a pin from which the actual BER can be inferred. Because this mode does not perform scanning of the eye to separate out deterministic jitter from random jitter effects, this method is less accurate under normal applied jitter conditions.

The user merely has to bring the BERMODE pin low and read the voltage on the VBER pin (see Figure 32). Alternatively, a 6-bit value can be read over the I²C.

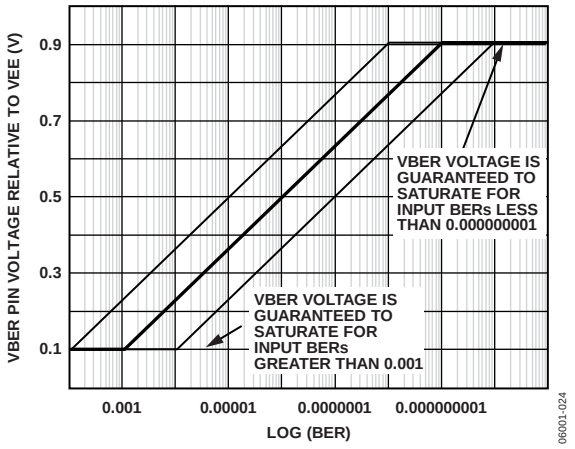


Figure 32. VBER vs. Bit Error Rate

SQUELCH MODE

Two squelch modes are available with the ADN2817/ADN2818: squelch DATAOUT and CLKOUT mode, and squelch DATAOUT or CLKOUT mode.

Squelch DATAOUT and CLKOUT mode is selected when CTRLC[1] = 0 (default mode). In this mode, when the squelch input, Pin 27, is driven to a TTL high state, both the clock and data outputs are set to the zero state to suppress downstream processing. If the squelch function is not required, Pin 27 should be tied to VEE.

Squelch DATAOUT or CLKOUT mode is selected when CTRLC[1] is 1. In this mode, when the squelch input is driven to a high state, the DATAOUT pins are squelched. When the squelch input is driven to a low state, the CLKOUT pins are squelched. This is especially useful in repeater applications, where the recovered clock may not be needed.

I²C INTERFACE

The ADN2817/ADN2818 support a 2-wire, I²C-compatible serial bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCK), carry information between any devices connected to the bus. Each slave device is recognized by a unique address. The ADN2817/ADN2818 have two possible 7-bit slave addresses for both read and write operations. The MSB of the 7-bit slave address is factory programmed to 1. Bit 5 of the slave address is set by Pin 19, SADDR5. Slave Address Bits[4:0] are defaulted to all 0s. The slave address consists of the 7 MSBs of an 8-bit word. The LSB of the word either sets a read or write operation (see Figure 18). Logic 1 corresponds to a read operation and Logic 0 corresponds to a write operation.

To control the device on the bus, the following protocol must be used. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCK remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address and the R/$\overline{W}$ bit). The bits are transferred from MSB to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCK lines waiting for the start condition and correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADN2817/ADN2818 act as standard slave devices on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/$\overline{W}$ bit. The ADN2817/ADN2818 have eight subaddresses to enable the user-accessible internal registers (see Table 8 through Table 16). It, therefore, interprets the first byte as the device address and the second byte as the starting subaddress. Auto-increment mode is supported, allowing data to be read from, or written to, the starting subaddress and each subsequent address without manually addressing the subsequent subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all registers.

Stop and start conditions can be detected at any stage of the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCK high period, the user should issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADN2817/ADN2818 do not issue an acknowledge and return to the idle condition.

If the user exceeds the highest subaddress while reading back in auto-increment mode, the highest subaddress register contents continue to be output until the master device issues a no acknowledge. This indicates the end of a read. In a no acknowledge condition, the SDA line is not pulled low on the ninth pulse. See Figure 19 and Figure 20 for sample read and write data transfers and Figure 21 for a more detailed timing diagram.

REFERENCE CLOCK (OPTIONAL)

A reference clock is not required to perform clock and data recovery with the ADN2817/ADN2818. However, support for an optional reference clock is provided. The reference clock can be driven differentially or single-ended. If the reference clock is not used, tie REFCLKP to VCC, and either leave REFCLKN floating or tie it to VEE (the inputs are internally terminated to VCC/2). See Figure 33 through Figure 35 for sample configurations.

The REFCLK input buffer accepts any differential signal with a peak-to-peak differential amplitude of greater than 100 mV (for example, LVPECL or LVDS) or a standard single-ended low voltage TTL input, providing maximum system flexibility. Phase noise and duty cycle of the reference clock are not critical and 100 ppm accuracy is sufficient.

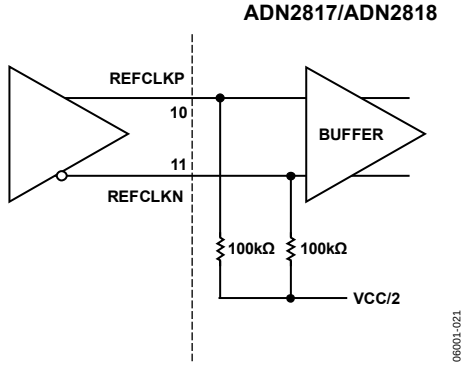


Figure 33. Differential REFCLK Configuration

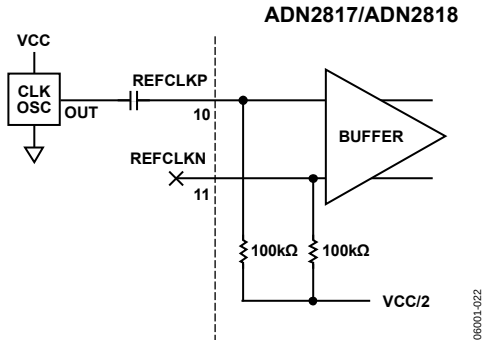


Figure 34. Single-Ended REFCLK Configuration

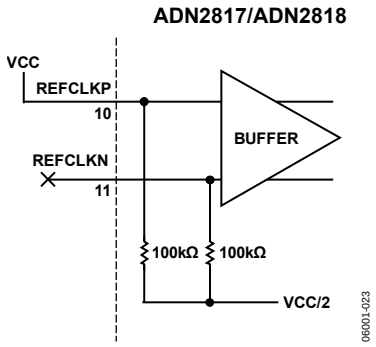


Figure 35. No REFCLK Configuration

The two uses of the reference clock are mutually exclusive. The reference clock can be used either as an acquisition aid for the ADN2817/ADN2818 to lock onto data, or to measure the frequency of the incoming data to within 0.01%. (There is the capability to measure the data rate to approximately ±10% without the use of a reference clock.) The modes are mutually exclusive because, in the first use, the user knows exactly what the data rate is and wants to force the part to lock onto only that data rate; in the second use, the user does not know what the data rate is and wants to measure it.

Lock to reference mode is enabled by writing 1 to I^2C Register Bit CTRLA[0]. Data rate readback mode is enabled by writing 1 to I^2C Register Bit CTRLA[1]. Writing a 1 to both of these bits at the same time causes an indeterminate state and is not supported.

Using the Reference Clock to Lock onto Data

Writing CTRLA[0] = 1 puts the ADN2817/ADN2818 into lock to REFCLK (LTR) mode. In this mode, the ADN2817/ADN2818 lock onto a frequency derived from the reference clock according to the following equation:

$$Data\ Rate/2^{CTRLA[5:2]} = REFCLK/2^{CTRLA[7:6]}$$

The user must know exactly what the data rate is and provide a reference clock that is a function of this rate. The ADN2817/ADN2818 can still be used as continuous rate devices in this configuration if a reference clock with a variable frequency is provided (see the AN-632 Application Note).

The reference clock can be anywhere between 10 MHz and 200 MHz. By default, the ADN2817/ADN2818 expect a reference clock of between 10 MHz and 25 MHz. If it is between 25 MHz and 50 MHz, 50 MHz and 100 MHz, or 100 MHz and 200 MHz, the user needs to configure the ADN2817/ADN2818 to use the correct reference frequency range by setting two bits of the CTRLA register, CTRLA[7:6].

Table 17. CTRLA[7:6] (f_{REF} Range) with CTRLA[5:2] (DIV_FREF Ratio) Settings

CTRLA[7:6]	Range (MHz)	CTRLA[5:2]	Ratio
00	10 to 25	0000	1
01	25 to 50	0001	2
10	50 to 100	n	2^n
11	100 to 200	1000	256

The user can specify a fixed integer multiple of the reference clock to lock onto using CTRLA[5:2], where CTRLA should be set to the data rate/DIV_FREF and DIV_FREF represents the divided-down reference referred to the 10 MHz to 25 MHz band. For example, if the reference clock frequency is 38.88 MHz and the input data rate is 622.08 Mbps, then CTRLA[7:6] is set to 01 to give a divided-down reference clock of 19.44 MHz. CTRLA[5:2] is set to 0101, that is, 5, because

622.08 Mbps/19.44 MHz = 2^5

When the CTRLA[7:2] value is correct and CTRLA[0] has been written to a Logic 1, it is recommended that a 1-to-0 transition be written to CTRLB[5] to initiate a new frequency acquisition with respect to the reference clock.

In this mode, if the ADN2817/ADN2818 lose lock for any reason, they relock onto the reference clock and continue to output a stable clock.

Though the ADN2817/ADN2818 operate in LTR mode, if the user ever changes the reference frequency, the f_{REF} range (CTRLA[7:6]), or the DIV_FREF ratio (CTRLA[5:2]), this must be followed by writing a 1-to-0 transition into the CTRLB[5] bit to initiate a new frequency acquisition.

A frequency acquisition can also be initiated in LTR mode by writing a 0-to-1 transition into CTRLA[0]; however, it is recommended that a frequency acquisition be initiated by writing a 1-to-0 transition into CTRLB[5], as explained previously.

Using the Reference Clock to Measure Data Frequency

The user can also provide a reference clock to measure the recovered data frequency. In this case, the user provides a reference clock, and the ADN2817/ADN2818 compare the frequency of the incoming data to the incoming reference clock and return a ratio of the two frequencies to 0.01% (100 ppm). The accuracy error of the reference clock is added to the accuracy of the ADN2817/ADN2818 data rate measurement. For example, if a 100 ppm accuracy reference clock is used, the total accuracy of the measurement is within 200 ppm.

The reference clock can range from 10 MHz to 200 MHz. The ADN2817/ADN2818 expects a reference clock between 10 MHz and 25 MHz by default. If it is between 25 MHz and 50 MHz, 50 MHz and 100 MHz, or 100 MHz and 200 MHz, the user needs to configure the ADN2817/ADN2818 to use the correct reference frequency range by setting two bits of the CTRLA register, CTRLA[7:6]. Using the reference clock to determine the frequency of the incoming data does not affect the manner in which the part locks onto data. In this mode, the reference clock is used only to determine the frequency of the data. For this reason, the user does not need to know the data rate to use the reference clock in this manner.

Prior to reading back the data rate using the reference clock, the CTRLA[7:6] bits must be set to the appropriate frequency range with respect to the reference clock being used. A fine data rate readback is then executed as follows:

1. Write a 1 to CTRLA[1]. This enables the fine data rate measurement capability of the ADN2817/ADN2818. This bit is level sensitive and does not need to be reset to perform subsequent frequency measurements.
2. Reset MISC[2] by writing a 1 followed by a 0 to CTRLB[3]. This initiates a new data rate measurement.
3. Read back MISC[2]. If it is 0, the measurement is not complete. If it is 1, the measurement is complete and the data rate can be read back on FREQ[22:0]. The time for a data rate measurement is typically 80 ms.
4. Read back the data rate from the FREQ2[6:0], FREQ1[7:0], and FREQ0[7:0] registers.

Use the following equation to determine the data rate:

$$f_{DATARATE} = (FREQ[22..0] \times f_{REFCLK})/2^{(14 + SEL_RATE)} \quad (1)$$

where:
FREQ[22:0] is the reading from FREQ2[6:0] (most significant byte), FREQ1[7:0], and FREQ0[7:0] (least significant byte). See Table 18.
$f_{DATARATE}$ is the data rate (Mbps).
f_{REFCLK} is the REFCLK frequency (MHz).
SEL_RATE is the setting from CTRLA[7:6].

Table 18.

D22	D21:D17	D16	D15	D14:D9	D8	D7	D6:D1	D0
FREQ2[6:0]			FREQ1[7:0]			FREQ0[7:0]		

For example, if the reference clock frequency is 32 MHz, it falls within the 25 MHz to 50 MHz range; therefore, the CTRLA[7:6] setting is 01 resulting in SEL_RATE = 1. For this example, the input data rate is 2.488 Gbps (OC-48). After following Step 1 through Step 4, the value that is read back on FREQ[22:0] = 0x26E010, which is equal to 2.5477×10^6. Plugging this value into Equation 1 yields

$((2.5477 \times 10^6) \times (32 \times 10^6))/(2^{(14 + 1)}) = 2.488$ Gbps

If subsequent frequency measurements are required, CTRLA[1] should remain set to 1. It does not need to be reset. The measurement process is reset by writing a 1 followed by a 0 to CTRLB[3]. This initiates a new data rate measurement. Follow Step 2 through Step 4 to read back the new data rate.

Note that a data rate readback is valid only if LOL is low. If LOL is high, the data rate readback is invalid.

ADDITIONAL FEATURES AVAILABLE VIA THE I²C INTERFACE

Coarse Data Rate Readback

The data rate can be read back over the I²C interface to approximately ±10% without needing an external reference clock. A 9-bit register, COARSE_RD[8:0], can be read back when LOL is deasserted. The eight MSBs of this register are the contents of the Rate[7:0] register. The LSB of the COARSE_RD register is Bit MISC[0].

Table 19 is a look-up table (LUT) that provides coarse data rate readback values to within ±10%.

LOS Configuration

The LOS detector output, Pin 22 (LOS), can be configured as either active high or active low. If CTRLC[2] is set to Logic 0 (default), the LOS pin is active high when a loss of signal condition is detected. Writing a 1 to CTRLC[2] configures the LOS pin to be active low when a loss of signal condition is detected.

Initiate Frequency Acquisition

A frequency acquisition can be initiated by writing a 1 followed by a 0 to the I²C Register Bit CTRLB[5]. This initiates a new frequency acquisition while keeping the ADN2817/ADN2818 in the operating mode that was previously programmed in the CTRLA, CTRLB, CTRLC, CTRLD, and CTRLE registers.

Rate Selectivity

The ADN2817/ADN2818 can operate in a limited range mode in situations where the user wants to restrict the data rates to which the device can lock. In this mode, the frequency acquisition range of the device is limited to a specific range of data rates. The acquisition range is determined by programming an upper and lower 9-bit code into the HI_CODE[8:1], LO_CODE[8:1], and CODE_LSB[1:0] I²C registers. See Table 20 for a look-up table (LUT) showing the correct register settings for each data rate. Table 20 has three columns: code, high limit, and low limit. The user programs the code value for the high limit data rate into HI_CODE and the code value for the low limit data rate into LO_CODE to set the appropriate range.

For example, if the user wants to limit the acquisition range of the ADN2817/ADN2818 to lock between 1 Gbps and 1.25 Gbps, the following steps must be taken:

1. Find the first code in Table 20 that corresponds to a data rate below 1.0 Gbps in the low limit column, that is, Code 236 or 011101100b. Set LO_CODE[8:1] = 01110110b (LO_CODE[0] is set in Register Bit CODE_LSB[0].)
2. Find the first code in Table 20 that corresponds to a data rate above 1.25 Gbps in the high limit column, that is, Code 258 or 100000010b. Set HI_CODE[8:1] = 10000001b (HI_CODE[0] is set in Register Bit CODE_LSB[1].)
3. Set CODE_LSB = 00000000b given that the HI_CODE[0] = 0 and LO_CODE[0] = 0.
4. Set SEL_MODE[3] = 1.
5. When there is a valid input to the device between 1.0 Gbps and 1.25 Gbps, write a 1-to-0 transition into CTRLB[5] to initiate a new frequency acquisition.

Double Data Rate Mode

Setting CTRLE = 0x02 puts the ADN2817/ADN2818 clock output through divide-by-two circuitry allowing direct interfacing to FPGAs that support data clocking on both rising and falling edges.

PRBS Generator/Detector

The ADN2817/ADN2818 have an integrated PRBS generator/detector for system testing purposes. The devices are configurable as either a PRBS detector or a PRBS generator. The two functions cannot be used at the same time.

The following steps configure the PRBS detector (PRBS 7 only):

1. Set CTRLE[2:0] = 0x5.
2. Set CTRLD[2:0] = 0x4 to enable the PRBS detector.

The PRBS error signal outputs on the DATAOUTP/DATAOUTN pins. Every time the PRBS detector detects an error, the DATAOUTP/DATAOUTN outputs pulse twice to a Logic 1, that is, DATAOUTP = 1, DATAOUTN = 0.

The following steps configure the PRBS generator (PRBS 7 only):

1. Set CTRLE[2:0] = 0x5.
2. Set CTRLD[2:0] = 0x1 to enable the PRBS generator.
3. Write a 1-to-0 transition into CTRLD[3] to initiate a PRBS 7 pattern.

Note that the PRBS generator is clocked by the VCO; therefore, the user needs to feed in a clock at half the desired frequency. For example, for an OC-48 PRBS pattern, input a 1.244 GHz clock to PIN/NIN. This appears as a 2.488 Gbps NRZ data pattern to the ADN2817/ADN2818. The recovered clock is 2.488 GHz, which clocks the PRBS generator to produce an OC-48 PRBS pattern on the outputs.

CLK Holdover Mode

This mode of operation is available in LTD mode. In CLK holdover mode, the output clock frequency remains within ±5% if the input data is removed or changed. To operate in this mode, the user writes to the I²C to put the part into CLK holdover mode by setting SEL_MODE[1] = 1. The user must then initiate a frequency acquisition by writing a 1-to-0 transition into CTRLB[5], at which time the device locks onto the input data rate. At this point, the output frequency remains within ±5% of the initial acquired value regardless of whether the input data is removed or the data rate changes.

It is important to note that all frequency acquisitions in this mode must be initiated by writing a 1-to-0 transition into CTRLB[5]. In this mode, the device does not automatically initiate a new frequency acquisition when the input is momentarily interrupted or if the input data rate changes.

CDR Bypass Mode

The CDR on the ADN2817/ADN2818 can be bypassed by setting Bit CTRLD[7] = 1. In this mode, the ADN2817/ADN2818 feed the input directly through the input amplifiers to the output buffer, completely bypassing the CDR.

Disable Output Buffers

The ADN2817/ADN2818 provide the option of disabling the output buffers for power savings. The clock output buffers can be disabled by setting Bit CTRLD[5] = 1. This reduces the total power consumption of the device by ~100 mW. For an additional 100 mW power savings, such as in low power standby mode, the data output buffers can also be disabled by setting Bit CTRLD[6] = 1.

APPLICATIONS INFORMATION

PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used for optimal performance.

Power Supply Connections and Ground Planes

For best practice, the use of one low impedance ground plane is recommended. To reduce series inductance, solder the VEE pins directly to the ground plane. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias can be used in parallel to reduce the series inductance, especially on Pin 23, which is the ground return for the output buffers. Connect the exposed pad to the ground plane using plugged vias so that solder does not leak through the vias during reflow.

Use of a 10 µF electrolytic capacitor between VCC and VEE is recommended at the location where the 3.3 V supply enters the PCB. When using 0.1 µF and 1 nF ceramic chip capacitors, they should be placed between the IC power supply (VCC and VEE), as close as possible to the ADN2817/ADN2818 VCC pins.

If connections to the supply and ground are made through vias, the use of multiple vias in parallel helps to reduce series inductance, especially on Pin 24, which supplies power to the high speed CLKOUTP/CLKOUTN and DATAOUTP/DATAOUTN output buffers. See the schematic in Figure 36 for recommended connections.

By using adjacent power supply and ground planes, excellent high frequency decoupling can be realized by using close spacing between the planes. This capacitance is given by

$$C_{PLANE} = 0.88\varepsilon_r A/d \text{ (pF)}$$

where:

ε_r is the dielectric constant of the PCB material.
A is the area of the overlap of power and ground planes (cm^2).
d is the separation between planes (mm).

For FR-4, $\varepsilon_r = 4.4$ and 0.25 mm spacing, $C \approx 15$ pF/cm^2.

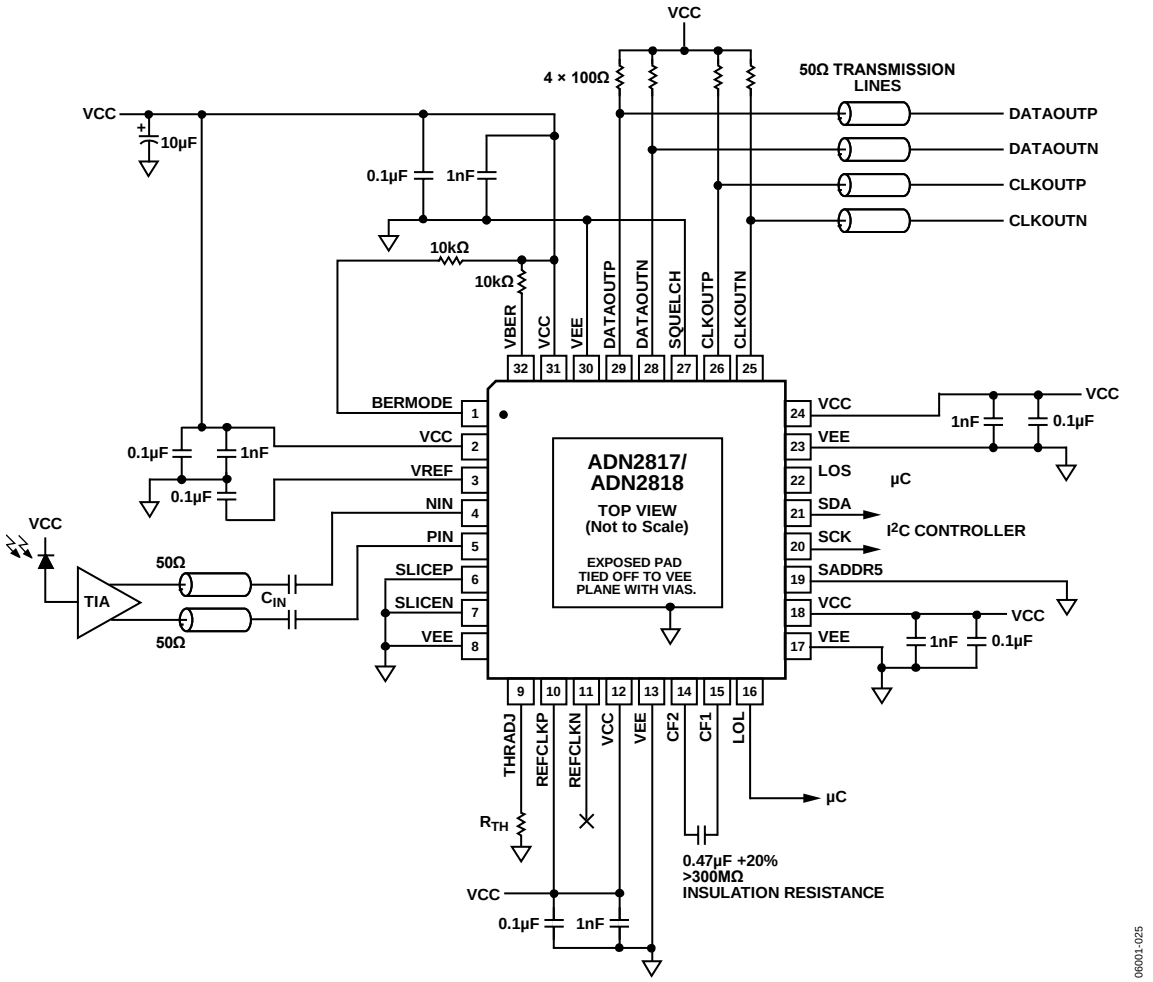


Figure 36. Typical ADN2817/ADN2818 Applications Circuit

Transmission Lines

Use of 50 Ω transmission lines is required for all high frequency input and output signals to minimize reflections: PIN, NIN, CLKOUTP, CLKOUTN, DATAOUTP, and DATAOUTN (also REFCLKP, REFCLKN, if using a high frequency reference clock, such as 155 MHz). It is also necessary for the PIN/NIN input traces to be matched in length, and the CLKOUTP, CLKOUTN, DATAOUTP, and DATAOUTN output traces to be matched in length to avoid skew between the differential traces.

All high speed CML outputs (CLKOUTP, CLKOUTN, DATAOUTP, and DATAOUTN) require 100 Ω back termination chip resistors connected between the output pin and VCC. Place these resistors as close as possible to the output pins. These 100 Ω resistors are in parallel with on-chip 100 Ω termination resistors to create a 50 Ω back termination (see Figure 37).

The high speed inputs (PIN and NIN) are internally terminated with 50 Ω to an internal reference voltage (see Figure 38). A 0.1 µF capacitor is recommended between VREF, Pin 3, and GND to provide an ac ground for the inputs.

As with any high speed mixed-signal design, take care to keep all high speed digital traces away from sensitive analog nodes.

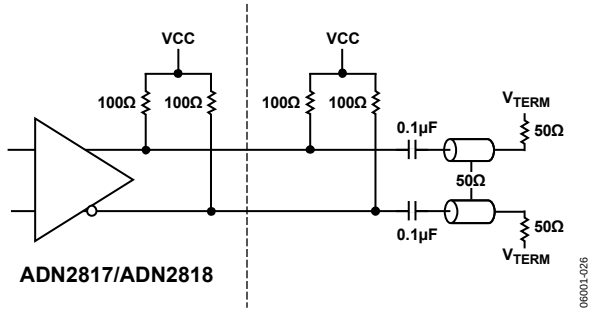


Figure 37. Typical ADN2817/ADN2818 Applications Circuit

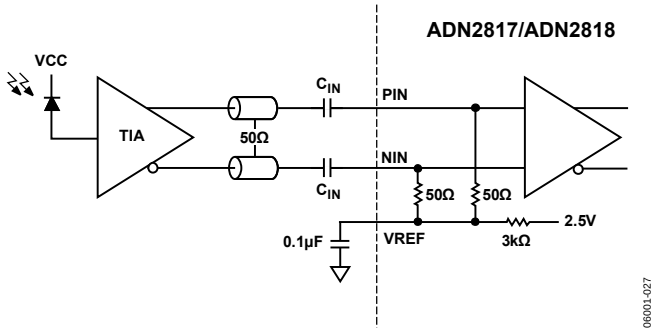


Figure 38. ADN2817/ADN2818 AC-Coupled Input Configuration

Soldering Guidelines for Lead Frame Chip Scale Package

The lands on the 32-lead LFCSP are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length, and 0.05 mm wider than the package land width. Center the land on the pad to ensure that the solder joint size is maximized. The bottom of the lead frame chip scale package has a central exposed pad. The pad on the printed circuit board should be at least as large as this exposed pad. The user must connect the exposed pad to VEE using plugged vias to prevent solder from leaking through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

Choosing AC Coupling Capacitors

AC coupling capacitors at the input (PIN, NIN) and output (DATAOUTP, DATAOUTN) of the ADN2817/ADN2818 must be chosen such that the device works properly over the full range of data rates used in the application. When choosing the capacitors, the time constant formed with the two 50 Ω resistors in the signal path must be considered. When a large number of consecutive identical digits (CIDs) are applied, the capacitor voltage can droop due to baseline wander (see Figure 39), causing pattern dependent jitter (PDJ).

The user must determine how much droop is tolerable and choose an ac coupling capacitor based on that amount of droop. The amount of PDJ can then be approximated based on the capacitor selection. The actual capacitor value selection may require some trade-offs between droop and PDJ.

For example, assuming that 2% droop can be tolerated, the maximum differential droop is 4%. Normalizing to peak-to-peak voltage,

$$Droop = \Delta V = 0.04\ V = 0.5\ V\ p\text{-}p\ (1 - e^{-t/\tau})\ ;\ \text{therefore, } \tau = 12t$$

where:
τ is the RC time constant (C is the ac coupling capacitor, and R = 100 Ω seen by C).
t is the total discharge time, which is equal to $n\,T$.
n is the number of CIDs.
T is the bit period.

Calculate the capacitor value by combining the equations for τ and t.

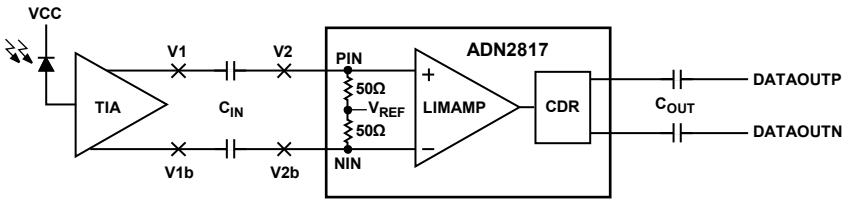
$$C = 12nT/R$$

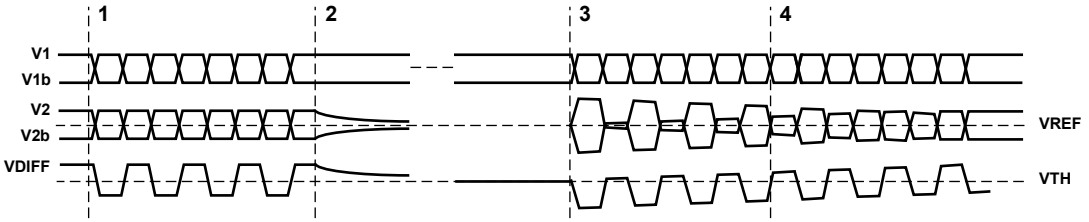
When the capacitor value is selected, the PDJ can be approximated as

$$PDJ_{ps\ p\text{-}p} = 0.5t_r(1 - e^{(-nT/RC)})/0.6$$

where:
$PDJ_{ps\ p\text{-}p}$ is the amount of pattern-dependent jitter allowed; <0.01 UI p-p typical.
t_r is the rise time, which is equal to 0.22/BW, where $BW \approx 0.7$ (bit rate).

Note that this expression for t_r is accurate only for the inputs. The output rise time for the ADN2817/ADN2818 is ~100 ps regardless of data rate.





VDIFF = V2 – V2b
VTH = ADN2817 QUANTIZER THRESHOLD

NOTES
1. DURING THE DATA PATTERNS WITH HIGH TRANSITION DENSITY, DIFFERENTIAL DC VOLTAGE AT V1 AND V2 IS ZERO.
2. WHEN THE OUTPUT OF THE TIA GOES TO CID, V1 AND V1b ARE DRIVEN TO DIFFERENT DC LEVELS. V2 AND V2b DISCHARGE TO THE VREF LEVEL WHICH EFFECTIVELY INTRODUCES A DIFFERENTIAL DC OFFSET ACROSS THE AC COUPLING CAPACITORS.
3. WHEN THE BURST OF DATA STARTS AGAIN, THE DIFFERENTIAL DC OFFSET ACROSS THE AC COUPLING CAPACITORS IS APPLIED TO THE INPUT LEVELS CAUSING A DC SHIFT IN THE DIFFERENTIAL INPUT. THIS SHIFT IS LARGE ENOUGH SUCH THAT ONE OF THE STATES, EITHER HIGH OR LOW DEPENDING ON THE LEVELS OF V1 AND V1b WHEN THE TIA WENT TO CID, IS CANCELLED OUT. THE QUANTIZER DOES NOT RECOGNIZE THIS AS A VALID STATE.
4. THE DC OFFSET SLOWLY DISCHARGES UNTIL THE DIFFERENTIAL INPUT VOLTAGE EXCEEDS THE SENSITIVITY OF THE ADN2817. THE QUANTIZER RECOGNIZES BOTH HIGH AND LOW STATES AT THIS POINT.

06001-028

Figure 39. Example of Baseline Wander

DC-COUPLED APPLICATION

The inputs to the ADN2817/ADN2818 can also be dc-coupled. This can be necessary in burst mode applications with long periods of CIDs and where baseline wander cannot be tolerated. If the inputs to the ADN2817/ADN2818 are dc-coupled, care must be taken not to violate the input range and common-mode level requirements of the ADN2817/ADN2818 (see Figure 40 through Figure 42). If dc coupling is required, and the output levels of the TIA do not adhere to the levels shown in Figure 41, level shifting and/or attenuation must occur between the TIA outputs and the ADN2817/ADN2818 inputs.

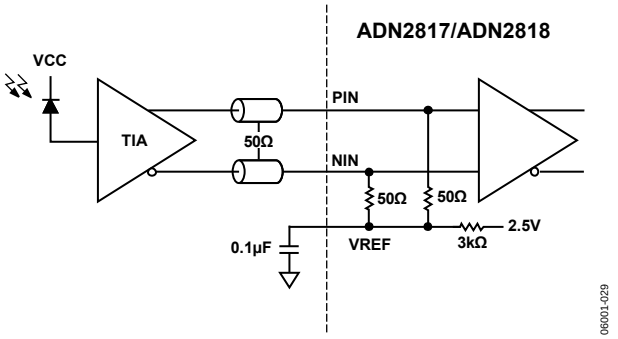


Figure 40. DC-Coupled Application

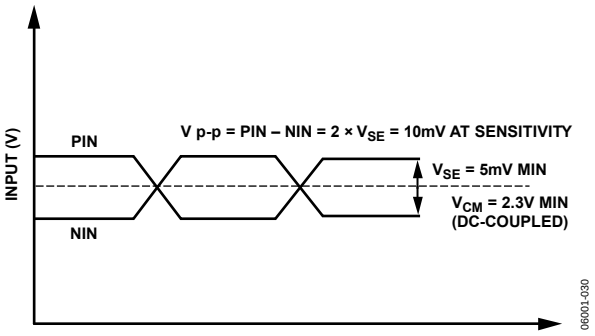


Figure 41. Minimum Allowed DC-Coupled Input Levels

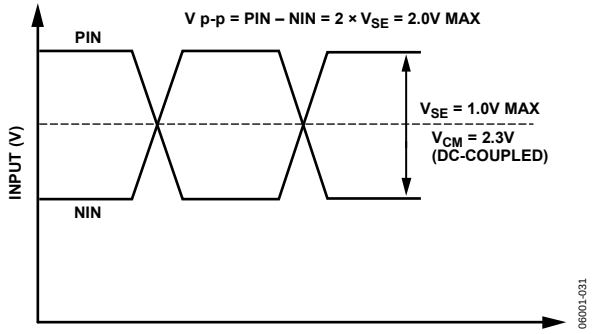


Figure 42. Maximum Allowed DC-Coupled Input Levels

COARSE DATA RATE READBACK LOOK-UP TABLE

Code is the 9-bit value read back from COARSE_RD[8:0].

Table 19. Coarse Data Rate Readback Look-Up Table

Code	f_{MID} (Hz)	Code	f_{MID} (Hz)	Code	f_{MID} (Hz)	Code	f_{MID} (Hz)
0	5.3205×10^6	49	15.2526×10^6	98	43.4353×10^6	147	127.4396×10^6
1	5.3202×10^6	50	15.5785×10^6	99	44.3782×10^6	148	130.4620×10^6
2	5.4294×10^6	51	15.9300×10^6	100	45.3877×10^6	149	133.7061×10^6
3	5.5473×10^6	52	16.3078×10^6	101	46.4691×10^6	150	137.1983×10^6
4	5.6735×10^6	53	16.7133×10^6	102	47.6260×10^6	151	140.9643×10^6
5	5.8086×10^6	54	17.1498×10^6	103	48.8696×10^6	152	145.0399×10^6
6	5.9533×10^6	55	17.6205×10^6	104	50.2170×10^6	153	149.7350×10^6
7	6.1087×10^6	56	18.1300×10^6	105	51.7728×10^6	154	154.5698×10^6
8	6.2771×10^6	57	18.7169×10^6	106	53.3614×10^6	155	159.8491×10^6
9	6.4716×10^6	58	19.3212×10^6	107	55.1069×10^6	156	165.6218×10^6
10	6.6702×10^6	59	19.9811×10^6	108	57.0156×10^6	157	171.9601×10^6
11	6.8884×10^6	60	20.7027×10^6	109	59.1111×10^6	158	178.9134×10^6
12	7.1269×10^6	61	21.4950×10^6	110	61.4309×10^6	159	186.5142×10^6
13	7.3889×10^6	62	22.3642×10^6	111	63.9919×10^6	160	170.2547×10^6
14	7.6789×10^6	63	23.3143×10^6	112	61.0114×10^6	161	170.2451×10^6
15	7.9990×10^6	64	21.2818×10^6	113	61.0103×10^6	162	173.7413×10^6
16	7.6264×10^6	65	21.2806×10^6	114	62.3141×10^6	163	177.5128×10^6
17	7.6263×10^6	66	21.7177×10^6	115	63.7198×10^6	164	181.5509×10^6
18	7.7893×10^6	67	22.1891×10^6	116	65.2310×10^6	165	185.8765×10^6
19	7.9650×10^6	68	22.6939×10^6	117	66.8530×10^6	166	190.5041×10^6
20	8.1539×10^6	69	23.2346×10^6	118	68.5992×10^6	167	195.4784×10^6
21	8.3566×10^6	70	23.8130×10^6	119	70.4821×10^6	168	200.8681×10^6
22	8.5749×10^6	71	24.4348×10^6	120	72.5199×10^6	169	207.0913×10^6
23	8.8103×10^6	72	25.1085×10^6	121	74.8675×10^6	170	213.4455×10^6
24	9.0650×10^6	73	25.8864×10^6	122	77.2849×10^6	171	220.4277×10^6
25	9.3584×10^6	74	26.6807×10^6	123	79.9245×10^6	172	228.0624×10^6
26	9.6606×10^6	75	27.5535×10^6	124	82.8109×10^6	173	236.4443×10^6
27	9.9906×10^6	76	28.5078×10^6	125	85.9801×10^6	174	245.7237×10^6
28	10.3514×10^6	77	29.5555×10^6	126	89.4567×10^6	175	255.9676×10^6
29	10.7475×10^6	78	30.7155×10^6	127	93.2571×10^6	176	244.0458×10^6
30	11.1821×10^6	79	31.9959×10^6	128	85.1274×10^6	177	244.0412×10^6
31	11.6571×10^6	80	30.5057×10^6	129	85.1226×10^6	178	249.2563×10^6
32	10.6409×10^6	81	30.5052×10^6	130	86.8707×10^6	179	254.8792×10^6
33	10.6403×10^6	82	31.1570×10^6	131	88.7564×10^6	180	260.9240×10^6
34	10.8588×10^6	83	31.8599×10^6	132	90.7755×10^6	181	267.4122×10^6
35	11.0945×10^6	84	32.6155×10^6	133	92.9383×10^6	182	274.3966×10^6
36	11.3469×10^6	85	33.4265×10^6	134	95.2521×10^6	183	281.9286×10^6
37	11.6173×10^6	86	34.2996×10^6	135	97.7392×10^6	184	290.0798×10^6
38	11.9065×10^6	87	35.2411×10^6	136	100.4340×10^6	185	299.4700×10^6
39	12.2174×10^6	88	36.2600×10^6	137	103.5457×10^6	186	309.1396×10^6
40	12.5543×10^6	89	37.4338×10^6	138	106.7228×10^6	187	319.6981×10^6
41	12.9432×10^6	90	38.6424×10^6	139	110.2139×10^6	188	331.2437×10^6
42	13.3403×10^6	91	39.9623×10^6	140	114.0312×10^6	189	343.9202×10^6
43	13.7767×10^6	92	41.4055×10^6	141	118.2222×10^6	190	357.8269×10^6
44	14.2539×10^6	93	42.9900×10^6	142	122.8619×10^6	191	373.0284×10^6
45	14.7778×10^6	94	44.7284×10^6	143	127.9838×10^6	192	340.5094×10^6
46	15.3577×10^6	95	46.6285×10^6	144	122.0229×10^6	193	340.4903×10^6
47	15.9980×10^6	96	42.5637×10^6	145	122.0206×10^6	194	347.4826×10^6
48	15.2529×10^6	97	42.5613×10^6	146	124.6282×10^6	195	355.0256×10^6

Code	f_{MID} (Hz)	Code	f_{MID} (Hz)	Code	f_{MID} (Hz)	Code	f_{MID} (Hz)
196	363.1019×10^6	219	639.3962×10^6	242	997.0253×10^6	265	1.6567×10^9
197	371.7531×10^6	220	662.4874×10^6	243	1.0195×10^9	266	1.7076×10^9
198	381.0083×10^6	221	687.8404×10^6	244	1.0437×10^9	267	1.7634×10^9
199	390.9568×10^6	222	715.6537×10^6	245	1.0696×10^9	268	1.8245×10^9
200	401.7362×10^6	223	746.0568×10^6	246	1.0976×10^9	269	1.8916×10^9
201	414.1826×10^6	224	681.0188×10^6	247	1.1277×10^9	270	1.9658×10^9
202	426.8911×10^6	225	680.9806×10^6	248	1.1603×10^9	271	2.0477×10^9
203	440.8554×10^6	226	694.9652×10^6	249	1.1979×10^9	272	1.9524×10^9
204	456.1247×10^6	227	710.0511×10^6	250	1.2366×10^9	273	1.9523×10^9
205	472.8887×10^6	228	726.2037×10^6	251	1.2788×10^9	274	1.9941×10^9
206	491.4474×10^6	229	743.5062×10^6	252	1.3250×10^9	275	2.0390×10^9
207	511.9351×10^6	230	762.0166×10^6	253	1.3757×10^9	276	2.0874×10^9
208	488.0916×10^6	231	781.9136×10^6	254	1.4313×10^9	277	2.1393×10^9
209	488.0824×10^6	232	803.4724×10^6	255	1.4921×10^9	278	2.1952×10^9
210	498.5126×10^6	233	828.3653×10^6	256	1.3620×10^9	279	2.2554×10^9
211	509.7584×10^6	234	853.7822×10^6	257	1.3620×10^9	280	2.3206×10^9
212	521.8480×10^6	235	881.7109×10^6	258	1.3899×10^9	281	2.3958×10^9
213	534.8244×10^6	236	912.2494×10^6	259	1.4201×10^9	282	2.4731×10^9
214	548.7933×10^6	237	945.7774×10^6	260	1.4524×10^9	283	2.5576×10^9
215	563.8571×10^6	238	982.8948×10^6	261	1.4870×10^9	284	2.6499×10^9
216	580.1596×10^6	239	1.0239×10^9	262	1.5240×10^9	285	2.7514×10^9
217	598.9401×10^6	240	976.1832×10^6	263	1.5638×10^9	286	2.8626×10^9
218	618.2792×10^6	241	976.1648×10^6	264	1.6069×10^9	287	2.9842×10^9

HI_CODE AND LO_CODE LOOK-UP TABLE

Code is the 9-bit value to be written into HI_CODE[8:0] and LO_CODE[8:0]. Use the high limit code for HI_CODE and the low limit code for LO_CODE.

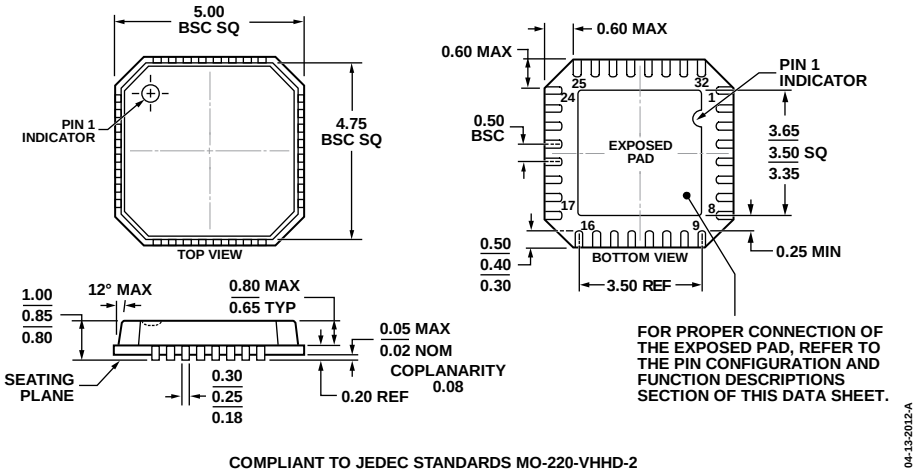
Table 20.

Code	Low Limit	High Limit	Code	Low Limit	High Limit
0	5.7633×10^6	4.8677×10^6	48	16.5410×10^6	13.9411×10^6
1	5.7631×10^6	4.8674×10^6	49	16.5402×10^6	13.9407×10^6
2	5.8777×10^6	4.9708×10^6	50	16.8827×10^6	14.2483×10^6
3	6.0011×10^6	5.0827×10^6	51	17.2521×10^6	14.5807×10^6
4	6.1328×10^6	5.2027×10^6	52	17.6479×10^6	14.9392×10^6
5	6.2738×10^6	5.3312×10^6	53	18.0712×10^6	15.3247×10^6
6	6.4245×10^6	5.4692×10^6	54	18.5258×10^6	15.7411×10^6
7	6.5859×10^6	5.6188×10^6	55	19.0145×10^6	16.1915×10^6
8	6.7593×10^6	5.7807×10^6	56	19.5415×10^6	16.6807×10^6
9	6.9599×10^6	5.9680×10^6	57	20.1465×10^6	17.2471×10^6
10	7.1641×10^6	6.1614×10^6	58	20.7665×10^6	17.8330×10^6
11	7.3860×10^6	6.3740×10^6	59	21.4403×10^6	18.4754×10^6
12	7.6292×10^6	6.6070×10^6	60	22.1738×10^6	19.1829×10^6
13	7.8947×10^6	6.8660×10^6	61	22.9747×10^6	19.9651×10^6
14	8.1855×10^6	7.1541×10^6	62	23.8487×10^6	20.8291×10^6
15	8.5061×10^6	7.4742×10^6	63	24.7993×10^6	21.7805×10^6
16	8.2705×10^6	6.9705×10^6	64	23.0530×10^6	19.4710×10^6
17	8.2701×10^6	6.9703×10^6	65	23.0523×10^6	19.4695×10^6
18	8.4414×10^6	7.1241×10^6	66	23.5108×10^6	19.8831×10^6
19	8.6260×10^6	7.2904×10^6	67	24.0044×10^6	20.3308×10^6
20	8.8239×10^6	7.4696×10^6	68	24.5310×10^6	20.8107×10^6
21	9.0356×10^6	7.6624×10^6	69	25.0951×10^6	21.3248×10^6
22	9.2629×10^6	7.8705×10^6	70	25.6980×10^6	21.8768×10^6
23	9.5073×10^6	8.0958×10^6	71	26.3436×10^6	22.4751×10^6
24	9.7707×10^6	8.3404×10^6	72	27.0373×10^6	23.1230×10^6
25	10.0733×10^6	8.6236×10^6	73	27.8396×10^6	23.8720×10^6
26	10.3832×10^6	8.9165×10^6	74	28.6564×10^6	24.6457×10^6
27	10.7202×10^6	9.2377×10^6	75	29.5438×10^6	25.4960×10^6
28	11.0869×10^6	9.5915×10^6	76	30.5167×10^6	26.4281×10^6
29	11.4873×10^6	9.9825×10^6	77	31.5787×10^6	27.4641×10^6
30	11.9244×10^6	10.4145×10^6	78	32.7422×10^6	28.6162×10^6
31	12.3996×10^6	10.8902×10^6	79	34.0244×10^6	29.8968×10^6
32	11.5265×10^6	9.7355×10^6	80	33.0819×10^6	27.8821×10^6
33	11.5261×10^6	9.7347×10^6	81	33.0805×10^6	27.8813×10^6
34	11.7554×10^6	9.9415×10^6	82	33.7655×10^6	28.4965×10^6
35	12.0022×10^6	10.1654×10^6	83	34.5041×10^6	29.1615×10^6
36	12.2655×10^6	10.4053×10^6	84	35.2957×10^6	29.8783×10^6
37	12.5475×10^6	10.6624×10^6	85	36.1424×10^6	30.6494×10^6
38	12.8490×10^6	10.9384×10^6	86	37.0517×10^6	31.4822×10^6
39	13.1718×10^6	11.2376×10^6	87	38.0290×10^6	32.3831×10^6
40	13.5186×10^6	11.5615×10^6	88	39.0830×10^6	33.3615×10^6
41	13.9198×10^6	11.9360×10^6	89	40.2930×10^6	34.4942×10^6
42	14.3282×10^6	12.3228×10^6	90	41.5329×10^6	35.6659×10^6
43	14.7719×10^6	12.7480×10^6	91	42.8807×10^6	36.9508×10^6
44	15.2584×10^6	13.2140×10^6	92	44.3477×10^6	38.3658×10^6
45	15.7894×10^6	13.7321×10^6	93	45.9493×10^6	39.9301×10^6
46	16.3711×10^6	14.3081×10^6	94	47.6975×10^6	41.6582×10^6
47	17.0122×10^6	14.9484×10^6	95	49.5986×10^6	43.5610×10^6

Code	Low Limit	High Limit
96	46.1061×10^6	38.9419×10^6
97	46.1045×10^6	38.9390×10^6
98	47.0217×10^6	39.7661×10^6
99	48.0087×10^6	40.6617×10^6
100	49.0620×10^6	41.6214×10^6
101	50.1902×10^6	42.6496×10^6
102	51.3960×10^6	43.7535×10^6
103	52.6872×10^6	44.9502×10^6
104	54.0746×10^6	46.2459×10^6
105	55.6792×10^6	47.7440×10^6
106	57.3128×10^6	49.2913×10^6
107	59.0876×10^6	50.9920×10^6
108	61.0334×10^6	52.8561×10^6
109	63.1575×10^6	54.9282×10^6
110	65.4843×10^6	57.2324×10^6
111	68.0487×10^6	59.7936×10^6
112	66.1639×10^6	55.7643×10^6
113	66.1609×10^6	55.7626×10^6
114	67.5309×10^6	56.9931×10^6
115	69.0082×10^6	58.3229×10^6
116	70.5914×10^6	59.7566×10^6
117	72.2848×10^6	61.2989×10^6
118	74.1034×10^6	62.9643×10^6
119	76.0580×10^6	64.7662×10^6
120	78.1660×10^6	66.7230×10^6
121	80.5861×10^6	68.9885×10^6
122	83.0658×10^6	71.3318×10^6
123	85.7613×10^6	73.9016×10^6
124	88.6953×10^6	76.7317×10^6
125	91.8987×10^6	79.8603×10^6
126	95.3950×10^6	83.3164×10^6
127	99.1972×10^6	87.1220×10^6
128	92.2121×10^6	77.8839×10^6
129	92.2090×10^6	77.8780×10^6
130	94.0434×10^6	79.5323×10^6
131	96.0174×10^6	81.3234×10^6
132	98.1240×10^6	83.2427×10^6
133	100.3804×10^6	85.2993×10^6
134	102.7920×10^6	87.5071×10^6
135	105.3744×10^6	89.9004×10^6
136	108.1491×10^6	92.4919×10^6
137	111.3583×10^6	95.4879×10^6
138	114.6257×10^6	98.5827×10^6
139	118.1753×10^6	101.9841×10^6
140	122.0668×10^6	105.7122×10^6
141	126.3150×10^6	109.8565×10^6
142	130.9686×10^6	114.4648×10^6
143	136.0974×10^6	119.5872×10^6
144	132.3278×10^6	111.5286×10^6
145	132.3218×10^6	111.5252×10^6
146	135.0619×10^6	113.9862×10^6
147	138.0164×10^6	116.6459×10^6
148	141.1829×10^6	119.5132×10^6
149	144.5697×10^6	122.5977×10^6
150	148.2068×10^6	125.9286×10^6
151	152.1160×10^6	129.5324×10^6
152	156.3320×10^6	133.4459×10^6
153	161.1721×10^6	137.9770×10^6
154	166.1317×10^6	142.6637×10^6
155	171.5227×10^6	147.8032×10^6
156	177.3906×10^6	153.4634×10^6
157	183.7974×10^6	159.7205×10^6
158	190.7899×10^6	166.6328×10^6
159	198.3944×10^6	174.2440×10^6
160	184.4242×10^6	155.7678×10^6
161	184.4181×10^6	155.7560×10^6
162	188.0868×10^6	159.0645×10^6
163	192.0348×10^6	162.6467×10^6
164	196.2480×10^6	166.4855×10^6
165	200.7608×10^6	170.5985×10^6
166	205.5841×10^6	175.0142×10^6
167	210.7488×10^6	179.8008×10^6
168	216.2983×10^6	184.9838×10^6
169	222.7166×10^6	190.9759×10^6
170	229.2514×10^6	197.1654×10^6
171	236.3506×10^6	203.9681×10^6
172	244.1336×10^6	211.4245×10^6
173	252.6300×10^6	219.7129×10^6
174	261.9373×10^6	228.9296×10^6
175	272.1948×10^6	239.1744×10^6
176	264.6556×10^6	223.0571×10^6
177	264.6437×10^6	223.0505×10^6
178	270.1237×10^6	227.9723×10^6
179	276.0329×10^6	233.2917×10^6
180	282.3657×10^6	239.0265×10^6
181	289.1393×10^6	245.1954×10^6
182	296.4136×10^6	251.8572×10^6
183	304.2321×10^6	259.0647×10^6
184	312.6640×10^6	266.8919×10^6
185	322.3443×10^6	275.9539×10^6
186	332.2633×10^6	285.3273×10^6
187	343.0453×10^6	295.6065×10^6
188	354.7812×10^6	306.9268×10^6
189	367.5947×10^6	319.4411×10^6
190	381.5798×10^6	333.2656×10^6
191	396.7887×10^6	348.4879×10^6
192	368.8485×10^6	311.5355×10^6
193	368.8362×10^6	311.5120×10^6
194	376.1735×10^6	318.1291×10^6
195	384.0696×10^6	325.2934×10^6
196	392.4961×10^6	332.9710×10^6
197	401.5216×10^6	341.1971×10^6
198	411.1681×10^6	350.0283×10^6
199	421.4977×10^6	359.6016×10^6
200	432.5966×10^6	369.9675×10^6
201	445.4332×10^6	381.9518×10^6

Code	Low Limit	High Limit
202	458.5027×10^6	394.3307×10^6
203	472.7012×10^6	407.9363×10^6
204	488.2673×10^6	422.8489×10^6
205	505.2599×10^6	439.4259×10^6
206	523.8745×10^6	457.8593×10^6
207	544.3897×10^6	478.3487×10^6
208	529.3112×10^6	446.1142×10^6
209	529.2874×10^6	446.1009×10^6
210	540.2475×10^6	455.9446×10^6
211	552.0658×10^6	466.5834×10^6
212	564.7314×10^6	478.0529×10^6
213	578.2786×10^6	490.3908×10^6
214	592.8272×10^6	503.7145×10^6
215	608.4642×10^6	518.1295×10^6
216	625.3279×10^6	533.7838×10^6
217	644.6885×10^6	551.9079×10^6
218	664.5266×10^6	570.6547×10^6
219	686.0907×10^6	591.2129×10^6
220	709.5624×10^6	613.8536×10^6
221	735.1895×10^6	638.8822×10^6
222	763.1596×10^6	666.5311×10^6
223	793.5774×10^6	696.9759×10^6
224	737.6969×10^6	623.0711×10^6
225	737.6724×10^6	623.0240×10^6
226	752.3471×10^6	636.2582×10^6
227	768.1392×10^6	650.5869×10^6
228	784.9921×10^6	665.9419×10^6
229	803.0432×10^6	682.3941×10^6
230	822.3363×10^6	700.0567×10^6
231	842.9953×10^6	719.2032×10^6
232	865.1931×10^6	739.9350×10^6
233	890.8664×10^6	763.9035×10^6
234	917.0055×10^6	788.6615×10^6
235	945.4024×10^6	815.8726×10^6
236	976.5346×10^6	845.6979×10^6
237	1.0105×10^9	878.8518×10^6
238	1.0477×10^9	915.7186×10^6
239	1.0888×10^9	956.6975×10^6
240	1.0586×10^9	892.2284×10^6
241	1.0586×10^9	892.2018×10^6
242	1.0805×10^9	911.8893×10^6
243	1.1041×10^9	933.1668×10^6
244	1.1295×10^9	956.1059×10^6
245	1.1566×10^9	980.7817×10^6
246	1.1857×10^9	1.0074×10^9
247	1.2169×10^9	1.0363×10^9
248	1.2507×10^9	1.0676×10^9
249	1.2894×10^9	1.1038×10^9
250	1.3291×10^9	1.1413×10^9
251	1.3722×10^9	1.1824×10^9
252	1.4191×10^9	1.2277×10^9
253	1.4704×10^9	1.2778×10^9
254	1.5263×10^9	1.3331×10^9
255	1.5872×10^9	1.3940×10^9
256	1.4754×10^9	1.2461×10^9
257	1.4753×10^9	1.2460×10^9
258	1.5047×10^9	1.2725×10^9
259	1.5363×10^9	1.3012×10^9
260	1.5700×10^9	1.3319×10^9
261	1.6061×10^9	1.3648×10^9
262	1.6447×10^{9v}	1.4001×10^9
263	1.6860×10^9	1.4384×10^9
264	1.7304×10^9	1.4799×10^9
265	1.7817×10^9	1.5278×10^9
266	1.8340×10^9	1.5773×10^9
267	1.8908×10^9	1.6317×10^9
268	1.9531×10^9	1.6914×10^9
269	2.0210×10^9	1.7577×10^9
270	2.0955×10^9	1.8314×10^9
271	2.1776×10^9	1.9134×10^9
272	2.1172×10^9	1.7845×10^9
273	2.1171×10^9	1.7844×10^9
274	2.1610×10^9	1.8238×10^9
275	2.2083×10^9	1.8663×10^9
276	2.2589×10^9	1.9122×10^9
277	2.3131×10^9	1.9616×10^9
278	2.3713×10^9	2.0149×10^9
279	2.4339×10^9	2.0725×10^9
280	2.5013×10^9	2.1351×10^9
281	2.5788×10^9	2.2076×10^9
282	2.6581×10^9	2.2826×10^9
283	2.7444×10^9	2.3649×10^9
284	2.8382×10^9	2.4554×10^9
285	2.9408×10^9	2.5555×10^9
286	3.0526×10^9	2.6661×10^9
287	3.1743×10^9	2.7879×10^9

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 43. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADN2817ACPZ	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-4	490
ADN2817ACPZ-RL	−40°C to +85°C	32-Lead LFCSP_VQ, 13″ Tape and Reel	CP-32-4	5,000
ADN2817ACPZ-RL7	−40°C to +85°C	32-Lead LFCSP_VQ, 7″ Tape and Reel	CP-32-4	1,500
ADN2818ACPZ	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-4	490
ADN2818ACPZ-RL	−40°C to +85°C	32-Lead LFCSP_VQ, 13″ Tape and Reel	CP-32-4	5,000
ADN2818ACPZ-RL7	−40°C to +85°C	32-Lead LFCSP_VQ, 7″ Tape and Reel	CP-32-4	1,500
EVAL-ADN2817EBZ		Evaluation Board for ADN2817		
EVAL-ADN2818EBZ		Evaluation Board for ADN2818		

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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