深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LM16080CCA

LCD Module User Manual

Prepared by: Date:	Checked by: Date:	Approved by: Date:

Rev.	Descriptions	Release Date
0.1	Prelimiay release	2011-01-20

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Table of Content

1. Basic Specifications 3
1.1 Display Specifications 3
1.2 Mechanical Specifications 3
1.3 Block Diagram 3
1.4 Terminal Functions 4
1.5 Interfacing Setting(FPC) 4
2. Absolute Maximum Ratings 5
3. Electrical Characteristics 5
3.1 DC Characteristics 5
3.2 AC Characteristics 6
3.3 Reset Input 9
4. Function Specifications 10
4.1 Application circuit (Example) 10
4.2 Resetting the LCD module 10
4.3 Display Memory Map 10
4.4 Display Commands 11
5. Design and Handling Precaution 12

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1. Basic Specifications

1.1 Display Specifications

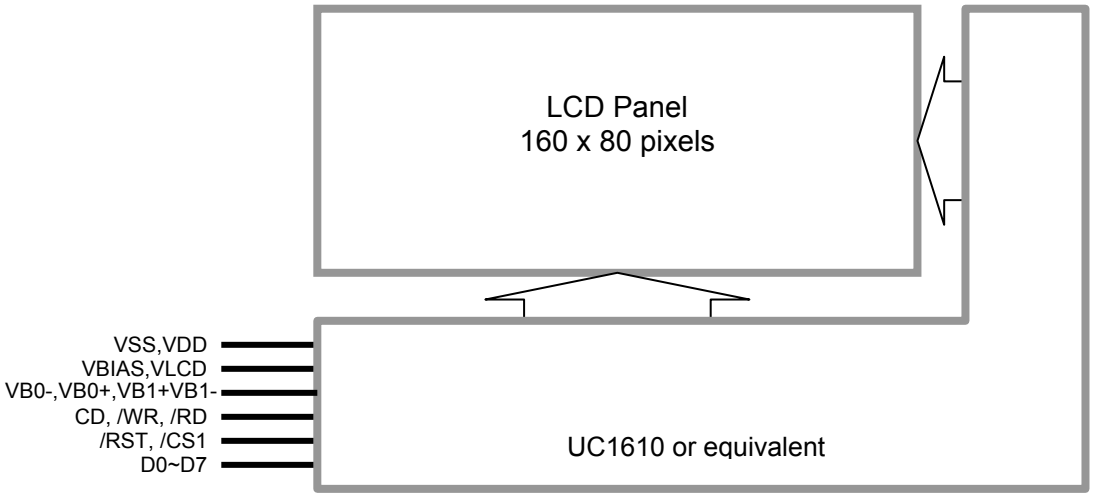
1) LCD Display Mode : FSTN, Positive, Transflective
2) Display Color : Display Data = “1” : Dark Gray (*1)
: Display Data = “0” : Light Gray (*2)
3) Viewing Angle : 6 H
4) Driving Method : 1/80 duty, 1/10bias

Note:
*1. Color tone may slightly change by Temperature and Driving Condition.
*2. The Color is defined as the inactive / background color

1.2 Mechanical Specifications

1) Outline Dimension : 59.6 x 43.0 x 4.2
(see attached Outline Drawing for details)

1.3 Block Diagram



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1.4 Terminal Functions

Pin No.	Pin Name	I/O	Descriptions			
			Display			
			8-bit parallel 80mode <default>	8-bit parallel 60mode	Serial	
					4wire	3wire
1	ESD	Power	Connect To VSS			
2	/CS	Input	Chip Select /CS=L, enable access to the LCD module /CS=H, disable access to the LCD module			
3	/RST	Input	Reset signal /RST = L, Initialization is executed /RST = H, Normal running.			
4	RS	Input	Register Select RS = H, Transferring the Display RAM data RS = L, Transferring the Instruction data			
5	/WR	Input	/WR=L→H, /RD=H; Data or Instruction latch into the LCD module		VSS	
6	/RD	Input	/WR=H, /RD=L; Data or Status read form the LCD module		VSS	
7	D0	I/O	8-bit Data bus Three state I/O terminal for display data or instruction data		VDD	VDD
8	D1	I/O			VSS	VDD
:	:	:			-	
11	D4	I/O			Serial data input	
:	:	:			-	
14	D7	I/O			Serial clock input	
15	VDD	Power	Poitive Power Supply			
16	NC	-	NO Connection Keep Open			
17	VSS	Power	0V Power Supply, Ground			
18	NC	-	NO Connection Keep Open			
19	NC	-	NO Connection Keep Open			
20	VB0-	Onput	Booster Capacitor Terminals			
21	VB0+					
22	VB1+					
23	VB1-					
24	NC	-	NO Connection Keep Open			
25	NC	-	NO Connection Keep Open			
26	VBIAS	Power	Connect a small bypass capacitor between VBIAS and VSS			
27	NC	-	NO Connection Keep Open			
28	NC	-	NO Connection Keep Open			
29	VLCD	Power	Power Booster Output			
30	ESD	Power	Connect To VSS			

1.5 Interfacing Setting(FPC)

BM0-	BM0+	BM1-	BM1+	Function Discription
close	open	open	close	80 mode 8 bit selected
open	close	open	close	68 mode 8 bit selected
open	open	close	open	serial mode

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2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	0	3.4	V	V_{SS} = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics

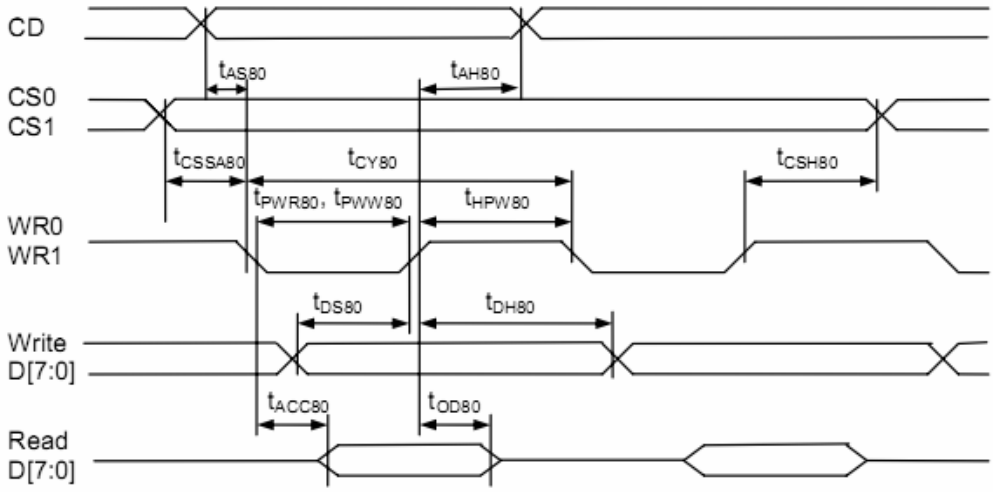
V_{SS}=0V, V_{DD} =3.3V, T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	V_{DD}	3.0	-	3.4	V	VDD
Input High Voltage	V_{IH}	$0.8V_{DD}$	-	V_{DD}	V	/CS, /RST, RS, /WR(R/W), /RD(E), D0-D5, D6(SCLK), D7(SID)
Input Low Voltage	V_{IL}	V_{SS}	-	$0.2V_{DD}$	V	
Output High Voltage (I_{OH}=-0.4mA)	V_{OH}	$0.8V_{DD}$	-	V_{DD}	V	D0-D7
Output Low Voltage (I_{OL}=+0.4mA)	V_{OL}	V_{SS}	-	$0.2V_{DD}$	V	
Operating Current	I_{DD}	-	0.94	2.7	mA	VDD

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3.2 AC Characteristics

3.2.1 8080 Interface



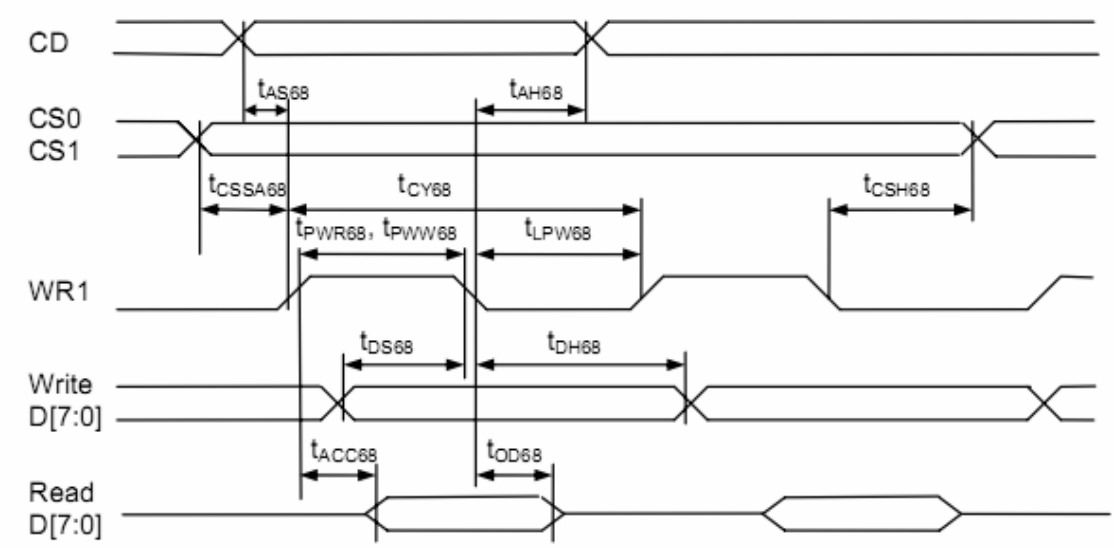
8080Interface Timing Diagram

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		5 15	–	nS
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	nS
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		70 70	–	nS
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		40 40	–	nS
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 70 40 70 40	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 15	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 25	60	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		5 5		nS

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3.2.2 6800 Interface



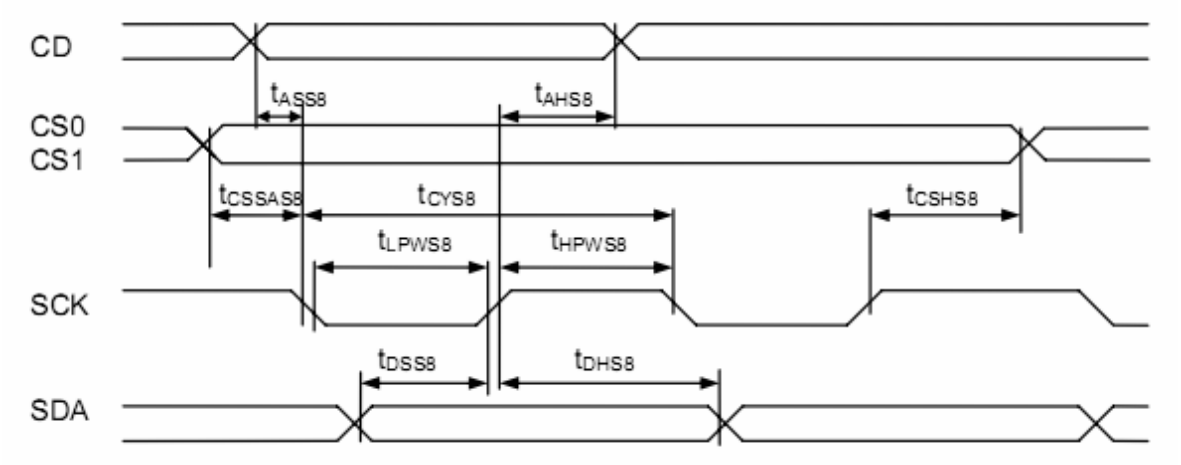
6800 Interface Timing Diagram

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		5 15	–	nS
t_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	nS
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		70 70	–	nS
t_{PWW68}		Pulse width 8 bits (write) 4 bits		40 40	–	nS
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 70 40 70 40	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 15	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 25	60	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		5 5		nS

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3.2.3 Serial Interface(for S8/S8uc)



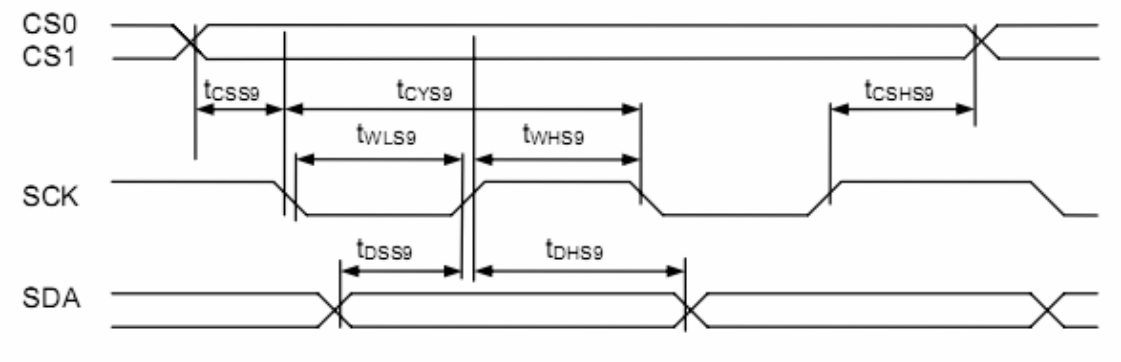
Serial Interface Timing Diagram(for S8/S8uc)

($2.5V \leq V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		5	–	nS
t_{AHS8}		Address hold time		20	–	nS
t_{CYS8}	SCK	System cycle time		125	–	nS
t_{LPWS8}		Low pulse width		60	–	nS
t_{HPWS8}		High pulse width		60	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		5 15		nS

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3.2.4 Serial Interface(for S9)



Serial Interface Timing Diagram(for S9)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		80	–	nS
t_{LPWS9}		Low pulse width		35	–	nS
t_{HPWS9}		High pulse width		35	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5		nS

3.3 Reset Input

($1.8V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		1	–	μS

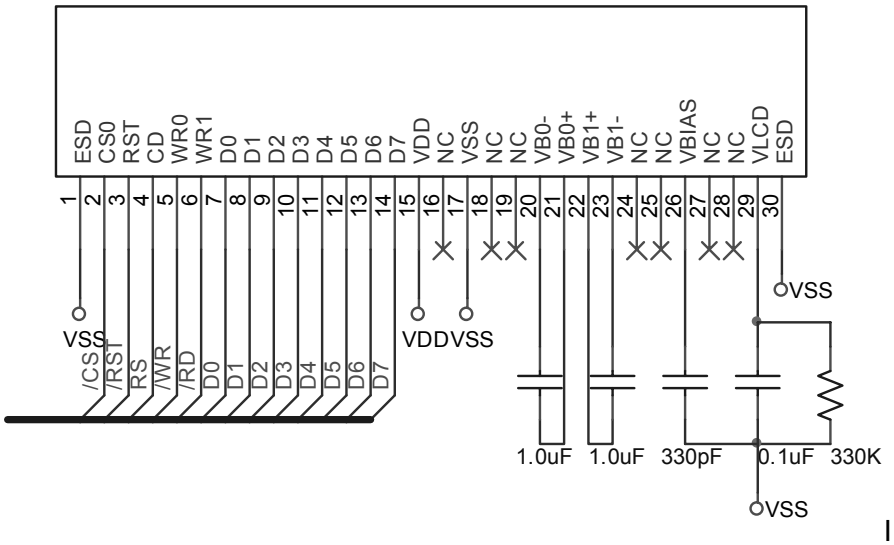


Reset Timing Diagram

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4. Function Specifications

4.1 Application circuit (Example)



Note: 8080 mode (Default setting), please refer to UC1610 datasheet for details

4.2 Resetting the LCD module

The LCD module should be initialized by setting /RST terminal at low level after the power supply stable.

4.3 Display Memory Map

Page Address	Data	LCD Module Top View						
0	D0 : D7							
1	D0 : D7							
2	D0 : D7							
: :					160x80 pixels			
7	D0 : D7							
8	D0 : D7							
9	D0 : D7							
Column Address		00h	01h	02h	. . .	9Dh	9Eh	9Fh

Note: Display start line = 0, COM0 Register=0, Duty Ratio = 1/80, MY=0,MX=0,LC0=0

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4.4 Display Commands

The following is a list of host commands supported by UC 1610

C/D 0:Control, 1:Data
W/R 0:Write Cycle 1:Read Cycle

\# Useful Data bits
\- Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	ID	MX	MY	WA	DE	PM7	PM6	1	Get Status	N/A
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	1
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control (double byte command)	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0, or 1	N/A
		0	0	#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0
10	Set Page Address	0	0	0	1	1	#	#	#	#	#	Set PA[4:0]	0
11	Set V_{BIAS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	B2H
		0	0	#	#	#	#	#	#	#	#		
12	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[8:7]	00b: Disable
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	00b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
18	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0b
19	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
20	Set LCD Gray Shade	0	0	1	1	0	1	0	0	#	#	Set LC[6:5]	00b
21	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
22	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
23	Set Test Control (double byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
24	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b: 11
25	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	AC[3]=0
26	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	AC[3]=1
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Set WPC0[7:0]	0
		0	0	#	#	#	#	#	#	#	#		
31	Set Window Programming Starting Page Address	0	0	1	1	1	1	0	1	0	1	Set WPP0[4:0]	0
		0	0	-	-	-	#	#	#	#	#		
32	Set Window Programming Ending Column Address	0	0	1	1	1	1	0	1	1	0	Set WPC1[7:0]	159
		0	0	#	#	#	#	#	#	#	#		
33	Set Window Programming Ending Page Address	0	0	1	1	1	1	0	1	1	1	Set WPP1[4:0]	31
		0	0	-	-	-	#	#	#	#	#		
34	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[4]	0: Disable

*All other bit patterns other than the commands listed above may result in underfined behavior

4.4.1 Power off the LCD Module

LCD module should enter sleep mode before power off.

4.4.2 Refreshing The LCD Module

It recommends that the operating modes and display contents should be refreshed periodically to prevent the effect of unexpected noise.

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5. Design and Handling Precaution

1. The LCD panel is made by glass. Any mechanical shock (eg. dropping form high place) will damage the LCD module.
2. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.
3. The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.
4. Never attempt to disassemble or rework the LCD module.
5. Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
6. When mounting the LCD module, make sure that it is free form twisting, warping and distortion.
7. Ensure to provide enough space (with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result.
8. Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
9. Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
10. LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
11. When peeling off the protective film from LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12. Take care and prevent get hurt by the LCD panel sharp edge.
13. Never operate the LCD module exceed the absolute maximum ratings.
14. Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
15. Never apply signal to the LCD module without power supply.
16. IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
17. LCD module reliability may be reduced by temperature shock.
18. When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module

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