features

- 11.2-GHz Bandwidth
- 5.5-kΩ Differential Transimpedance
- 8.5-pA/√Hz Typical Input Referred Noise
- 2-mA Maximum Input Current
- Received Signal Strength Indication
- CML Data Outputs
- Offset Cancellation
- Single 3.3-V Supply
- Bare-Die Option

applications

- SONET OC−192
- 10-Gbps Ethernet Receivers
- 10-Gbps Fibre Channel Receivers

description

The ONET9901TA is a high-speed transimpedance amplifier used in SDH/SONET systems with data rates up to 10.7 Gbps. It features a low input referred noise, 11.2-GHz bandwidth and a 5.5-kΩ transimpedance.

The ONET9901TA device is available in die form and requires a single 3.3-V supply. The ONET9901TA is power efficient and dissipates less than 100 mW (typical). The ONET9901TA is characterized for operations from 0°C to 85°C.

available options

T_A	PACKAGED DEVICE
0°C to 85°C	ONET9901TAY



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block diagram

The ONET9901TA is a high performance 10.7-Gbps transimpedance amplifier that can be segmented into the signal path, filter, and offset cancellation block. The signal path consists of a transimpedance amplifier stage, a voltage amplifier, and an output buffer. The filter circuit provides a filtered VCC for the photodiode. The offset correction circuit uses an internal low-pass filter to cancel the dc on the input and it provides a signal to monitor the received signal strength. A simplified block diagram of the ONET9901TA is shown in Figure 1.

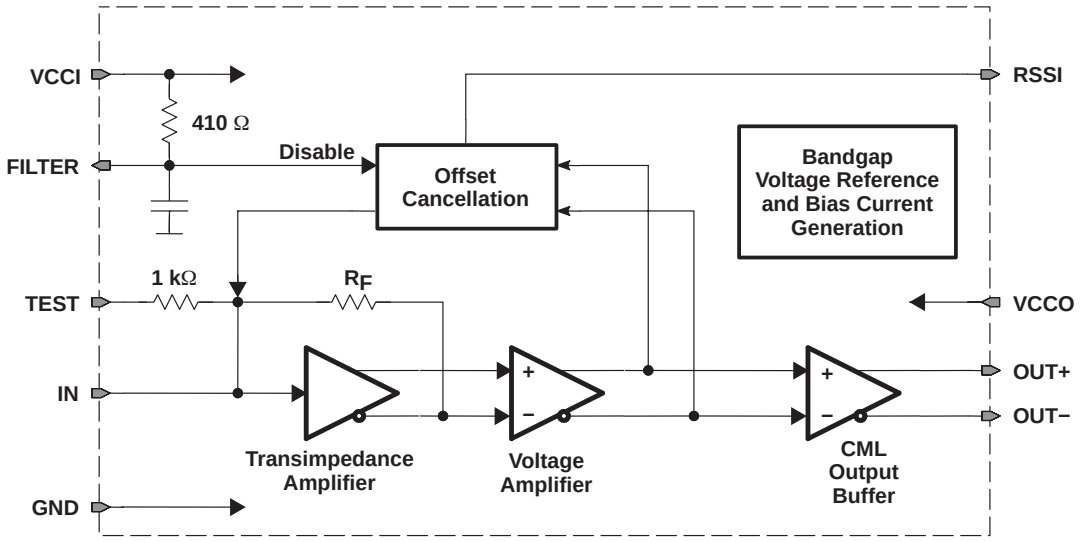


Figure 1. Block Diagram

signal path

The first stage of the signal path is a transimpedance amplifier that takes the photodiode current and converts it to a voltage signal. The second stage is a voltage amplifier that provides additional gain. The output of the second stage feeds the output buffer and the offset cancellation circuitry. The third and final signal path stage of the ONET9901TA is the output buffer. The output buffer provides CML outputs with an on-chip 50-Ω back-termination to VCCO.

filter circuitry

The filter pin provides a filtered VCC for the photodiode bias. The on-chip low-pass filter for the photodiode VCC is implemented using a filter resistor of 410 Ω and an internal capacitor. If additional filtering is required for the application, an external capacitor should be connected to the FILTER pin.

offset cancellation and RSSI

The offset cancellation circuitry performs low pass filtering of the output of the voltage amplifier. This senses the dc offset at the input of the ONET9901TA. The circuitry subtracts current from the input to effectively cancel the dc. The sensed current is mirrored and is used to generate the RSSI output through an external 10-kΩ resistor. To disable the offset correction loop, the FILTER pin should be tied to GND.

bond pad assignment

The ONET9901TA is available as bare-die. The location of the bondpads is shown in Figure 2. The circuit is characterized for ambient temperatures between 0°C and 85°C.

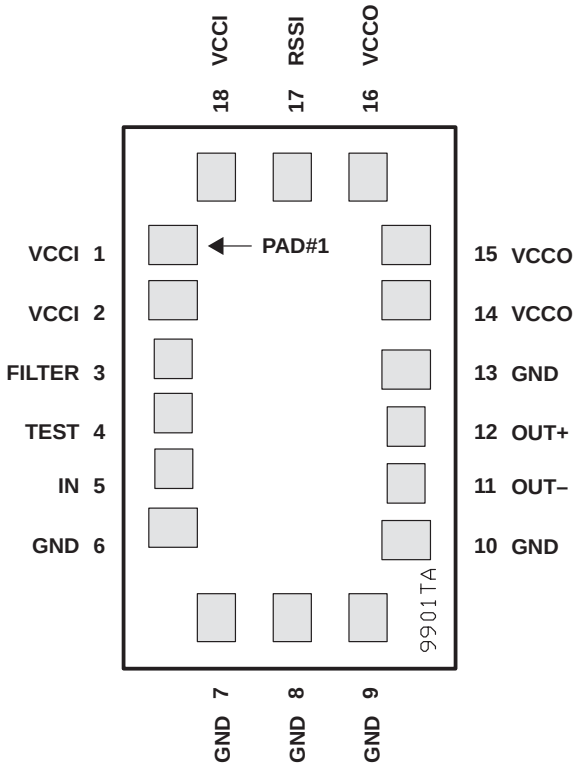


Figure 2. Bond Pad Assignment of the ONET9901TA

terminal functions

The following table shows a pad description for the ONET9901TA.

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
VCCI	1, 2, 18	Supply	Input stage 3.3-V ±10% supply voltage.
FILTER	3	Analog	Bias voltage for the photodiode (connects to an internal 410-Ω resistor to VCCI). To disable the offset correction loop, connect the FILTER pin to GND.
TEST	4	Analog in	Test pad. Connects to IN via a 1-kΩ resistor.
IN	5	Analog in	Data input to TIA
GND	6−10,13	Supply	Circuit ground
OUT−	11	Analog out	Inverted data output. On-chip 50-Ω back-terminated to VCCO.
OUT+	12	Analog out	Non-inverted data output. On-chip 50-Ω back-terminated to VCCO.
VCCO	14−16	Supply	Output stage 3.3-V ±10% supply voltage.
RSSI	17	Analog out	Analog output voltage proportional to the input data amplitude. Indicates the strength of the received signal (RSSI).

absolute maximum ratings

over operating free-air temperature range unless otherwise noted†

		VALUE	UNIT
V_{CCI}, V_{CCO}	Supply voltage, See Note 1	–0.3 to 4	V
$V_{(FILTER)}$, $V_{(OUT+)}$, $V_{(OUT−)}$, $V_{(RSSI)}$	Voltage at FILTER, OUT+, OUT−, and RSSI, See Note 1	–0.3 to 4	V
$I_{(IN)}$, $I_{(TEST)}$	Supply current into IN and TEST	−5 to 5	mA
$I_{(FILTER)}$	Supply current into FILTER	−8 to 8	mA
$I_{(OUT+)}$, $I_{(OUT−)}$	Continuous current at outputs	−25 to 25	mA
ESD	ESD rating at all pins	2	kV (HBM)
$T_{J(max)}$	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	−65 to 85	°C
T_A	Operating free-air temperature range	0 to 85	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{CCI}, V_{CCO}	3	3.3	3.6	V
Operating free-air temperature, T_A	0		85	°C

dc electrical characteristics

over recommended operating conditions (unless otherwise noted), typical operating condition is at $V_{CCI} = V_{CCO} =$ 3.3 V and $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
I_{CC}	Supply current			30	41	mA
V_{IN}	Input bias voltage			0.84	0.96	V
r_o	Output resistance	Single-ended to VCC		50		Ω
$r_{(FILTER)}$	Photodiode filter resistance		330	410	500	Ω

ac electrical characteristics

over recommended operating conditions (unless otherwise noted), typical operating condition is at V_{CCI} = V_{CCO} = 3.3 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IN,OVL}$	AC input overload current		2			mA_{p-p}
	Input linear range	0.95 < linearity < 1.05	50	60		μA_{p-p}
A_{RSSI}	RSSI gain	10-kΩ load, See Note 2	1500	2000	2500	V/A
$Z_{(21)}$	Small signal transimpedance	Differential output, 10 μA_{p-p} < I_{IN} = < 50 μA_{p-p}	4400	5500	6600	Ω
$BW_{(H_3dB)}$	Small signal bandwidth	C_{PD} = 0.2 pF		11.2		GHz
$BW_{(L_3dB)}$	Low frequency −3 dB bandwidth	−3 dB, I_{IN} = < 50 μA_{p-p} dc		17		kHz
$BW_{(H_3dB_RSSI)}$	RSSI bandwidth			5		kHz
$I_{N,IN}$	Input referred RMS noise	C_{PD} = 0.2 pF		900		nA
	Input referred noise density	C_{PD} = 0.2 pF		8.5		pA/√Hz
DJ	Deterministic jitter	I_{IN} < 1.3 mA_{p-p} (K28.5 pattern)		7		ps_{p-p}
		I_{IN} = 2 mA_{p-p} (K28.5 pattern)		11	22	
$V_{OD(max)}$	Maximum differential output voltage	I_{IN} = 1 mA_{p-p}		500	700	mV_{p-p}

NOTE 2: On the chip, a 6725-Ω resistor is used in parallel to the external 10-kΩ resistor, resulting in a total 4-kΩ resistor for a typical process. By choosing an appropriate external resistor, the typical RSSI gain can be adjusted. Without an external resistor, the RSSI gain is approximately 3360 V/A under typical conditions.

APPLICATION INFORMATION

Figure 3 shows the ONET9901TA being used as a receiver in a typical fiber optic application. The ONET9901TA converts the electrical current generated by the PIN photodiode into a differential voltage output. The FILTER input provides a dc bias voltage for the PIN that is low pass filtered by the combination of the internal 410-Ω resistor and internal capacitor. For additional power supply filtering, use an external capacitor (C_{FILTER}). The RSSI output is used to mirror the photodiode output current and must be connected via a 10-kΩ resistor to GND or left open. Within the ONET9901TA, the OUT+ and OUT− pins are internally terminated by a 50-Ω pullup to VCCO.

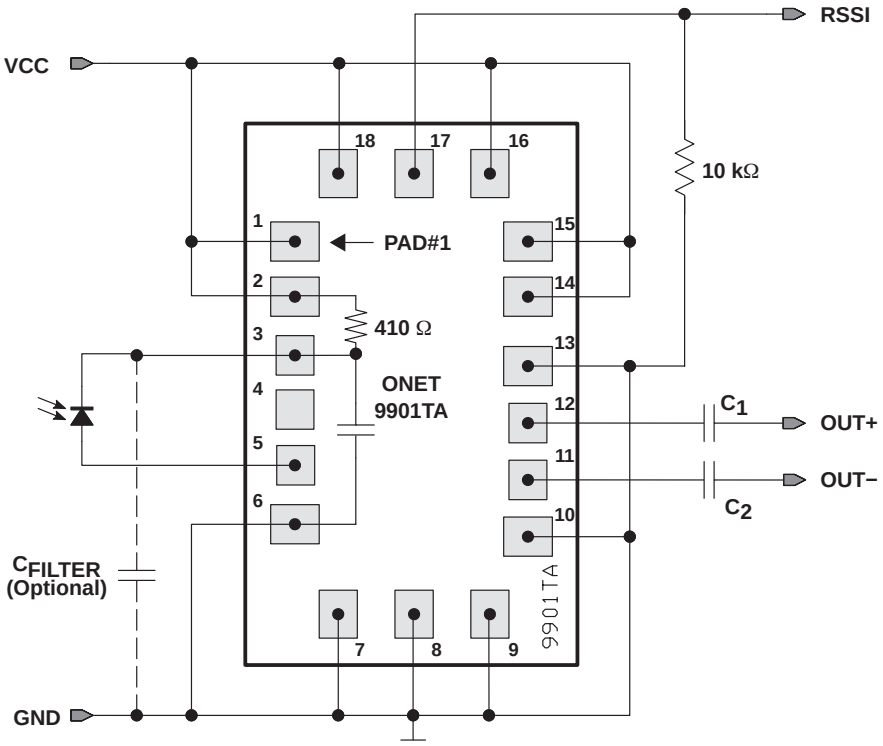


Figure 3. Basic Application Circuit

board layout

Careful attention to board layout parasitics and external components is necessary to achieve optimal performance with a high-performance transimpedance amplifier like the ONET9901TA.

Recommendations that optimize performance include:

1. Minimize total capacitance on the IN pad by using a low-capacitance photodiode and paying attention to stray capacitances. Place the photodiode close to the ONET9901TA die in order to minimize the bond wire length and thus the parasitic inductance.
2. The external filter capacitor (C_{FILTER}) may have an impact on the transfer function of the TIA and must be chosen with care based on the module implementation.
3. Use identical termination and symmetrical transmission lines at the differential output pins OUT+ and OUT–.
4. Use short bond wire connections for the supply terminals VCCI, VCCO, and GND. Provide sufficient supply voltage filtering.

chip dimensions and pad locations

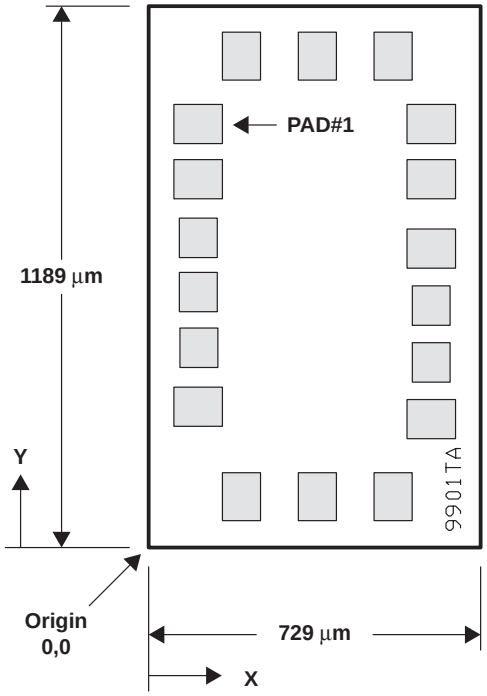


Figure 4. Chip Dimensions and Pad Locations

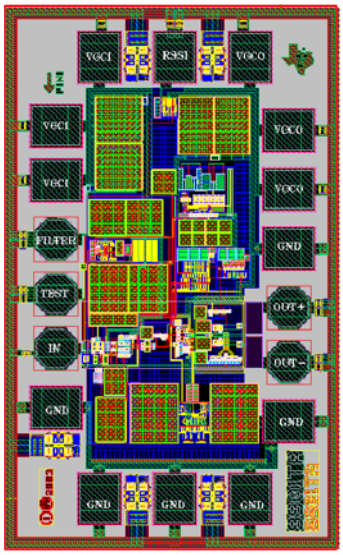


Figure 5. Chip Layout

PAD	LOWER LEFT COORDINATE		UPPER RIGHT COORDINATE		SYMBOL	TYPE	DESCRIPTION
	x [μm]	y [μm]	x [μm]	y [μm]			
1	57	887	162	972	VCCI	Supply	Input stage 3.3-V ±10% supply voltage
2	57	767	162	852	VCCI	Supply	Input stage 3.3-V ±10% supply voltage
3	67	637	152	722	FILTER	Analog	Bias voltage for photodiode
4	67	517	152	602	TEST	Analog in	Test pad. Connects to IN via a 1-kΩ resistor
5	67	397	152	482	IN	Analog in	Data input to TIA
6	57	267	162	352	GND	Supply	Circuit ground
7	162	57	247	162	GND	Supply	Circuit ground
8	327	57	412	162	GND	Supply	Circuit ground
9	492	57	577	162	GND	Supply	Circuit ground
10	567	237	672	322	GND	Supply	Circuit ground
11	577	367	662	452	OUT–	Analog out	Inverted data output
12	577	487	662	572	OUT+	Analog out	Non-inverted data output
13	567	617	672	702	GND	Supply	Circuit ground
14	567	747	672	832	VCCO	Supply	Output stage 3.3-V ±10% supply voltage
15	567	877	672	962	VCCO	Supply	Output stage 3.3-V ±10% supply voltage
16	492	1027	577	1132	VCCO	Supply	Output stage 3.3-V ±10% supply voltage
17	327	1027	412	1132	RSSI	Analog out	RSSI output voltage signal
18	162	1027	247	1132	VCCI	Supply	Input stage 3.3-V ±10% supply voltage

Table 1. Pad Locations and Description of the ONET9901TA

TYPICAL CHARACTERISTICS

INPUT REFERRED NOISE CURRENT vs AVERAGE INPUT CURRENT

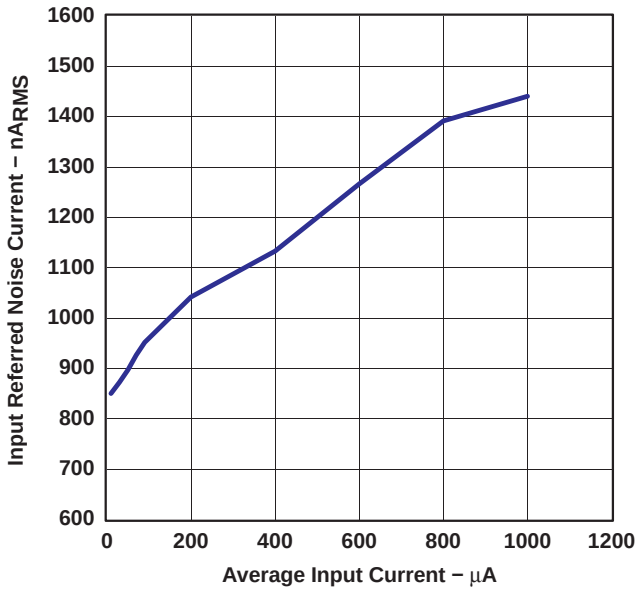


Figure 6

INPUT REFERRED NOISE CURRENT vs AMBIENT TEMPERATURE

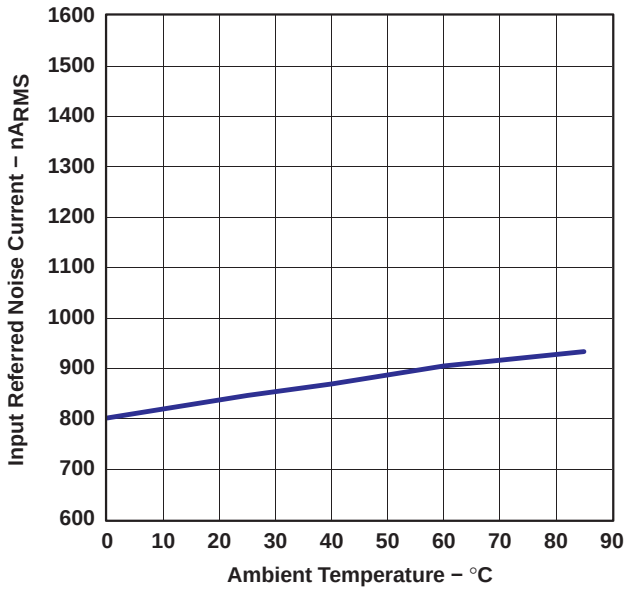


Figure 7

DIFFERENTIAL OUTPUT VOLTAGE vs INPUT CURRENT

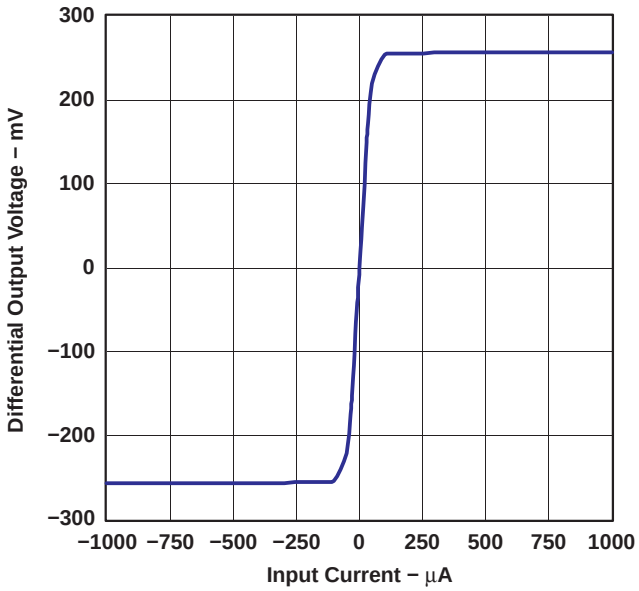


Figure 8

TRANSIMPEDANCE vs AMBIENT TEMPERATURE

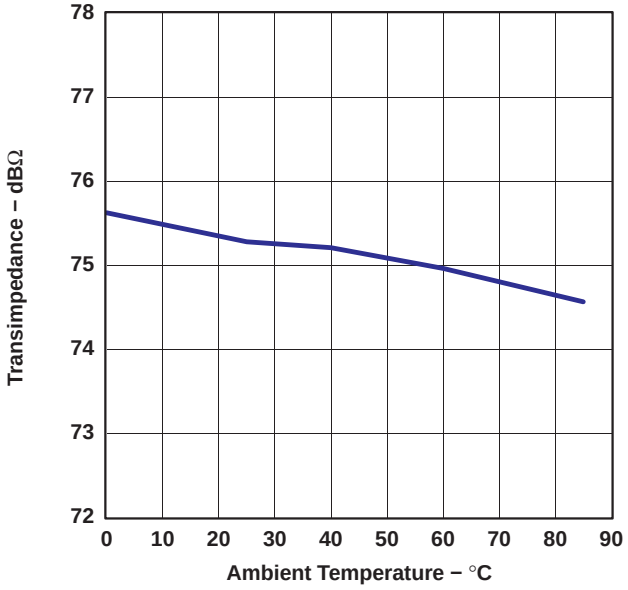


Figure 9

TYPICAL CHARACTERISTICS

SMALL SIGNAL BANDWIDTH
vs
AMBIENT TEMPERATURE

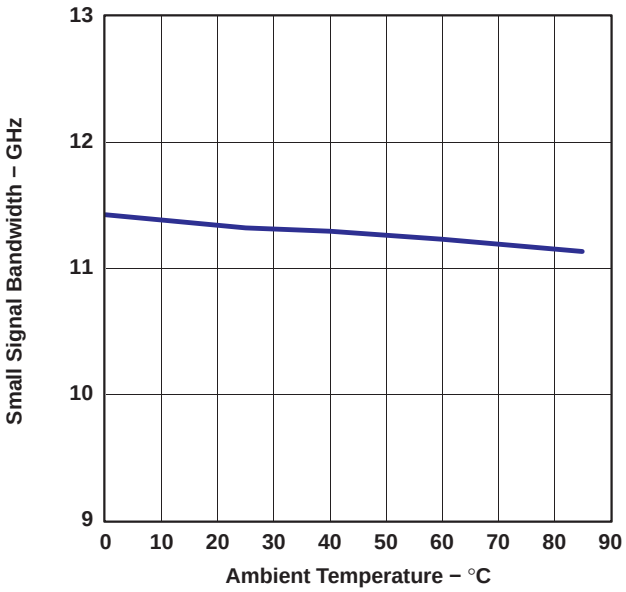


Figure 10

RSSI OUTPUT VOLTAGE
vs
AVERAGE INPUT CURRENT

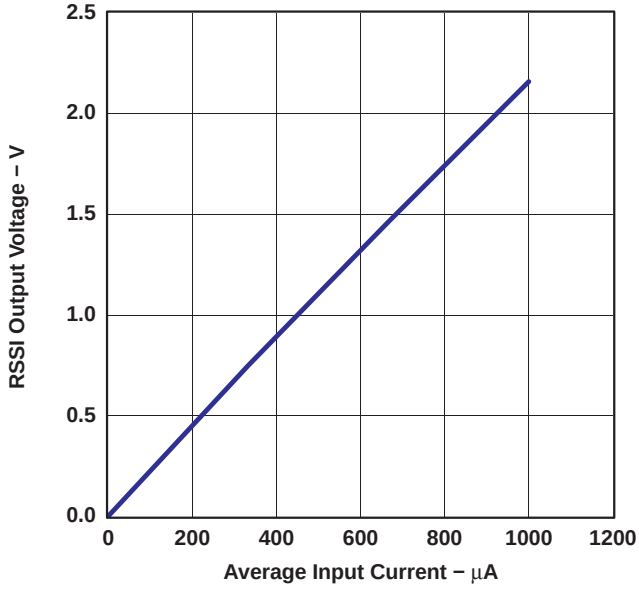


Figure 11

DETERMINISTIC JITTER
vs
INPUT CURRENT

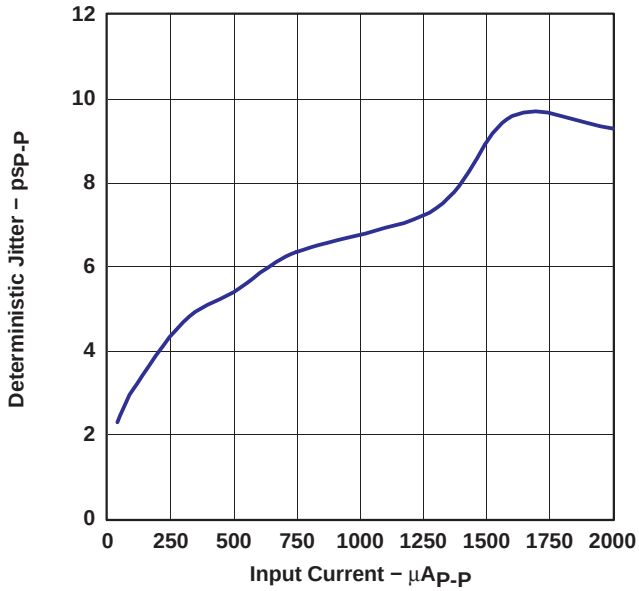


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT EYE DIAGRAM AT 10.7 GBPS AND 20 μA_{P-P} INPUT CURRENT

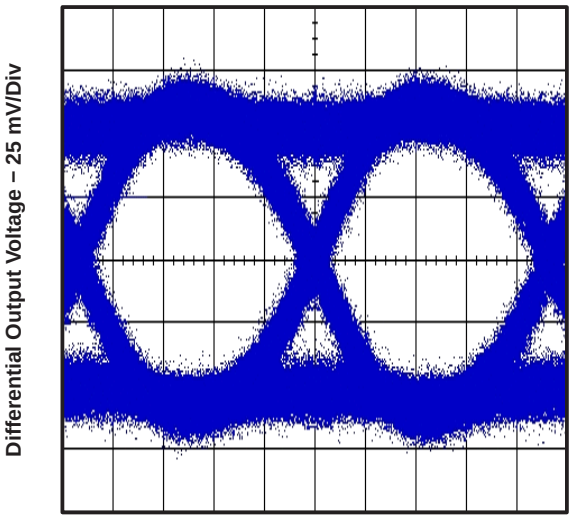


Figure 13

OUTPUT EYE DIAGRAM AT 10.7 GBPS AND 2 mA_{P-P} INPUT CURRENT

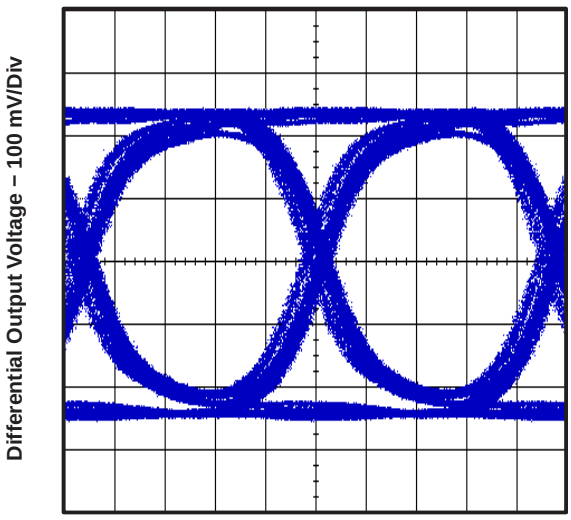


Figure 14

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ONET9901TAY	ACTIVE	XCEPT	Y	0	360	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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