Am29LV160M

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with “Am” and “MBM”. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **25974** Revision **B** Amendment **0** Issue Date **August 11, 2003**

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Am29LV160M

16 Megabit (2 M x 8-Bit/1 M x 16-Bit) MirrorBit™ 3.0 Volt-only Boot Sector Flash Memory

Data Sheet

PRELIMINARY

Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
  - 3 V for read, erase, and program operations
- **Manufactured on 0.23 µm MirrorBit™ process technology**
  - Fully compatible with Am29LV160D device
- **SecSi™ (Secured Silicon) Sector region**
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and thirty-one 64 Kbyte sectors (byte mode)
  - One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **Top or bottom boot block configurations available**
- **Minimum 100,000 erase cycle guarantee per sector**
- **20-year data retention at 125°C**

Performance Characteristics

- **High performance**
  - Access times as fast as 70 ns
  - 0.7 s typical sector erase time
- **Low power consumption (typical values at 5 MHz)**
  - 400 nA standby mode current
  - 15 mA read current
  - 40 mA program/erase current
  - 400 nA Automatic Sleep mode current
- **Package options**
  - 48-ball Fine-pitch BGA
  - 64-ball Fortified BGA
  - 48-pin TSOP

Software Features

- Program Suspend & Resume: read other sectors before programming operation is completed
- Erase Suspend & Resume: read/program other sectors before an erase operation is completed
- Data# polling & toggle bits provide status
- Unlock Bypass Program command reduces overall multiple-word programming time
- CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices

Hardware Features

- Sector Protection: hardware-level method of preventing write operations within a sector
- Temporary Sector Unprotect: V_{ID}-level method of changing code in locked sectors
- Hardware reset input (RESET#) resets device
- Ready/Busy# output (RY/BY#) indicates program or erase cycle completion

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General Description

The Am29LV160M is a 16 Mbit, 3.0 Volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words. The device is offered in a 48-ball Fine-pitch BGA, 64-ball Fortified BGA, and 48-pin TSOP packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. The device requires only a **single 3.0 volt power supply** for both read and write functions, designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply. The device can also be programmed in standard EPROM programmers.

The device offers access times of 70, 85, 90, and 100 ns. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

The **SecSi™ (Secured Silicon) Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

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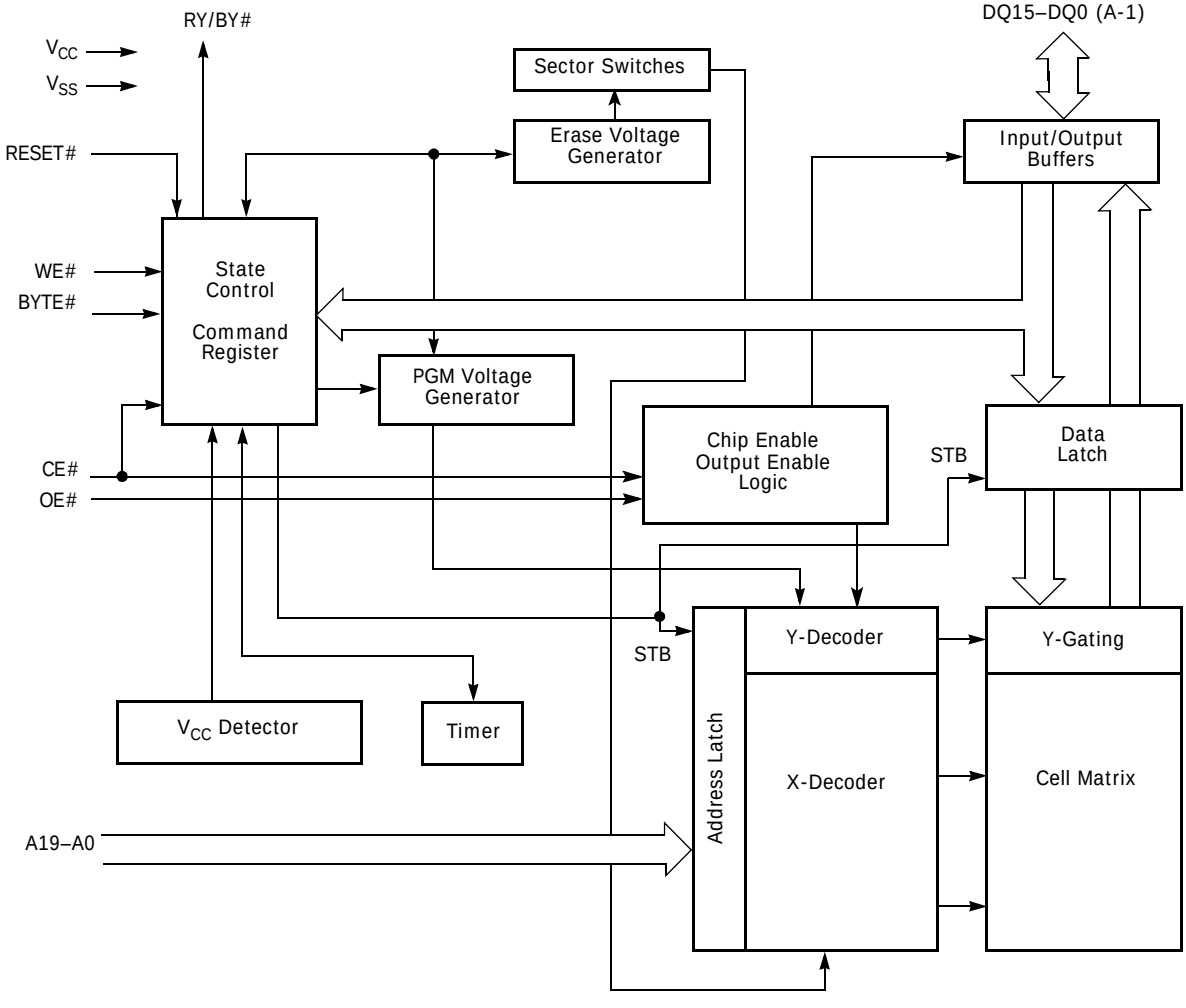
Product Selector Guide

Family Part Number		Am29LV160M			
Speed Option	Regulated Voltage Range: V_{CC} = 3.0–3.6 V	**70R (Note 2)**			
	Full Voltage Range: V_{CC} = 2.7–3.6 V		**85 (Note 2)**	**90**	**100**
Max access time, ns (t_{ACC})		70	85	90	100
Max CE# access time, ns (t_{CE})		70	85	90	100
Max OE# access time, ns (t_{OE})		30	35	35	50

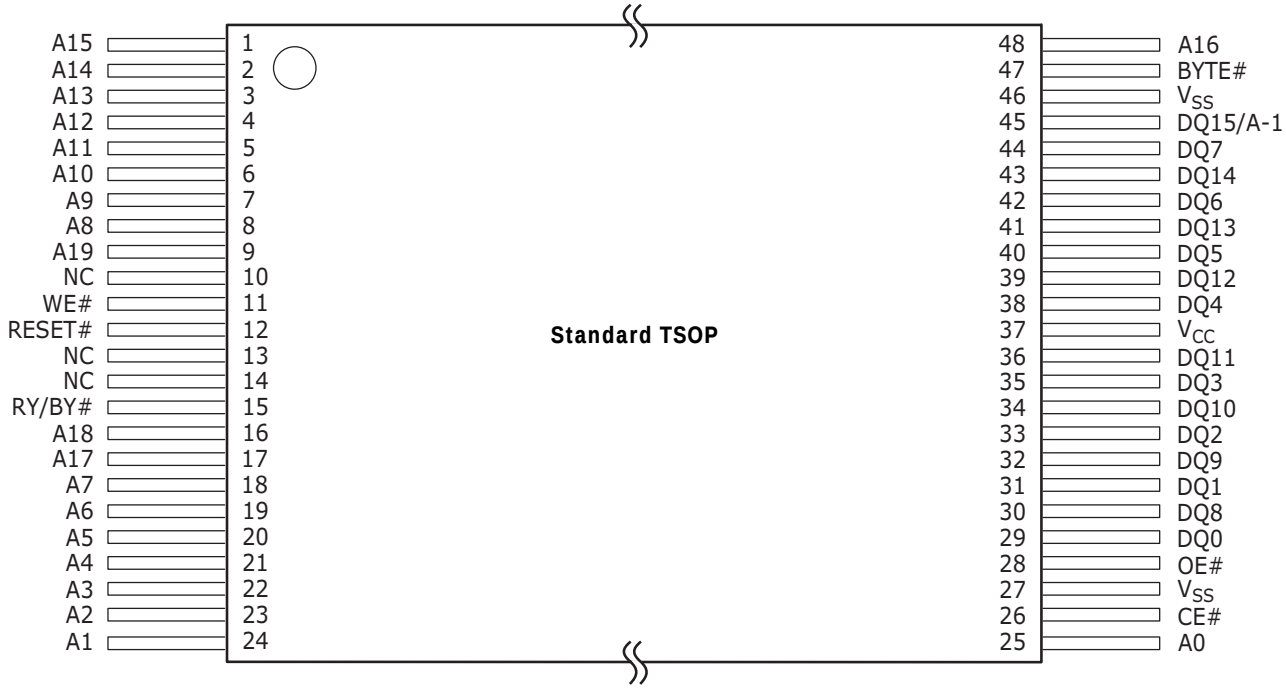
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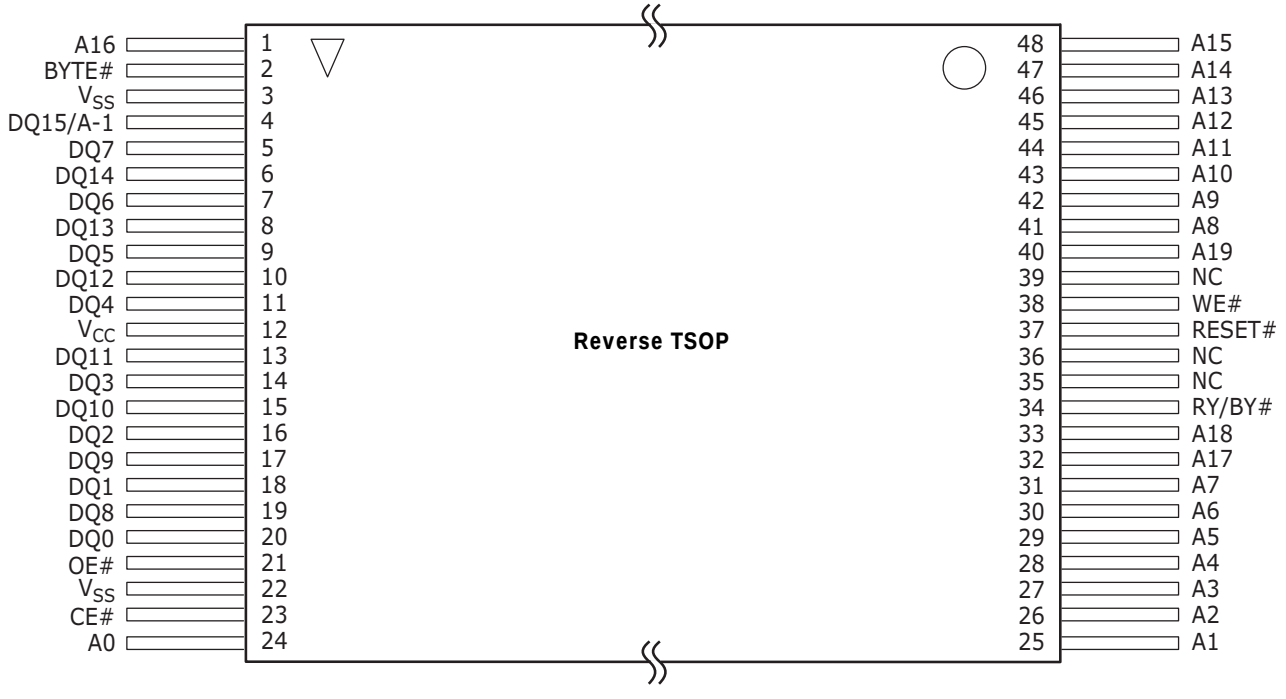
1. *See "AC Characteristics" for full specifications.*
2. *Contact sales office or representative for availability and ordering information.*

Block Diagram



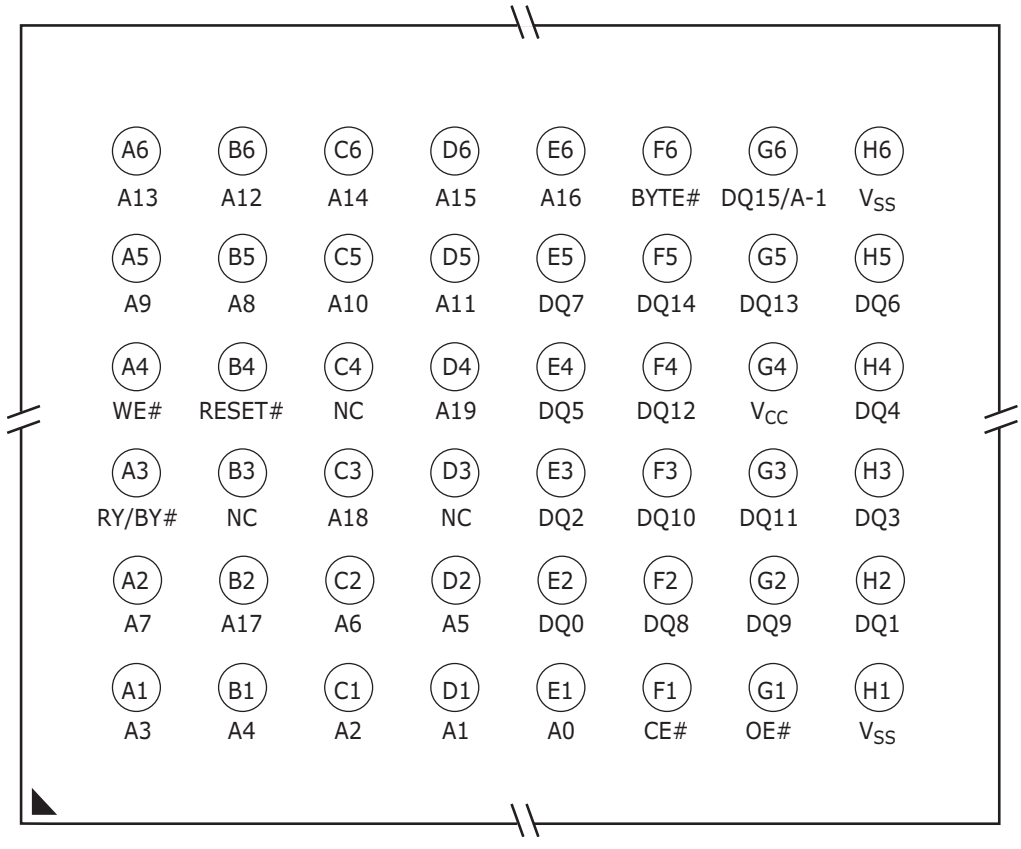
Connection Diagrams





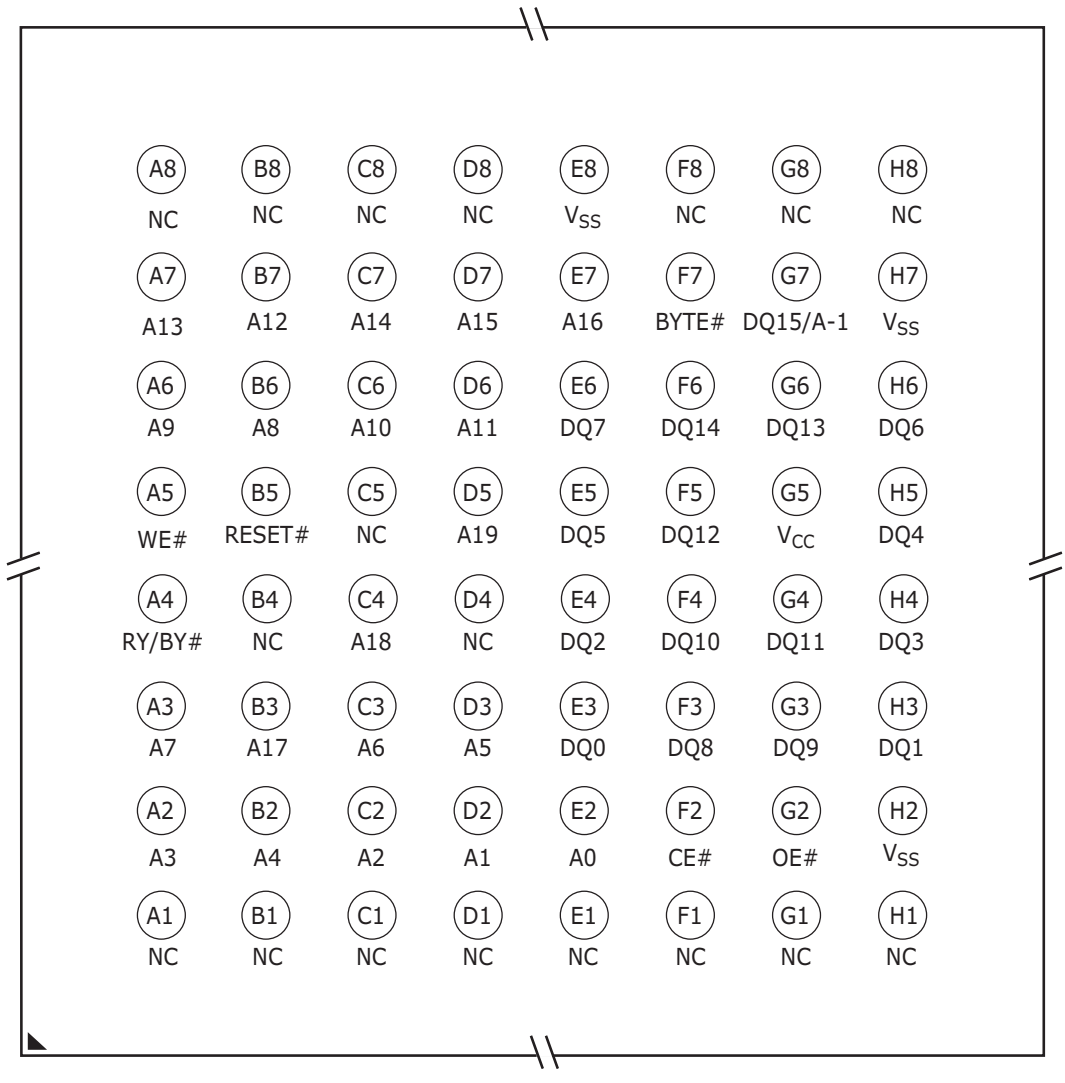
Connection Diagrams

Fine-pitch BGA
Top View, Balls Facing Down



Connection Diagrams

64-Ball Fortified BGA
Top View, Balls Facing Down



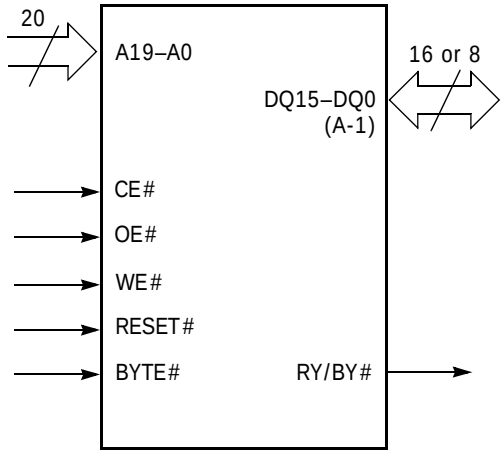
Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP, BGA, SSOP, PDIP, PLCC). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Pin Configuration

A19–A0	=	20 addresses
DQ14–DQ0	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	=	Selects 8-bit or 16-bit mode
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin
RY/BY#	=	Ready/Busy output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

Logic Symbol



Ordering Information

Standard Products

Spansion standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am29LV160M T I00 E I

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)

PACKAGE TYPE
E = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 048)
F = 48-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR048)
WA = 48-ball Fine-Pitch Ball Grid Array (FBGA)
0.80 mm pitch, 6 x 8 mm package (FBA048)
PC = 64-ball Fortified Ball Grid Array (BGA)
1.0 mm pitch, 13 x 11 mm package (LAA064)

SPEED OPTION
See Product Selector Guide and Valid Combinations

BOOT CODE SECTOR ARCHITECTURE
T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION
Am29LV160M
16 Megabit (2M x 8-Bit/1M x 16-Bit) MirrorBit™ Flash Memory
3.0 Volt-only Read, Program, and Erase

Valid Combinations for TSOP Packages		Access Time (ns)	V_{CC} Voltage Range
Am29LV160MT90, Am29LV160MB90	EI, FI	90	2.7–3.6 V
Am29LV160MT100, Am29LV160MB100		100	

Valid Combinations for FBGA Packages			Access Time (ns)	V_{CC} Voltage Range
Order Number		Package Marking		
Am29LV160MT90, Am29LV160MB90	WAI	L160MT90VI, L160MB90VI	90	2.7–3.6 V
	PCI	L160MT90PI, L160MB90PI		
Am29LV160MT100, Am29LV160MB100	WAI	L160MT10VI, L160MB10VI	100	
	PCI	L160MT10PI, L160MB10PI		

Note: *For 70R and 85 speed options shown in product selector guide, contact a sales office or representative for availability and ordering information.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29LV160M Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	Addresses (Note 1)	DQ0–DQ7	DQ8–DQ15	
							BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = H, A1 = H, A0 = L	D_{IN}	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Addresses are A19:A0 in word mode (BYTE# = V_{IH}), A19:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Protection/Unprotection" section.*

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to Figure 13 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to "Word/Byte Configuration" for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The "Word/Byte Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 2 and 3 indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Command Definitions" section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to "AC Characteristics" for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

In the DC Characteristics table, I_{CC3} and I_{CC4} represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin to V_{IL} for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3$ V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 14 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Sector Address Tables (Am29LV160MT)

Sector	A19	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
										Byte Mode (x8)	Word Mode (x16)
SA0	0	0	0	0	0	X	X	X	64/32	000000–00FFFF	000000–007FFF
SA1	0	0	0	0	1	X	X	X	64/32	010000–01FFFF	008000–00FFFF
SA2	0	0	0	1	0	X	X	X	64/32	020000–02FFFF	010000–017FFF
SA3	0	0	0	1	1	X	X	X	64/32	030000–03FFFF	018000–01FFFF
SA4	0	0	1	0	0	X	X	X	64/32	040000–04FFFF	020000–027FFF
SA5	0	0	1	0	1	X	X	X	64/32	050000–05FFFF	028000–02FFFF
SA6	0	0	1	1	0	X	X	X	64/32	060000–06FFFF	030000–037FFF
SA7	0	0	1	1	1	X	X	X	64/32	070000–07FFFF	038000–03FFFF
SA8	0	1	0	0	0	X	X	X	64/32	080000–08FFFF	040000–047FFF
SA9	0	1	0	0	1	X	X	X	64/32	090000–09FFFF	048000–04FFFF
SA10	0	1	0	1	0	X	X	X	64/32	0A0000–0AFFFF	050000–057FFF
SA11	0	1	0	1	1	X	X	X	64/32	0B0000–0BFFFF	058000–05FFFF
SA12	0	1	1	0	0	X	X	X	64/32	0C0000–0CFFFF	060000–067FFF
SA13	0	1	1	0	1	X	X	X	64/32	0D0000–0DFFFF	068000–06FFFF
SA14	0	1	1	1	0	X	X	X	64/32	0E0000–0EFFFF	070000–077FFF
SA15	0	1	1	1	1	X	X	X	64/32	0F0000–0FFFFF	078000–07FFFF
SA16	1	0	0	0	0	X	X	X	64/32	100000–10FFFF	080000–087FFF
SA17	1	0	0	0	1	X	X	X	64/32	110000–11FFFF	088000–08FFFF
SA18	1	0	0	1	0	X	X	X	64/32	120000–12FFFF	090000–097FFF
SA19	1	0	0	1	1	X	X	X	64/32	130000–13FFFF	098000–09FFFF
SA20	1	0	1	0	0	X	X	X	64/32	140000–14FFFF	0A0000–0A7FFF
SA21	1	0	1	0	1	X	X	X	64/32	150000–15FFFF	0A8000–AFFFF
SA22	1	0	1	1	0	X	X	X	64/32	160000–16FFFF	0B0000–0B7FFF
SA23	1	0	1	1	1	X	X	X	64/32	170000–17FFFF	0B8000–0BFFFF
SA24	1	1	0	0	0	X	X	X	64/32	180000–18FFFF	0C0000–0C7FFF
SA25	1	1	0	0	1	X	X	X	64/32	190000–19FFFF	0C8000–0CFFFF
SA26	1	1	0	1	0	X	X	X	64/32	1A0000–1AFFFF	0D0000–0D7FFF
SA27	1	1	0	1	1	X	X	X	64/32	1B0000–1BFFFF	0D8000–0DFFFF
SA28	1	1	1	0	0	X	X	X	64/32	1C0000–1CFFFF	0E0000–0E7FFF
SA29	1	1	1	0	1	X	X	X	64/32	1D0000–1DFFFF	0E8000–0EFFFF
SA30	1	1	1	1	0	X	X	X	64/32	1E0000–1EFFFF	0F0000–0F7FFF
SA31	1	1	1	1	1	0	X	X	32/16	1F0000–1F7FFF	0F8000–0FBFFF
SA32	1	1	1	1	1	1	0	0	8/4	1F8000–1F9FFF	0FC000–0FCFFF
SA33	1	1	1	1	1	1	0	1	8/4	1FA000–1FBFFF	0FD000–0FDFFF
SA34	1	1	1	1	1	1	1	X	16/8	1FC000–1FFFFF	0FE000–0FFFFF

Note: *Address range is A19:A-1 in byte mode and A19:A0 in word mode. See "Word/Byte Configuration" section.*

Table 3. Sector Address Tables (Am29LV160MB)

Sector	A19	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
										Byte Mode (x8)	Word Mode (x16)
SA0	0	0	0	0	0	0	0	X	16/8	000000–003FFF	000000–001FFF
SA1	0	0	0	0	0	0	1	0	8/4	004000–005FFF	002000–002FFF
SA2	0	0	0	0	0	0	1	1	8/4	006000–007FFF	003000–003FFF
SA3	0	0	0	0	0	1	X	X	32/16	008000–00FFFF	004000–007FFF
SA4	0	0	0	0	1	X	X	X	64/32	010000–01FFFF	008000–00FFFF
SA5	0	0	0	1	0	X	X	X	64/32	020000–02FFFF	010000–017FFF
SA6	0	0	0	1	1	X	X	X	64/32	030000–03FFFF	018000–01FFFF
SA7	0	0	1	0	0	X	X	X	64/32	040000–04FFFF	020000–027FFF
SA8	0	0	1	0	1	X	X	X	64/32	050000–05FFFF	028000–02FFFF
SA9	0	0	1	1	0	X	X	X	64/32	060000–06FFFF	030000–037FFF
SA10	0	0	1	1	1	X	X	X	64/32	070000–07FFFF	038000–03FFFF
SA11	0	1	0	0	0	X	X	X	64/32	080000–08FFFF	040000–047FFF
SA12	0	1	0	0	1	X	X	X	64/32	090000–09FFFF	048000–04FFFF
SA13	0	1	0	1	0	X	X	X	64/32	0A0000–0AFFFF	050000–057FFF
SA14	0	1	0	1	1	X	X	X	64/32	0B0000–0BFFFF	058000–05FFFF
SA15	0	1	1	0	0	X	X	X	64/32	0C0000–0CFFFF	060000–067FFF
SA16	0	1	1	0	1	X	X	X	64/32	0D0000–0DFFFF	068000–06FFFF
SA17	0	1	1	1	0	X	X	X	64/32	0E0000–0EFFFF	070000–077FFF
SA18	0	1	1	1	1	X	X	X	64/32	0F0000–0FFFFF	078000–07FFFF
SA19	1	0	0	0	0	X	X	X	64/32	100000–10FFFF	080000–087FFF
SA20	1	0	0	0	1	X	X	X	64/32	110000–11FFFF	088000–08FFFF
SA21	1	0	0	1	0	X	X	X	64/32	120000–12FFFF	090000–097FFF
SA22	1	0	0	1	1	X	X	X	64/32	130000–13FFFF	098000–09FFFF
SA23	1	0	1	0	0	X	X	X	64/32	140000–14FFFF	0A0000–0A7FFF
SA24	1	0	1	0	1	X	X	X	64/32	150000–15FFFF	0A8000–0AFFFF
SA25	1	0	1	1	0	X	X	X	64/32	160000–16FFFF	0B0000–0B7FFF
SA26	1	0	1	1	1	X	X	X	64/32	170000–17FFFF	0B8000–0BFFFF
SA27	1	1	0	0	0	X	X	X	64/32	180000–18FFFF	0C0000–0C7FFF
SA28	1	1	0	0	1	X	X	X	64/32	190000–19FFFF	0C8000–0CFFFF
SA29	1	1	0	1	0	X	X	X	64/32	1A0000–1AFFFF	0D0000–0D7FFF
SA30	1	1	0	1	1	X	X	X	64/32	1B0000–1BFFFF	0D8000–0DFFFF
SA31	1	1	1	0	0	X	X	X	64/32	1C0000–1CFFFF	0E0000–0E7FFF
SA32	1	1	1	0	1	X	X	X	64/32	1D0000–1DFFFF	0E8000–0EFFFF
SA33	1	1	1	1	0	X	X	X	64/32	1E0000–1EFFFF	0F0000–0F7FFF
SA34	1	1	1	1	1	X	X	X	64/32	1F0000–1FFFFF	0F8000–0FFFFF

Note: *Address range is A19:A-1 in byte mode and A19:A0 in word mode. See the "Word/Byte Configuration" section.*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 4. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Tables 2 and 3). Table 4 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Tables 10–11. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 4. Autoselect Codes (High Voltage Method)

Description	Mode	CE#	OE#	WE#	A19 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID		L	L	H	X	X	V_{ID}	X	L	X	L	L	X	01h (AMD)
Device ID: Am29LV160M (Top Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	C4h
	Byte	L	L	H									X	C4h
Device ID: Am29LV160M (Bottom Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	49h
	Byte	L	L	H									X	49h
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	H	L	X	01h (protected)
													X	00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Note: *The autoselect codes may also be accessed in-system via command sequences. See Tables 10–11.*

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The device is normally shipped with all sectors unprotected. However, the ExpressFlash™ Service offers the option of programming and protecting sectors at the factory prior to shipping the device. Contact a sales office or representative for details.

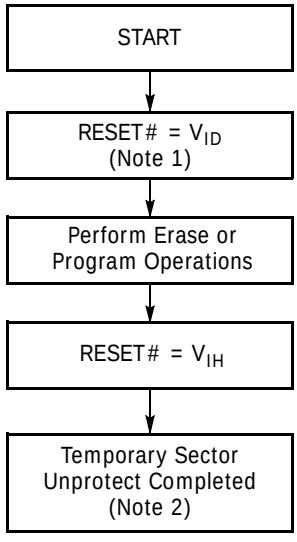
It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

Sector protection and unprotection requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows

the algorithms and Figure 23 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure shows the algorithm, and Figure 22 shows the timing diagrams, for this feature.



Notes:

1. *All protected sectors unprotected.*
2. *All previously protected sectors are protected once again.*

Figure I. Temporary Sector Unprotect Operation

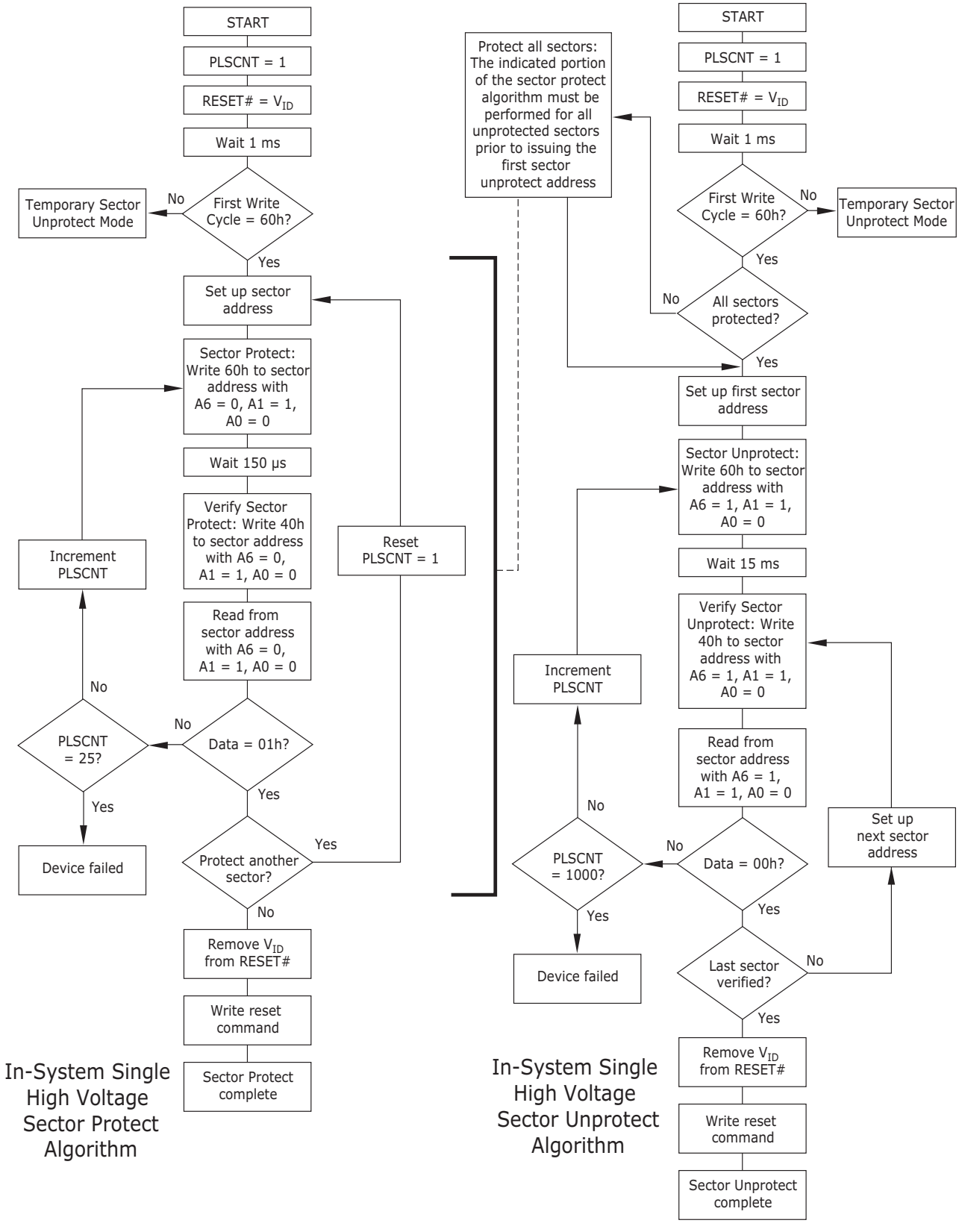


Figure 2. In-System Single High Voltage Sector Protect/Unprotect Algorithms

SecSi (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 256 bytes in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The device is offered with the SecSi Sector either customer lockable (standard shipping option) or factory locked (contact a sales office or representative for ordering information). The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the SecSi Sector Indicator Bit permanently set to a "0." The factory-locked version is always protected when shipped from the factory, and has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "1." Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

The SecSi sector address space in this device is allocated as follows:

Table 5. SecSi Sector Addressing

SecSi Sector Address Range		Customer Lockable	ESN Factory Locked	ExpressFlash Factory Locked
x16	x8			
000000h–000007h	000000h–00000Fh	Determined by customer	ESN	ESN or determined by customer
000008h–00007Fh	000010h–0000FFh		Unavailable	Determined by customer

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

Customer Lockable: SecSi Sector NOT Programmed or Protected At the Factory

Unless otherwise specified, the device is shipped such that the customer may program and protect the 256-byte SecSi sector.

The system may program the SecSi Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See Command Definitions.

Programming and protecting the SecSi Sector must be used with caution since, once protected, there is no procedure available for unprotecting the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, ex-

cept that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.

- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 3.

Once the SecSi Sector is programmed, locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing within the remainder of the array.

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In devices with an ESN, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. An ESN Factory Locked device has a 16-byte random ESN at addresses 000000h–000007h. Please contact your local sales office or representative for details on ordering ESN Factory Locked devices.

Customers may opt to have their code programmed by the manufacturer through the ExpressFlash service (Express Flash Factory Locked). The devices are then shipped from the factory with the SecSi Sector permanently locked. Contact an sales office or representative for details on using the ExpressFlash service.

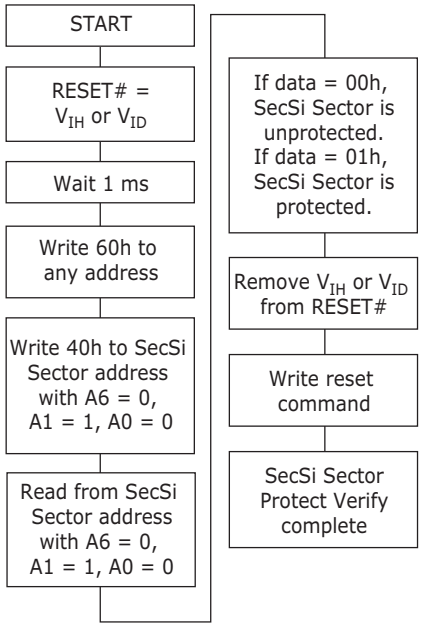


Figure 3. SecSi Sector Protect Verify

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 6–9. In word mode, the upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 6–9. The system must write the reset command to return the device to the read/reset mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available online at http://www.amd.com/flash/cfi. Alternatively, contact an sales office or representative for copies of these documents.

Table 6. CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 7. System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0007h	Typical timeout per single byte/word write 2^N µs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0001h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 8. Device Geometry Definition

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0015h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0004h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0000h 0000h 0040h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	0001h 0000h 0020h 0000h	Erase Block Region 2 Information
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0080h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	001Eh 0000h 0000h 0001h	Erase Block Region 4 Information

Table 9. Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0033h	Minor version number, ASCII
45h	8Ah	0008h	Address Sensitive Unlock (Bit 1–0) 0b = Required, 1b = Not Required Process Technology (Bits 7–2) 0010b = 0.23 µm MirrorBit
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400 mode, 04 = 29LV800A mode
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, 01 = Supported
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Tables 10–11 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Tables 10–11 define the valid register command sequences. *Note that writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. A reset command is then required to set the device for the next operation.*

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operations table provides the read parameters, and Figure 13 shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Tables 10–11 show the address and data requirements. This method is an alternative to that shown in Table 4, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address XX02h in word mode (or XX04h in byte mode) returns XX01h if that sector is protected, or 00h if it is unprotected. Refer to Tables 2 and 3 for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Word/Byte Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Tables 10–11 show the address and data requirements for the byte program command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.*

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

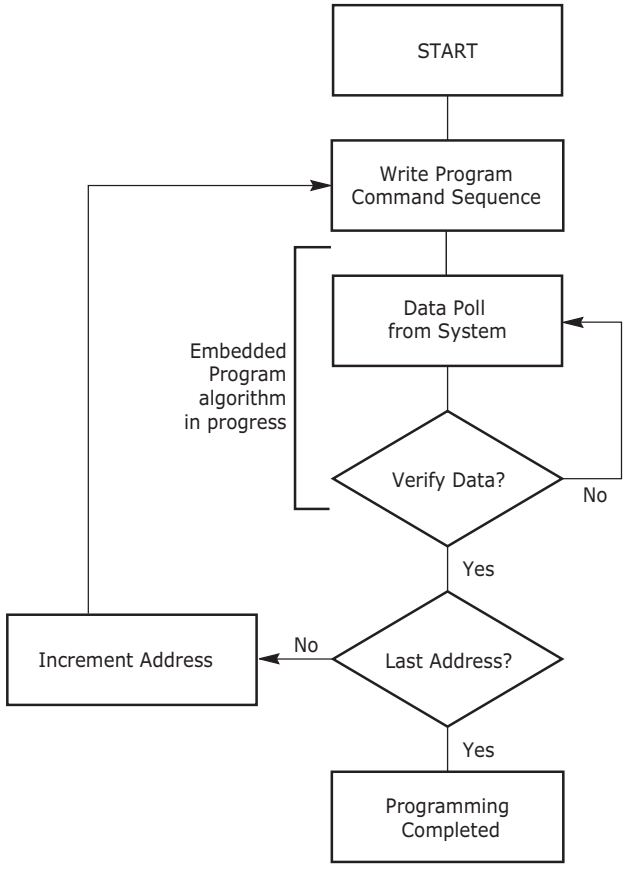
Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a "0" back to a "1".** Attempting to do so may halt the operation and set DQ5 to "1," or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Tables 10–11 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data.

Figure 4 illustrates the algorithm for the program operation. See the Erase/Program Operations table in "AC Characteristics" for parameters, and to Figure 17 for timing diagrams.



Notes: *See Tables 10 and 11 for program command sequence.*

Figure 4. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Tables 10–11 show the address and data requirements for the chip erase command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when an erase operation is in progress.*

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See "Autoselect Command Sequence" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 5 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to Figure 18 for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Tables 10–11 show the address and data requirements for the sector erase command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when an erase operation is in progress.*

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to "Write Operation Status" for information on these status bits.)

Figure 5 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to Figure 18 for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase Suspend command.

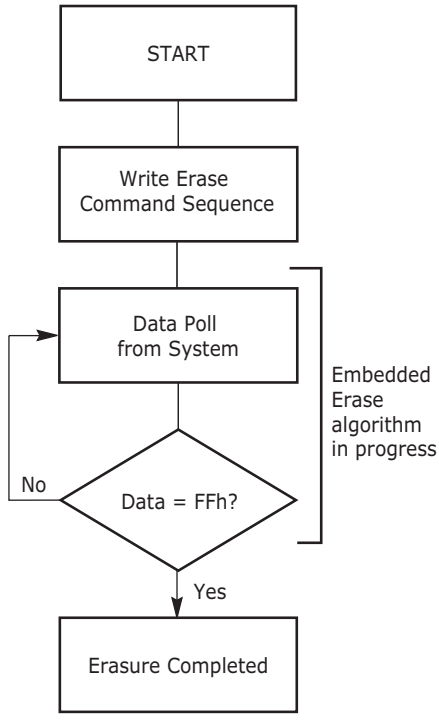
When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Erase Resume command (address bits are “don’t care”) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.



Notes:

1. *See Tables 10–11 for erase command sequence.*
2. *See “DQ3: Sector Erase Timer” for more information.*

Figure 5. Erase Operation

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15 µs maximum (5 µs typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the SecSi Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device re-

verts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

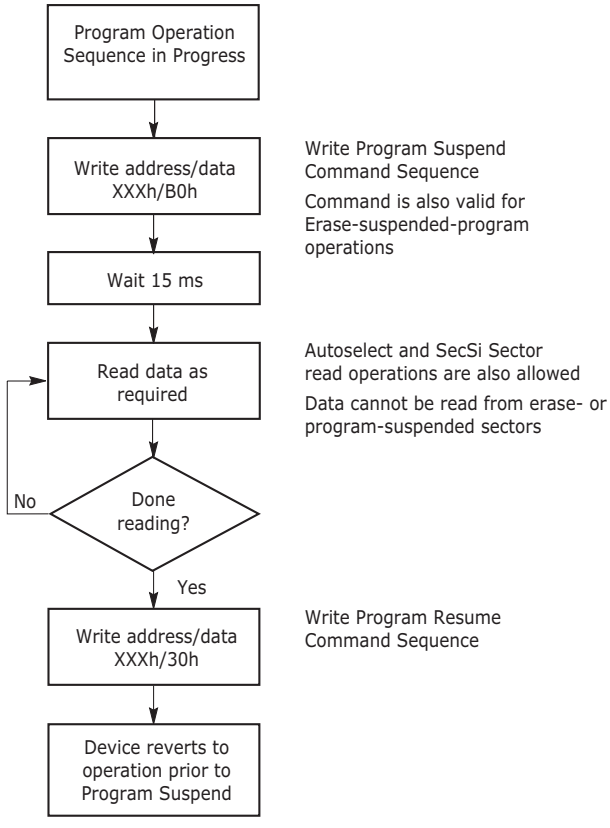


Figure 6. Program Suspend/Program Resume

Command Definitions Tables

Table 10. Command Definitions (x16 Mode, BYTE# = V_{IH})

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
	Device ID, Top Boot (Note 8)	6	555	AA	2AA	55	555	90	X01	22C4				
	Device ID, Bottom Boot (Note 8)	6	555	AA	2AA	55	555	90	X01	2249				
	SecSi™ Sector Factory Protect	4	555	AA	2AA	55	555	90	X03	(Note 9)				
	Sector Group Protect Verify (Note 9)	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
Enter SecSi Sector Region		3	555	AA	2AA	55	555	88						
Exit SecSi Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 10)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (Note 12)		1	BA	B0										
Program/Erase Resume (Note 13)		1	BA	30										
CFI Query (Note 14)		1	55	98										

Legend:

X = Don't care

RA = Read Address of memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A19–A15 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells indicate read cycles. All others are write cycles.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AA as shown in table, address bits above A11 and data bits above DQ7 are don't care.*
5. *No unlock or command cycles required when device is in read mode.*
6. *Reset command is required to return to read mode (or to erase-suspend-read mode if previously in Erase Suspend) when device is in autoselect mode, or if DQ5 goes high while device is providing status information.*
7. *Fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See Autoselect Command Sequence section for more information.*
8. *Device ID must be read in three cycles.*
9. *Data is 00h for an unprotected sector group and 01h for a protected sector group.*
10. *Unlock Bypass command is required prior to Unlock Bypass Program command.*
11. *Unlock Bypass Reset command is required to return to read mode when device is in unlock bypass mode.*
12. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Erase Suspend mode. Erase Suspend command is valid only during a sector erase operation.*
13. *Erase Resume command is valid only during Erase Suspend mode.*
14. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

Table II. Command Definitions (x8 Mode, BYTE# = V_{IL})

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01				
	Device ID, Top Boot (Note 8)	6	AAA	AA	555	55	AAA	90	X02	C4				
	Device ID, Bottom Boot (Note 8)	6	AAA	AA	555	55	AAA	90	X02	49				
	SecSi™ Sector Factory Protect	4	AAA	AA	555	55	AAA	90	X06	(Note 9)				
	Sector Group Protect Verify (Note 9)	4	AAA	AA	555	55	AAA	90	(SA)X04	00/01				
Enter SecSi Sector Region		3	AAA	AA	555	55	AAA	88						
Exit SecSi Sector Region		4	AAA	AA	555	55	AAA	90	XXX	00				
Program		4	AAA	AA	555	55	AAA	A0	PA	PD				
Unlock Bypass		3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program (Note 10)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)		2	XXX	90	XXX	00								
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Program/Erase Suspend (Note 12)		1	BA	B0										
Program/Erase Resume (Note 13)		1	BA	30										
CFI Query (Note 14)		1	AA	98										

Legend:

X = Don't care

RA = Read Address of memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A19–A15 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells indicate read cycles. All others are write cycles.*
4. *During unlock and command cycles, when lower address bits are 555 or AAA as shown in table, address bits above A11 are don't care.*
5. *No unlock or command cycles required when device is in read mode.*
6. *Reset command is required to return to read mode (or to erase-suspend-read mode if previously in Erase Suspend) when device is in autoselect mode, or if DQ5 goes high while device is providing status information.*
7. *Fourth cycle of autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See Autoselect Command Sequence section or more information.*
8. *Device ID must be read in three cycles.*
9. *Data is 00h for an unprotected sector group and 01h for a protected sector group.*
10. *Unlock Bypass command is required prior to Unlock Bypass Program command.*
11. *Unlock Bypass Reset command is required to return to read mode when device is in unlock bypass mode.*
12. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Erase Suspend mode. Erase Suspend command is valid only during a sector erase operation.*
13. *Erase Resume command is valid only during Erase Suspend mode.*
14. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

Write Operation Status

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 12 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

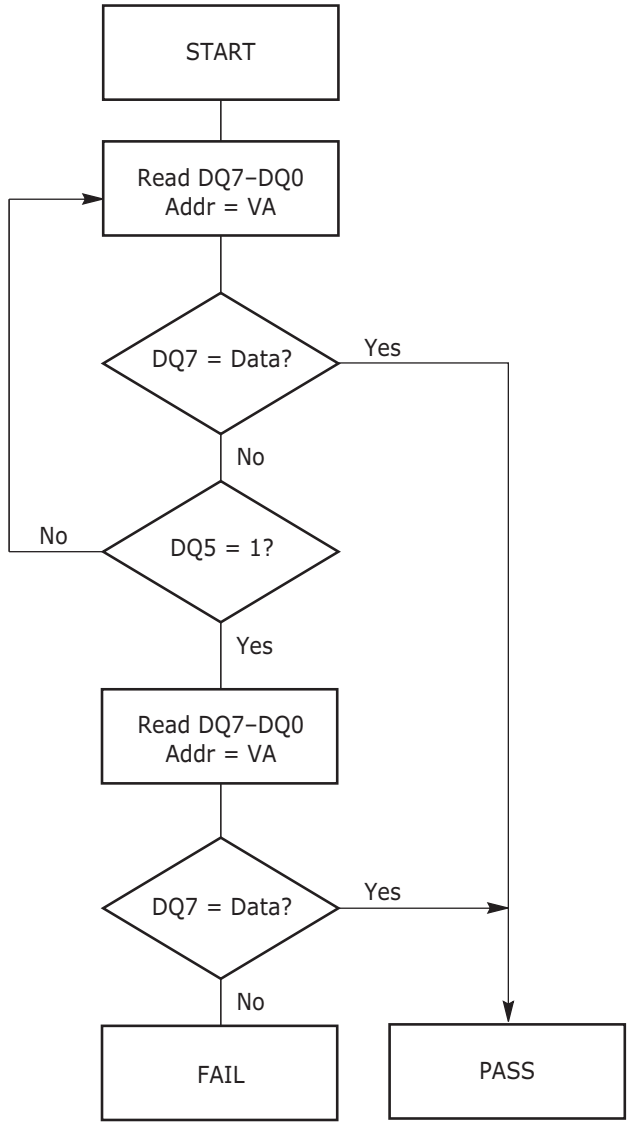
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to “1”; prior to this, the device outputs the “complement,” or “0.” The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. Figure 19, Data# Polling Timings (During Embedded Algorithms), in the “AC Characteristics” section illustrates this.

Table 12 shows the outputs for Data# Polling on DQ7. Figure 7 shows the Data# Polling algorithm.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 7. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 12 shows the outputs for RY/BY#. Figures 13, 14, 17 and 18 show RY/BY# for read, reset, program, and erase operations, respectively.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on "DQ7: Data# Polling").

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 12 shows the outputs for Toggle Bit I on DQ6. Figure 8 shows the toggle bit algorithm in flowchart form, and the section "Reading Toggle Bits DQ6/DQ2" explains the algorithm. Figure 20 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 21 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on "DQ2: Toggle Bit II".

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 12 to compare outputs for DQ2 and DQ6.

Figure 8 shows the toggle bit algorithm in flowchart form, and the section "Reading Toggle Bits DQ6/DQ2" explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 20 shows the toggle bit timing diagram. Figure 21 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 8 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 8).

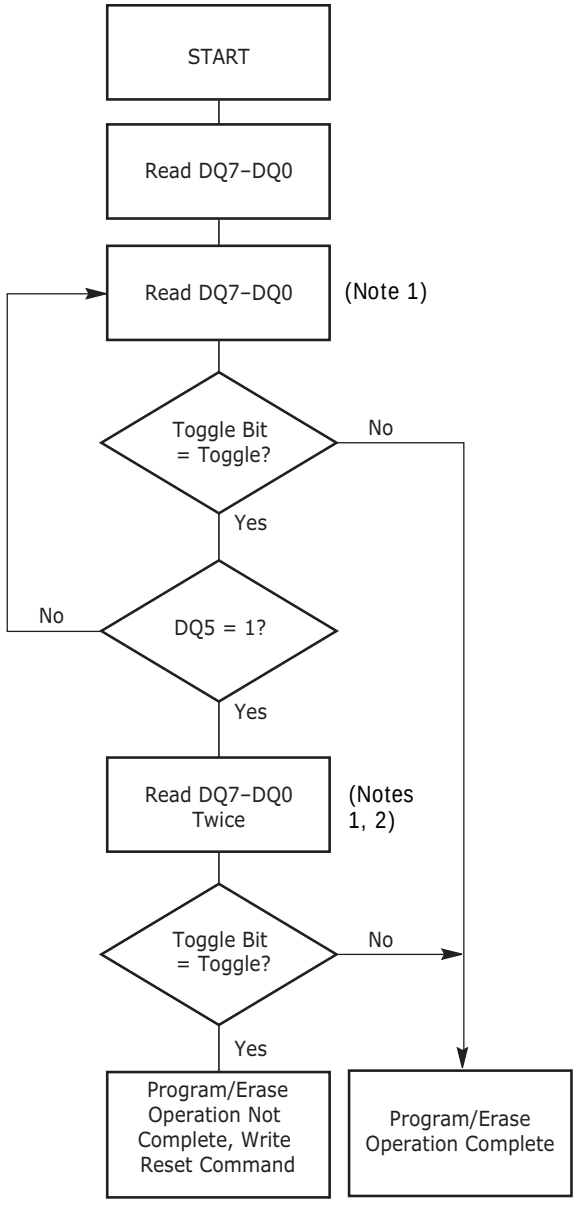


Figure 8. Toggle Bit Algorithm

Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to "1". See text.*

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." **Only an erase operation can**

change a "0" back to a "1." Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a "1."

Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from "0" to "1." The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 µs. See also the "Sector Erase Command Sequence" section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is "1", the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 12 shows the outputs for DQ3.

Table 12. Write Operation Status

Operation			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)					1
		Non-Program Suspended Sector	Data					1
Erase Suspend Mode	Reading within Erase Suspended Sector		1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector		Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

Absolute Maximum Ratings

Storage Temperature, Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

A9, OE#, and RESET# (Note 2) . . . . . –0.5 V to +12.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC}+0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 10.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

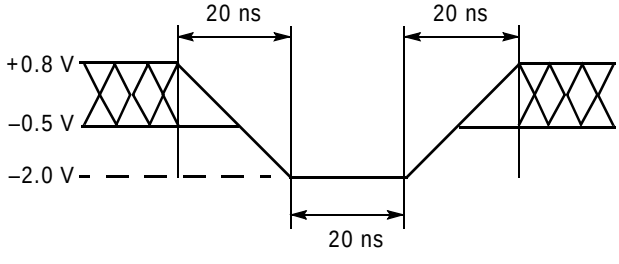


Figure 9. Maximum Negative Overshoot Waveform

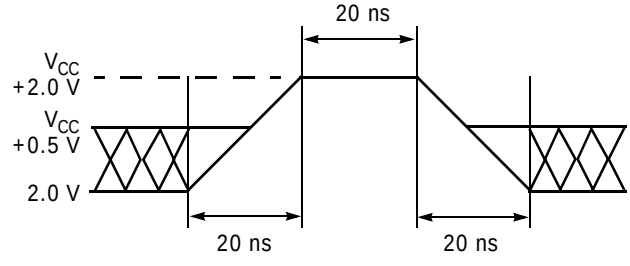


Figure 10. Maximum Positive Overshoot Waveform

Operating Ranges

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range . . . . . 3.0 V to 3.6 V

V_{CC} for full voltage range . . . . . 2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics

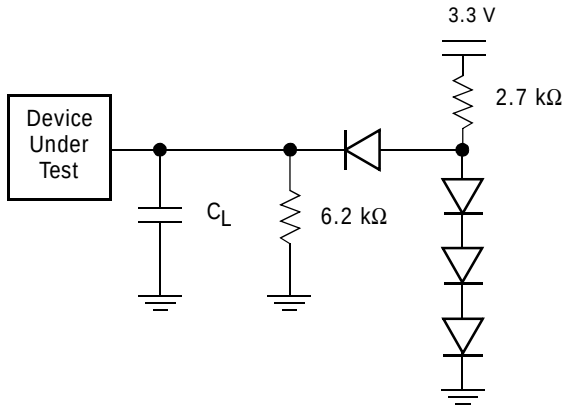
CMOS Compatible

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = $V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	V_{CC} = $V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LR}	Reset Leakage Current	V_{CC} = $V_{CC\ max}$; RESET# = 12.5 V				35	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = $V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		15	30	mA
			1 MHz		2	10	
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		15	30	
			1 MHz		2	10	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3, 5)	CE# = V_{IL}, OE# = V_{IH}			40	60	mA
I_{CC3}	V_{CC} Standby Current (Notes 2, 4)	CE#, RESET# = V_{CC}±0.3 V			0.4	5	µA
I_{CC4}	V_{CC} Standby Current During Reset (Notes 2, 4)	RESET# = V_{SS} ± 0.3 V			0.8	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4, 6)	V_{IH} = V_{CC} ± 0.3 V; V_{IL} = V_{SS} ± 0.3 V			0.4	5	µA
V_{IL1}	Input Low Voltage 1(6, 7)			–0.5		0.8	V
V_{IH1}	Input High Voltage 1 (6, 7)			1.9		V_{CC} + 0.5	V
V_{IL2}	Input Low Voltage 2 (6, 8)			–0.5		0.3 x V_{IO}	V
V_{IH2}	Input High Voltage 2 (6, 8)			1.9		V_{IO} + 0.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.3 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, V_{CC} = $V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.0 mA, V_{CC} = $V_{CC\ min}$		0.85 x V_{CC}			V
V_{OH2}		I_{OH} = -100 µA, V_{CC} = $V_{CC\ min}$		V_{CC}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 4)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}. Typical V_{CC} is 3.0 V.*
2. *Maximum I_{CC} specifications are tested with V_{CC} = V_{CC}max.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *At extended temperature range (>+85°C), typical current is 5 µA and maximum current is 10 µA.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.*
6. *Not 100% tested.*
7. *V_{CC} voltage requirements.*
8. *V_{IO} voltage requirements.*

Test Conditions



Note: *Diodes are IN3064 or equivalent*

Figure I1. Test Setup

Table I3. Test Specifications

Test Condition	70R, 85	90, 100	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

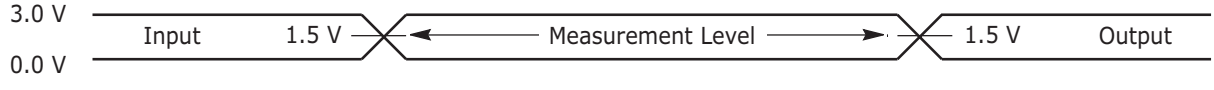


Figure I2. Input Waveforms and Measurement Levels

AC Characteristics

Read Operations

Parameter		Description		Test Setup		Speed Options				Unit
JEDEC	Std					70R	85	90	100	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	85	90	100	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	70	85	90	100	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	85	90	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	35	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	25	30	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	25	30	30	30	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0				ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11 and Table 13 for test specifications.*

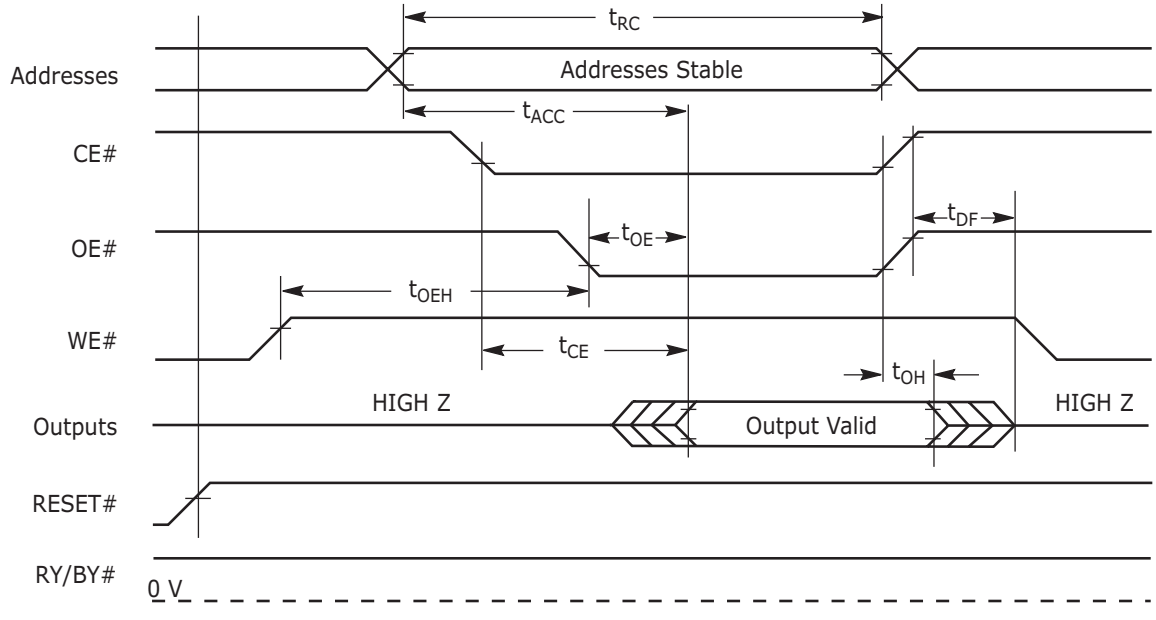


Figure 13. Read Operations Timings

AC Characteristics

Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode		Min	20	µs
	t_{RB}	RY/BY# Recovery Time		Min	0	ns

Note: *Not 100% tested.*

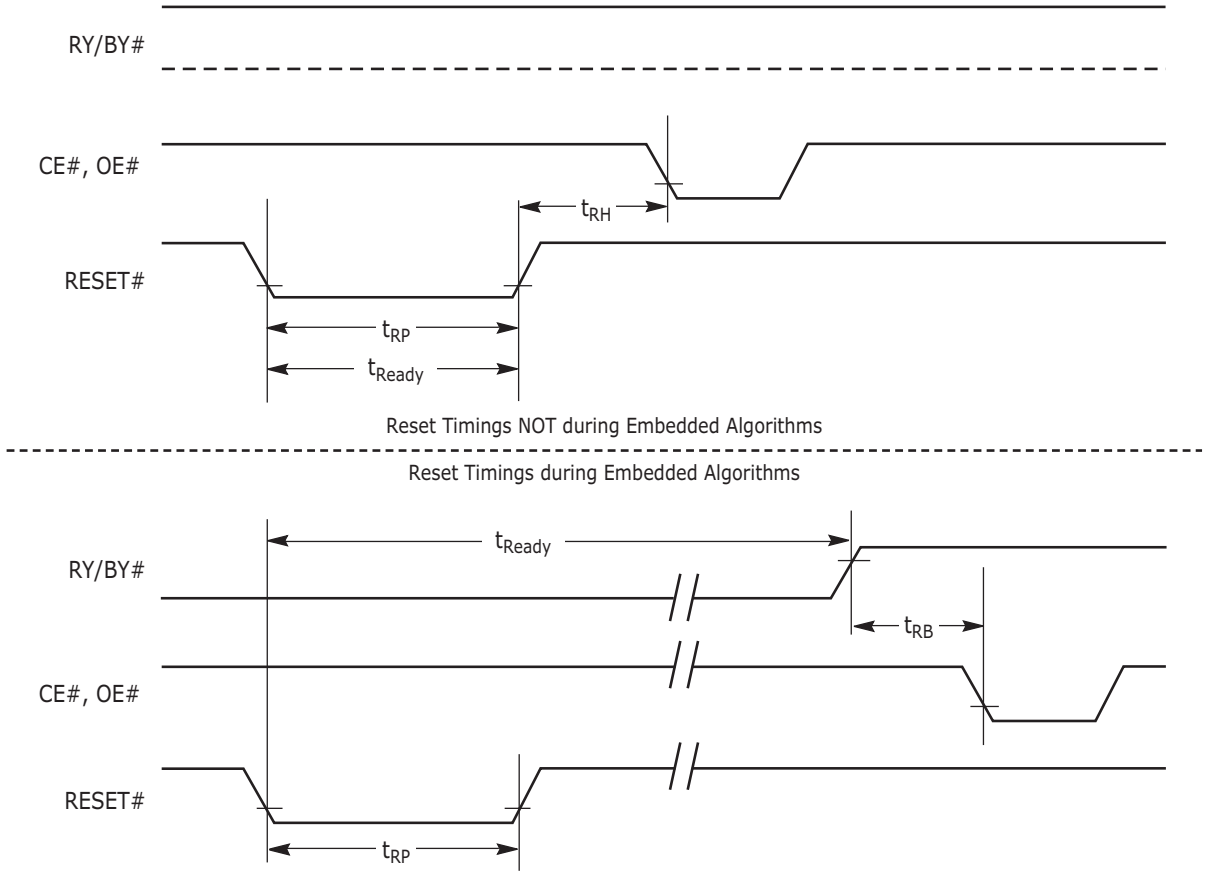


Figure 14. RESET# Timings

AC Characteristics

Word/Byte Configuration (BYTE#)

Parameter		Description		Speed Options				Unit
JEDEC	Std			70R	85	90	100	
	t_{ELFL}/t_{ELFH}	CE# to BYTE# Switching Low or High	Max	5				ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	25	30	30	30	ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	70	85	90	100	ns

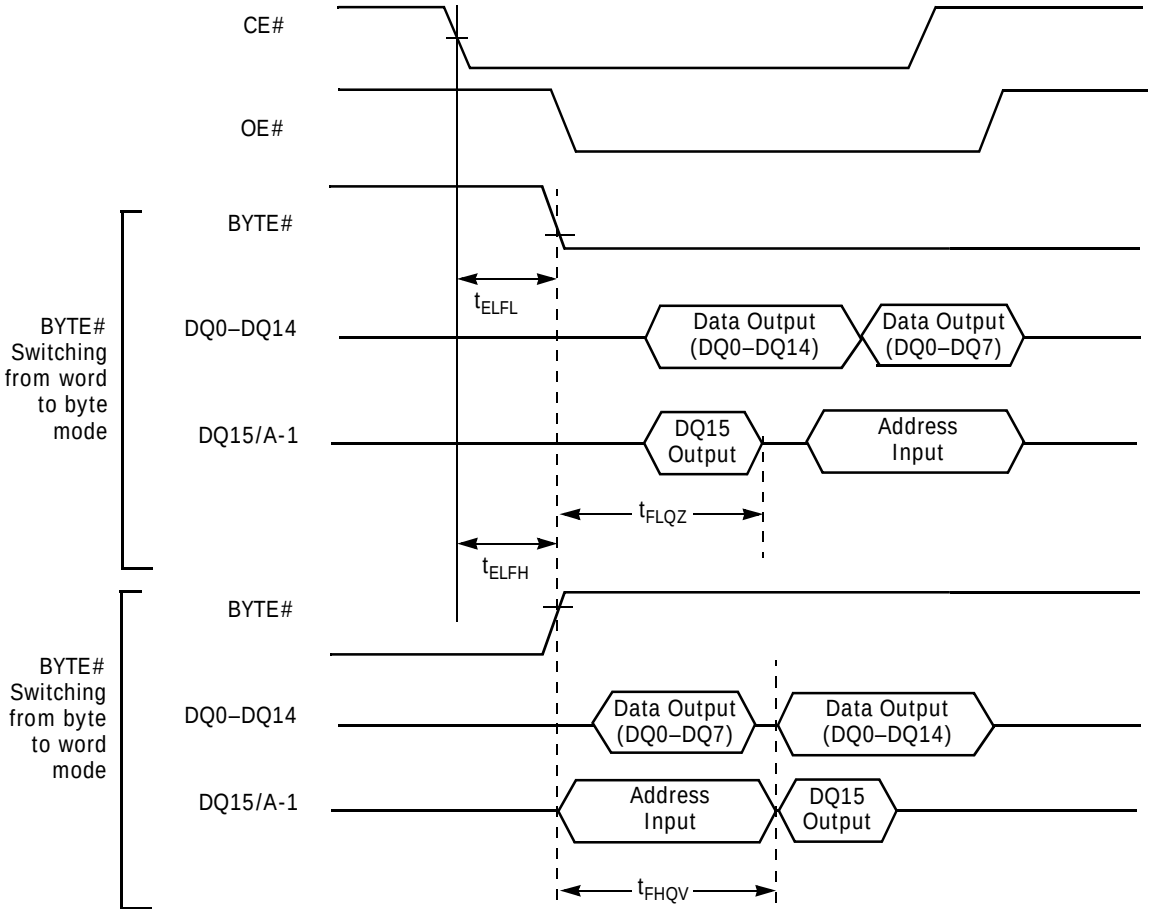


Figure 15. BYTE# Timings for Read Operations

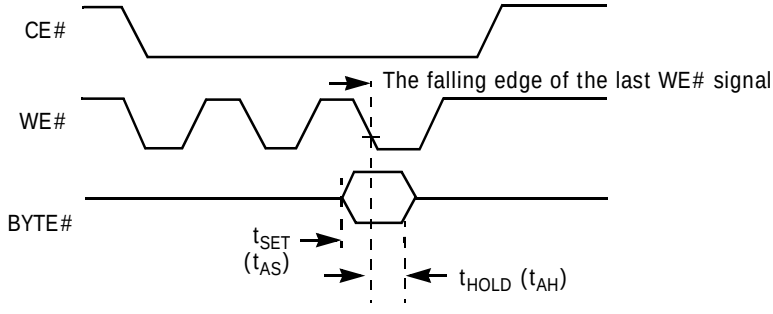


Figure 16. BYTE# Timings for Write Operations

Note: *Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.*

AC Characteristics

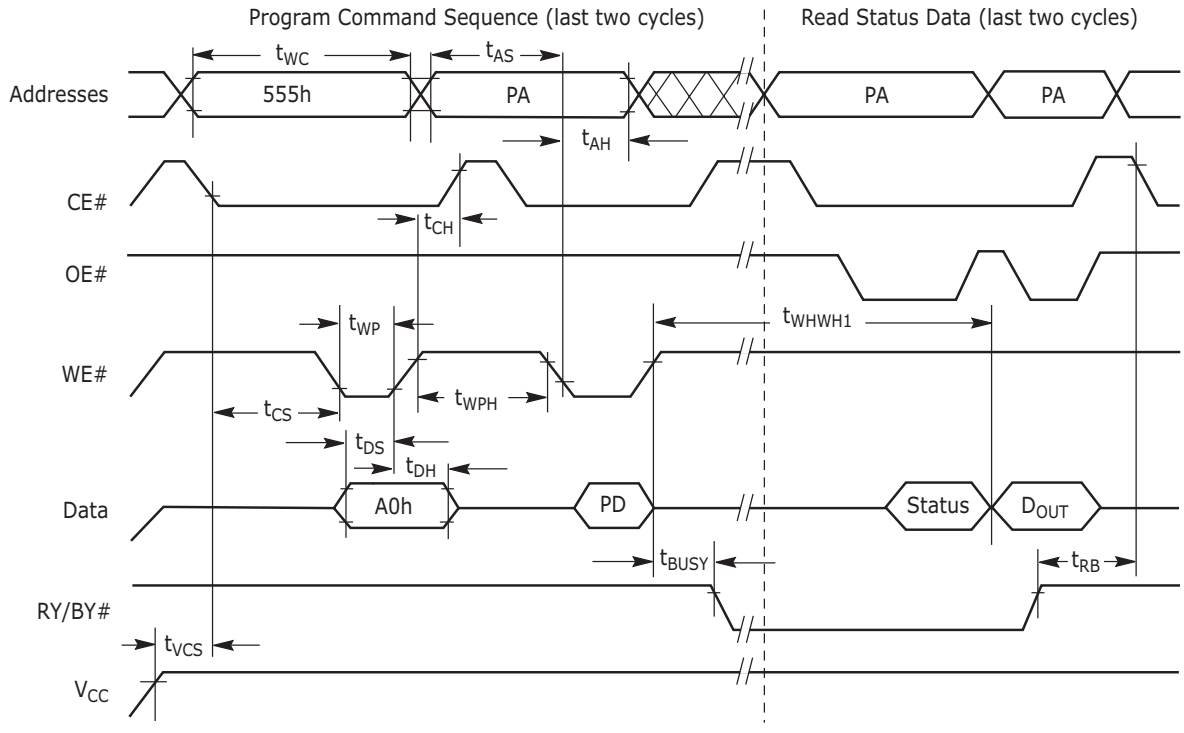
Erase/Program Operations

Parameter		Description			Speed Options				Unit
JEDEC	Std				70R	85	90	100	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	85	90	100	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	45	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OES}	Output Enable Setup Time		Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	12				µs
			Word	Typ	12				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7				sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50				µs
	t_{RB}	Recovery Time from RY/BY#		Min	0				ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Min	90				ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*

AC Characteristics

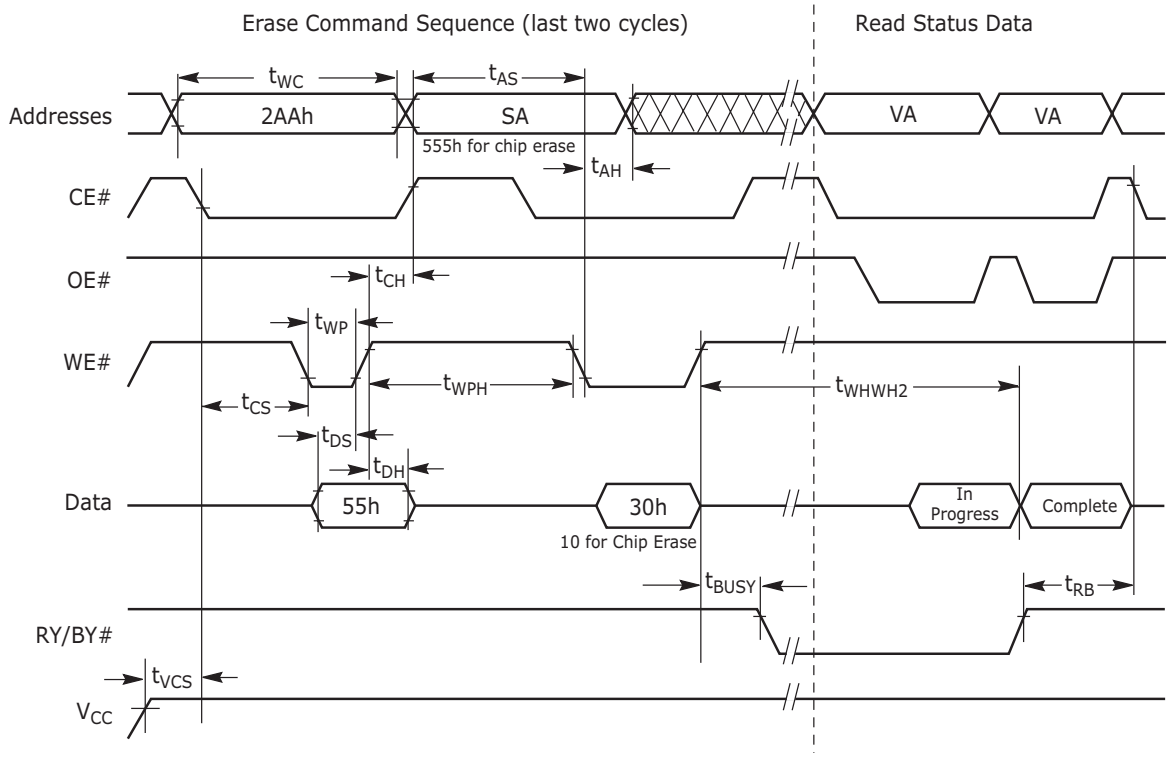


Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 17. Program Operation Timings

AC Characteristics

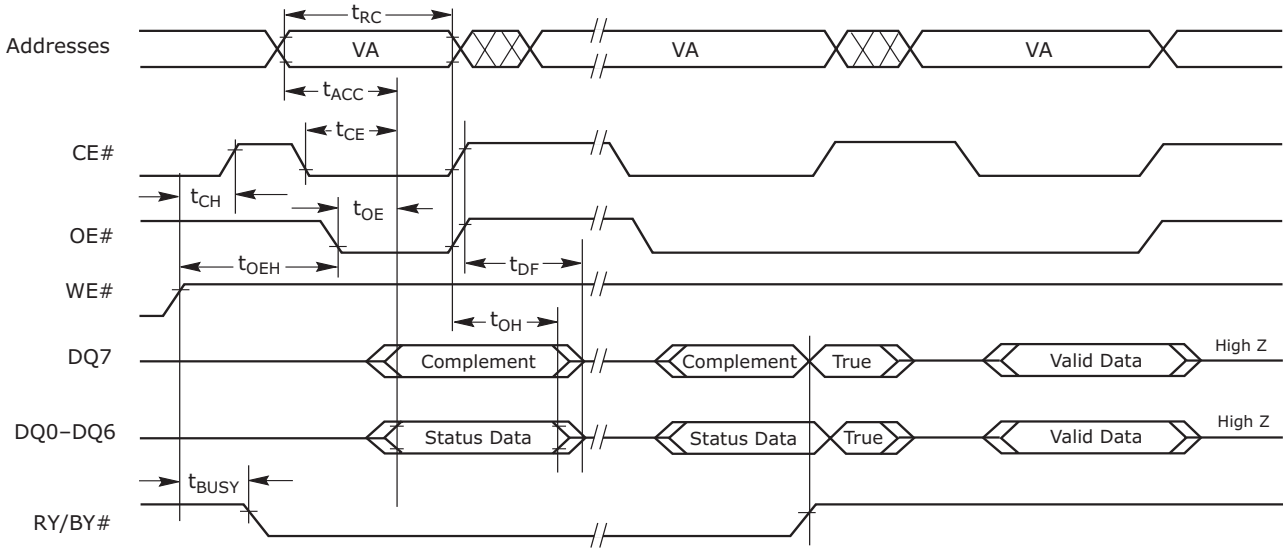


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").*
2. *Illustration shows device in word mode.*

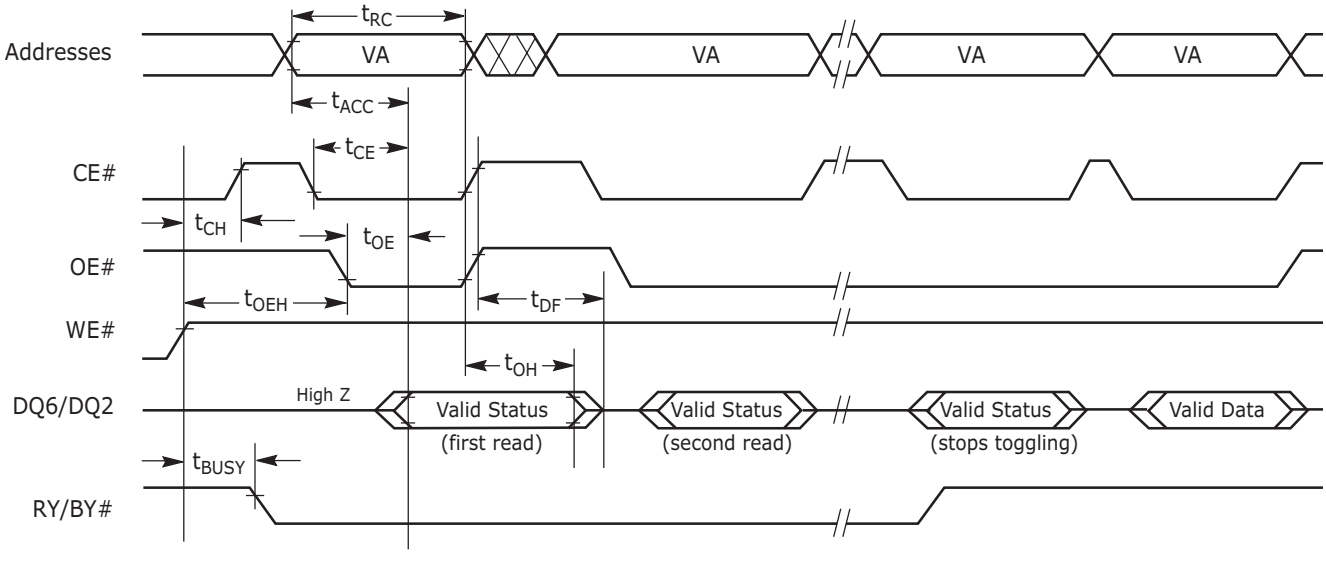
Figure 18. Chip/Sector Erase Operation Timings

AC Characteristics



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

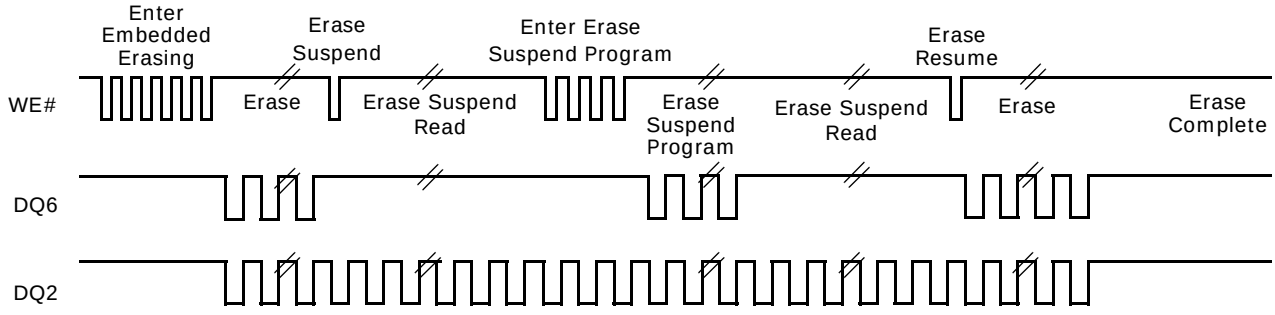
Figure 19. Data# Polling Timings (During Embedded Algorithms)



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 20. Toggle Bit Timings (During Embedded Algorithms)

AC Characteristics



Note: *The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

Figure 21. DQ2 vs. DQ6 for Erase and Erase Suspend Operations

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

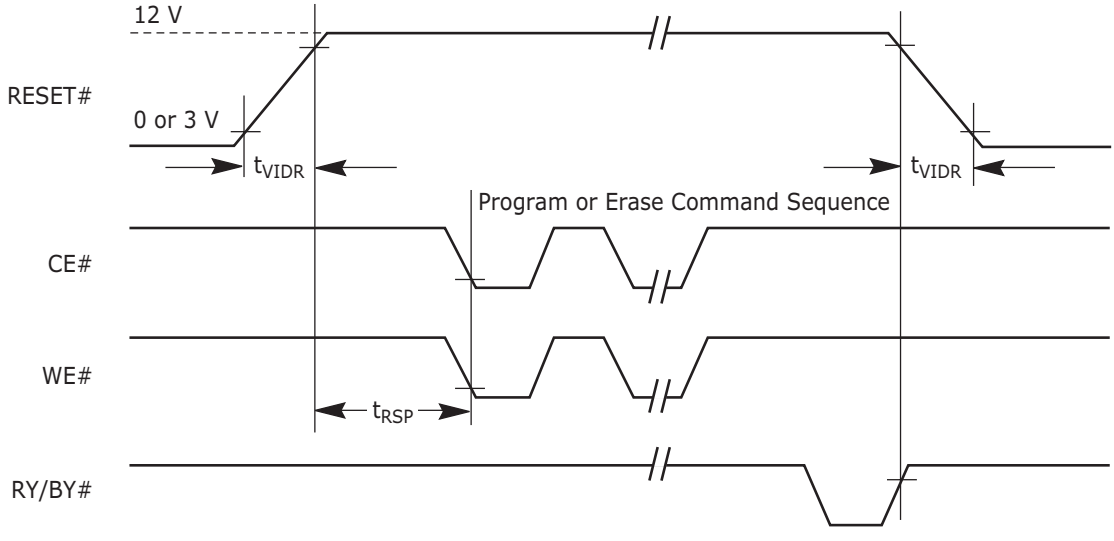
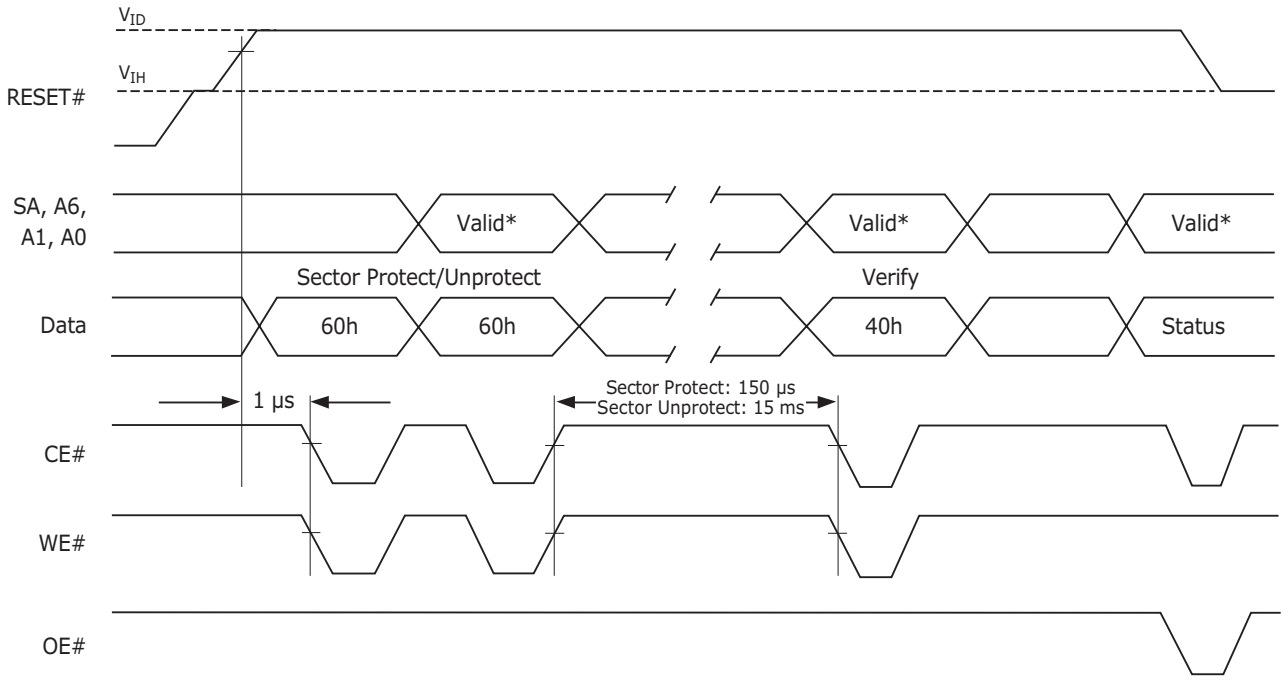


Figure 22. Temporary Sector Unprotect/Timing Diagram

AC Characteristics



Note: *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 23. Sector Protect/Unprotect Timing Diagram

AC Characteristics

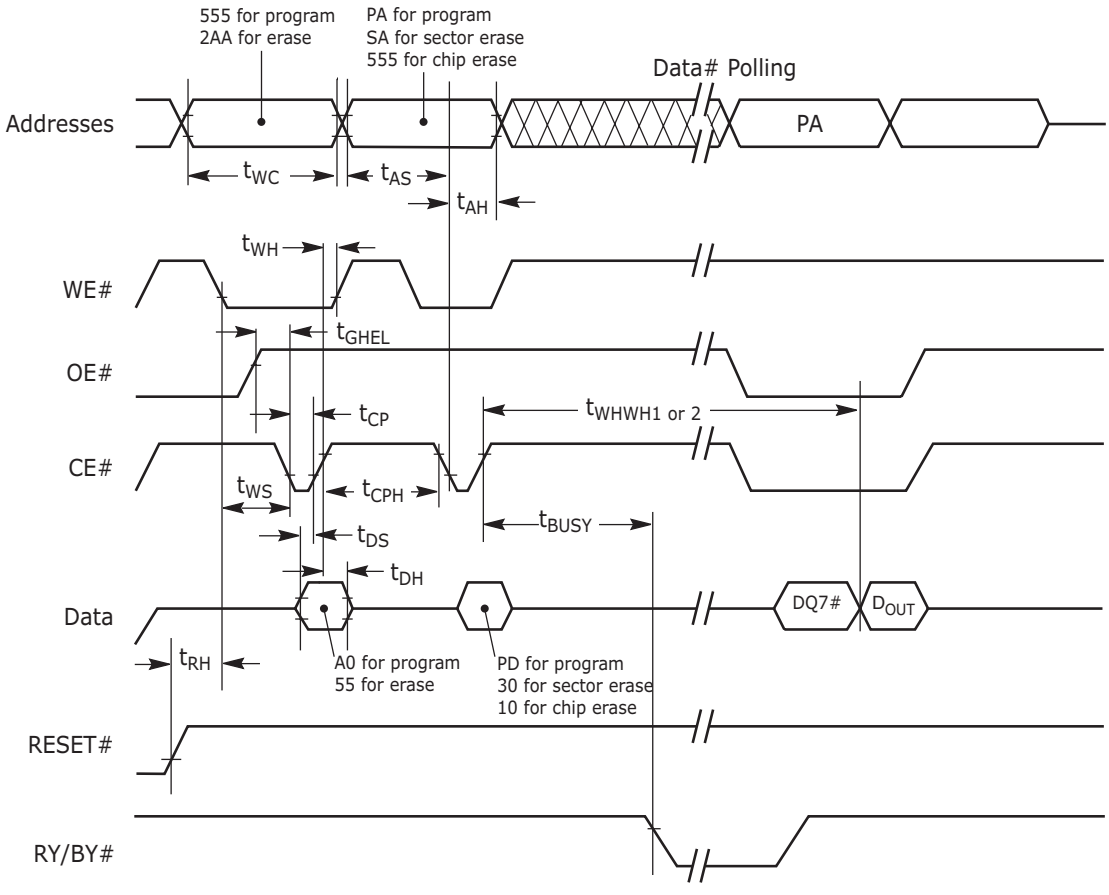
Alternate CE# Controlled Erase/Program Operations

Parameter		Description			Speed Options				Unit
JEDEC	Std				70R	85	90	100	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	85	90	100	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	45	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OES}	Output Enable Setup Time		Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35	35	35	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	12				µs
			Word	Typ	12				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7				sec

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*

AC Characteristics



Notes:

1. *PA = program address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.*
2. *Figure indicates the last two bus cycles of the command sequence.*
3. *Word mode address used as an example.*

Figure 24. Alternate CE# Controlled Write Operation Timings

Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.7	15	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		25		s	
Byte Programming Time		12	210	µs	Excludes system level overhead (Note 5)
Word Programming Time		12	210	µs	
Chip Programming Time (Note 3)	Byte Mode	25.2	66	s	
	Word Mode	12.6	33	s	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Tables 2–3 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

Latchup Characteristics

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.*

TSOP Pin and BGA Package Capacitance

Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	7.5	pF
			Fine-pitch BGA	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	8.5	12	pF
			Fine-pitch BGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	7.5	9	pF
			Fine-pitch BGA	3.9	4.7	pF

Notes:

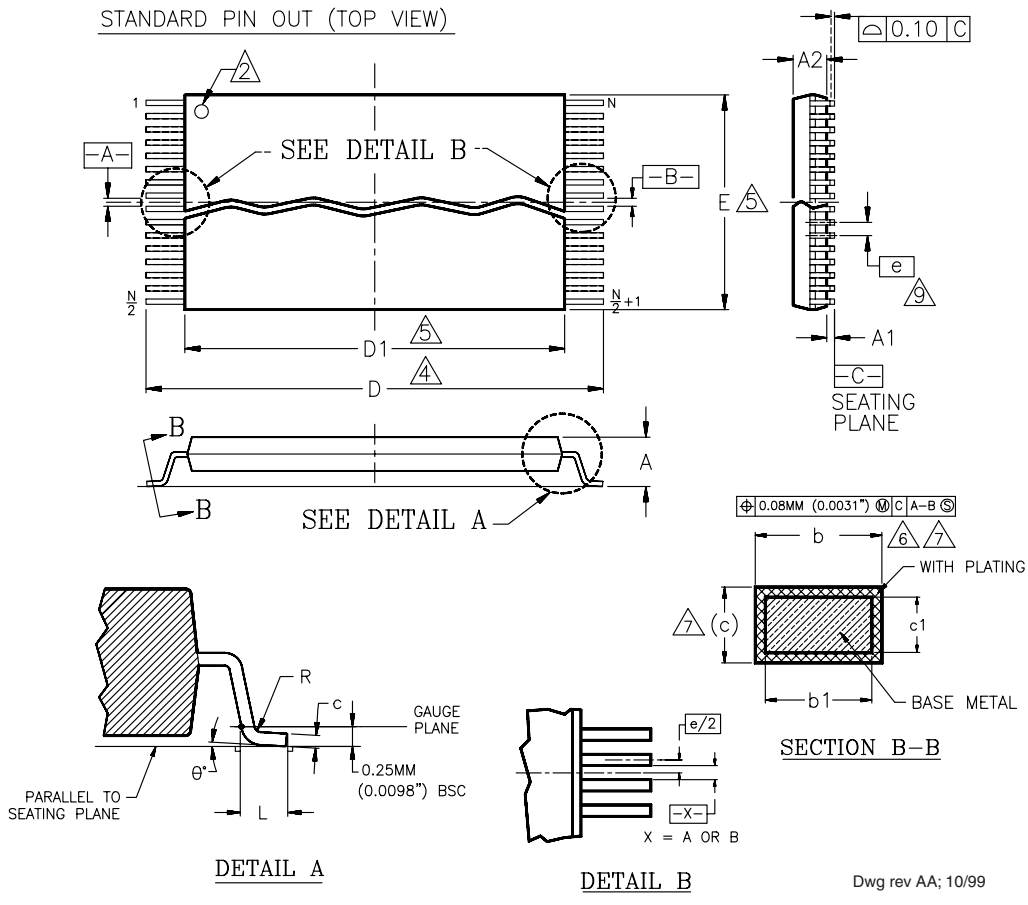
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

Data Retention

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

Physical Dimensions

TS 048—48-Pin Standard TSOP



Package	TS 48		
Jedec	MO-142 (B) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	48		

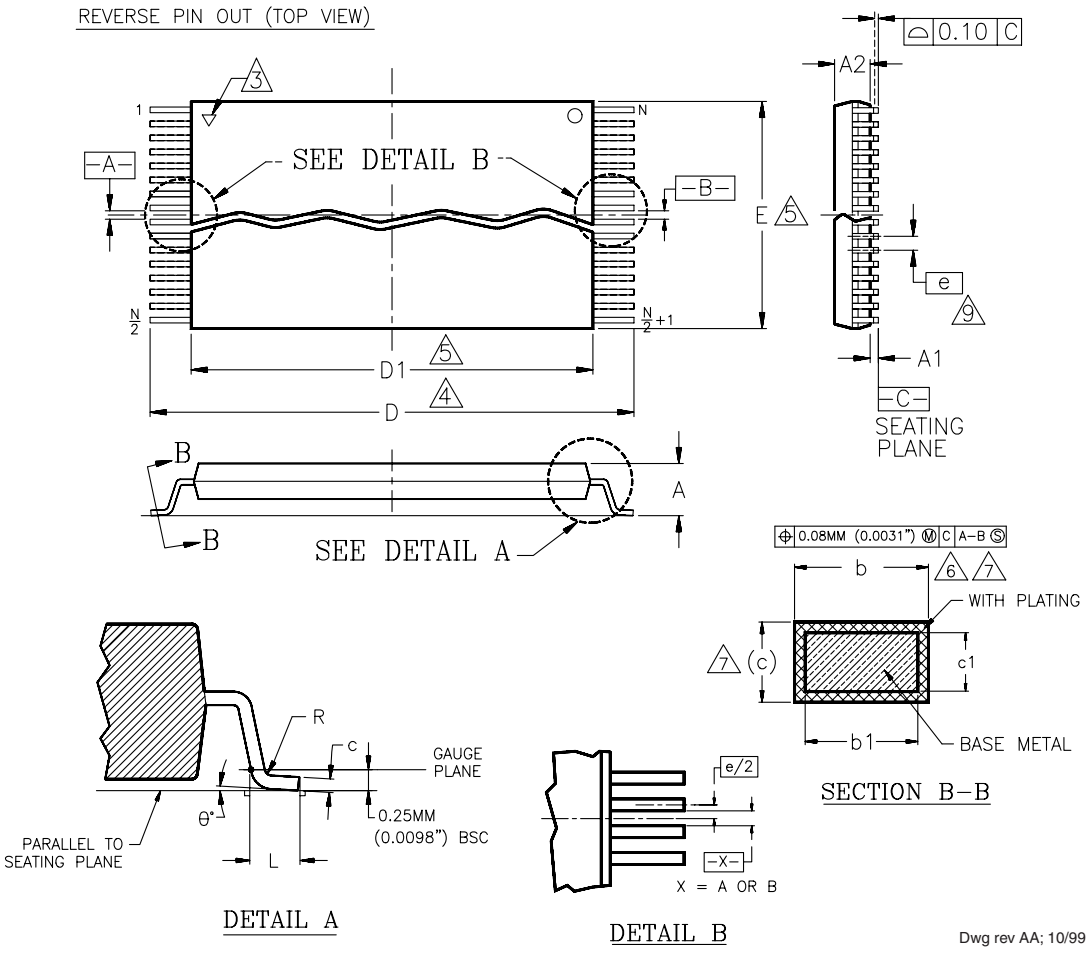
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

Note: *BSC is an ANSI standard for Basic Space Centering.*

Physical Dimensions

TSR048—48-Pin Reverse TSOP



Package	TSR 48		
Jedec	MO-142 (B) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	48		

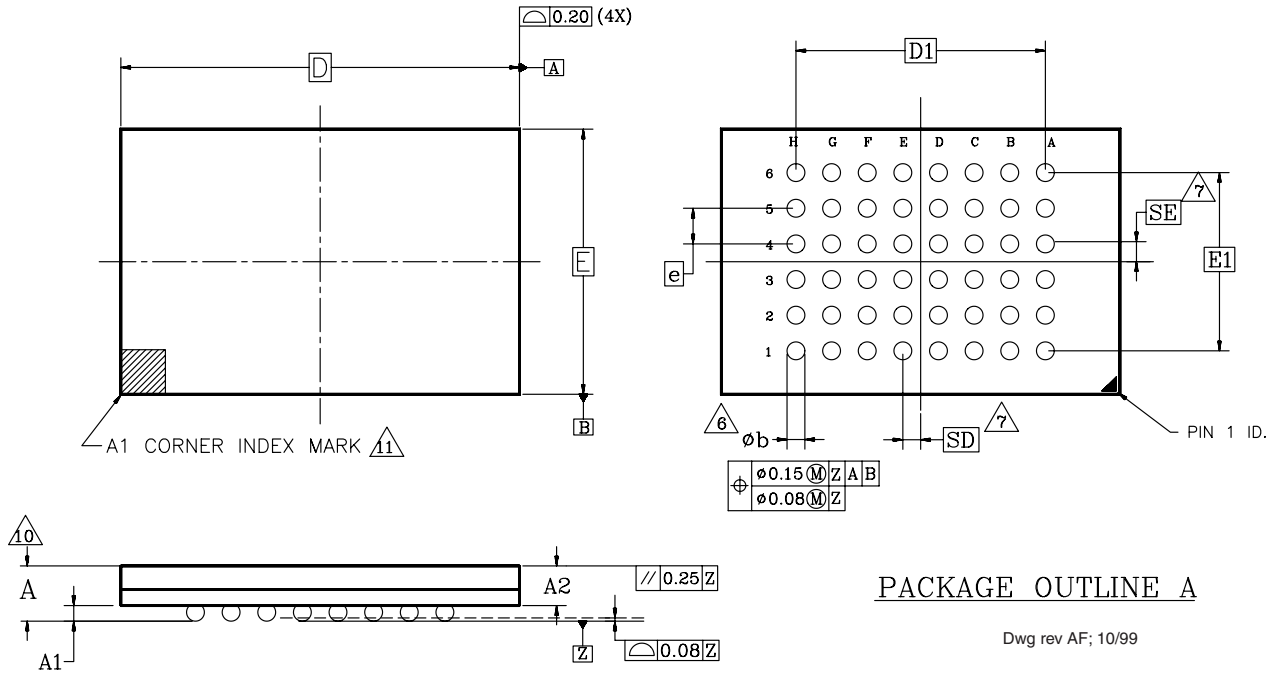
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

Note: *BSC is an ANSI standard for Basic Space Centering.*

Physical Dimensions

FBA048—48-Ball Fine-Pitch Ball Grid Array (BGA)
6 x 8 mm Package



PACKAGE OUTLINE A

Dwg rev AF; 10/99

PACKAGE	xFBA 048			
JEDEC	N/A			
	6.15mmx8.15mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	OVERALL THICKNESS
A1	0.20	–	–	BALL HEIGHT
A2	0.84	–	0.94	BODY THICKNESS
D	8.15 BSC			BODY SIZE
E	6.15 BSC			BODY SIZE
D1	5.60 BSC			BALL FOOTPRINT
E1	4.00 BSC			BALL FOOTPRINT
MD	8			ROW MATRIX SIZE D DIRECTION
ME	6			ROW MATRIX SIZE E DIRECTION
N	48			TOTAL BALL COUNT
b	0.25	0.30	0.35	BALL DIAMETER
e	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC			SOLDER BALL PLACEMENT

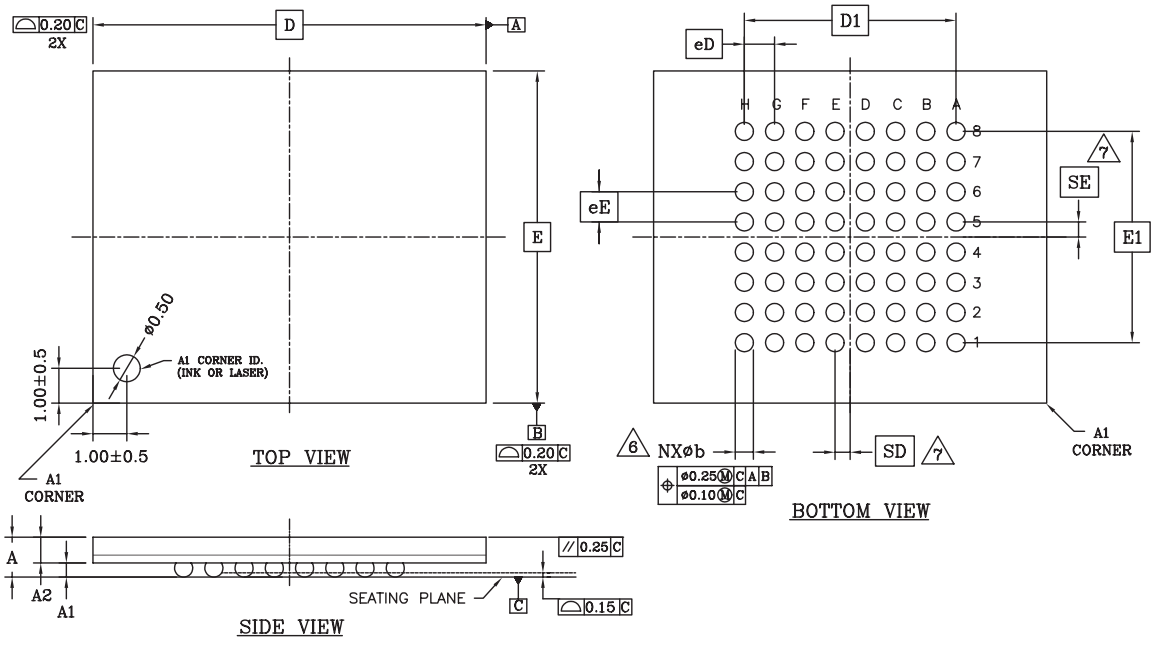
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" IN THE PACKAGE DRAWING INDICATE THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. FOR PACKAGE THICKNESS A IS THE CONTROLING DIMENSION.
11. A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTION OR OTHER MEANS.

Note: *BSC is an ANSI standard for Basic Space Centering.*

Physical Dimensions

LAA064—64-Ball Fortified Ball Grid Array (BGA)
13 x 11 mm Package



PACKAGE	LAA 064			
JEDEC	N/A			
	13.00x11.00 mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	NOTE
A	–	–	1.40	PROFILE HEIGHT
A1	0.40	–	–	STANDOFF
A2	0.60	–	–	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	7.00 BSC.			MATRIX FOOTPRINT
E1	7.00 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	64			BALL COUNT
øb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC.			BALL PITCH – D DIRECTION
eE	1.00 BSC.			BALL PITCH – E DIRECTION
SD/SE	0.50 BSC.			SOLDER BALL PLACEMENT
	A1–A8, K1–K8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM "C".
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

Note: *BSC is an ANSI standard for Basic Space Centering.*

Revision Summary

Revision A (June 24, 2002)

Initial release.

Revision A + 1 (July 3, 2002)

Added LAA064 package.

Corrected power consumption currents.

Changed DC Characteristics Zero Power Flash tables to TBD.

Corrected minimum erase and program cycle endurance.

Revision A+2 (December 6, 2002)

Global

Removed 44-pin SO package. Deleted dashes from ordering part numbers.

Distinctive Characteristics

Added information for SecSi sector, Program Suspend & Resume. Corrected erase endurance to 100K cycles. Changed section flow to match other MirrorBit data sheets.

General Description

Changed section flow to match other MirrorBit data sheets.

Connection Diagrams

Corrected Fortified BGA diagram: balls C5, D8, D4, and F1 are now NC.

Ordering Information and Operating Ranges

Removed Commercial and Extended temperature ranges. Corrected Fine-pitch BGA type to 6 x 8 mm package, FBA048.

Added package markings for the LAA064.

SecSi (Secured Silicon) Sector Flash Memory Region

Added section.

Program Suspend/Program Resume Command Sequence

Added text and flowchart.

Sector Protection/Unprotection

Deleted reference to alternate, high-voltage method of sector protection.

Command Definitions

Modified introductory paragraph to indicate device behavior when presented with incorrect commands and data. Added mode restrictions to first paragraphs of program, sector erase and chip erase subsections.

Command Definitions tables

Replaced previous table with two tables. Byte mode and word mode are now shown separately. Added SecSi Sector Factory Protect command sequence.

Table 10. Write Operation Status

Added Program Suspend Mode rows to table.

BGA and TSOP Capacitance

Added fine-pitch BGA capacitance to table.

AC Characteristics tables

Typical sector erase time is now 0.4 s in all tables.

Physical Dimensions

Corrected Fortified BGA drawing to FBA048.

Revision A+3 (January 6, 2003)

Global

Deleted references to WP# and ACC. The Am29LV160M does not offer those features.

Command Definitions table

Deleted references to write buffers. This device does not offer that feature.

AC Characteristics

Erase and Program Operations table; Alternate CE# Controlled Erase/Operations table: Changed t_{WHWH1} to TBD.

Revision A+4 (June 16, 2003)

Global

Changed status from Advance Information to Preliminary.

Modified speed options available.

Product Selector Guide

Added Note #2.

Ordering Information

Corrected OPN tables and added Note.

SecSi (Secured Silicon) Sector Flash Memory Region

Replaced text in this section.

Command Definitions

Modified Legend.

Erase / Program Operations and Alternate CE# Controlled Erase / Program Operations

Inserted values for all TBD.

Erase and Programming Performance

Inserted values for all TBD.

Revision B (August 11, 2003)

Global

Modified speed options available. Converted document formatting to Spansion template. Changed data sheet status from Advance Information to Preliminary.

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