TEXAS INSTRUMENTS

UCC29002, UCC29002-1, UCC39002

SLUS495I – SEPTEMBER 2001 – REVISED MAY 2016

UCC2900x, UCC39002 Advanced 8-Pin Load-Share Controller

1 Features

- High Accuracy, Better Than 1% Current Share Error at Full Load
- High-Side or Low-Side (GND Reference) Current-Sense Capability
- Ultra-Low Offset Current Sense Amplifier
- Single Wire Load Share Bus
- Full Scale Adjustability
- Intel® SSI Load Share Specification Compliant
- Disconnect from Load Share Bus at Stand-By
- Load Share Bus Protection Against Shorts to GND or to the Supply Rail
- 8-Pin MSOP Package Minimizes Space
- Lead-Free Assembly

2 Applications

- Modules With Remote-Sense Capability
- Modules With Remote-Sense Capability
- Modules With Remote-Sense Capability
- In Conjunction With the Internal Feedback E/A of OEM Power Supply Units

3 Description

The UCC39002 device is an advanced, high-performance, and low-cost load share controller that provides all necessary functions to parallel multiple independent power supplies or DC-to-DC modules. Targeted for high-reliability applications in server, workstation, telecom, and other distributed power systems, the controller is suitable for N+1 redundant systems or high current applications where off-the-shelf power supplies must be paralleled.

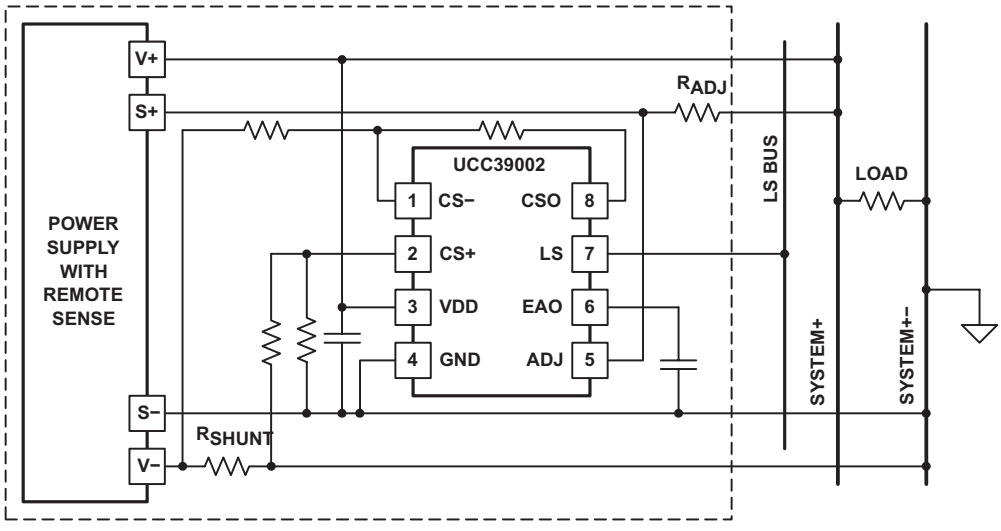
The BiCMOS UCC39002 is based on the automatic master or slave architecture of the UC3902 and UC3907 load share controllers. The device provides better than 1% current share error between modules at full load by using a very low offset post-package-trimmed current sense amplifier and a high-gain negative feedback loop. And with the amplifier's common-mode range of 0 V to the supply rail, the current sense resistor, R_{SHUNT}, can be placed in either the GND return path or in the positive output rail of the power supply.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC29002	SOIC (8)	4.90 mm × 3.91 mm
UCC29002-1	VSSOP (8)	3.00 mm × 3.00 mm
UCC39002	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Low-Side Current-Sensing Application



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4 Revision History

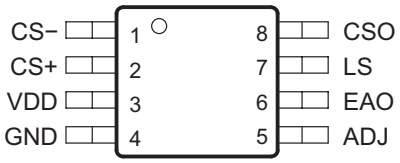
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (August 2007) to Revision I	Page
• Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

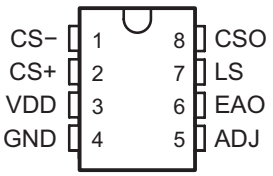
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5 Pin Configuration and Functions

D or DGK Package
8-Pin SOIC or VSSOP
Top View



P Package
8-Pin PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADJ	5	O	Adjust amplifier output. This is the buffered output of the error amplifier block to adjust output voltage of the power supply being controlled. This pin must always be connected to a voltage equal to or greater than V_{EAO} + 1 V.
CS–	1	I	Current sense amplifier inverting input.
CS+	2	I	Current sense amplifier noninverting input.
CSO	8	O	Current sense amplifier output.
EAO	6	O	Output for load share error amplifier. (Transconductance error amplifier.)
GND	4	–	Ground. Reference ground and power ground for all device functions. Return the device to the low current sense−path of the converter.
LS	7	I/O	Load share bus. Output of the load share bus driver amplifier.
VDD	3	I	Power supply providing bias to the device. Bypass with a good quality, low ESL 0.1-µF to 1-µF, maximum, capacitor as close to the VDD pin and GND as possible.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{DD}	Supply voltage, current limited	−0.3	15	V
V_{DD}	Supply voltage, voltage source	−0.3	13.5	V
V_{CS+}, V_{CS-}	Input voltage, current sense amplifier	–0.3	V_{DD} + 0.3	V
V_{CSO}	Current sense amplifier output voltage	−0.3	V_{DD}	V
V_{LS}	Load share bus voltage	−0.3	V_{DD}	V
	Supply current (I_{DD} + I_{ZENER})		10	mA
V_{ADJ}	Adjust pin input voltage	V_{EAO} +1 V < V_{ADJ} ≤ V_{DD}		
I_{ADJ}	Adjust pin sink current		6	mA
T_J	Operating junction temperature range	−55	150	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage, voltage source	4.575	13.5	V
V_{CSO}	Current sense amplifier output voltage	0	11.8	V
V_{LS}	Load share bus voltage	0	V_{DD} – 1.7	V
I_{ADJ}	Adjust pin sink current		4.55	mA

6.4 Thermal Information

THERMAL METRIC(1)		UCC2900x/UCC39002			UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.9	168.0	54.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.6	61.9	43.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	88.8	31.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.9	7.3	21.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.0	87.2	31.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

V_{DD} = 12 V, 0°C < 70°C for the UCC39002, –40°C < T_A < 105°C for the UCC29002 and UCC29002-1, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL							
	Supply current	LS with no load, ADJ = 5 V			2.5	3.5	mA
	VDD clamp voltage	IDD = 6 mA		13.5	14.25	15	V
UNDERVOLTAGE LOCKOUT							
	Start-up voltage(1)			4.175	4.375	4.575	V
	Hysteresis			0.2	0.375	0.55	V
CURRENT SENSE AMPLIFIER							
V_{IO}	Input offset voltage	T_A = 25 C, V_{IC} = 0.5 V or 11.5 V, V_{CSO} = 5 V		−100		100	µV
		Overtemperature variation			±10		µV/ C
A_V	Gain			75	90		dB
CMRR	Common-mode rejection ratio			75	90		dB
I_{BIAS}	Input bias current (CS+, CS−)			−0.6		0.6	µA
V_{OH}	High-level output voltage (CSO)	0.1 V ≤ ([CS+] − [CS−]) ≤ 0.4 V, I_{OUT_CSO} = 0 mA		10.7	11	11.8	V
V_{OL}	Low-level output voltage (CSO)	−0.4 V ≤ ([CS+] − [CS−]) ≤ 0.1 V, I_{OUT_CSO} = 0 mA		0	0.1	0.15	V
I_{OH}	High-level output current (CSO)	V_{CSO} = 10 V		−1	−1.5		mA
I_{OL}	Low-level output current (CSO)	V_{CSO} = 1 V		1	1.5		mA
GBW	Gain bandwidth product(2)				2		MHz
LOAD SHARE DRIVER (LS)							
V_{RANGE}	Input voltage range			0		10	V
V_{OUT}	Output voltage	V_{CSO} = 1 V		0.995	1	1.005	V
		V_{CSO} = 10 V		0.995	10	1.005	V
V_{OL}	Low-level output voltage	V_{CSO} = 0 V, I_{OUT_LS} = 0 mA		0	0.1	0.15	V
V_{OH}	High-level output voltage(2)				V_{DD} – 1.7		V
I_{OUT}	Output current	0.5 V ≤ V_{LS} ≤ 10 V		−1	−1.5		V
I_{SC}	Short-circuit current	V_{LS} = 0 V, V_{CSO} = 10 V		−10	−20		mA
V_{SHTDN}	Driver shutdown threshold	V_{CS-} − V_{CS+}		0.3	0.5	0.7	V
LOAD SHARE BUS PROTECTION							
I_{ADJ}	Adjust amplifier current	V_{CSO} = 2 V, V_{EAO} = 2 V, V_{LS} = V_{DD}, V_{ADJ} = 5 V		0	5	10	µA
		V_{CSO} = 2 V, V_{EAO} = 2 V, V_{LS} = 0 V, V_{ADJ} = 5 V		0	5	10	µA
ERROR AMPLIFIER							
V_{OH}	High-level output voltage	I_{OUT_EAO} = 0 mA		3.5	3.65	3.8	V
g_M	Transconductance	I_{EAO} = ± 50 µA			14		mS
I_{OH}	High-level output current	V_{LS} − V_{CSO} = 0.4 V, R_{EAO} = 2.2 kΩ		0.7	0.85	1	mA
ADJ BUFFER							
V_{IO}	Input offset voltage(2)	V_{ADJ} = 1.5 V, V_{EAO} = 0 V			−60		mV
I_{SINK}	Sink current	V_{ADJ} = 5.0 V, V_{EAO} = 0 V		0	5	10	µA
I_{SINK}	Sink current	T_A = 25°C	V_{ADJ} = 5.0 V, V_{EAO} = 2.0 V, LS = floating	3.6	3.95	4.3	mA
		0°C ≤ T_A ≤ 70°C		3.45	3.95	4.45	mA
		−40°C ≤ T_A ≤ 105°C		3.35	3.95	4.55	mA

(1) Enables the load share bus at start-up.
(2) Ensured by design. Not production tested.

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6.6 Typical Characteristics

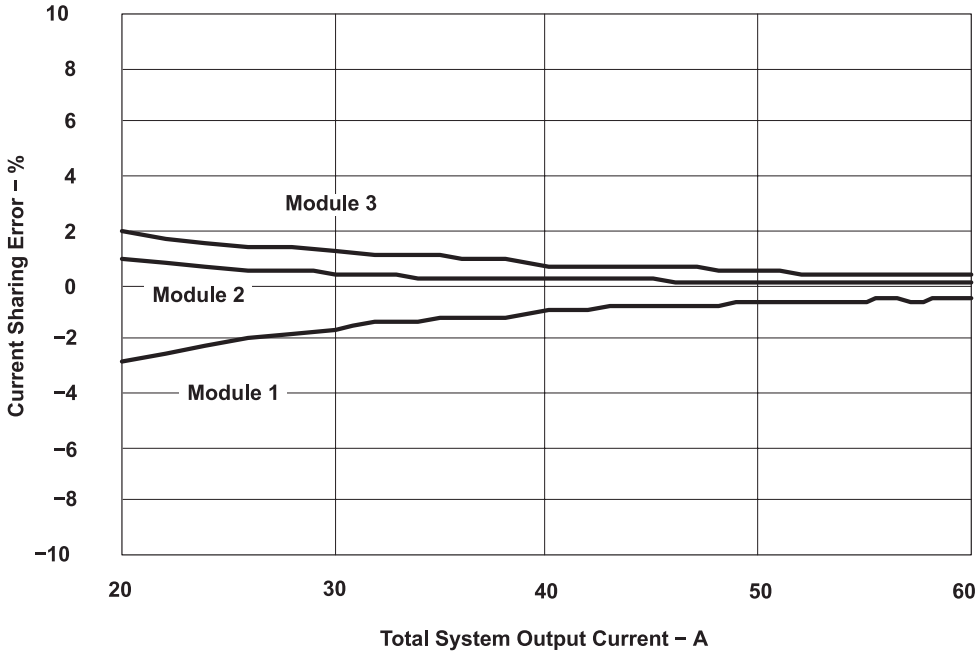


Figure 1. Resultant Load Current Sharing Accuracy, as Measured Across Shunts from the Output of Each Module

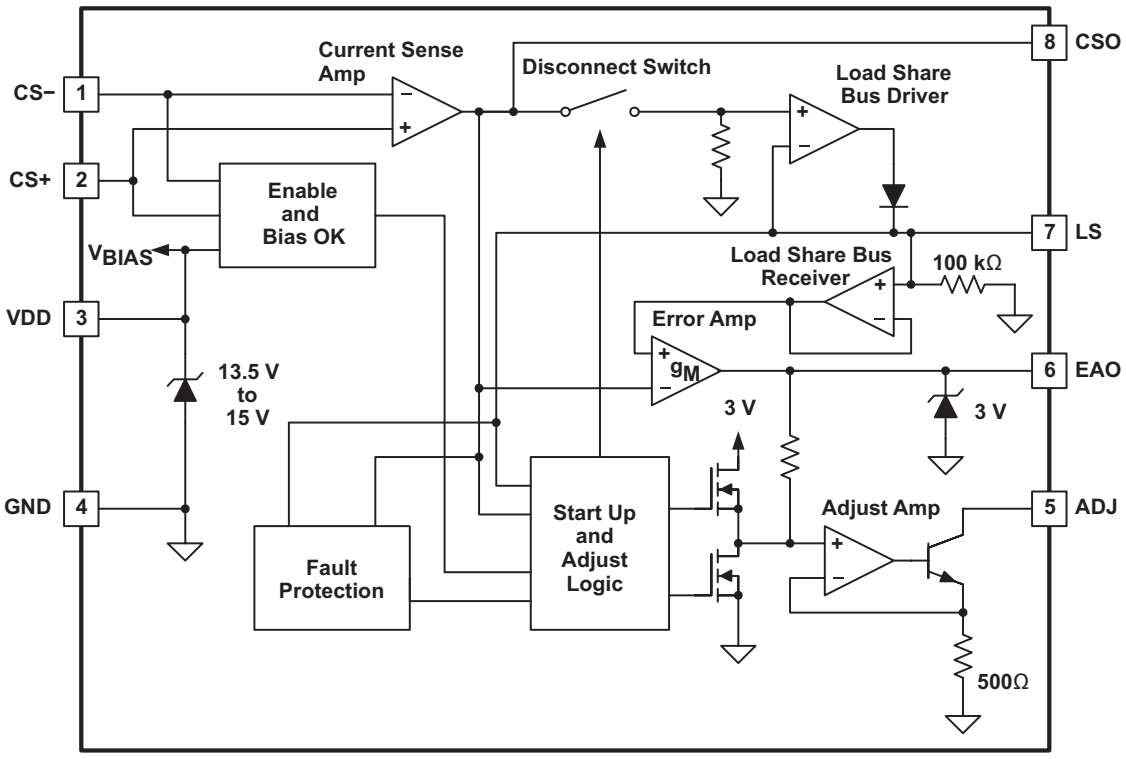
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7 Detailed Description

7.1 Overview

The UCC39002 is an advanced, high-performance, low-cost load-share controller that provides all the necessary functions to parallel multiple independent power supplies and modules. The UCC39002 can easily parallel currently available and popular synchronous buck converters, such as those designed with the TPS40050 controller.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Differential Current Sense Amplifier (CS+, CS−, CSO)

The UCC39002 features a high-gain and high-precision amplifier to measure the voltage across a low-value current sense resistor. Because the amplifier is fully uncommitted, the current sense gain is user programmable. The extremely low input offset voltage of the UCC39002 current sense amplifier makes it suitable to measure current information across a low value sense resistor. Furthermore, the input common mode range includes ground and the positive supply rail of the UCC39002 (V_{DD}). Accordingly, the current sense resistor can be placed in the ground return path or in the positive output rail of the power supply V_O as long as $V_O \leq V_{DD}$. The current sense amplifier is not unity gain stable and must have a minimum gain of three.

7.3.2 Load Share Bus Driver Amplifier (CSO)

This is a unity-gain buffer amplifier to provide separation between the load share bus voltage and the output of the current sense amplifier. The circuit implements an ideal diode with virtually 0-V forward voltage drop by placing the diode inside the feedback loop of the amplifier. The diode function is used to automatically establish the role of the master module in the system. The UCC39002 which is assigned to be the master uses the load share bus driver amplifier to copy its output current information on to the load share bus.

Feature Description (continued)

All slave units, with lower output current levels by definition, have this *ideal diode* reversed biased ($V_{CSO} < V_{LS}$). Consequently, the V_{CSO} and V_{LS} signals will be separated. That allows the error amplifier of the UCC39002 to compare its respective module's output current to the master module's output current and make the necessary corrections to achieve a balanced current distribution.

Since the bus is always driven by a single load share bus driver amplifier, the number of modules (n) are limited by the output current capability of the amplifier according to Equation 1:

$$n = \frac{100\ k\Omega \times I_{OUT,MIN}}{V_{LS,FULL_SCALE}} \quad (1)$$

where

- 100 kΩ is the input impedance of the LS pin as shown in the block diagram,
- $I_{OUT,MIN}$ is given in the data sheet
- and $V_{LS,FULL_SCALE}$ is the maximum voltage on the load share bus at full load.

NOTE

The number of parallel units can be increased by reducing the full scale bus voltage, that is, by reducing the current sense gain.

7.3.3 Load Share Bus Receiver Amplifier (LS)

The load share bus receiver amplifier is a unity-gain buffer monitoring the load share bus voltage. Its primary purpose is to ensure that the load share bus is not loaded by the internal impedances of the UCC39002. The LS pin is already internally compensated and has an internal 15-kHz filter. Adding external capacitance, including stray capacitance, must be avoided to maintain stability

7.3.4 Error Amplifier (EAO)

As pictured in the block diagram, the UCC39002 employs a transconductance also called g_M type error amplifier. The g_M amplifier was chosen because it requires only one pin, the output to be accessible for compensation.

The purpose of the error amplifier is to compare the average, per module current level to the output current of the respective module controlled by the UCC39002. It is accommodated by connecting the buffered V_{LS} voltage to its noninverting input and the V_{CSO} signal to its inverting input. If the average per module current, represented by the load share bus is higher than the module's own output current, an error signal will be developed across the compensation components connected between the EAO pin and ground. The error signal is than used by the adjust amplifier to make the necessary output voltage adjustments to ensure equal output currents among the parallel operated power supplies.

In case the UCC39002 assumes the role of the master load share controller in the system or it is used in conjunction with a stand alone power module, the measured current signal on V_{CSO} is approximately equal to the V_{LS} voltage. To avoid erroneous output voltage adjustment, the input of the error amplifier incorporates a typically 25-mV offset to ensure that the inverting input of the error amplifier is biased higher than the noninverting input. Consequently, when the two signals are equal, there will be no adjustment made and the initial output voltage set point is maintained.

7.3.5 Adjust Amplifier Output (ADJ)

A current proportional to the error voltage V_{EAO} on pin 6 is sunk by the ADJ pin. This current flows through the adjust resistor R_{ADJ} and changes the output voltage of the module controlled by the UCC39002. The amplitude of the current is set by the 500-Ω internal resistor between ground and the emitter of the amplifier's open collector output transistor according to Figure 2. The adjust current value is given in Equation 2:

$$I_{ADJ} = \frac{V_{EAO}}{500\ \Omega} \quad (2)$$

At the master module V_{EAO} is 0 V, thus the adjust current must be zero as well. This ensures that the output voltage of the master module remains at its initial output voltage set point at all times.

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Feature Description (continued)

Furthermore, at insufficient bias level, during a fault or when the UCC39002 is disabled, the noninverting input of the adjust amplifier is pulled to ground to prevent erroneous adjustment of the module's output voltage by the load share controller.

7.3.6 Enable Function (CS+, CS−)

The two inputs of the current sense amplifier are also used for implementing an ENABLE function. During normal operation CS− = CS+ and the internal offset added between the CS− voltage and the inverting input of the enable comparator ensures that the UCC39002 is always enabled. By forcing the CS− pin approximately 0.5 V above the CS+ pin, the UCC39002 can be forced into a disable mode. While disabled, the UCC39002 disconnects itself from the load share bus and its adjust current is zero.

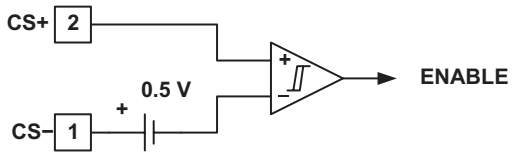


Figure 2. Enable Comparator

7.3.7 Fault Protection

Accidentally, the load share bus might be shorted to ground or to the positive bias voltage of the UCC39002. These events might result in erroneous output voltage adjustment. For that reason, the load share bus is continuously monitored by a window comparator as shown in Figure 3.

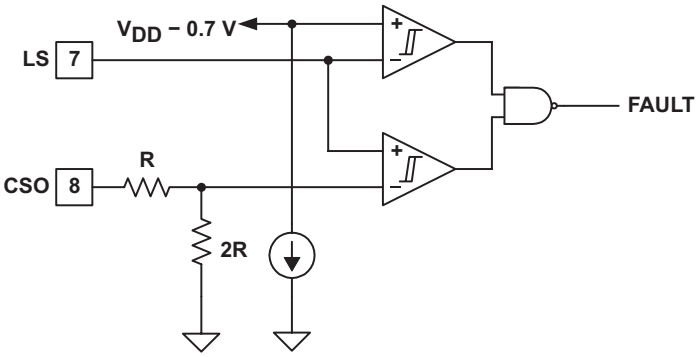


Figure 3. Fault Protection Comparators

The FAULT signal is handled by the start-up and adjust logic which pulls the noninverting input of the adjust amplifier low when the FAULT signal is asserted.

7.3.8 Start-Up and Adjust Logic

The start-up and adjust logic responds to unusual operating conditions during start up, fault and disable. Under these circumstances the information obtainable by the error amplifier of the UCC39002 is not sufficient to make the right output voltage adjustment, therefore the adjust amplifier is forced to certain known states. Similarly, the driver amplifier of UCC39002 is disabled during these conditions.

In the UCC39002 and UCC29002, during start-up, the load share driver amplifier is disabled by the disconnect switch and the adjust amplifier is forced to sink the maximum current through the adjust resistor. This operating mode ensures that the module controlled by the UCC39002 will be able to quickly engage in sharing the load current since its output will be adjusted to a sufficiently high voltage immediately at turnon. Both the load share driver and the adjust amplifiers revert to normal operation as soon as the measured current exceeds 80% of the average per module current level represented by the LS bus voltage. The UCC29002 and UCC29001 does not have this logic at start up. In this way, the UCC2900x does not adjust the output of the module to its maximum adjustment range at turn on and engages load sharing at more moderate rate.

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Feature Description (continued)

In case of a fault shorting the load share bus to ground or to the bias of the UCC39002 the load share bus driver and the adjust amplifiers are disabled. The same action takes place when the UCC39002 is disabled using the CS+ and CS− pins or when the bias voltage is below the minimum operating voltage.

7.3.9 Bias and Bias OK Circuit (VDD)

The UCC39002 is built on a 15-V, high-performance BiCMOS process. Therefore, the maximum voltage across the V_{DD} and GND pins (pin 3 and 4 respectively) is limited to 15 V. The recommended maximum operating voltage is 13.5 V which corresponds to the tolerance of the on-board 14.2-V Zener clamp circuit. In case the bias voltage could exceed the 13.5-V limit, the UCC39002 should be powered through a current limiting resistor. The current into the V_{DD} pin must be limited to 10 mA as listed in *Absolute Maximum Ratings*.

The bypass capacitor for VDD is also the compensation for the input active clamp of the device and, as such, must be placed as close to the device pins (VDD and GND) as possible, using a good-quality, low-ESL capacitor, including trace length. The device is optimized for a capacitor value of 0.1 µF to 1 µF.

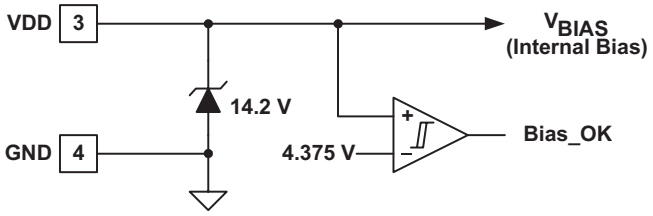


Figure 4. V_{DD} Clamp and Bias Monitor

The UCC39002 does not have an undervoltage lockout circuit. The bias OK comparator works as an enable function with a 4.375-V threshold. While V_{DD} < 4.375 V the load share control functions are disabled. While this might be inconvenient for some low voltage applications it is necessary to ensure high accuracy. The load share accuracy is dependent on working with relatively large signal amplitudes on the load share bus. If the internal offsets, current sense error and ground potential difference between the UCC39002 controllers are comparable in amplitude to the load share bus voltage, they can cause significant current distribution error in the system. The maximum voltage on the load share bus is limited approximately 1.7 V below the bias voltage level (V_{DD}) which would result in an unacceptably low load share bus amplitude therefore poor accuracy at low V_{DD} levels. To circumvent this potential design problem, the UCC39002 does not operate below the above mentioned 4.375-V bias voltage threshold. If the system does not have a suitable bias voltage available to power the UCC39002, TI recommends using an inexpensive charge pump which can generate the bias voltage for all the UCC39002s in the load share system.

The maximum V_{DD} of the UCC39002 is 15 V. For higher-voltage applications, use the application solution as recommended in Figure 5. A Zener clamp on the VDD pin is provided internally so the device can be powered from higher voltage rails using a minimum number of external components.

The CSA inputs must be adjusted so as to not exceed their absolute maximum voltage ratings.

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Feature Description (continued)

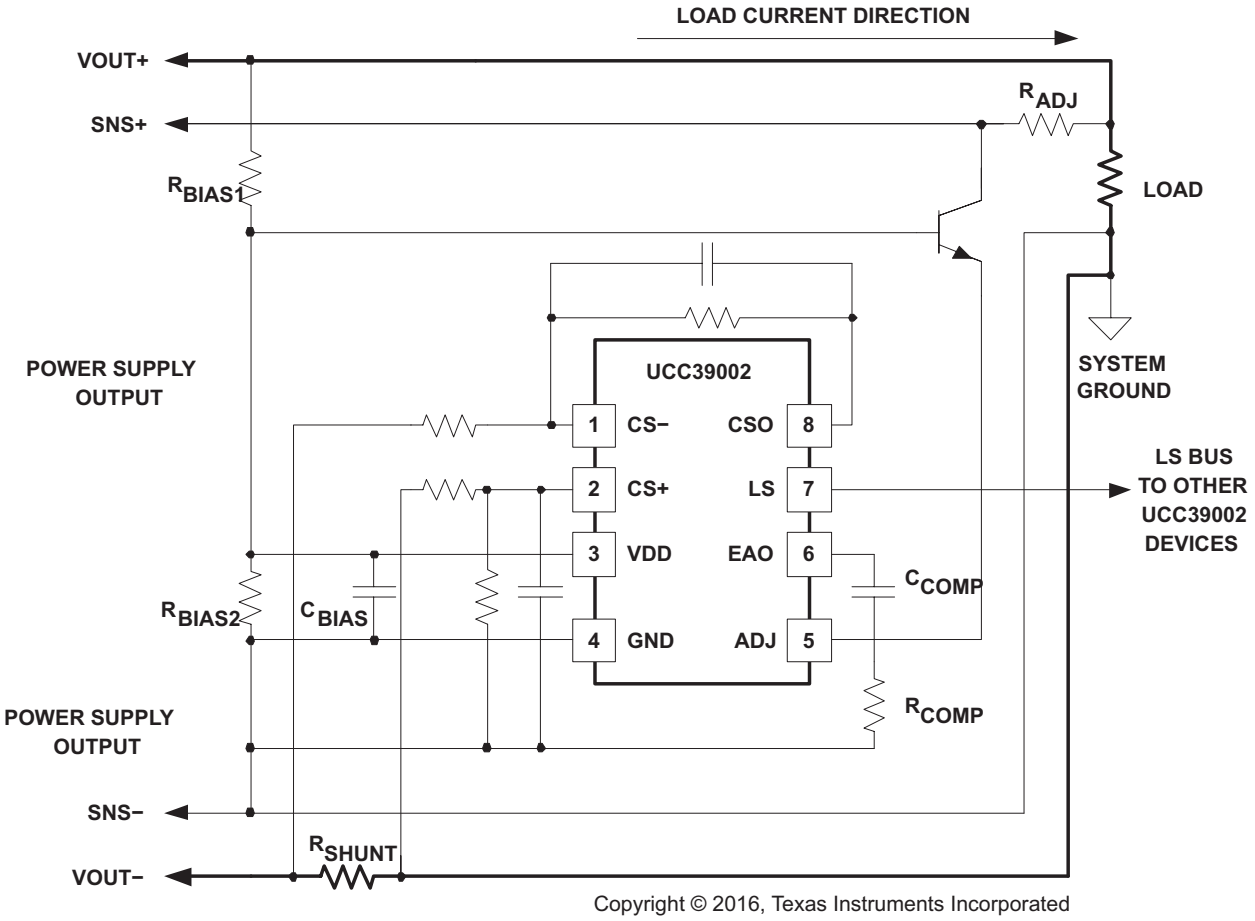


Figure 5. High Voltage Application

The following is a practical step-by-step design procedure on how to use the UCC39002 to parallel power modules for load sharing.

7.3.10 Paralleling the Power Modules

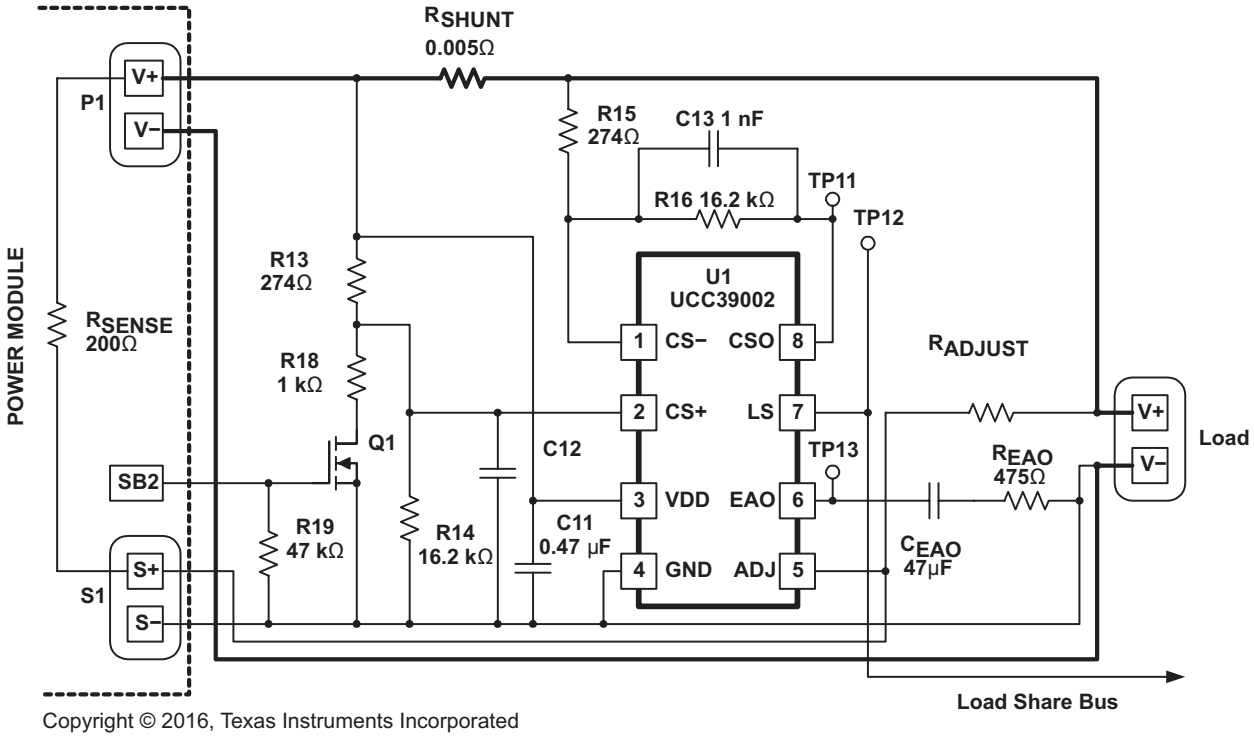
- V_{OUT} = nominal output voltage of the modules to be paralleled
- $I_{OUT(max)}$ = maximum output current of each module to be paralleled
- ΔV_{ADJ} = maximum output voltage adjustment range of the power modules to be paralleled
- N = number of modules

NOTE

The power modules to be paralleled must be equipped with true remote sense or access to the feedback divider of the module's error amplifier.

A typical high side application for a single module is shown in Figure 6 and is repeated for each module to be paralleled.

Feature Description (continued)



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Figure 6. Typical High-Side Application for Single Power Module

In Figure 6, P1 represents the output voltage terminals of the module, S1 represents the remote sense terminals of the module, and a signal on the SB2 terminal will enable the disconnect feature of the device. The load share bus is the common bus between all of the paralleled load share controllers. VDD must be decoupled with a good-quality ceramic capacitor returned directly to GND.

7.3.11 Measuring the Loop of the Modules

Using the configuration in Figure 7, measure the unity-gain crossover frequency of the power modules to be paralleled. A typical resultant bode plot is shown in Figure 8.

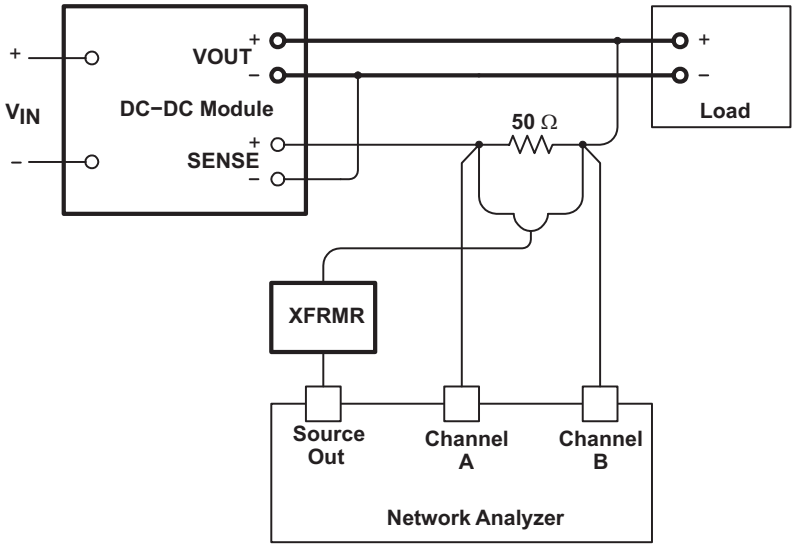


Figure 7. Unity-Gain Crossover Frequency Measurement Connection Diagram

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Feature Description (continued)

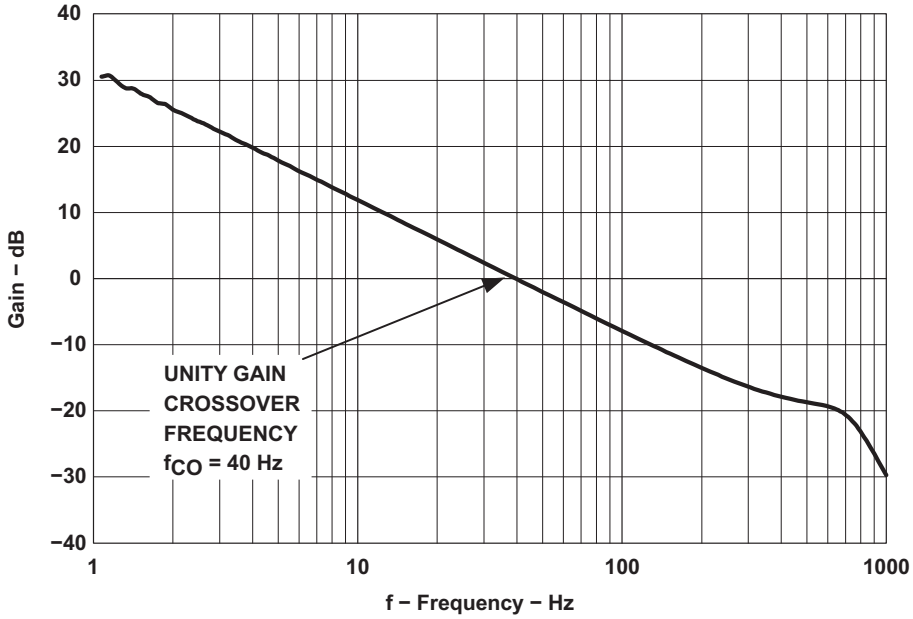


Figure 8. Power Module Bode Plot

7.4 Device Functional Modes

7.4.1 Fault

This condition occurs if the load share bus is shorted high or low. Under this condition the device responds by pulling the inverting input of the adjust amplifier low. See *Fault Protection* for details.

7.4.2 Start-Up

During start up the load share driver amplifier is disabled and the adjust amplifier is forced to sink the maximum current through the adjust resistor. See *Start-Up and Adjust Logic* for details.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC39002 is an advanced, high-performance load-share controller that provides all the necessary functions to parallel multiple independent power supplies or DC-to-DC modules. This load-share circuit is based upon the automatic master or slave architecture used in the UC3902 and the UC3907 load-share controllers providing better than 1% current-share error between the modules at full load.

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8.2 Typical Application

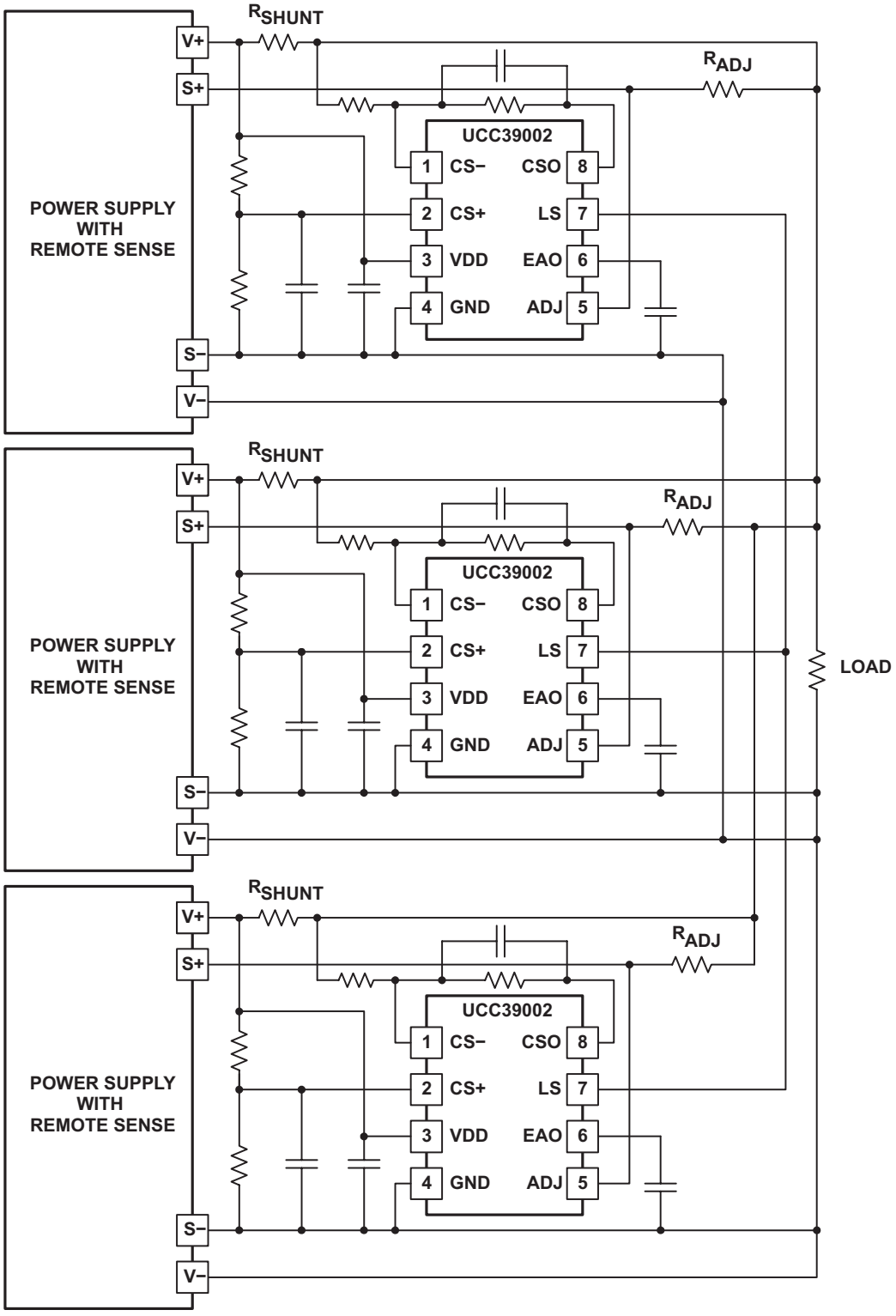


Figure 9. Typical High-Side Current-Sensing Application

Typical Application (continued)

8.2.1 Design Requirements

In order to properly configure and design with the UCC39002 it necessary to gather requirements for the following system level performance metrics.

1. Required system level stability to include phase margin (φ_m), gain margin (g_m), and bandwidth (f_{bw}). Typical values are φ_m = 45 °, g_m = 10 dB, and f_{bw}= f_s/10 where f_s is the switching frequency.

2. Required current sharing accuracy. Typically this is 1 %.

8.2.2 Detailed Design Procedure

The following is a practical step-by-step design procedure on how to use the UCC39002 to parallel power modules for load sharing.

8.2.2.1 The Shunt Resistor

Selection of the shunt resistor is limited by its voltage drop at maximum module output current. This voltage drop should be much less than the voltage adjustment range of the module shown in Equation 3:

$$I_{OUT(max)} \times R_{SHUNT} << \Delta V_{ADJ(max)} \tag{3}$$

Other limitations for the sense resistor are the desired minimum power dissipation and available component ratings.

8.2.2.2 The CSA Gain

The gain of the current sense amplifier is configured by the compensation components between Pin 1, CS−, and Pin 8, CSO, of the load share device. The voltage at the CSO pin is limited by the saturation voltage of the internal current sense amplifier and must be at least two volts less than VDD in Equation 4:

$$V_{CSO(max)} < VDD - 2\ V \tag{4}$$

The maximum current sense amplifier gain is equal to Equation 5:

$$A_{CSA} = \frac{V_{CSO}}{R_{SHUNT} \times I_{OUT(max)}} \tag{5}$$

Referring to Figure 6, the gain is equal to R16/R15 and a high-frequency pole, configured with C13, is used for noise filtering. This impedance is mirrored at the CS+ pin of the differential amplifier as shown.

The current sense amplifier output voltage, V_{CSO}, serves as the input to the unity gain LS bus driver. The module with the highest output voltage forward biases the internal diode at the output of the LS bus driver and determine the voltage on the load share bus, V_{LS}. The other modules act as slaves and represent a load on the I_{VDD} of the module due to the internal 100-kΩ resistor at the LS pin. This increase in supply current for the master module is equal to N(V_{LS}/100 kΩ).

8.2.2.3 Determining R_{ADJUST}

The Sense+ terminal of the module is connected to the ADJ pin of the load-share controller. By placing a resistor between this ADJ pin and the load, an artificial Sense+ voltage is created from the voltage drop across R_{ADJUST} due to the current sunk by the internal NPN transistor. The voltage at the ADJ pin must be maintained at approximately 1 V above the voltage at the EAO pin. This is necessary in order to keep the transistor at the output of the internal adjust amplifier from saturating. To fulfill this requirement, R_{ADJUST} is first calculated using Equation 6:

$$R_{ADJUST} \geq \frac{\left(\Delta V_{ADJ(max)} - I_{OUT(max)} \times R_{SHUNT}\right) \times 500\ \Omega}{\left[V_{OUT} - \Delta V_{ADJ(max)} - 1\ V - \left(\frac{\Delta V_{ADJ(max)}}{R_{SENSE}} \times 500\ \Omega\right)\right]} \tag{6}$$

where

- R_{SHUNT} is the current sense resistor,
- and R_{SENSE} is the internal resistance between V_{OUT+} and SENSE+ within the module.

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Typical Application (continued)

Also needed for consideration is the actual adjust pin current. The maximum sink current for the ADJ pin, I_{ADJmax}, is 6 mA as determined by the internal 500-Ω emitter resistor and 3-V clamp. The value of adjust resistor, R_{ADJUST}, is based upon the maximum adjustment range of the module, ΔV_{ADJmax}. This adjust resistor is determined using Equation 7:

$$R_{ADJUST} \geq \frac{\left[\Delta V_{ADJ(max)} - I_{OUT(max)} \times R_{SHUNT}\right]}{I_{ADJ(max)} - \frac{\Delta V_{ADJ(max)}}{R_{SENSE}}} \quad (7)$$

By selecting a resistor that meets both of these minimum requirements, the ADJ pin will be at least 1 V greater than the EAO voltage and the adjust pin sink current will not exceed its 6 mA maximum.

8.2.2.4 Error Amplifier Compensation

The total load-share loop unity-gain crossover frequency, f_{CO}, must be set at least one decade below the measured crossover frequency of the paralleled modules previously measured, $f_{CO(module)}$. (See Figure 8) Compensation of the transconductance error amplifier is accomplished by placing the compensation resistor, R_{EAO}, and capacitor, C_{EAO}, between EAO and GND. The values of these components is determined using Equation 8 and Equation 13.

$$C_{EAO} = \left(\frac{g_M}{2\pi f_{CO}}\right)(A_{CSA})(A_V)(A_{ADJ})\left(\left|A_{PWR}(f_{CO})\right|\right) \quad (8)$$

where

- g_M is the transconductance of the error amplifier, typically 14 mS,
- f_{CO} is equal to the desired crossover frequency in Hz of the load share loop, typically fCO (module)/10,
- A_{CSA} is the CSA gain,
- A_V is the voltage gain,
- A_{ADJ} is the gain associated with the adjust amplifier,
- $|A_{PWR}(f_{CO})|$ is the measured gain of the power module at the desired load share crossover frequency, f_{CO}, converted to V/V from dB

$$A_{CSA} = \frac{R16}{R15} \quad (9)$$

$$A_V = \frac{R_{SHUNT}}{R_{LOAD}},\ R_{LOAD} = \frac{V_{OUT}}{I_{OUT(max)}} \quad (10)$$

$$A_{ADJ} = \frac{R_{ADJUST} \times R_{SENSE}}{(R_{ADJUST} \times R_{SENSE}) \times 500\ \Omega} \quad (11)$$

$$\left|A_{PWR}(f_{CO})\right| = 10\left(\frac{G_{MODULE}(f_{CO})}{20}\right) \quad (12)$$

where

- $G_{MODULE}(f_{co})$ is the measured value of the gain from Figure 8, at the desired crossover frequency.

Once the C_{EAO} capacitor is determined, R_{EAO} is selected to achieve the desired loop response, using Equation 13:

$$R_{EAO} = \sqrt{\left(\frac{1}{gm \times \left|A_{PWR}(f_{CO})\right| \times A_V \times A_{CSA} \times A_{ADJ}}\right)^2 - \left(\frac{1}{2\pi(f_{CO})(C_{EAO})}\right)^2} \quad (13)$$

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Typical Application (continued)

8.2.3 Application Curve

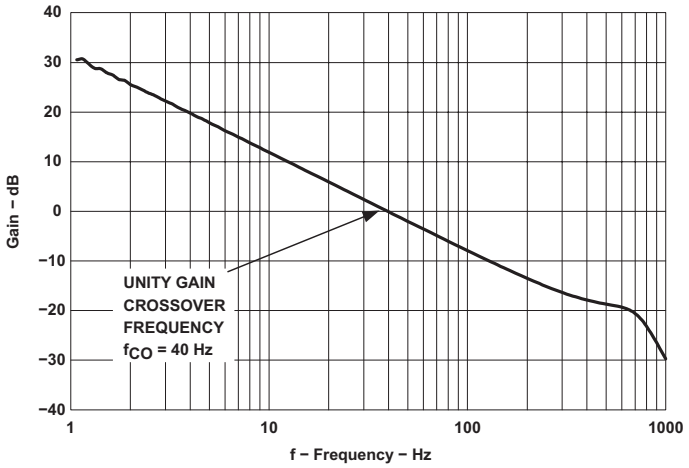


Figure 10. Power Module Bode Plot

9 Power Supply Recommendations

V_{DD} must be decoupled with a good-quality ceramic capacitor returned directly to GND. The device is optimized for a capacitor value of 0.1 µF to 1 µF.

10 Layout

10.1 Layout Guidelines

The bypass capacitor for V_{DD} is also the compensation for the input active clamp of the device and, as such, must be placed as close to the device pins (V_{DD} and GND) as possible, using a good-quality, low-ESL capacitor, including trace length.

10.2 Layout Example

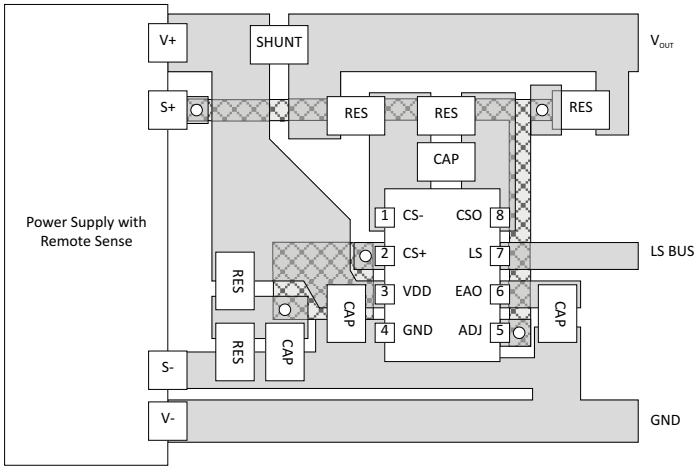


Figure 11. Layout Example

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For further details, refer to the following document:

- Reference Design, *48-V_{IN}, 12-V_{OUT} Loadshare System Using UCC39002 with Three DC/DC PH-100S4 Modules*, SLUA270

For a more complete description of general load sharing topics, refer to the following documents.

- Application Note, *The UC3902 Load Share Controller and Its Performance in Distributed Power Systems*, SLUA128
- Application Note, *UC3907 Load Share IC Simplifies Parallel Power Supply Design*, SLUA147

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC29002	Click here	Click here	Click here	Click here	Click here
UCC29002-1	Click here	Click here	Click here	Click here	Click here
UCC39002	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

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TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC29002D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	29002	Samples
UCC29002D/1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	290021	Samples
UCC29002D/1G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	290021	Samples
UCC29002DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	29002	Samples
UCC29002DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	29002	Samples
UCC29002DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	29002	Samples
UCC29002DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	29002	Samples
UCC29002DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	29002	Samples
UCC29002DR/1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	290021	Samples
UCC29002P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	UCC29002P	Samples
UCC39002D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	39002	Samples
UCC39002DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	39002	Samples
UCC39002DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	0 to 70	39002	Samples
UCC39002DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	0 to 70	39002	Samples
UCC39002DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	39002	Samples
UCC39002DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	39002	Samples
UCC39002P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC39002P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

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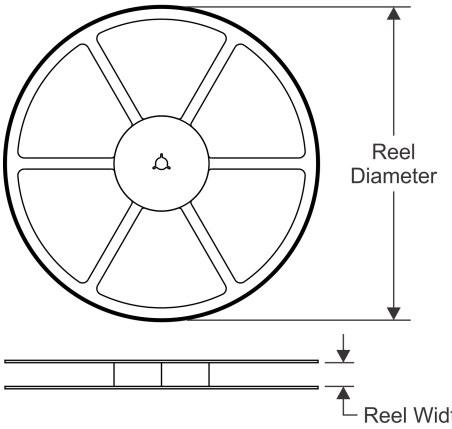
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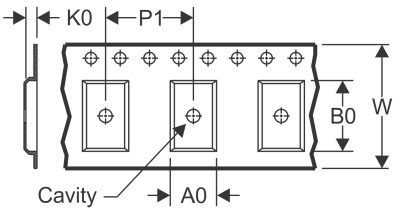
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TAPE AND REEL INFORMATION

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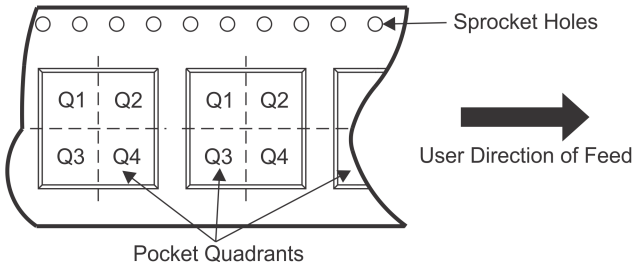


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

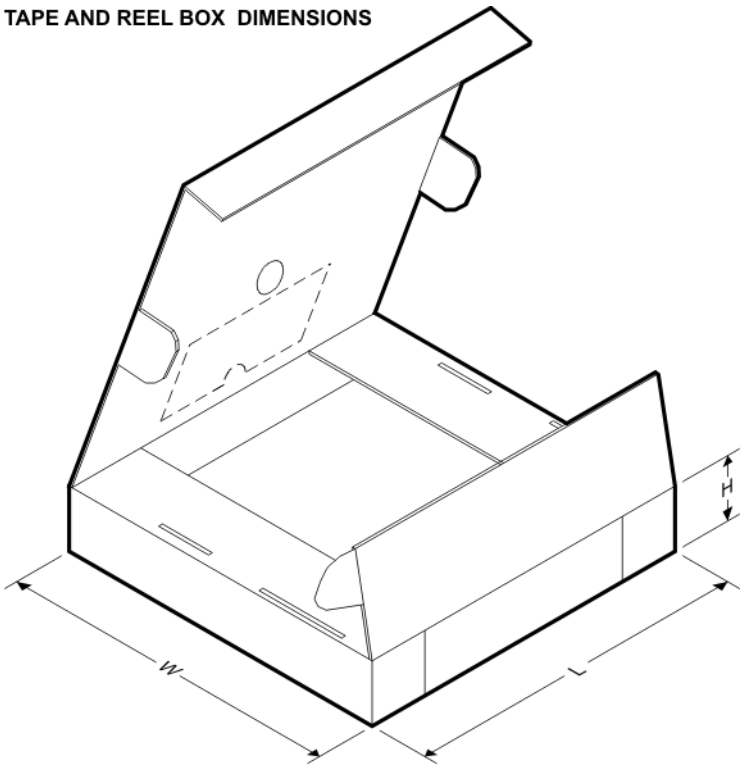
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC29002DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC29002DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC29002DR/1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC39002DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC39002DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

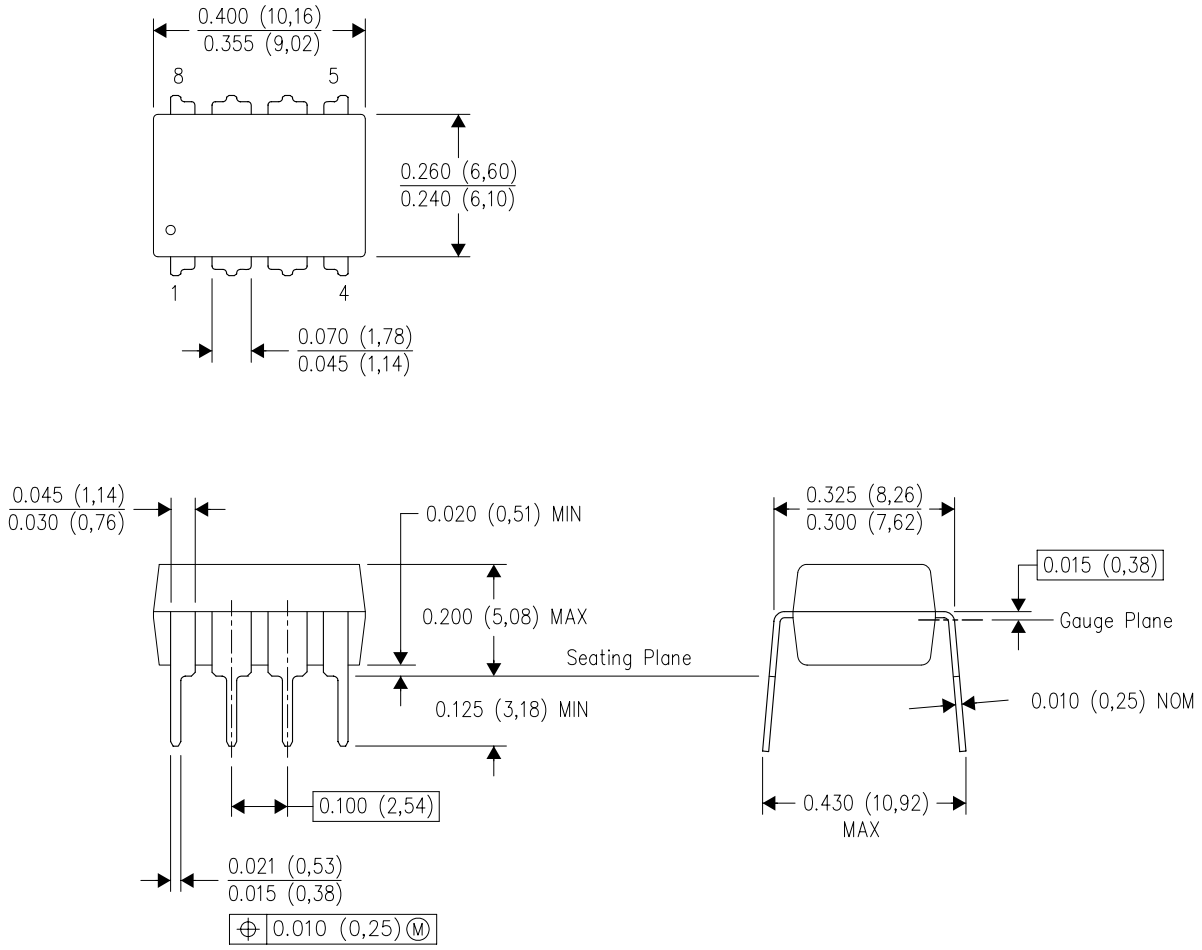
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

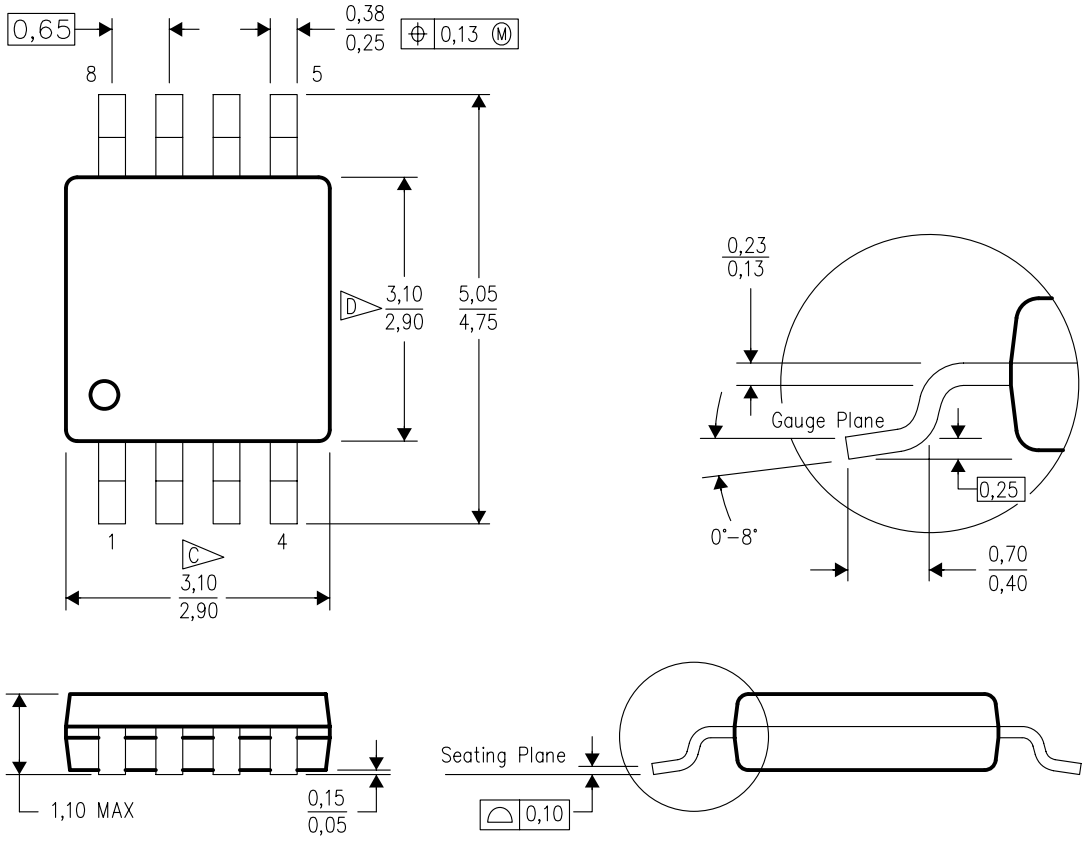
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC29002DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC29002DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC29002DR/1	SOIC	D	8	2500	340.5	338.1	20.6
UCC39002DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC39002DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



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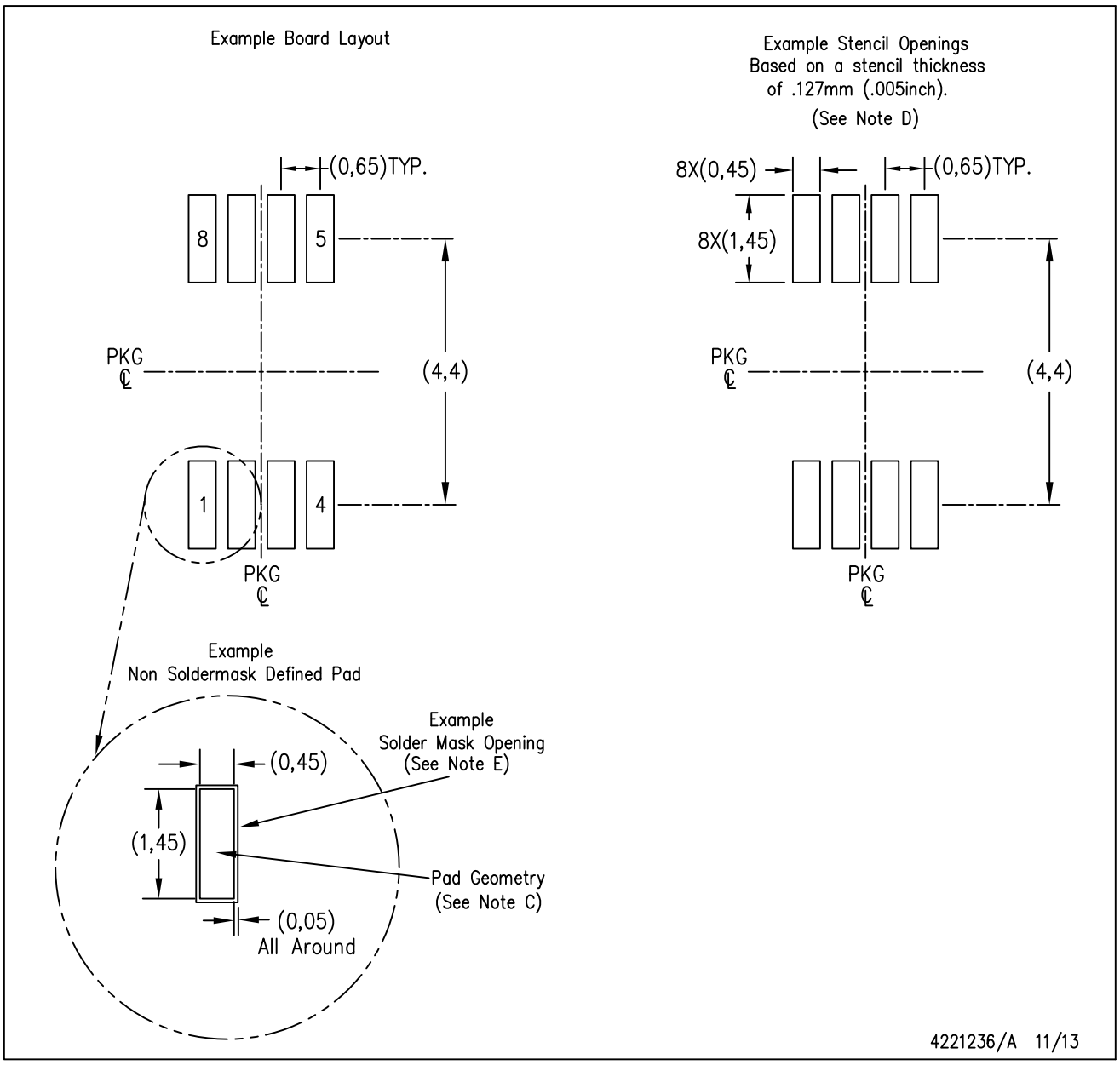
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

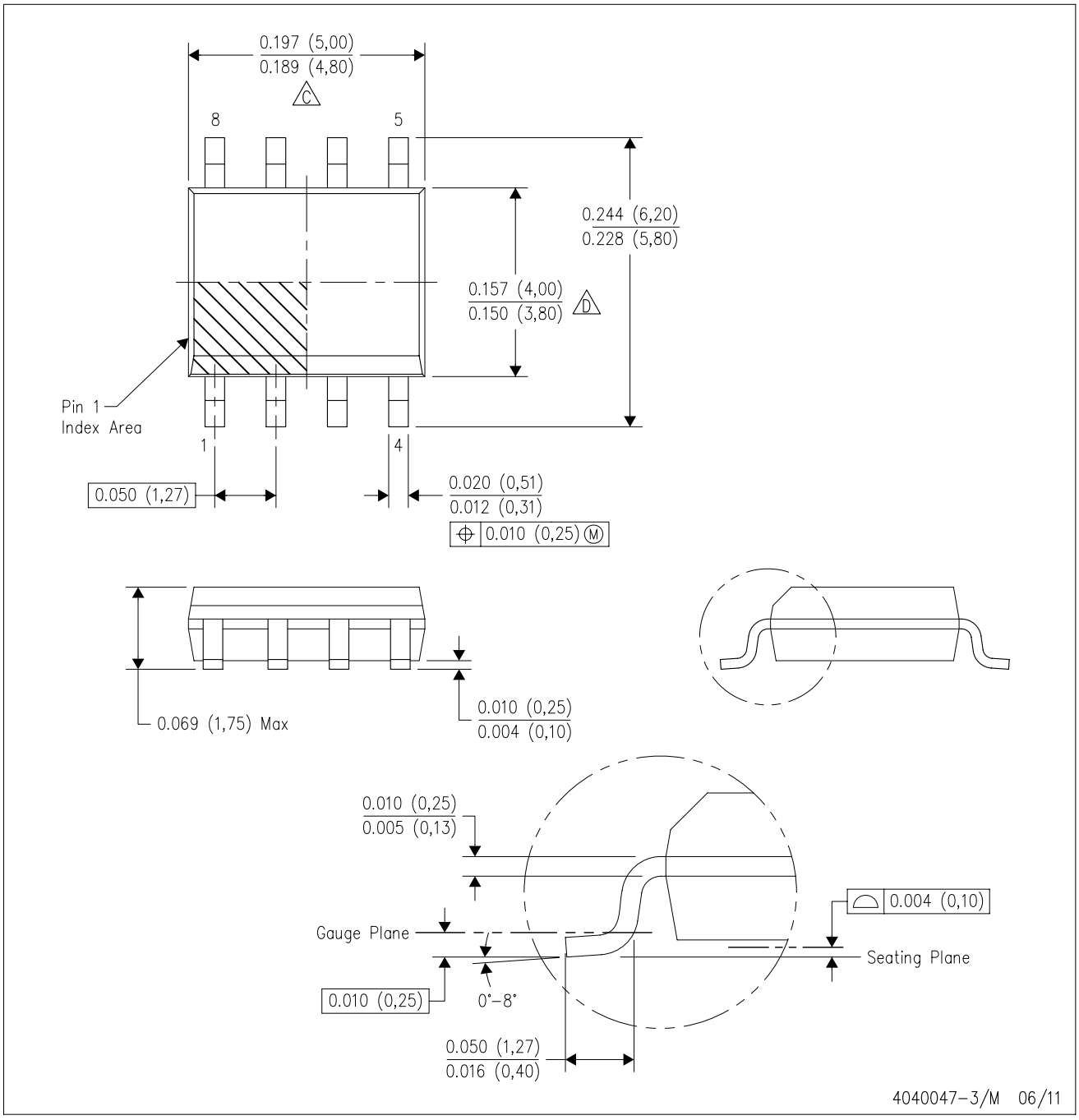
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



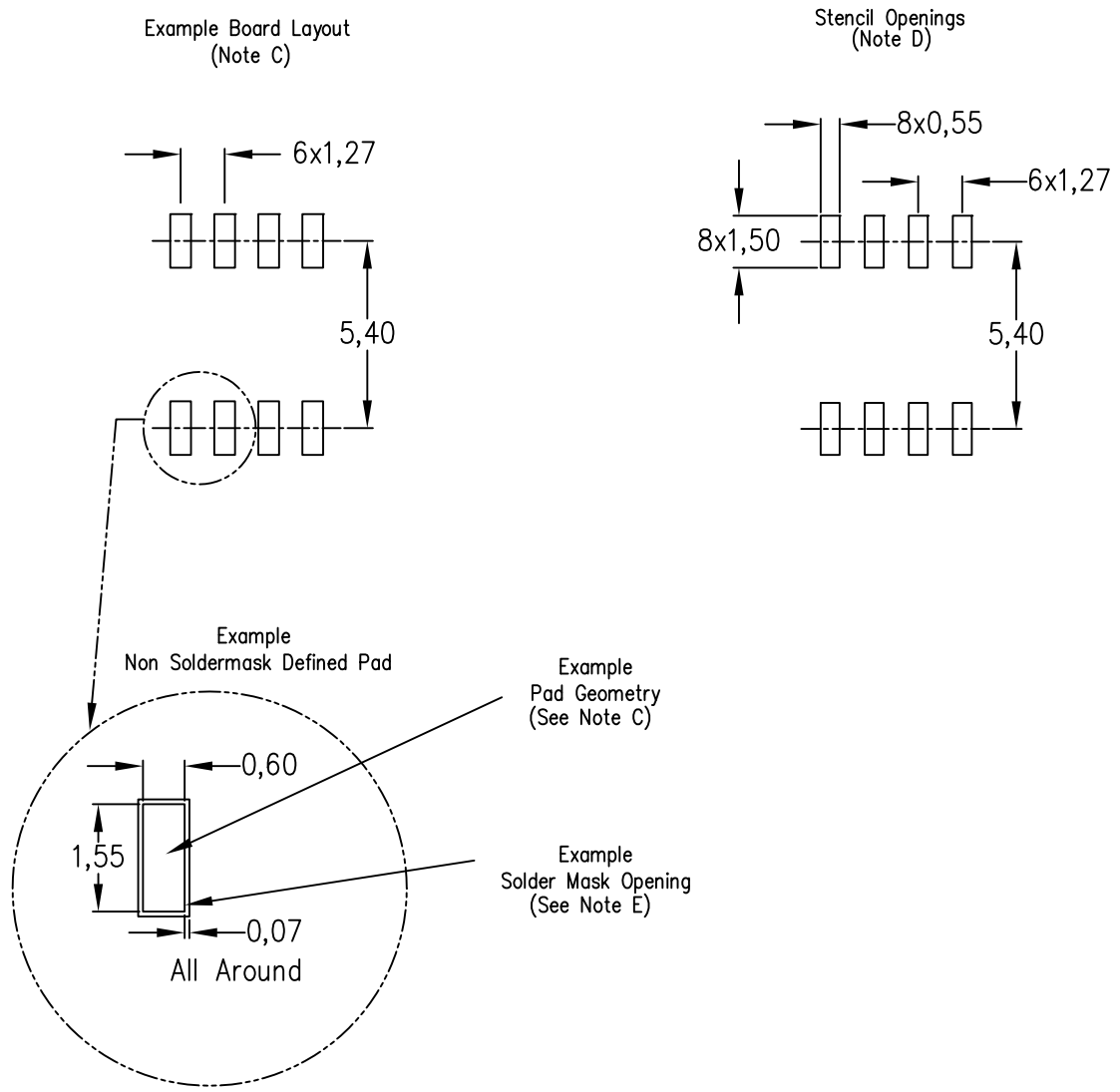
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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