FAIRCHILD SEMICONDUCTOR™

December 2000

QFET™

# FQPF17N08L

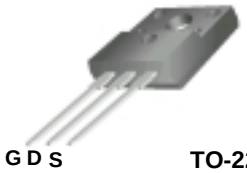
## 80V LOGIC N-Channel MOSFET

### General Description

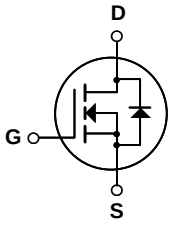
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand a high energy pulse in the avalanche and commutation modes. These devices are well suited for low voltage applications such as automotive, high efficiency switching for DC/DC converters, and DC motor control.

### Features

- 11.2A, 80V, $R_{DS(on)}$ = 0.1Ω @$V_{GS}$ = 10 V
- Low gate charge ( typical 8.8 nC)
- Low Crss ( typical 29 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating
- Low level gate drive requirements allowing direct operation from logic drives




**TO-220F**
**FQPF Series**




## Absolute Maximum Ratings

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | | FQPF17N08L | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 80 | V |
| $I_D$ | Drain Current - Continuous ($T_C$ = 25°C) | | 11.2 | A |
| | - Continuous ($T_C$ = 100°C) | | 7.9 | A |
| $I_{DM}$ | Drain Current - Pulsed | (Note 1) | 44.8 | A |
| $V_{GSS}$ | Gate-Source Voltage | | ± 20 | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 100 | mJ |
| $I_{AR}$ | Avalanche Current | (Note 1) | 11.2 | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 3.0 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 6.5 | V/ns |
| $P_D$ | Power Dissipation ($T_C$ = 25°C) | | 30 | W |
| | - Derate above 25°C | | 0.2 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +175 | °C |
| $T_L$ | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | | 300 | °C |

## Thermal Characteristics

| Symbol | Parameter | Typ | Max | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | -- | 5.0 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | -- | 62.5 | °C/W |

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## Electrical Characteristics

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 80 | -- | -- | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | -- | 0.08 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 80 V, $V_{GS}$ = 0 V | -- | -- | 1 | μA |
| | | $V_{DS}$ = 64 V, $T_C$ = 150°C | -- | -- | 10 | μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1.0 | -- | 2.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 5.6 A<br>$V_{GS}$ = 5 V, $I_D$ = 5.6 A | -- | 0.076<br>0.090 | 0.100<br>0.115 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 25 V, $I_D$ = 5.6 A (Note 4) | -- | 11.4 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | -- | 400 | 520 | pF |
| $C_{oss}$ | Output Capacitance | | -- | 120 | 155 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 29 | 37 | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 40 V, $I_D$ = 16.5 A, $R_G$ = 25 Ω (Note 4, 5) | -- | 7 | 25 | ns |
| $t_r$ | Turn-On Rise Time | | -- | 290 | 590 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 20 | 50 | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 75 | 160 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 64 V, $I_D$ = 16.5 A, $V_{GS}$ = 5 V (Note 4, 5) | -- | 8.8 | 11.5 | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 2.0 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 5.4 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 11.2 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 44.8 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 11.2 A | -- | -- | 1.5 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_S$ = 16.5 A, $dI_F$ / dt = 100 A/μs (Note 4) | -- | 55 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 85 | -- | nC |

**Notes:**
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 1.1mH, $I_{AS}$ = 11.2A, $V_{DD}$ = 25V, $R_G$ = 25 Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 16.5A, di/dt ≤ 300A/μs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

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## Typical Characteristics

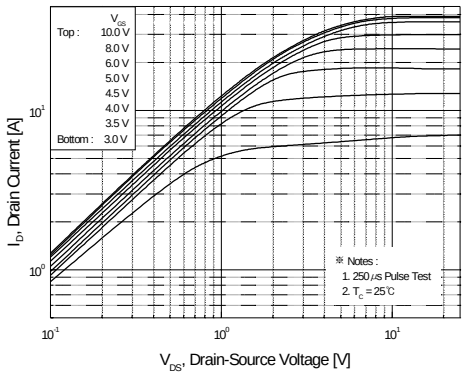



**Figure 1. On-Region Characteristics**

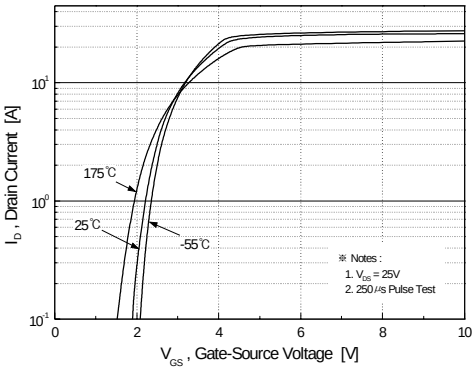



**Figure 2. Transfer Characteristics**

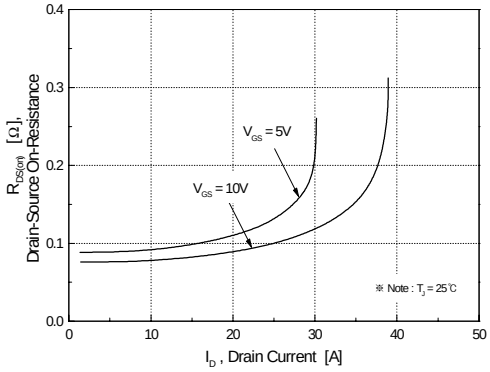



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

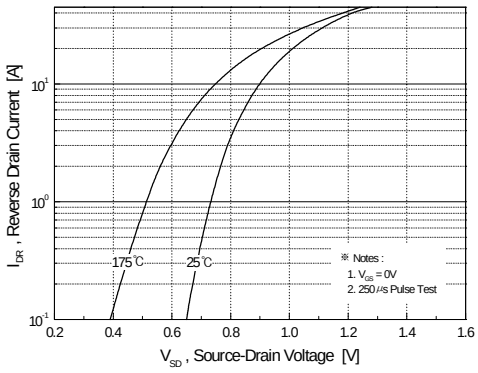



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

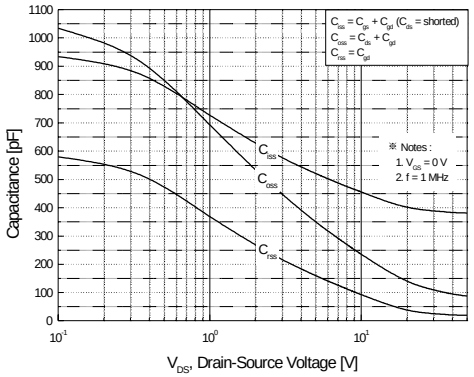



**Figure 5. Capacitance Characteristics**

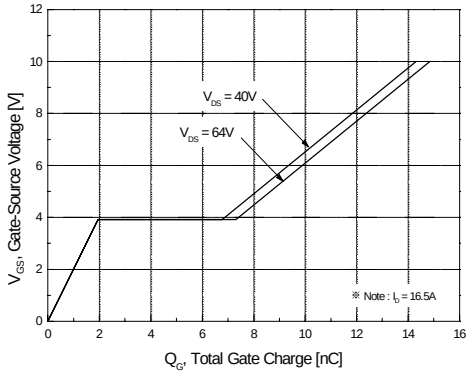



**Figure 6. Gate Charge Characteristics**

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## Typical Characteristics (Continued)

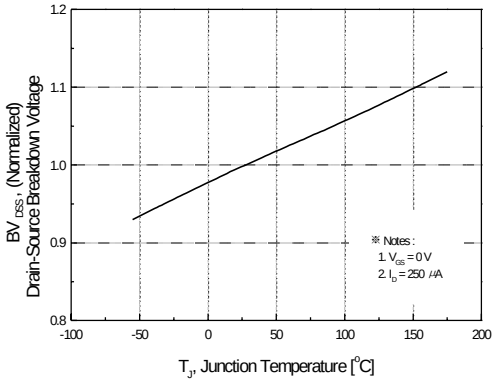



**Figure 7. Breakdown Voltage Variation vs. Temperature**

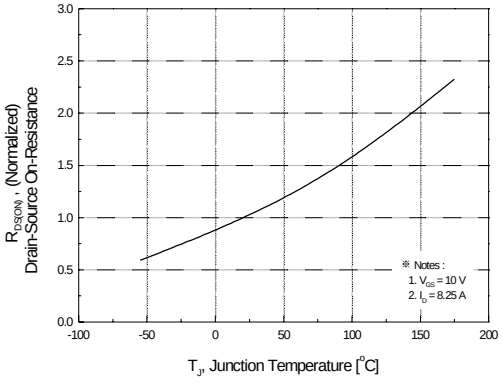



**Figure 8. On-Resistance Variation vs. Temperature**

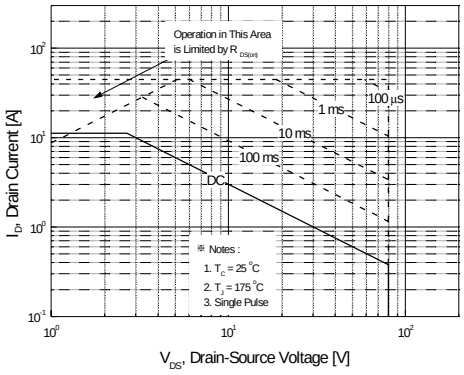



**Figure 9. Maximum Safe Operating Area**

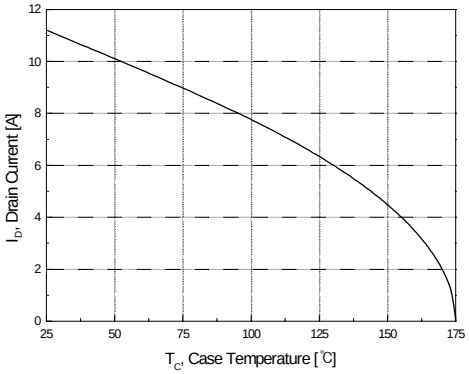



**Figure 10. Maximum Drain Current vs. Case Temperature**

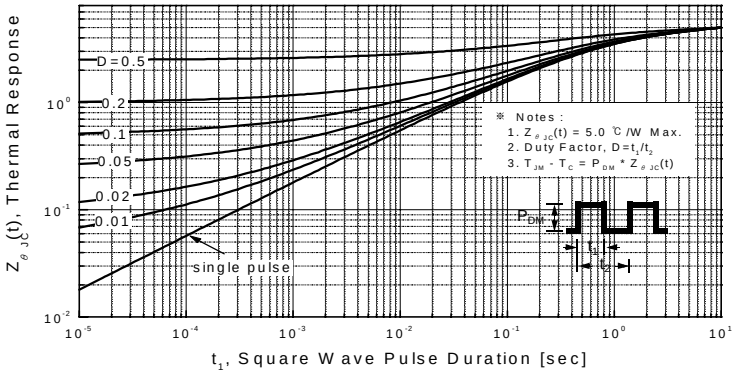
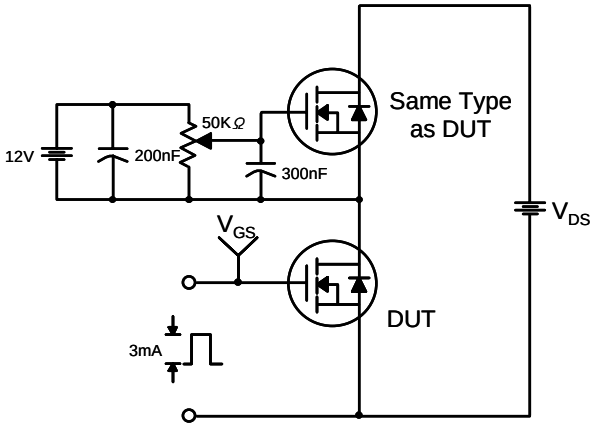
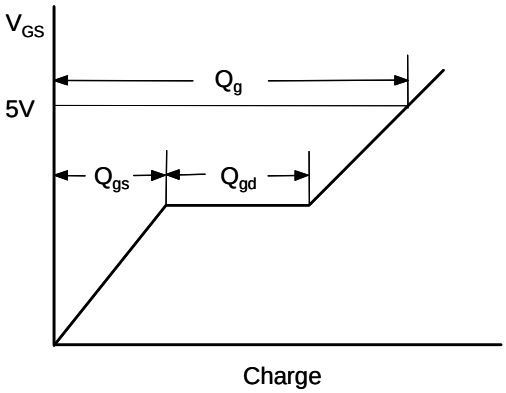



**Figure 11. Transient Thermal Response Curve**

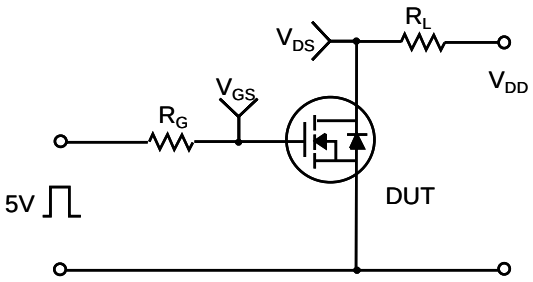
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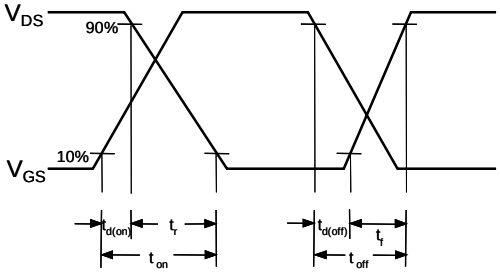
### Gate Charge Test Circuit & Waveform



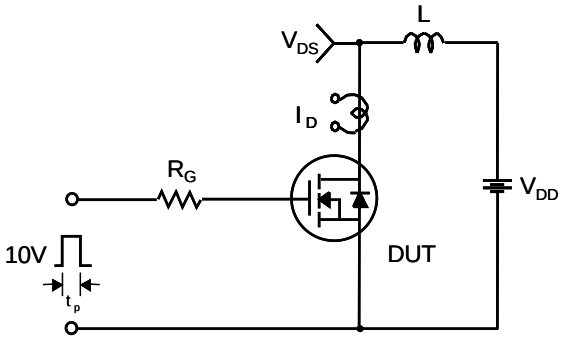




### Resistive Switching Test Circuit & Waveforms

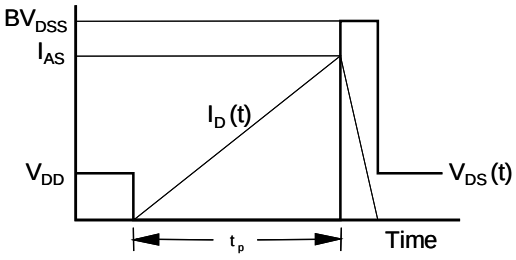



### Unclamped Inductive Switching Test Circuit & Waveforms

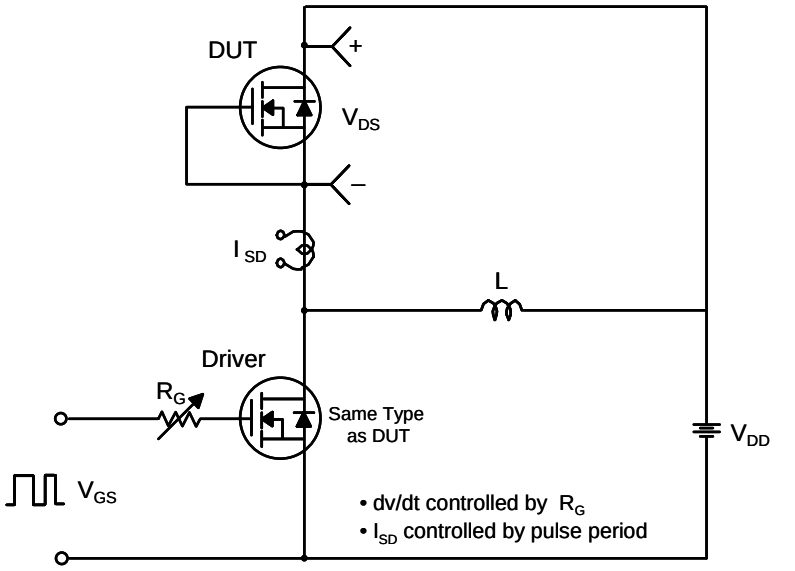


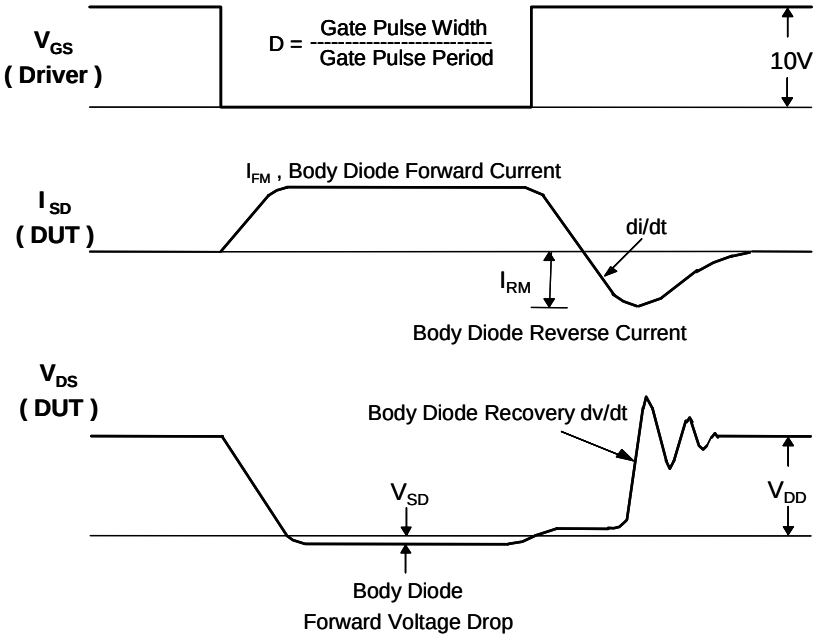

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$




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**Peak Diode Recovery dv/dt Test Circuit & Waveforms**

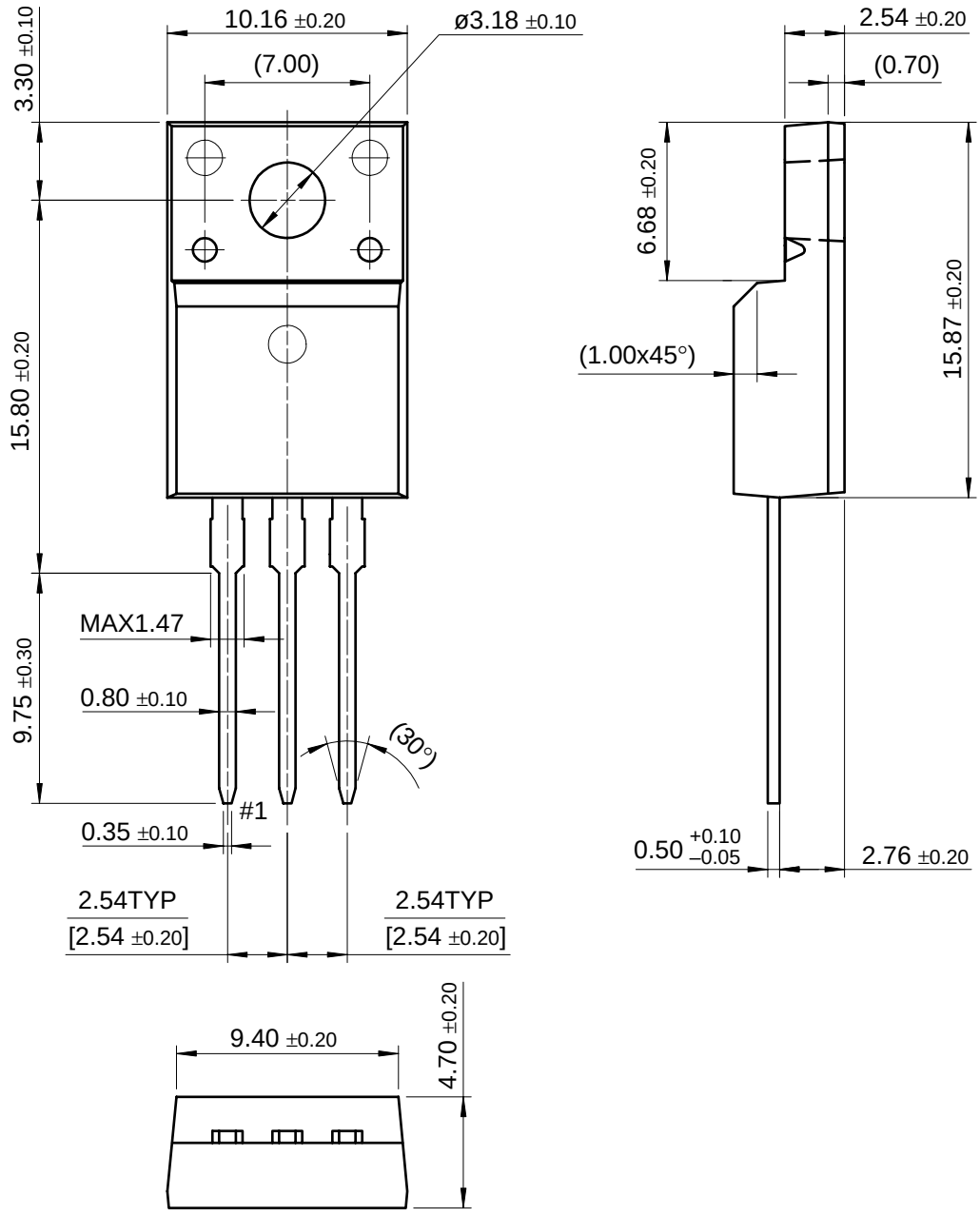



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**Package Dimensions**

# TO-220F




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