

USING THE Si3400 AND Si3401 POE PD CONTROLLERS IN ISOLATED AND NON-ISOLATED DESIGNS

1. Introduction

Power over Ethernet (PoE) is an IEEE standard (IEEE 802.3af) for delivering power through Ethernet cables. 802.3af specifies two options for this as shown in Figures 1 and 2.

The option shown in Figure 1 must be used for "midspan equipment", which injects power on the Ethernet connection of an existing Ethernet link. Endpoint equipment, such as an Ethernet switch, can use either option.

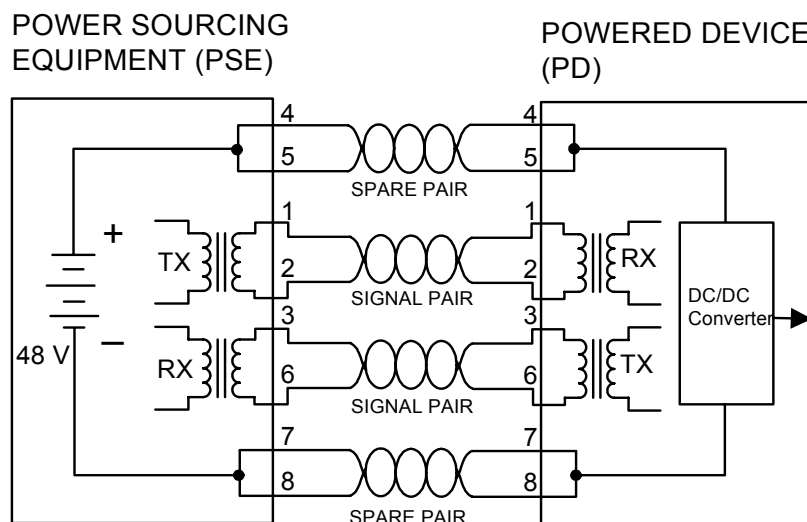


Figure 1. Power Delivered over Spare Pair

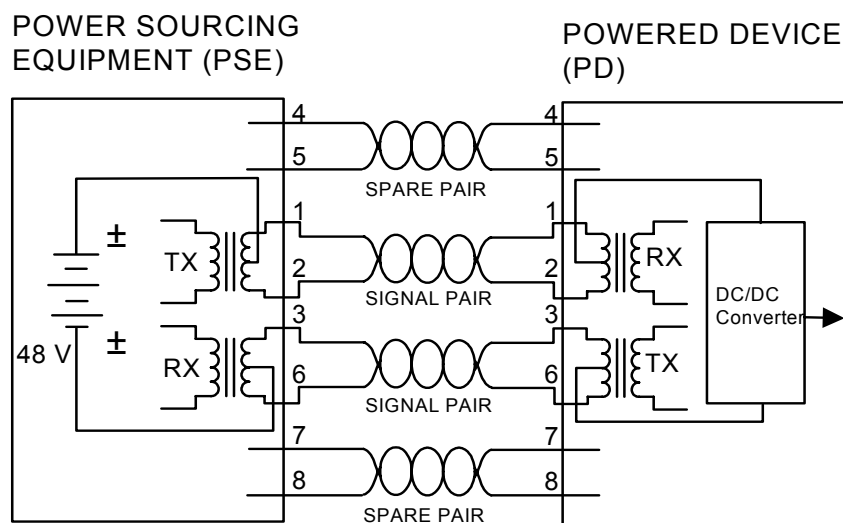


Figure 2. Power Delivered over Signal Pair

AN296

The Power Sourcing Equipment (PSE) supplies 44 to 57 VDC and must be isolated from earth ground. The powered device (PD) must not consume more than 12.95 W, which translates to no more than 350 mA of steady state input current, allowing for 20 Ω of cabling resistance between the PSE and PD. This means that with practical conversion efficiencies, approximately 10 W of regulated power is available to PD devices, making PoE a preferred alternative for powering devices, such as VoIP phones, wireless routers, and security devices, because it eliminates the need for a power source, greatly simplifies installation, and allows easy power backup through an uninterruptible power source (UPS) on the PSE end. The advantages of IEEE 802.3af-compliant equipment include:

- This standard provides a standard way for the PSE to recognize that the PD side is PoE-enabled and not supply power unless a valid signature is detected, thus eliminating the possibility of damaging equipment that is not PoE-enabled.
- This standard provides a method of allowing the 802.3af PD device to supply classification information to the PSE so that the PSE can determine the load requirements of the multiple pieces of PD equipment it is powering.
- This standard ensures interoperability of PSE and PD devices from different manufacturers.

The Si3400/01 is a highly-integrated and efficient PD signature and dc-dc converter integrated circuit. It is fully compatible with 802.3af and has a two-step inrush current-limiting feature to allow PD designs that are compatible with pre-standard PSE equipment. It supports PD designs that require isolation between the Ethernet cables and powered equipment as well as the lower-cost option without isolation for fully-enclosed devices.

This application note covers the basic operation of the Si3400/01 as well as design equations and selection criteria for signature resistors and capacitors, dc-dc converter power train, input filter, output filter, feedback and compensation, soft-start, duty cycle limits, and switcher current limit. The Si3400/01 also feature integrated surge protection, which will be discussed in the final section of this application note.

2. Typical Application Schematics

Figures 3 and 4 show the basic application circuits for the Si3400 and Si3401 evaluation boards.

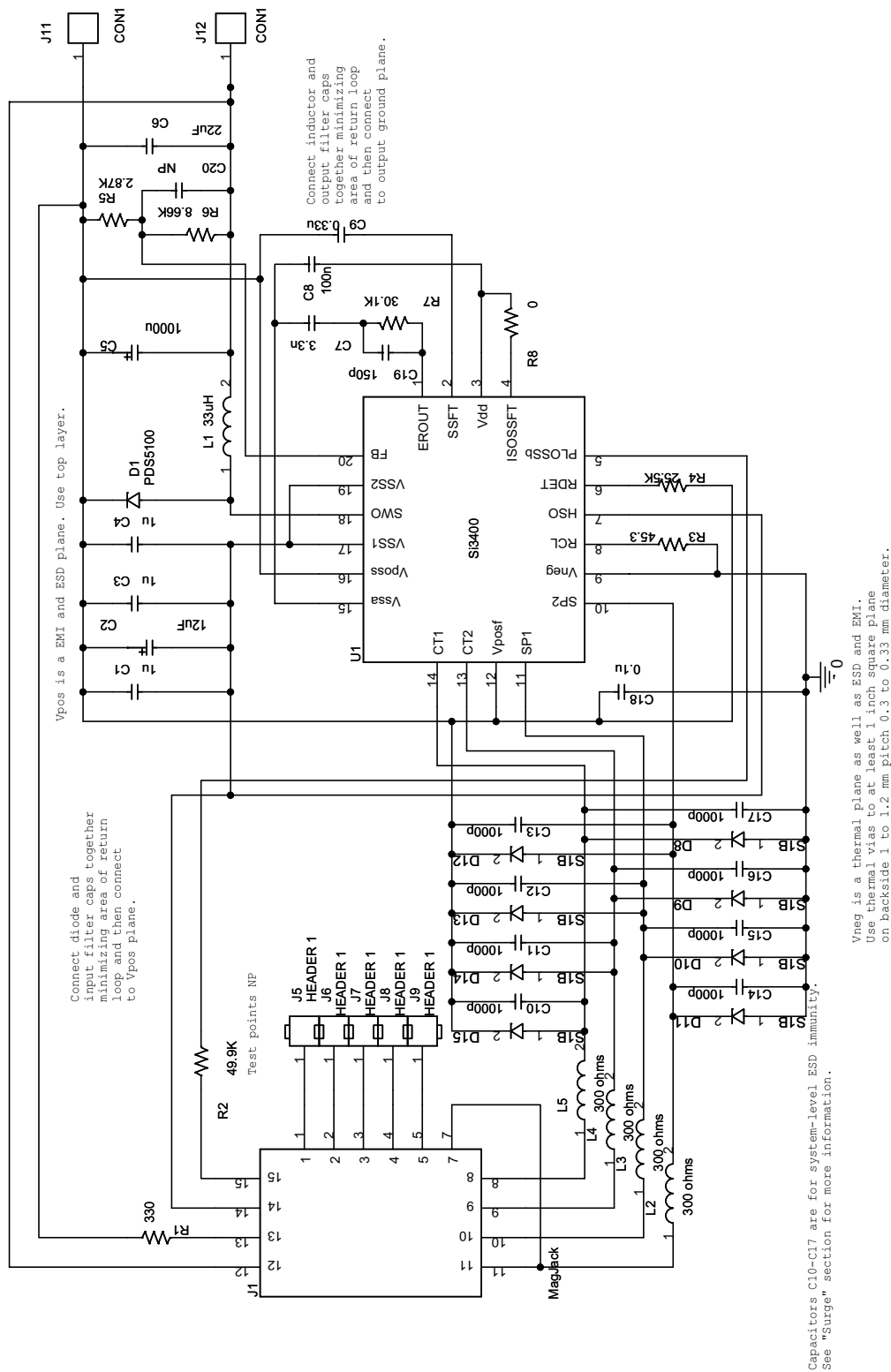


Figure 3. Non-Isolated Buck Configuration for Si3400-EVB and Si3401-EVB (5 V Output)

3. Basic Detection, Classification, and Power Sequencing

The circuit configurations in Figures 3 and 4 have the same operation during detection, classification, and power sequencing. A full power cycle is shown in Figure 5.

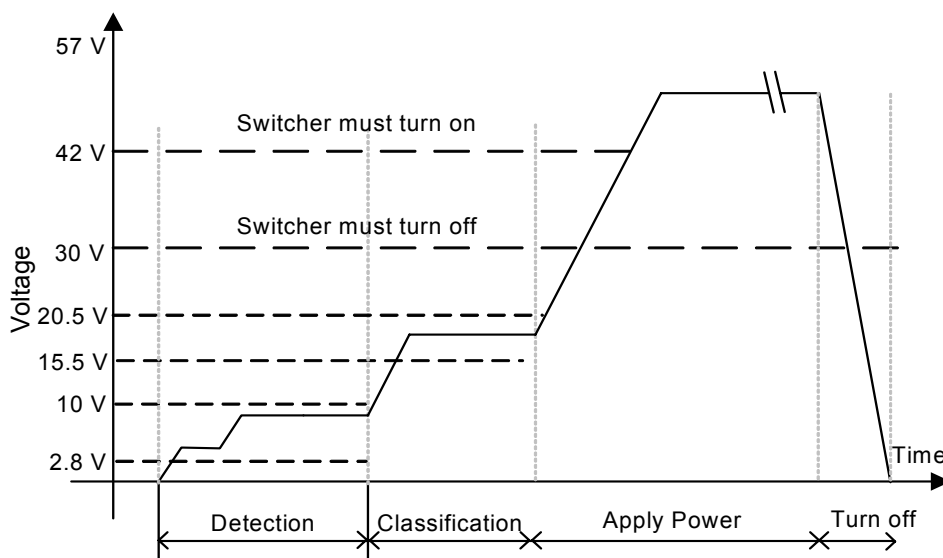


Figure 5. Full Power Cycle

As will be described in more detail below, a low voltage is used to detect a valid PD; a higher voltage is used to classify the power level of the PD, and full power operation starts at a voltage of 42 to 57 V.

3.1. Detection

During the detection phase, the PSE applies two voltages between 2.8 and 10 V dc and measures the current (with a current limit of 5 mA). The slope of the I-V characteristic of the PD must be between 23.75 and 26.25 k Ω . This slope is set by the resistor, RDET (R4 in Figures 3 and 4). Additionally, the input capacitance must be between 50 and 120 nF, which is set by the capacitor, CDET (C1 in Figures 3 and 4).

The low voltage and current applied in the detect phase as well as the requirement for specific values of resistance and capacitance makes it unlikely that non-PoE enabled equipment will be recognized if plugged into PSE equipment that supports PoE.

3.2. Classification

During the classification phase, the PSE applies a voltage between 15.5 and 20.5 V, current-limited to 100 mA, and determines the maximum output power requirement.

Class	Power Level that the PSE Must Support
0	15.4 W
1	4.0 W
2	7 W
3	15.4 W
4	Reserved (Treat as Class 0)

Over the range of 14.5 to 20.5 V, the PD current during the classification stage must be as shown in Table 1.

Table 1. Classification Stage PD Current

Class	Minimum Current	Maximum Current	Units
0	0	4	mA
1	9	12	mA
2	17	20	mA
3	26	30	mA
4	36	44	mA

The classification current for the Si3400/01 is set by the resistor, R_{class} (R3 in Figures 3 and 4).

3.3. Powerup

During detection and classification, the PD must isolate the switcher input filter and not apply power to the load. After completion of this phase, the PSE ramps up to between 44 and 57 V, and PD turns on by closing the internal hot swap switch.

The PD must turn on at an input voltage of 42 V. After turning on, this voltage can drop to 37 V due to cabling resistance.

The Si3400/01 hot swap switch has a two-step current limit. The input filter capacitor is first charged to within about 1.3 V of its final value at a typical current of 150 mA. When the filter input capacitor is nearly charged, the current limit is increased to over 400 mA, and the switcher is allowed to turn on. The hot swap switch operates at the higher current limit as long as the input filter is charged to about 30 V to allow for any switcher startup transients.

The Si3400/01 is designed so that the hot swap switch current limit is generally not the limitation in terms of the amount of power the PD can draw. This limit is intended to be set by the switching regulator and load or by the power sourcing equipment.

However, to limit inrush current as the switcher turns on, the switcher design supports soft-start operation, which is further described in the detailed switcher descriptions of this application note.

Figure 6 shows the input current and output voltage vs. time when 48 VDC is suddenly applied to the PD circuit. The initial current spike is due to the charging of the 0.1 μ F input capacitor. For this particular device, the filter capacitor charges up with a current limit of 108 mA in 17 msec. At this point, the current limit increases, and the capacitor is allowed to fully charge the last 1.3 V, resulting in a brief current spike.

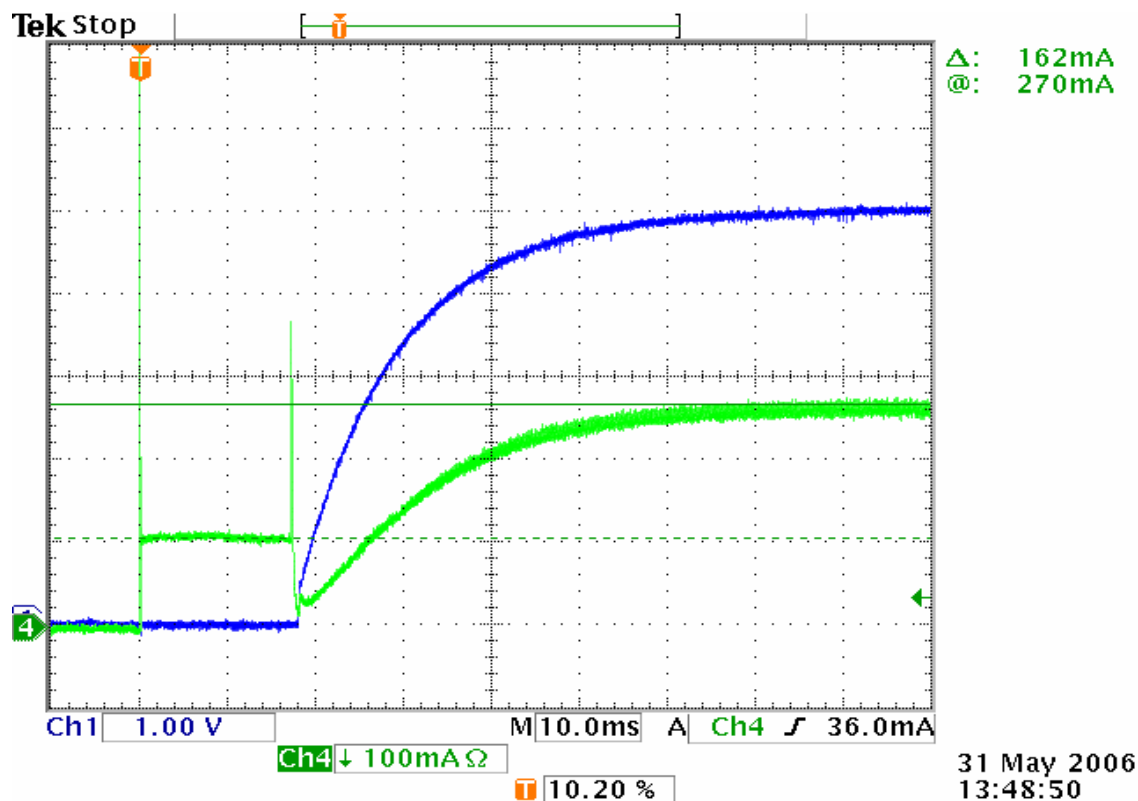


Figure 6. Typical Startup Waveform with 2.5 Ω Load

3.4. Maintain Power Signature

The PSE detects the dc current to the PD by either looking for the low ac impedance of the input filter or making sure that it is drawing current.

For this reason, the input filter capacitor must be >5 μF, and the load must be such that the input current is >10 mA. Since the Si3400/01 is designed to be very efficient and dissipate very little power, there is a minimal load current requirement of 250 mW (50 mA at 5 V output) so as to draw >10 mA from the input supply. It has also been observed that if the switcher is operated with no load, the switcher tends to pulse on and off, which may be undesirable. For this reason, it is recommended that a 250 mW load always be present.

3.5. Turn Off

As the PSE reduces input voltage, the PD is required to turn off at 30 V. Failure to maintain power signature or a system-initiated denial of power to the PD will result in the system cycling back through the detection and classification phases.

The Si3400/01 has approximately 4 V of hysteresis between turn-on and turn-off with respect to the voltage across the switcher input filter capacitor so that inrush current at startup will not cause the part to turn off.

Additionally, the Si3400/01 has an early power loss feature where the voltage on the cable side of the diode bridge is sensed. If this voltage drops to between 25 and 30 V, the power loss signal (PLOSS) is asserted. This allows for early detection of power removal while the switcher input capacitor is still charged.

3.6. Signature Resistors and Capacitors and Component Selection Criteria

The Si3400/01 is designed to meet 802.3af signature requirements with RDET (connected to pin RDET) = 25.5 k Ω , $\pm 1\%$. Recommended resistor values for RCLASS (connected to pin RCL) are listed in Table 2.

Table 2. RCLASS Recommended Resistor Values

Class	Power Level that the PSE Must Support	RCLASS $\pm 1\%$
0	15.4 W	Open circuit
1	4.0 W	127 Ω
2	7 W	69.8 Ω
3	15.4 W	45.3 Ω
4	Reserved—treat as Class 0	30.9 Ω

The voltage across these resistors is limited so that 0603 or larger surface mount resistors may be used.

CSIG should be a 100 V X7R type surface mount with tolerance of $\pm 10\%$. While this type of capacitor exhibits a strong voltage and temperature dependence, the 50–120 nF requirement of 802.3af will be met.

3.7. Input Filter

802.3af requires that the input filter capacitor be greater than 5 μF . Additionally, the ripple at the RJ-45 input at the switching frequency of approximately 350 kHz must be less than 150 mV. To reduce the chance of conducted or radiated emissions due to induced common-mode voltage on the Ethernet cable pairs, it may be desirable to further reduce the input ripple.

To maintain the $>5 \mu\text{F}$ input capacitance, an aluminum electrolytic capacitor, such as a Sanyo 100ME12AX or Panasonic EEUFC120, is used. This capacitor has an ESR of up to 0.4 Ω and results in excessive input ripple because of the ripple current from the switcher, which can be as much as 3 A. To keep input ripple down, it is recommended that additional X7R surface mount capacitors be used in parallel (for example, a 1 μF , 100 V, X7R 1210 capacitor with an ESR of less than 0.6 Ω is available from several vendors).

As will be explained in the section about surge protection, the input filter capacitor also helps absorb surge current. If the input capacitor is too large, the reaction time of the hot swap switch current limit function increases. An input filter capacitor of 15 μF total has been found to be a good compromise.

4. DC-DC Converter Operation

There are two basic configurations for the dc-dc converter: buck and flyback. Additionally, the converter may be designed so that its power output is electrically isolated from the power input. Isolation is required per IEEE 802.3af when the PD does not provide the isolation.

In the non-isolated case, the buck topology is generally used, and, in the isolated case, the flyback topology is generally used. It is possible to use the flyback topology in the non-isolated case, although this is not described in detail in this application note.

The equations used for determining all of the components surrounding the switching converter are briefly described below. A spreadsheet utility has also been developed to enable easy calculations of component values.

4.1. Non-Isolated Buck Design

Under most conditions, the current through the inductor (L1 in Figure 3) is continuous, and the voltage across the inductor switches from positive to negative as shown in Figure 7.

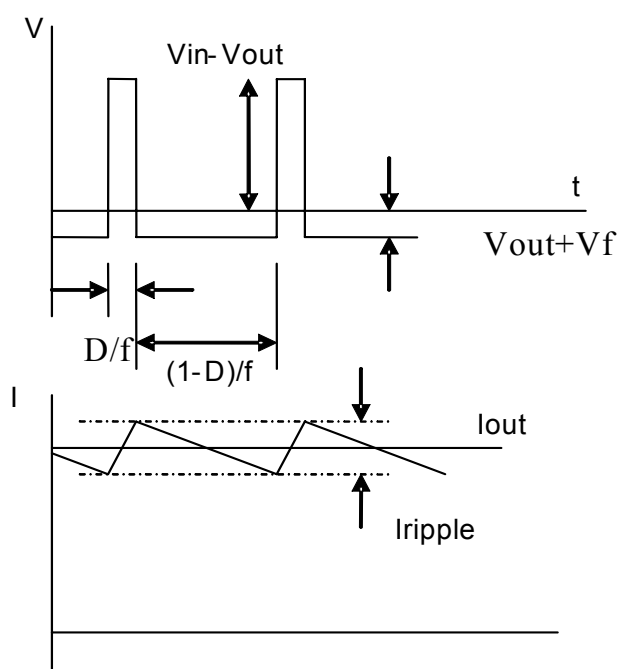


Figure 7. Voltage Polarity

The average voltage across the inductor must be zero; so, the duty cycle is:

$$D \times (V_{in} - V_{out}) = (1 - D) \times (V_{out} + V_f)$$

Where V_{out} is the desired output voltage; V_f is the forward drop of the diode (D1 in Figure 3), and V_{in} varies with the PD input voltage, which is generally 42–55 V. Solving:

$$D = \frac{(V_{out} + V_f)}{(V_{in} + V_f)}$$

The ripple current that has to be supported in the output filter is:

$$I_{ripple} = \frac{(V_{in} - V_{out}) \times (V_{out} + V_f)}{((V_{in} + V_f) \times L \times F)}$$

AN296

Where L is the inductance.

$$L = 33 \mu\text{H}, V_{\text{out}} = 3.3 \text{ V}, V_{\text{in}} = 55 \text{ V}, V_f = 0.7 \text{ V}$$

F is the internally-set switch frequency of approximately 350 kHz.

$$I_{\text{ripple}} = 321 \text{ mA}$$

This is the ripple current into the output filter. The peak-to-peak ripple current that must be handled by the input filter is equal to the average current delivered to the output plus half of the ripple current in the inductor.

The rectifier diode in the non-isolated design must be rated for at least the input voltage. Generally, a 100 V diode is chosen for margin. A Schottky diode is preferred to avoid the large voltage drop and excess power associated with stored charge. Typical part numbers are PDS5100 from Diodes Incorporated or the equivalent UPS5100 from Microsemi. Note that these 100 V diodes have a larger forward drop than the lower voltage diodes used for the non-isolated design below.

Overall efficiency is determined by dividing the output power by the input power including conduction losses in the inductor, rectifier, switching FET, input bridge, and hot swap switch, as well as bias and switching losses.

4.1.1. Output Voltage—Non-Isolated Design

The output voltage in the isolated case is determined by R3 and R4 according to the following equation:

$$V_{\text{out}} = 1.23 \times \left(1 + \frac{R6}{R5} \right)$$

For example, for a 5 V output, values of 8.66 k Ω for R6 and 2.87 k Ω for R5 are recommended.

4.1.2. Output Filter and Loop Stability—Non-Isolated Design

Generally, the current in the output inductor is continuous (does not return to zero). The current becomes discontinuous for very light loads, but the continuous mode of operation is most difficult to stabilize due to the LC filter resonance that occurs in this case.

The output filter section has a resonant frequency described by the following equation:

$$\frac{1}{2 \times \pi \times \sqrt{LC}}$$

The circuit will be critically damped with a resistance of:

$$2 \times \sqrt{\frac{L}{C}}$$

For a typical 33 μH inductor and 1000 μF filter cap, the resonant frequency is 876 Hz, and the resistance for critical damping is 0.36 Ω .

The damping resistance is a combination of capacitor ESR, inductor series resistance, and switch and diode resistance. It has been found that the combination of switcher FET resistance and Schottky diode effective series resistance results in an effective 0.5–1 Ω in series with the inductance for the recommended applications circuit. This damps the output resonance and allows for the use of low ESR filter capacitors without stability concerns.

The error amplifier is a transconductance type amplifier with $g_m = 50 \text{ mmho}$. Capacitor C_c provides roll-off of the loop gain at

$$F = \frac{g_m}{2\pi C_c} \times \frac{V_{\text{IN}}}{1.5 \text{ V}}$$

where 1.5 V is the voltage swing at ER_{OUT} that would vary the duty cycle from zero to 100%.

A typical V_{IN} of 50 V and C_c of 3.3 nF gives a crossover at 8 kHz, ignoring the output filter.

The network of R_c and C_c stabilizes the feedback loop by introducing a zero in the feedback loop. It has been found that values of 3.3 nF (C_7 in Figure 3) and 30.1 k Ω (R_7 in Figure 3) work well. This translates to a zero at 1.6 kHz. Finally, the 150 pF capacitor (C_{19} in Figure 3) gives a pole at 35 kHz for the final gain rolloff. With these values, a typical Bode plot is shown in Figure 8.

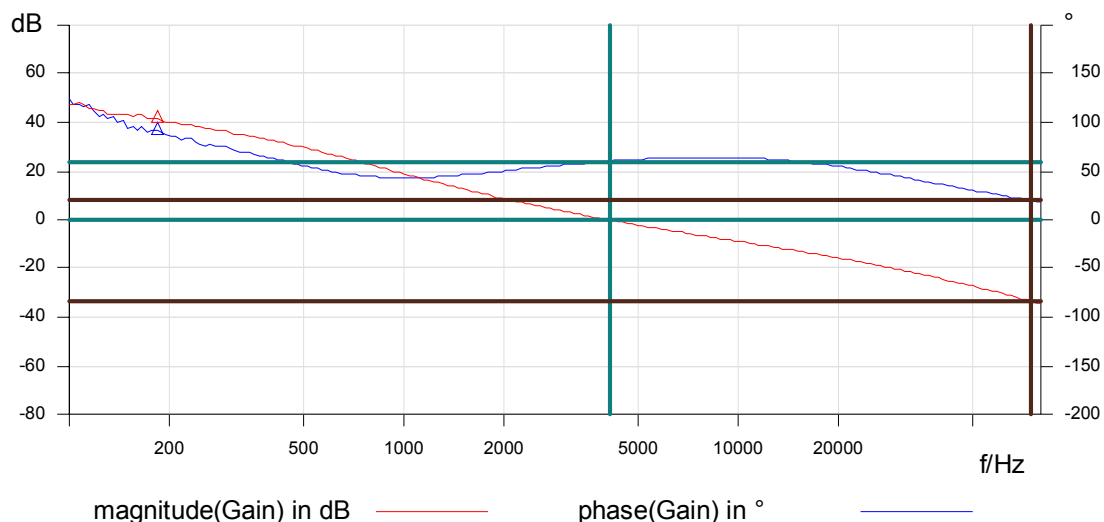


Figure 8. Typical Bode Plot

While this is a very conservative design, there is quite a bit of variation in the output capacitor value and ESR, particularly with temperature. For designs that must operate below 0 °C, it has been found that a low ESR 560 μ F capacitor such as the Panasonic EEU-FM0J561 gives better results with the same stability network.

4.1.3. Soft Start Non-Isolated Case

In the non-isolated case, capacitor C_{SS} (C_9 in Figure 3) acts to allow the duty cycle of the switcher FET to gradually increase. There is an internal impedance of 50 k Ω in the Si3400/01 that works in combination with C_{SS} to slowly ramp the reference voltage to the error amplifier. A typical C_{SS} of 0.33 nF gives a soft-start time constant of 10 ms, which is a good value for a 1000 μ F output filter capacitor. A typical startup waveform with a 2.5 Ω load is shown in Figure 5 on page 5.

4.2. Isolated Flyback Design

For the isolated design, a flyback transformer approach is used. In a flyback transformer, the primary inductance is "charged" when the main switcher FET turns on, and the energy stored in this inductance is delivered to the secondary when the switcher FET turns off. This type of circuit may be designed to operate in either the continuous or discontinuous mode. In the continuous mode, current always flows in either the transformer primary or secondary. In the discontinuous mode, the secondary current drops to zero before the next cycle of primary current. Typical waveforms are shown in Figure 9.

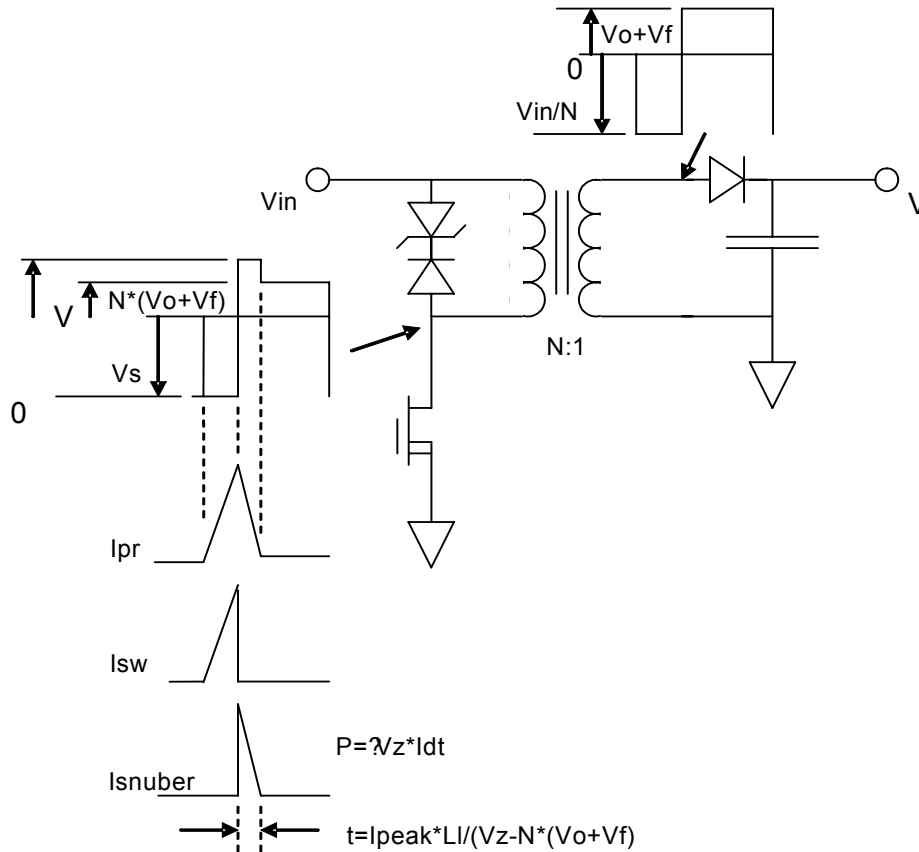


Figure 9. Typical Waveforms

A transformer with a turns ratio of N:1 is used to help reduce peak currents.

In the discontinuous mode, the output power, $I_0 \times V_0$, must be supplied by the $\frac{1}{2} \times LI^2$ energy stored in the transformer with some margin for switching losses. If ϵ is the margin for switching losses (typically 90%), then:

$$P_0 = I_0 \times V_0 = \frac{1}{2} \times I_p^2 \times L_m \times f \times \epsilon$$

Where P_0 , I_0 , and V_0 are output power, current and voltage, and I_p , L_m , and f are transformer primary peak current, magnetizing inductance, and operating frequency.

The portion of the switching waveform where the FET is on d_1 is:

$$d_1 = I_p \times L_m \times \frac{f}{V_p}$$

Where V_p is the input voltage.

The time, d_2 , where current flows in the secondary is:

$$d_2 = V_p \times \frac{d_1}{(N \times (V_0 + V_f))}$$

Where V_0 is the output voltage (plus diode drop), and N is the transformer turns ratio.

Solving with the constraint that $d_1 + d_2 = 1$ gives the following:

$$I_0 = \left[\varepsilon \times \frac{V_0 + V_f}{(2 \times f \times L_m)} \right] \times \left[\frac{N}{\left(1 + N \times \frac{(V_0 + V_f)}{V_p} \right)} \right]^2$$

For a given power transformer magnetizing inductance, turns ratio, output voltage, frequency, and input voltage, this gives the output current at which the current becomes continuous and always flows in either the transformer primary or secondary.

$L_m = 40 \mu\text{H}$ gives a good compromise between transformer size (larger L_m gives a larger transformer) and peak current (larger L_m gives smaller peak current at the input and output).

Plugging in $V_0 + V_f = 4 \text{ V}$, $V_p = 48 \text{ V}$, $N = 4$, $L_m = 40 \mu\text{H}$, $\varepsilon = 0.9$, and $f = 380 \text{ kHz}$ gives:

$$I_0 = 0.68 \text{ A}$$

Above this current, the transformer current becomes continuous in that there is always current flow in either the transformer primary or secondary.

For larger output current, the duty cycle stays fairly constant at

$$D = N \times \frac{(V_0 + V_f)}{(V_p + N(V_0 + V_f))}$$

In the continuous mode, the average current while the switcher FET is on is determined by setting the average input power after an efficiency, ε , to equal the average output power:

$$I_{\text{avg}} \times V_p \times \varepsilon \times D = I_0 \times (V_0 + V_f)$$

In this mode of operation, there is a change in primary current while the FET is on

$$\Delta I = \frac{V_p \times D}{(L_m \times f)}$$

The peak current that the transformer must handle is

$$I_{\text{peak}} = I_{\text{avg}} + \frac{\Delta I}{2}$$

For the same transformer above with $I_0 = 3 \text{ A}$, the peak transformer current is 1.85 A.

Increasing the turns ratio decreases peak current, particularly on the primary side. However, the secondary voltage is reflected back to the primary, and the increased turns ratio also increases the voltage on the switcher FET. Additionally, transformer leakage inductance causes an additional spike of voltage on the switcher FET, which must be clamped by a snubber.

The FET maximum drain voltage is 80 V, and the maximum voltage at V_{pos} is about 55 V; so, the snubber must clamp to 25 V.

A Zener diode and fast recovery diode are recommended to clamp the output at less than 25 V above V_{POS} .

Increasing the turns ratio will increase snubber power. Therefore, there is an optimal turns ratio that compromises between high peak current at a low turns ratio and high snubber power at a high turns ratio.

Silicon Laboratories, Inc. has partnered with Coilcraft to develop flyback transformers that are optimized for maximum efficiency of the Si3400/01 at 3.3, 5, and 12 V output. Recommended part numbers are FA2924-AL for 3.3 V (40 μ H and 1:0.3 turns ratio), FA2805-CL for 5 V (40 μ H and 1:0.4 turns ratio), and FA2925-AL for 12 V (40 μ H and 1:1 turns ratio). Contact Silicon Laboratories for other output supply configurations and recommendations.

The rectifier for 3.3 or 5 V output does not need as high a voltage rating because the transformer turns ratio limits the reverse voltage to $(1/N) \times V_{in}$. The PDS1040 from diodes incorporated or the equivalent UPS1040 from Microsemi can be used, and these parts have much lower forward drop and overall loss due to their lower voltage rating of 40 V. For 12 V output, the PS5100 is recommended.

4.2.1. Output Voltage—Isolated Design

In the isolated design, a TLV431 (U5 in Figure 4) is used as an isolated reference voltage. The TLV431 is available from many suppliers and regulates at a reference voltage of 1.24 V; so, the output voltage is:

$$V_{out} = 1.24 \times (1 + R5/R6)$$

An opto-isolator, such as PS2911 (U6 in Figure 4), which is also available from many suppliers, is used to couple the error signal back to the Si3400/01.

4.2.2. Output Filter and Loop Stability—Isolated Design

In the flyback design, even if the transformer current always flows in the transformer primary or secondary (i.e. is continuous), the secondary current does not flow during the time that primary current flows; thus, there is always a large ripple current in the output that must be filtered. For the isolated design, it is recommended that a pi-section filter be used with a 1.0 μ H inductor, such as Coilcraft D01608-102ML.

The feedback compensation for the isolated case was chosen to be type 3 for improved load transient response. The initial pole in the feedback path is determined by the Miller multiplied capacitance of C9 working against the R8 plus Thevin equivalent resistance of the voltage sense divider R5//R6.

$$\text{Pole} = 1/(2 \times \pi \times C9 \times \text{TLV431 gain} \times (R5 \times R6)/(R6 + R6) + R8)$$

A typical value of R8 in parallel with R6 is 9.16 k Ω , TLV431 gain = 700, and C41 = 15 nF. These values set this pole at about 0.8 Hz. Variations in the TLV 431 gain increase open loop gain and decrease the pole value so that the roll-off from this pole tends to be independent of TLV431 gain.

The overall design is that the C9-R8 zero compensates the R11-C21 pole so:

$$C9 \times R8 \text{ approximately} = R11 \times C21$$

The double zero for phase margin is determined by C21-R12 and C8 against the Thevin equivalent impedance of R5//R6. Recommended values of C8 = 560 pF and R12 = 100 Ω put the double zero at about 7 kHz. A final pole determined by C8 and R9 at 95 kHz eliminates high-frequency gain peaking. Typical Bode plots are shown in Figure 10 for the continuous case.

This compensation results in the load transient response of Figures 11 and 12 for a worst-case load transient that starts at very light load (discontinuous case) and ends with a heavy load (continuous case). Further optimization of this result is possible with larger or lower ESR output filter capacitors.

4.2.3. Soft Start Isolated Case

For the isolated case, a capacitor is connected between pin ISOSSFT and V_{SS} . A typical value is 1.0 μ F. This feature is available beginning with Rev. E silicon. Silicon Labs does not recommend disabling isolated soft start. For revisions before Rev. E, tie this pin to V_{DD} .

A typical trace of isolated mode start-up is shown in Figure 13.

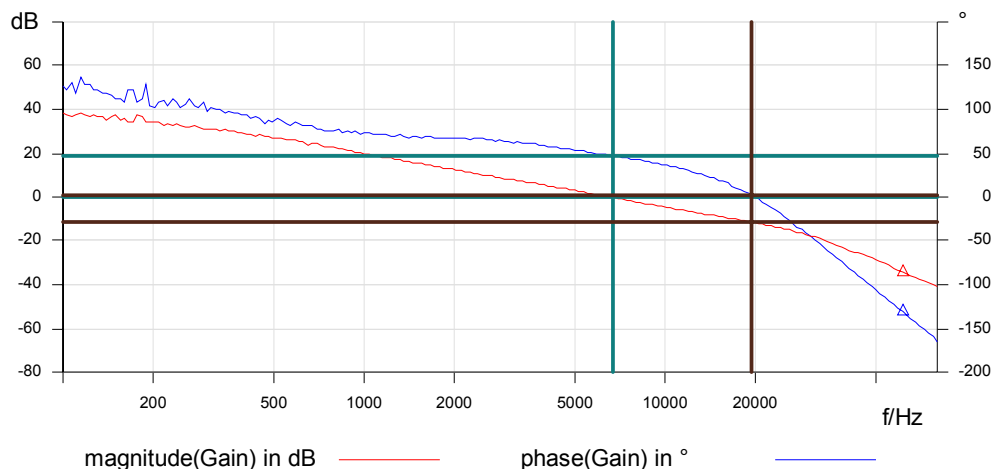
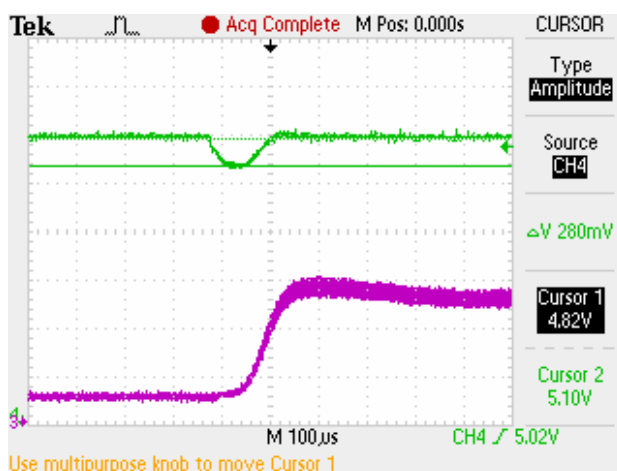
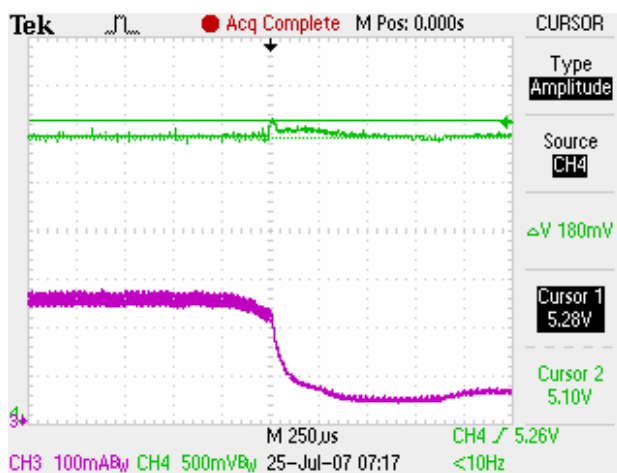


Figure 10. Continuous Mode



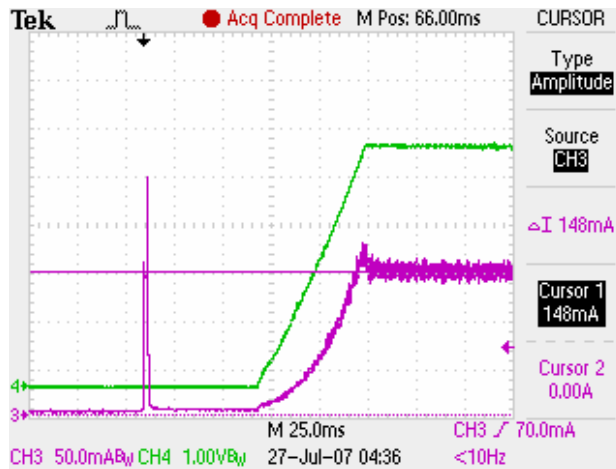
Note: Upper trace is output voltage at 500 mV/div (5 V nominal) and lower trace is input current at 100 mA/div.

Figure 11. 2.5 W Load to 10 W Load



Note: Upper trace is output voltage at 500 mV/div (5 V nominal) and lower trace is input current at 100 mA/div.

Figure 12. 10 W Load to 2.5 W Load



Note: Input current at 50 mA/div and output voltage at 1 V/div.

Figure 13. Isolated Mode Startup with 5 W Load

5. Surge

The Si3400/01 has an input clamp that will protect it against surges as spelled out in IEEE 802.3af.

IEEE 802.3af specifies a 1000 V surge with 0.3 μ sec rise time and 50 μ sec fall time applied to each conductor through a series resistance of 402 Ω . Because this pulse is generally applied to all conductors, the differential current at the input is generally very limited. The Zener clamp itself can withstand about 1 A of surge for 50 μ sec.

The Si3400/01 is designed to handle a 50 μ sec, 5 A pulse that would result from applying the surge to either both Tx or Rx pairs and grounding the other pair. This is accomplished by turning on the hot swap switch while disabling the switcher if current flows in the input clamp. During the 50 μ s transient, a large portion of the input energy is redirected to the switcher input capacitor. For this reason, a 15 μ F minimum input capacitor is recommended.

The Si3400/01 is also required to survive the application of telephony ringing voltage. 802.3af specifies 56 V dc + 175 V peak ringing applied through 400 Ω source impedance at a frequency of 20 to 60 Hz. In this case, the switcher could turn on during the ringing application, which would be very undesirable and could cause damage to the switcher FET. To prevent this from happening, the switcher is actively shut down when there is any current >1 mA flowing through the clamp.

Continuous application of such a large ringing signal will damage the Si3400/01 (although it will not cause a safety hazard). However, such a large ringing signal should also cause a "ring trip" or apparent off-hook indication at the central office within 200 msec. It has been found that the Si3400/01 can withstand application of telephony ringing for over one second before damage occurs; so, in general, telephony ringing will not cause damage.

Refer to "AN315: Robust Electrical Surge Immunity for PoE PDs through Integrated Protection Output" for more information on surge test immunity results.

In some applications, up to 16 kV of system-level ESD immunity is required. The standard Si3400/01 EVB designs meet this requirement when the input is not powered. However, when the input is powered and the Si3400/01 is producing an output through the dc-dc converter, damage may occur to the input diode bridges for ESD events above 4 kV when applied to the output terminals if C10 to C17 are not used. Capacitors C10 to C17 allow passing system-level ESD events in excess of 16 kV.

For isolated applications that require a high level of system-level ESD immunity, the capacitors are recommended. For non-isolated applications, it is generally not possible for an ESD event (at the output supply) to occur because the output terminals of the dc-dc converter are generally not accessible while input power is applied. However, even for non-isolated designs, there is a possibility large ESD events may reach the power supply terminals, in which case capacitors (C10 to C17) are also recommended.

6. Use with an Auxiliary Power Supply

In some applications, it is desirable to be able to use either the power from the RJ45 Power over Ethernet or from a low-cost auxiliary power supply. This is very easy to do with the Si3400/01, and a 48 V auxiliary supply is shown in Figure 14.

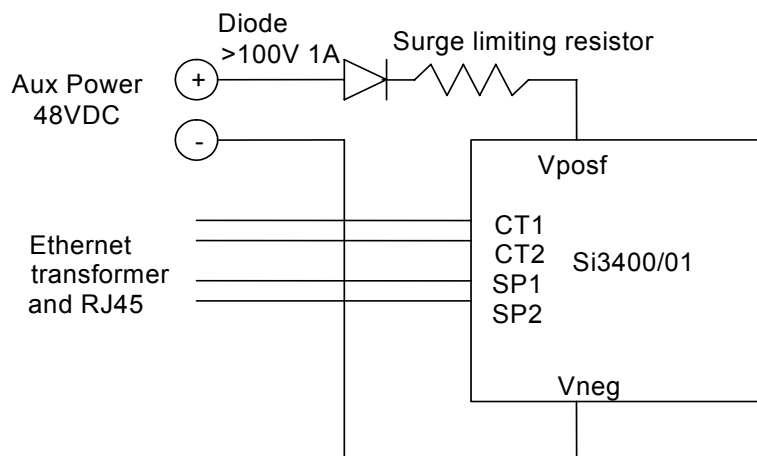


Figure 14. 48 V Auxiliary Supply

The auxiliary power source must supply between 41 and 56 V and at least 15 W for class 0 or 3 equipment (less if the equipment is class 1 or 2). It must also have output that is isolated from earth ground. To prevent damage from hot insertion suddenly charging the 0.1 μF input capacitor, a 2 Ω surge limiting resistor in series with the auxiliary power supply is recommended.

This provides a very simple and inexpensive means of providing auxiliary power. The diode bridges in the Si3400/01 ensure that no power is fed back to the PSE.

The auxiliary power source always provides the power if it is plugged in first because the PSE will not successfully complete the detection and classification cycle. If the PSE is plugged in first, the auxiliary power or the auxiliary power source could provide the power, whichever has the greater output voltage. If the auxiliary power source provides the power, the PSE will generally sense a disconnect.

The Si3400/01 $\overline{\text{PLOSS}}$ signal indicates whether power is being provided from the auxiliary power source.

It is also possible to use a lower-voltage auxiliary power source, such as 12 V by diode OR at the output of the switching converter, as shown in Figure 15.

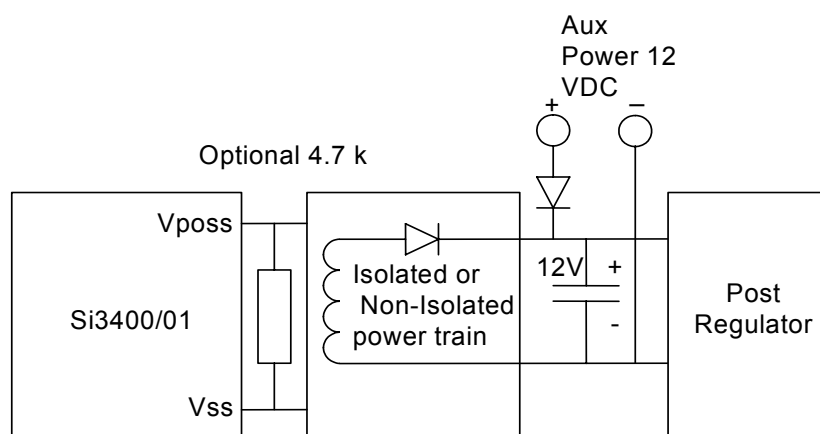


Figure 15. 12 V Auxiliary Supply

AN296

This option may be preferable when a post regulator is required for generation of very low voltages, such as 1.8 V, or when the post regulator is required for low noise.

With the post regulator option, the larger output voltage will again supply the power. In this case, the Si3400/01 will attempt to go through the detection and classification cycle, but if the AUX supply is providing the power, the Si3400/01 will not draw enough dc current, and the PSE may disconnect and cycle continuously. To prevent this, it is possible to add a 4.7 k Ω , 1 W resistor from VPOSF to VSS of the Si3400/01 to ensure >10 mA power drain from the PSE. If this resistor is added, the PSE will always have >10 mA power drain and will stay connected even if the auxiliary power source is providing the load current.

In this option, the $\overline{\text{PLOSS}}$ indicator will not be active when the auxiliary power source is providing the power and the PSE is not present.

7. Layout, EMI, and EMC Considerations

Refer to the files located at www.silabs.com/PoE under the documentation page for examples of recommended PCB layouts in the evaluation board user's guides. Silicon Labs strongly recommends adhering to the layouts shown in these designs to avoid potential performance issues. In general, four-layer PCB designs yield the most robust design, as shown in the evaluation board user's guides. Two-layer PCB designs must be carefully considered. Silicon Labs strongly recommends all two-layer PCB designs be reviewed before fabrication.

Submit PCB schematics and layout files to PoEinfo@silabs.com for feedback and recommendations on these designs.

7.1. Thermal Considerations

The thermal pad of the Si3400/01 must be connected to a heat spreader. Generally, a 2 in² bottom plane connected to the thermal pad of the Si3400/01 and electrically connected to Vneg is recommended. While the heat spreader generally is not a circuit ground, it is a good reference plane for the Si3400/01 and is also useful as a shield layer for EMI reduction.

With the 2 in² thermal plane on an outer layer, the thermal impedance of the Si3400/01 was measured at 44 °C/W. As an added data point, 54 °C/W was measured with a 1 in² plane on an inner layer.

Due to heating of the ambient air from the Schottky diode etc., the effective thermal impedance can be considerably higher than this. It is not unusual for the Si3400/01 junction temperature to rise 70 °C. The Si3400/01 is rated up to a junction temperature of 140 °C, with thermal shutdown to 160 °C typical. If such a high junction temperature is a concern, it can be reduced by bypassing the on-chip diode bridges as discussed in "AN313: Using the Si3400 and Si3401 in High Power Applications". Diode bridge bypass for full-power applications should also be considered in a two-layer design where it is difficult to include such a large thermal plane.

7.2. Voltage Considerations

Since the Si3400/01 is not exposed to dc voltages over 60 V dc, it is generally considered to be a safety-extra-low-voltage (SELV) circuit, and there are no particular spacing requirements other than those of high-yield board manufacture.

7.3. Current Considerations

Pins CT1, CT2, SP1, SP2, HSO, and V_{POSF} carry up to 325 mA dc. 12 mil traces have been found to be adequate. Pins SWO and V_{SS} carry current spikes of up to several amps, although the dc current is no more than 325 mA, and 25 mil traces are used for these pins. Output current can be up to 3 A depending on output voltage, and 50 mil traces are recommended in the output section.

7.4. EMI and EMC Considerations

As with any switching converter, care in the overall circuit design and layout is required to meet the stringent requirements for EMI (i.e. CISPR 22 Class B in the 30 MHz to 1 GHz band) and EMC (i.e. EN55022 in the 150 kHz to 30 MHz band). While the comments in this section apply to both the isolated flyback approach and non-isolated topologies, the flyback topology is the most challenging and, therefore, the focus of the discussion.

To prevent radiated emissions, care must be taken to keep the circuit nodes with high ac voltage very short and to keep the current loops carrying high ac current of a very small diameter.

Referring to Figure 4, the circuit nodes with high voltage swing are as follows:

- The node connecting SWO (Si3400/01 pin 18) and the transformer primary
- The node connecting the transformer secondary to the anode of D2

These circuit nodes should be kept extremely short to minimize EMI. While the current flowing is fairly high (about 1 A on the primary side and 3 A on the secondary side), trace width should be limited to about 25 mils to cut down on radiation. While it is possible to reduce radiation by routing these nodes on an inner layer, in practice, it should be possible to arrange the layout so that these two nodes are sufficiently short that there is little advantage to be gained by this. An R-C snubber across the transformer primary or across the output rectifier can reduce dV/dt and thus radiation. In practice, it has been found that the secondary side snubber is quite effective, but the primary side snubber is not helpful in this regard due to the high current peak associated with switcher FET turn on in the case of the primary side snubber.

AN296

The loops carrying high ac current are as follows:

- The loop from the input filter, C1–C4, to the transformer retuning from the transformer to SWO, then to V_{SS} and back to the input filter capacitors.
- The loop from the transformer secondary to D3, the filter capacitor C6, and returning to the transformer secondary.
- The loop associated with the primary side snubber and transformer.

These loops should be kept small in diameter to avoid EMI. An effective way of doing this is to route the return for the loop underneath the source for the loop as much as possible, effectively shrinking the loop diameter to almost zero.

Ferrite beads L2–L5 are primarily for conducted emissions reduction, although they have been found to improve radiated emissions as well.

Using these methods, the test result shown in Figure 16 has been obtained for EMI.

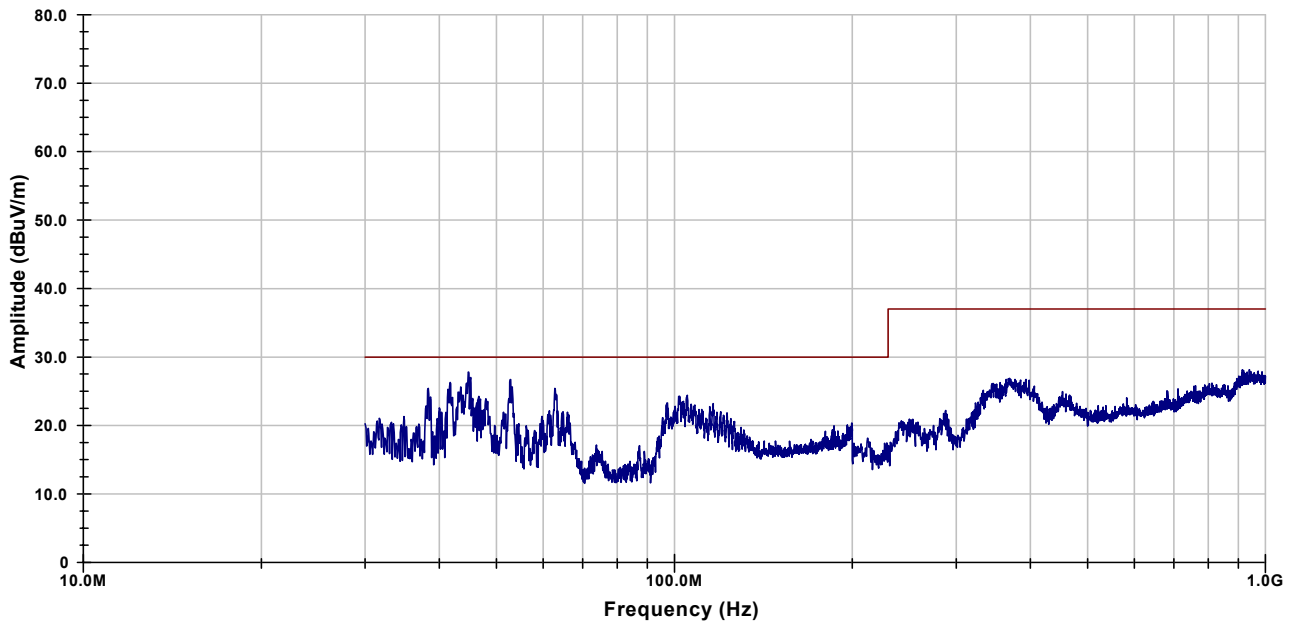


Figure 16. Radiated Emissions Test Result

Lab testing of conducted emissions has shown that if the power output is not referenced to earth ground (as is the case in many applications), conducted emissions are not a problem because there are no path-induced common-mode disturbances on the loop. However, it has been found that if the output has an earth ground reference, common-mode current can be quite high at lower frequencies.

Figure 17 is the measured conducted emissions result. For the grounded-output case, a common-mode choke, such as the Coilcraft BU9-2820R5BL, is required due to a possible ground loop.

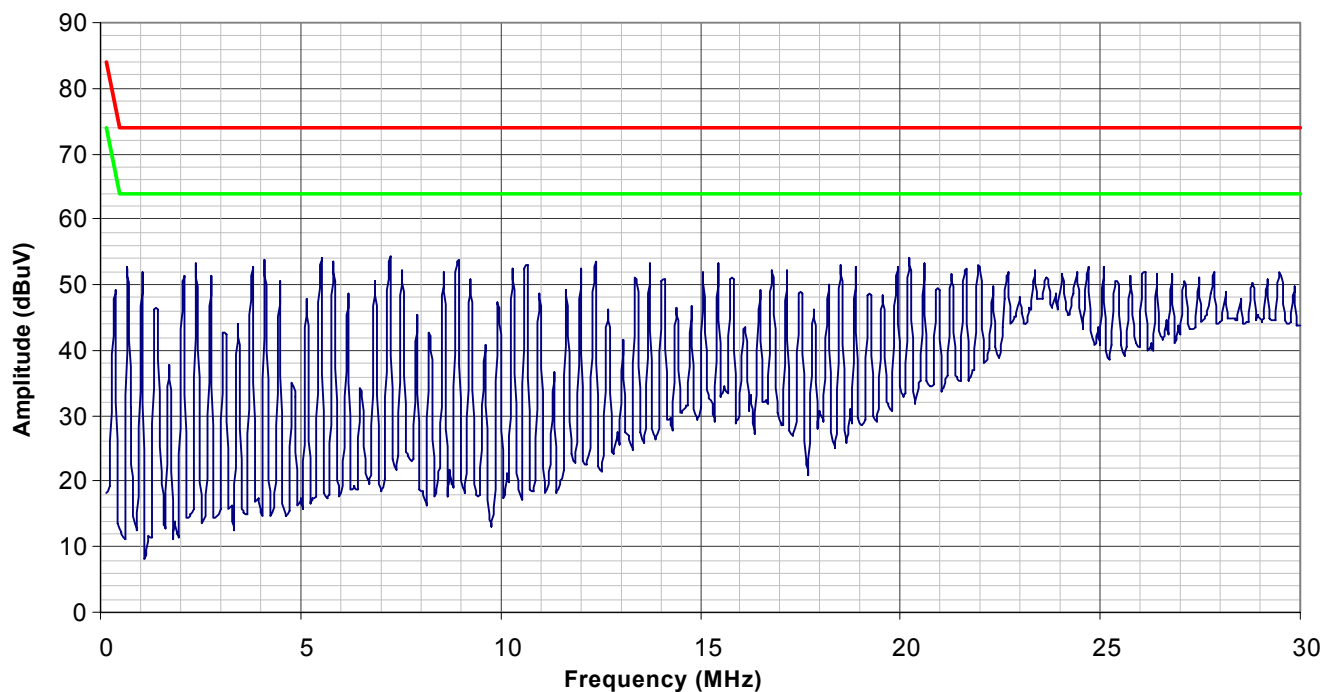


Figure 17. Conducted Emissions Test Result

7.5. Minimum Load Considerations

To ensure the switcher does not pulse on and off when no load is on the output, Silicon Labs recommends a ≥ 250 mW load be present. See "3.4. Maintain Power Signature" on page 7 for more information.

8. Conclusion

This application note has covered the basic operation and design equations for the Si3400/01, allowing the design of highly-integrated and efficient PDs for PoE applications.

As mentioned earlier, reference designs and design spreadsheets are also available at www.silabs.com/PoE to assist in the easy design-in process for the Si3400/01. The spreadsheets should be used in conjunction with this application note, and additional documentation is included within the spreadsheet. The evaluation boards and reference designs are documented separately and include example layouts and BOM lists.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated schematics and BOM with optimized values for Rev C, Si3400
- Updated performance information with measured results for Rev C Si3400
- Added new section, "6. Use with an Auxiliary Power Supply" on page 17.

Revision 0.2 to Revision 0.3

- Updated RCLASS information.
- Updated recommended applications circuits.

Revision 0.3 to Revision 0.4

- Modified text.
- Updated Figure 4 on page 4 to same as in EVB User's Guide.
- Added "7. Layout Guidelines".
- Updated "6. Use with an Auxiliary Power Supply" on page 17.
 - Added important information about connecting auxiliary supplies.
- Updated Figure 14 on page 17.
 - Added important information about connecting auxiliary supplies.

Revision 0.4 to Revision 0.5

- Updated Figure 4, "Isolated Flyback Configuration for Si3400ISO-EVB and Si3401ISO-EVB (5 V Output)," on page 4.
- Updated Section 7 to read "7. Layout, EMI, and EMC Considerations" on page 19.

Revision 0.5 to Revision 0.6

- Updated Revision D silicon to include addition of the VSSA (pin 15) and for optimized EMI, ESD, and load transient response.
- Pin ISOSSFT (pin 4) added throughout document for revisions CZ and higher. Function available on Revision E and higher.

Revision 0.6 to Revision 0.7

- Pin ISOSSFT (pin 4) added throughout document. This function is available on Revision E and higher.

Revision 0.7 to Revision 0.8

- Document updated throughout to support Rev E updates
- Updated Figure 3 on page 3.
- Updated Figure 4 on page 4.
- Updated "4.1.1. Output Voltage—Non-Isolated Design" on page 10.
- Updated "4.1.2. Output Filter and Loop Stability—Non-Isolated Design" on page 10.
- Updated "4.1.3. Soft Start Non-Isolated Case" on page 11.
- Updated Figure 8 on page 11.
- Updated "4.2. Isolated Flyback Design" on page 11.
- Updated "4.2.1. Output Voltage—Isolated Design" on page 14.
- Updated "4.2.2. Output Filter and Loop Stability—Isolated Design" on page 14.
- Updated "4.2.3. Soft Start Isolated Case" on page 14.
- Updated Figure 11 on page 15.
- Updated Figure 12 on page 15.
- Updated Figure 14 on page 17.
- Updated "6. Use with an Auxiliary Power Supply" on page 17.
- Updated "7.4. EMI and EMC Considerations" on page 19.

NOTES:

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