

NTE56051 & NTE56052 TRIAC, 8A Low Logic Level

Description:

The NTE56051 and NTE56052 are glass passivated, Low Logic Level TRIACs in a TO220 type package designed for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits, and other low power gate trigger circuits.

Absolute Maximum Ratings:

Repetitive Peak Off-State Voltage (Note 1), V_{DRM}	
NTE56051	500V
NTE56052	600V
RMS On-State Current (Full Sine Wave, $T_{MB} \leq 102^{\circ}\text{C}$), $I_T(\text{RMS})$	8A
Non-Repetitive Peak On-State Current, I_{TSM}	
(Full Sine Wave, $T_J = +125^{\circ}\text{C}$ prior to Surge, with Reapplied V_{DRMmax})	
$t = 20\text{ms}$	55A
$t = 16.7\text{ms}$	60A
I^2t for Fusing ($t = 10\text{ms}$), I^2t	$15\text{A}^2\text{sec}$
Repetitive Rate-of-Rise of On-State Current after Triggering, dI_T/dt	
($I_{TM} = 12\text{A}$, $I_G = 0.2\text{A}$, $dI_G/dt = 0.2\text{A}/\mu\text{s}$)	
$MT_2 (+)$, $G (+)$	$50\text{A}/\mu\text{s}$
$MT_2 (+)$, $G (-)$	$50\text{A}/\mu\text{s}$
$MT_2 (-)$, $G (-)$	$50\text{A}/\mu\text{s}$
$MT_2 (-)$, $G (+)$	$10\text{A}/\mu\text{s}$
Peak Gate Current, I_{GM}	2A
Peak Gate Voltage, V_{GM}	5V
Peak Gate Power, P_{GM}	5W
Average Gate Power (Over Any 20ms Period), $P_{G(AV)}$	500mW
Operating Junction Temperature, T_J	$+125^{\circ}\text{C}$
Storage Temperature Range, T_{stg}	-40° to $+150^{\circ}\text{C}$
Thermal Resistance, Junction-to-Mounting Base, R_{thJMB}	
Full Cycle	2.0K/W
Half Cycle	2.4K/W
Typical Thermal Resistance, Junction-to-Ambient, R_{thJA}	60K/W

Note 1. Although not recommended, off-state voltages up to 800V may be applied without damage, but the TRIAC may switch to the on-State. The rate-of-rise of current should not exceed $6\text{A}/\mu\text{s}$.

Electrical Characteristics: ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
Gate Trigger Current MT ₂ (+), G (+)	I _{GT}	V _D = 12V, I _T = 0.1A	–	2.5	5	mA
MT ₂ (+), G (–)			–	3.5	5	mA
MT ₂ (–), G (–)			–	3.5	5	mA
MT ₂ (–), G (+)			–	6.5	10	mA
Latching Current MT ₂ (+), G (+)	I _L	V _D = 12V, I _T = 0.1A	–	1.6	15	mA
MT ₂ (+), G (–)			–	8.5	20	mA
MT ₂ (–), G (–)			–	1.2	15	mA
MT ₂ (–), G (+)			–	2.5	20	mA
Holding Current	I _H	V _D = 12V, I _T = 0.1A	–	1.5	10	mA
On–State Voltage	V _T	I _T = 5A	–	1.4	1.7	V
Gate Trigger Voltage	V _{GT}	V _D = 12V, I _T = 0.1A	–	0.7	1.5	V
		V _D = 400V, I _T = 0.1A, T _J = +125°C	0.25	0.4	–	V
Off–State Leakage Current	I _D	V _D = V _{DRM} max, T _J = +125°C	–	0.1	0.5	mA
Dynamic Characteristics						
Critical Rate–of–Rise of Off–State Voltage	dV _D /dt	V _{DM} = 67% V _{DRM} max, T _J = +125°C, Exponential Waveform, R _{GK} = 1kΩ	–	5	–	V/μs
Gate Controlled Turn–On Time	t _{gt}	I _{TM} = 12A, V _D = V _{DRM} max, I _G = 0.1A, dI _G /dt = 5A/μs	–	2	–	μs

