

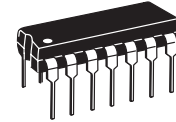
8-Bit Serial-Input/ Parallel-Output Shift Register

High-Performance Silicon-Gate CMOS

The 74HC164A is identical in pinout to the LS164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The MC74HC164A is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs.

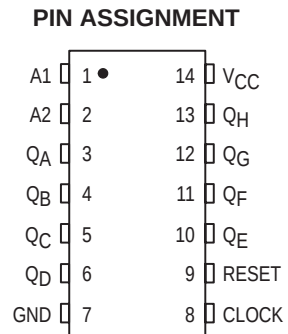
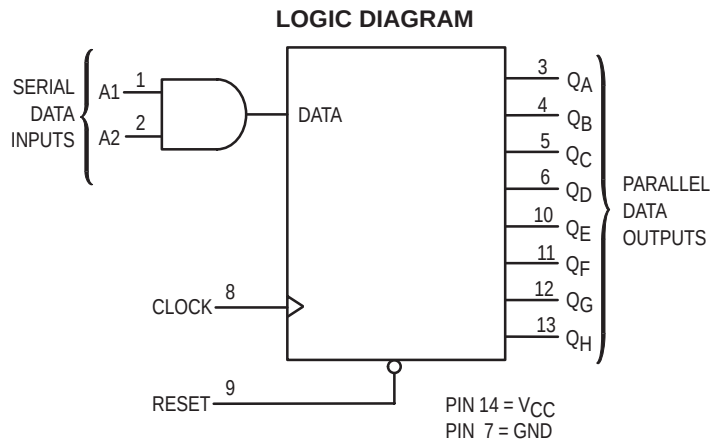
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates



DIP-14
N SUFFIX
CASE 646



SOP-14
D SUFFIX
CASE 751A



FUNCTION TABLE

Inputs				Outputs			
Reset	Clock	A1	A2	Q _A	Q _B	... Q _H	
L	X	X	X	L	L	... L	
H	⌊	X	X	No Change			
H	⌋	H	D	D	Q _{An}	... Q _{Gn}	
H	⌋	D	H	D	Q _{An}	... Q _{Gn}	

D = data input

Q_{An} – Q_{Gn} = data shifted from the preceding stage on a rising edge at the clock input.

ORDERING INFORMATION

Device	Package	Shipping
74HC164N	DIP-14	2000 / Box
74HC164M/TR	SOP-14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55°C to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 2.4 \text{ mA}$	3.0	2.48	2.34	2.20	
		$ I_{out} \leq 4.0 \text{ mA}$	4.5	3.98	3.84	3.70	
		$ I_{out} \leq 5.2 \text{ mA}$	6.0	5.48	5.34	5.20	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55°C to 25°C	≤ 85°C	≤ 125°C	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	10	10	10	MHz
		3.0	20	20	20	
		4.5	40	35	30	
		6.0	50	45	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	160	200	250	ns
		3.0	100	150	200	
		4.5	32	40	48	
		6.0	27	34	42	
t _{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	175	220	260	ns
		3.0	100	150	200	
		4.5	35	44	53	
		6.0	30	37	45	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		180	

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, A1 or A2 to Clock (Figure 3)	2.0	25	35	40	ns
		3.0	15	20	25	
		4.5	7	8	9	
		6.0	5	6	6	
t _h	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	2.0	3	3	3	ns
		3.0	3	3	3	
		4.5	3	3	3	
		6.0	3	3	3	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	3	3	3	ns
		3.0	3	3	3	
		4.5	3	3	3	
		6.0	3	3	3	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	50	60	75	ns
		3.0	26	35	45	
		4.5	12	15	20	
		6.0	10	12	15	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	50	60	75	ns
		3.0	26	35	45	
		4.5	12	15	20	
		6.0	10	12	15	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

A1, A2 (Pins 1, 2)

Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high level to be entered into the shift register, both A1 and A2 inputs must be high, thereby allowing one input to be used as a data-enable input. When only one serial input is used, the other must be connected to V_{CC} .

Clock (Pin 8)

Shift Register Clock. A positive-going transition on this pin shifts the data at each stage to the next stage. The shift

register is completely static, allowing clock rates down to DC in a continuous or intermittent mode.

OUTPUTS

QA – QH (Pins 3, 4, 5, 6, 10, 11, 12, 13)

Parallel Shift Register Outputs. The shifted data is presented at these outputs in true, or noninverted, form.

CONTROL INPUT

Reset (Pin 9)

Active-Low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip-flops and sets Outputs QA – QH to the low level state.

SWITCHING WAVEFORMS

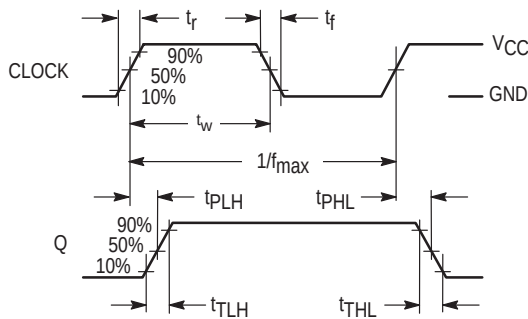


Figure 1.

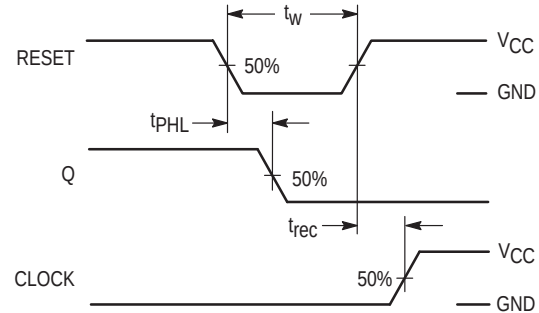


Figure 2.

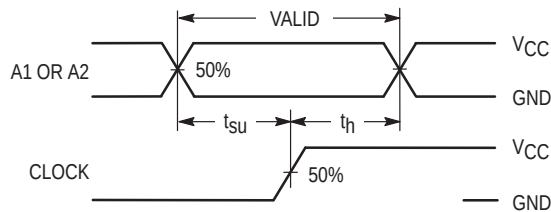
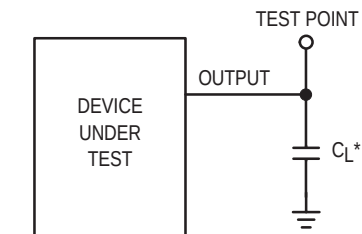


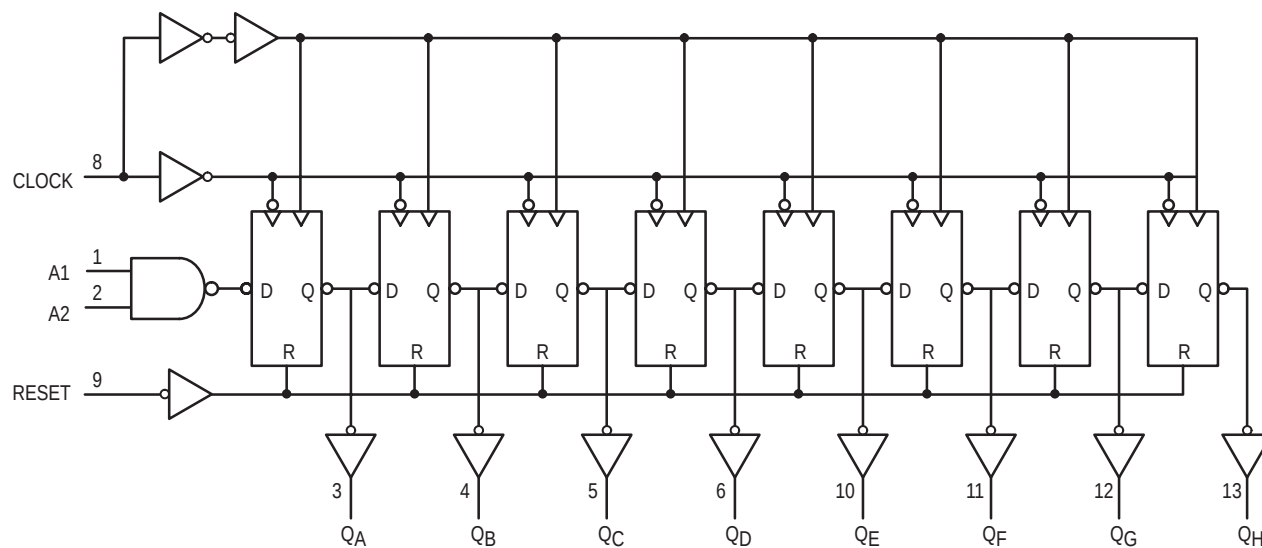
Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM

