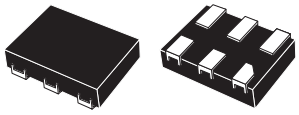
STG3159

Low voltage 1Ω max single SPDT switch with break-before-make feature

Features

- High speed:
  - t_{PD} = 1.5ns (Typ.) at V_{CC} = 3.0V
  - t_{PD} = 1.5ns (Typ.) at V_{CC} = 2.3V
- Ultra low power dissipation:
  - I_{CC} = 0.2µA (Max.) at T_A = 85°C
- Low "ON" resistance:
  - R_{ON} = 1.0Ω (T_A = 25ºC) at V_{CC} = 4.3V
  - R_{ON} = 1.1Ω (T_A = 25ºC) at V_{CC} = 3.0V
  - R_{ON} = 1.7Ω (T_A = 25ºC) at V_{CC} = 1.8V
- Wide operating voltage range:
  - V_{CC} (OPR) = 1.65V to 4.5V single supply
- 4.5V Tolerant and 1.8V compatible threshold on digital control input at V_{CC} = 2.3V to 3.0V
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD Performance tested per JESD22
  - 2000V Human-body model (A114-B, Class II)
  - 200V Machine model (A115-A)
  - 1000V Charged-device model (C101)



DFN6L

Description

The STG3159 is a high-speed CMOS low voltage single analog S.P.D.T. (Single Pole Dual Throw) switch or 2:1 Multiplexer /Demultiplexer switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.65V to 4.3V, making this device ideal for portable applications.

The device offers very low ON-Resistance (1Ω) at V_{CC} = 4.3V. The SEL inputs are provided to control the switch. The switch S1 is ON (they are connected to common Ports Dn) when the SEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low; the switch S2 is ON (it is connected to common Port D) when the SEL input is held low and OFF (high impedance state exists between the two ports) when SEL is held high.

Additional key features are fast switching speed, break-before-make delay time and Ultra Low Power Consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Order codes

Part number	Package	Packaging
STG3159DTR	DFN6L (1.2mm x 1mm)	Tape and Reel

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2 Electrical ratings 4

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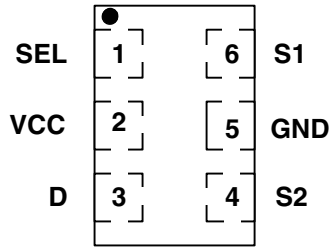
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1 Pin connections and functions

Figure 1. Pin connections (top through view)



DFN6L

Table 1. Truth table

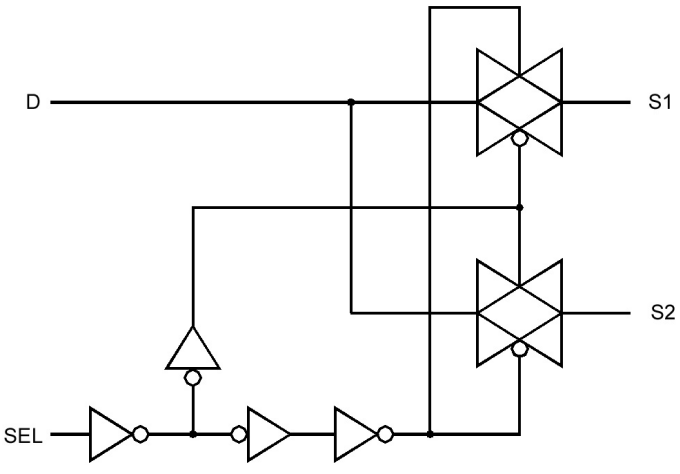
Sel	Switch S1	Switch S2
H	ON	OFF (1)
L	OFF (1)	ON

1. High impedance

Table 2. Pin descriptions

Pin Nº	Symbol	Name and function
6, 4	S1, S2	Independent channels
3	D	Common channels
1	SEL	Control
2	V_{CC}	Positive supply voltage
5	GND	Ground (0V)

Figure 2. Input equivalent circuit



2 Electrical ratings

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC Input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC Control input voltage	-0.5 to 5.5	V
V_O	DC Output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC Input diode current on control pin (V_{SEL} < 0V)	-50	mA
I_{IK}	DC Input diode current (V_{SEL} < 0V)	±50	mA
I_{OK}	DC Output diode current	±20	mA
I_O	DC Output current	±200	mA
I_{OP}	DC Output current peak (pulse at 1ms, 10% duty cycle)	±400	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70ºC (1)	1120	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	300	°C

1. Derate above 70ºC by 18.5mW/C

Table 4. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		1.65 to 4.5	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.5	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-55 to 125	°C
dt/dv	Input rise and fall time control input	V_{CC} = 1.65V to 2.7V	0 to 20	ns/V
		V_{CC} = 3.0 to 4.5V	0 to 10	

1. Truth table guaranteed: 1.2V to 4.5V

3 Electrical characteristics

3.1 DC electrical characteristics

Table 5. DC specifications

Symbol	Parameter	Test conditions		Value							Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High level input voltage	1.65-1.95		$0.65V_{CC}$			$0.65V_{CC}$		$0.65V_{CC}$		V
		2.3-2.5		1.2			1.2		1.2		
		2.7-3.0		1.3			1.3		1.3		
		3.3-3.6		1.4			1.4		1.4		
		4.3		1.6			1.6		1.6		
V_{IL}	Low level input voltage	1.65-1.95				0.40		0.40		0.40	V
		2.3-2.5				0.60		0.60		0.60	
		2.7-3.0				0.60		0.60		0.60	
		3.3-3.6				0.60		0.60		0.60	
		4.3				0.80		0.80		0.80	
R_{PEAK}	Switch ON peak resistance	1.8	V_S = 0V to V_{CC} I_S = 100mA		2.2	3.0		3.5			Ω
		2.7			1.3	1.6		1.8			
		3.0			1.2	1.5		1.7			
		4.3			1.1	1.2		1.4			
R_{ON}	Switch On resistance	1.8	V_S = 0.9V I_S = 100mA		1.7	2.3		2.7			Ω
		2.7	V_S = 1.3V I_S = 100mA		1.2	1.5		1.7			
		3.0	V_S = 1.5V I_S = 100mA		1.1	1.2		1.6			
		4.3	V_S = 2.5V I_S = 100mA		1.0	1.1		1.3			
ΔR_{ON}	ON resistance match between channels (1)	1.8	V_S @ R_{ON} Max I_S = 100mA		0.06						Ω
		2.7			0.05						
		3.0			0.05						
		4.3			0.05						
R_{FLAT}	ON resistance flatness (2)	1.8	V_S = 0V to V_{CC} I_S = 100mA		1.0	1.5		1.5			Ω
		2.7			0.45	0.60		0.70			
		3.0			0.40	0.50		0.60			
		4.3			0.37	0.50		0.60			

Table 5. DC specifications (continued)

Symbol	Parameter	Test conditions		Value							Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_{OFF}	OFF state leakage current (SN), (D)	4.3	V_S = 0.3 or 4V			±20		±100			nA
I_{IN}	Input leakage current	0 – 4.3	V_{SEL} = 0 to 4.3V			±0.1		±1			µA
I_{CC}	Quiescent supply current	1.65 – 4.3	V_{SEL} = V_{CC} or GND			±0.05		±0.2		±1	µA
I_{CCLV}	Quiescent supply current low voltage driving	4.3	V_{SEL} = 1.65V		±17	±35		±70			µA
		4.3	V_{SEL} = 1.80V		±15	±30		±60			
		4.3	V_{SEL} = 2.60V		±5	±10		±20			

1. $\Delta R_{ON} = R_{ON(Max)} - R_{ON(Min)}$
2. Flatness is defined as the difference between the maximum and minimum value of ON-resistance as measured over the specified analog signal ranges.

3.2 AC electrical characteristics

Table 6. AC Electrical characteristics (C_L = 35pF, R_L = 50Ω, t_r = t_f ≤5ns)

Symbol	Parameter	Test conditions		Value							Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation delay	1.65-1.95	V_S = OPEN		0.15						ns
		2.3-2.7			0.14						
		3.0-3.3			0.13						
		3.6-4.3			0.13						
t_{ON}	Turn-ON time	1.65-1.95	V_S = 0.8V		36						ns
		2.3-2.7	V_S = 1.5V		22	32		42			
		3.0-3.3			16	26		36			
		3.6-4.3			13	23		33			
t_{OFF}	Turn-OFF time	1.65-1.95	V_S = 0.8		29						ns
		2.3-2.7	V_S = 1.5V		17	27		37			
		3.0-3.3			12	23		33			
		3.6-4.3			11	21		31			
t_D	Break before make time delay	1.65-1.95	C_L = 35pF R_L = 50Ω V_S = 1.5V		15						ns
		2.3-2.7			10						
		3.0-3.3			8						
		3.6-4.3			6						
Q	Charge injection	1.65	C_L = 100pF V_{GEN} = 0V R_{GEN} = 0Ω		16						pC
		2.3			22						
		3			26						
		4.3			33						

3.3 Analog switch characteristics

Table 7. Analog switch characteristics (C_L = 5pF, R_L = 50Ω, T_A = 25°C)

Symbol	Parameter	Test conditions		Value							Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
OIRR	Off Isolation (1)	1.65-4.3	V_S = 1V_{RMS} f = 100kHz		-80						dB
Xtalk	Crosstalk	1.6-4.3	V_S = 1V_{RMS} f = 100kHz		-80						dB
THD	Total harmonic distortion	2.3-4.3	R_L = 600Ω V_S = 2V_{PP} f = 20Hz to 20 kHz		0.03						%
BW	-3dB bandwidth	1.65-4.3	R_L= 50Ω		150						MHz
C_{IN}	Control pin input capacitance				6						pF
C_{ON}	Sn port capacitance when switch is enabled	3.3	f = 1MHz		52						
C_{OFF}	Sn port capacitance when switch is disabled	3.3	f = 1MHz		25						
C_D	D Port Capacitance when Switch is Enabled	3.3	f = 1MHz		50						

1. OFF Isolation = 20Log_{10} (V_D/V_S), V_D = output. V_S = input to OFF switch.

4 Test circuits

Figure 3. ON-Resistance

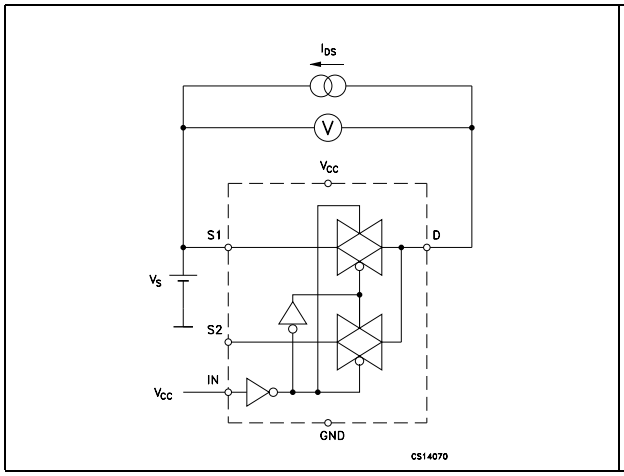


Figure 4. Bandwidth

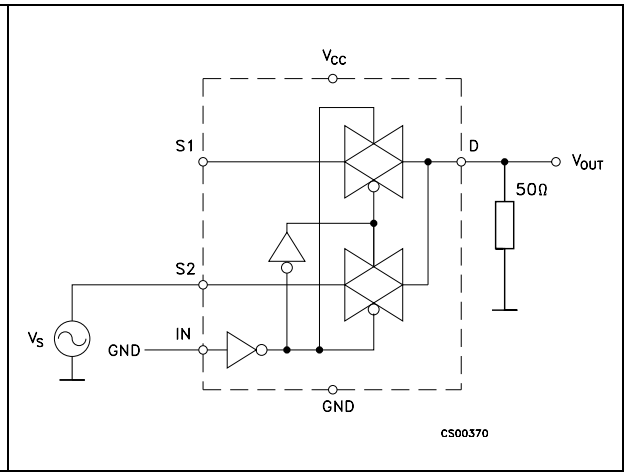


Figure 5. OFF Leakage

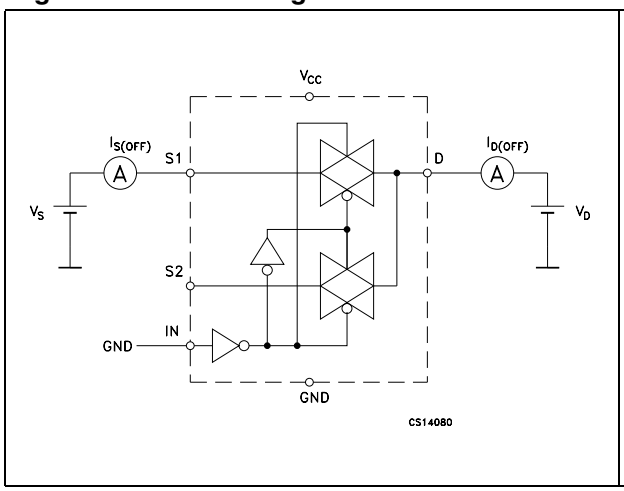


Figure 6. Channel to channel crosstalk

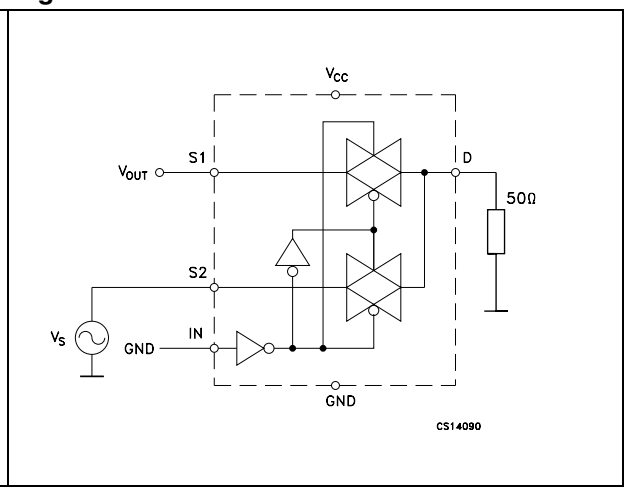


Figure 7. OFF Isolation

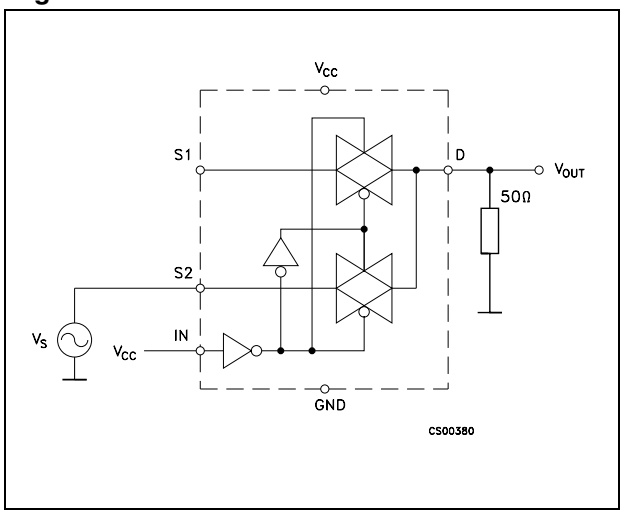
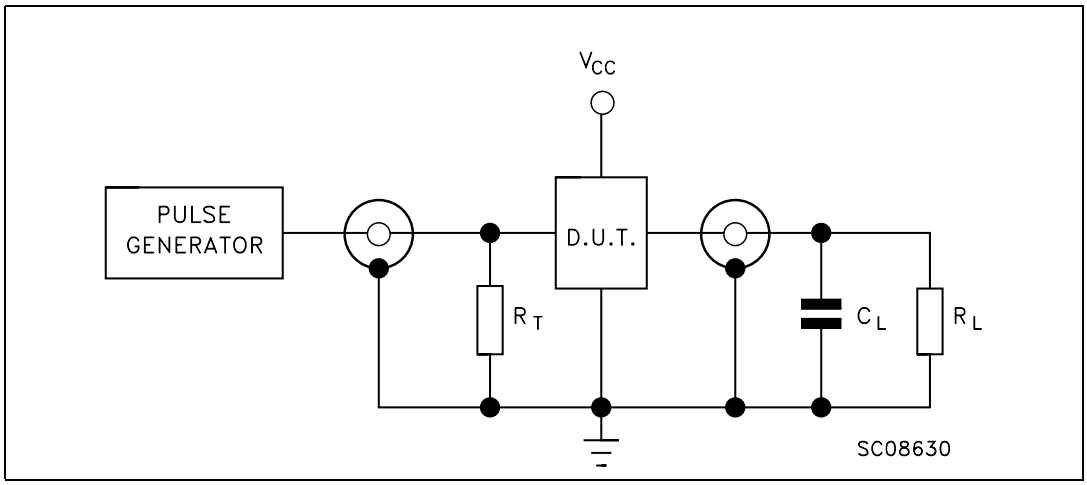


Figure 8. Test circuit



Note: C_L = 5/35pF or equivalent: (includes jig capacitance)

R_L = 50Ω or equivalent

R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 9. Break-before-make time delay

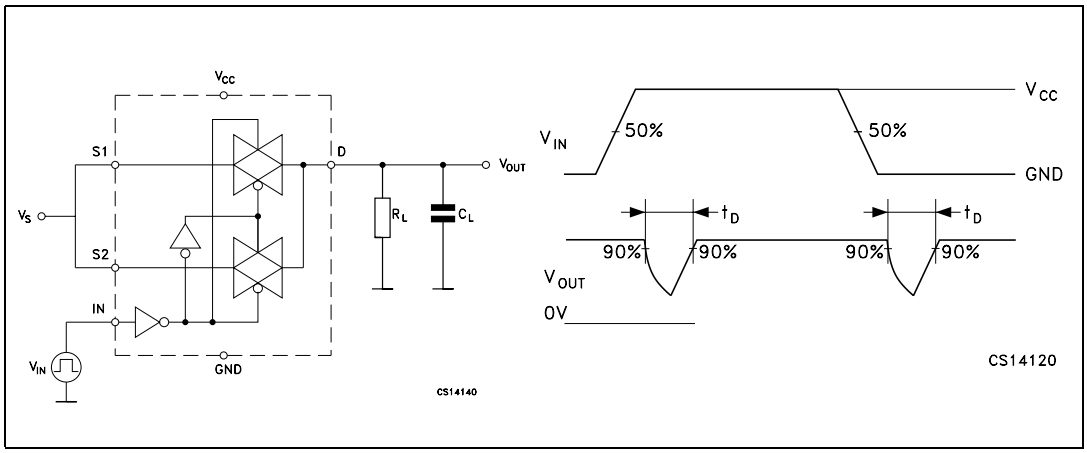


Figure 10. Switching time and charge injection
(V_{GEN} = 0V, R_{GEN} = 0Ω, R_L = 1MΩ, C_L = 100pF)

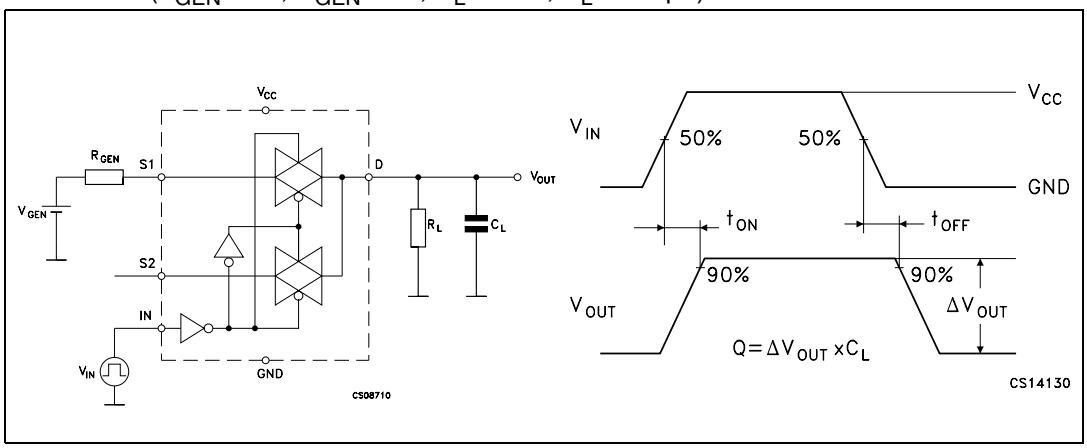
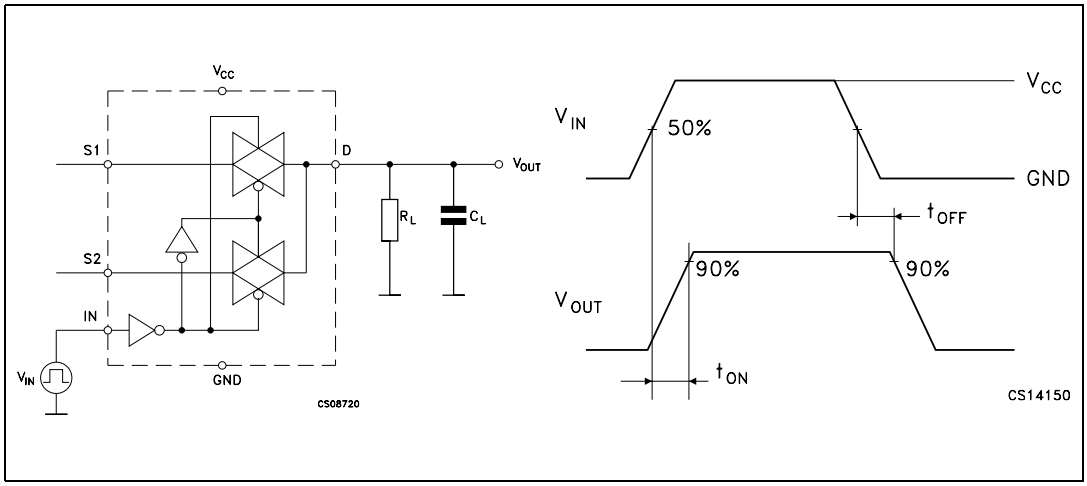


Figure 11. Turn ON, turn OFF delay time



5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 8. DFN6 (1.2mm x 1mm) Mechanical data

Dim.	mm.			inch		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.50	0.45	0.55	0.019	0.017	0.021
A1	0.02	0	0.05	0.001	0	0.002
A3	0.127			0.005		
b	0.20	0.15	0.25	0.007	0.006	0.010
D	1.20	1.10	1.30	0.047	0.043	0.051
E	1	0.90	1.10	0.039	0.035	0.043
e	0.40			0.015		
L	0.35	0.30	0.40	0.013	0.011	0.015
L1	0.45	0.40	0.50	0.017	0.015	0.019

Figure 12. Package dimensions

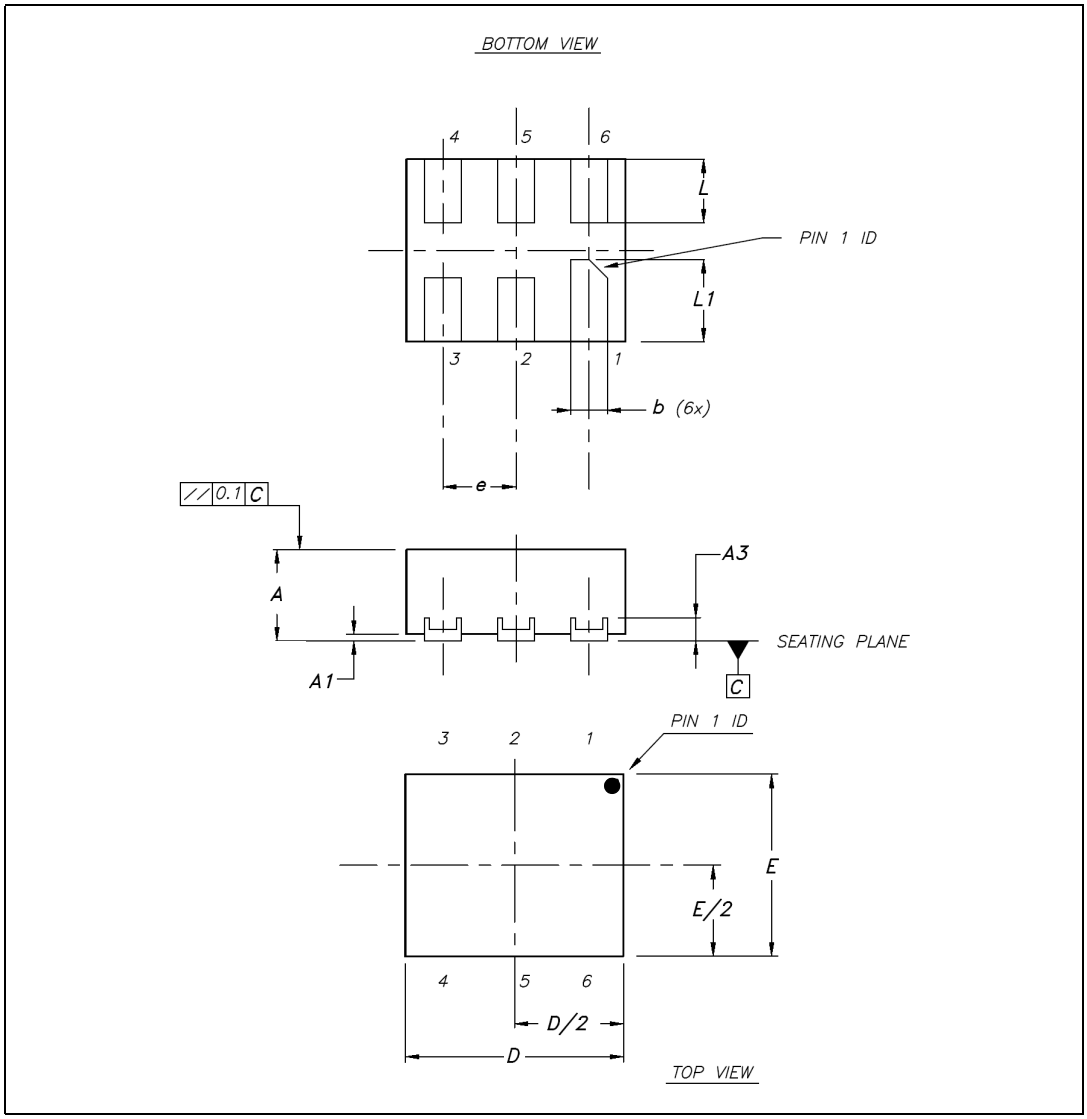


Table 9. DFN6 Foot print recommendation

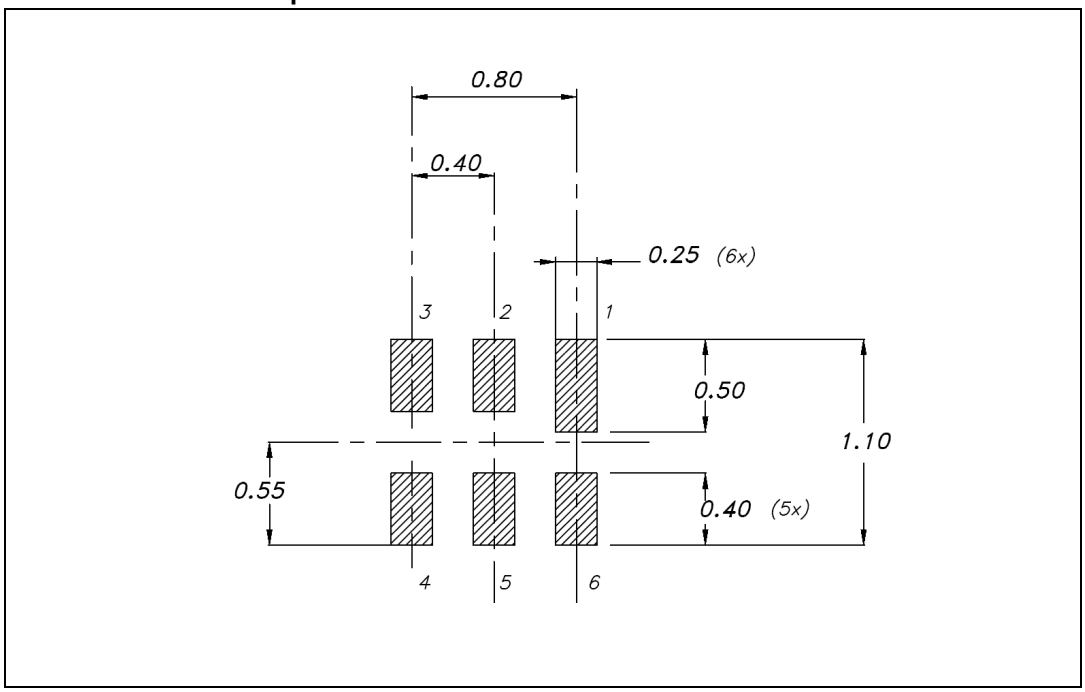


Table 10. DFN6L Tape information

Dim	mm.	inch
D	1.50 +0.1/0	0.059 +0.004/0
E	1.75 ±0.1	0.069 ±0.004
Po	4.00 ±0.1	0.157 ±0.004
T max.	0.40	0.016
D1 min.	1	0.039
F	3.5 ±0.05	0.138 ±0.002
K max.	2.40	0.094
P2	2.00 ±0.05	0.079 ±0.002
R	25	0.984
W	8.00 ±0.30	0.315 ±0.012
P1	4.00	0.157
Ao, Bo, Ko	0.05 min to 0.50 max.	0.002 min to 0.020 max.

Figure 13. DFN6L Tape information

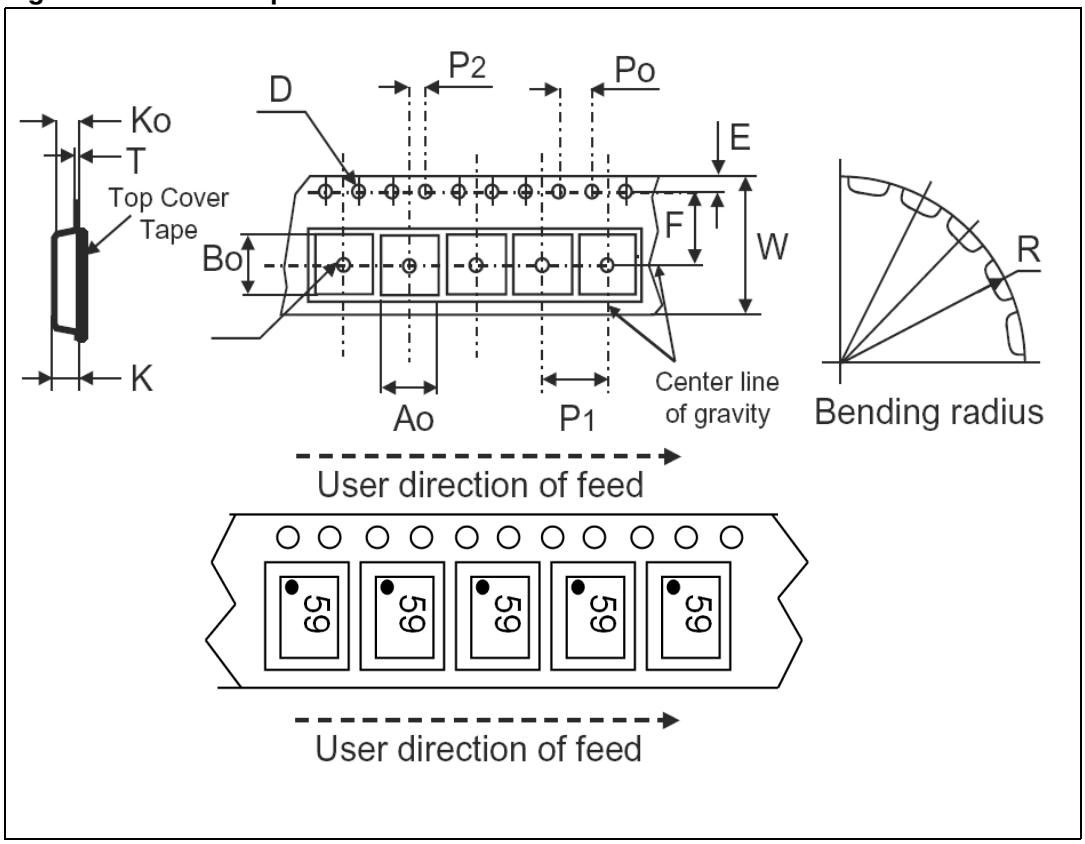
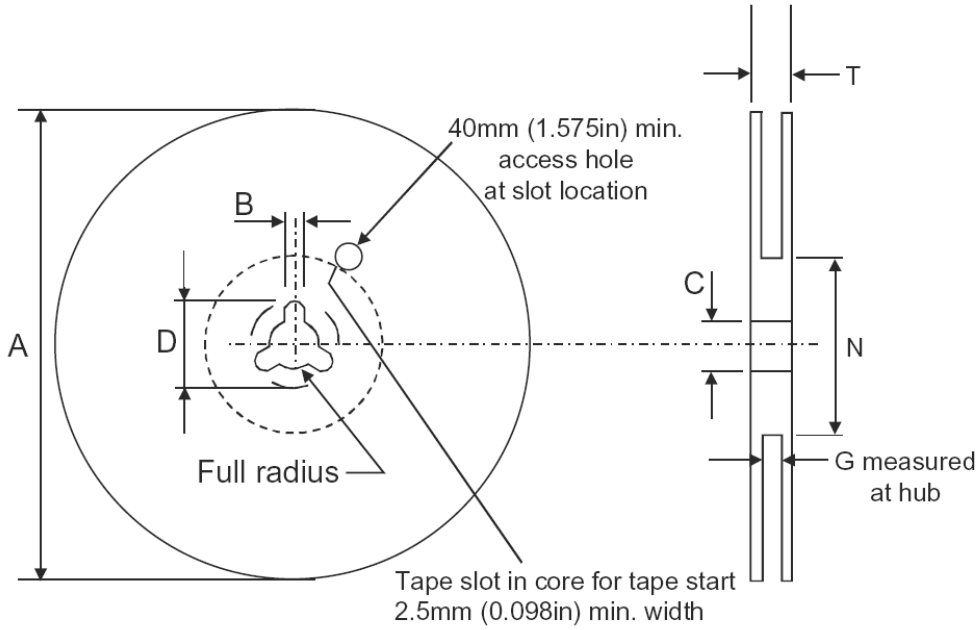


Table 11. DFN6L Reel information

Dim	mm.	inch
Tape size	8.0 ±0.30	0.315 ±0.012
A max.	180.0	7.086
B min.	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D min.	20.2	0.795
N min.	60	2.362
G	8.4 +2/-0	0.319 +0.079/-0
T max.	14.4	0.567

Figure 14. DFN6L Reel information



6 Revision history

Table 12. Revision history

Date	Revision	Changes
06-Dec-2006	1	First release

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