DATA SHEET

GPM8F3732B

48 Pin 8-bit Microcontroller with 32KB Flash

Preliminary

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Version 0.4

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Table of Contents

PAGE

Table of Contents **2**

1. GENERAL DESCRIPTION **5**

2. FEATURES **5**

3. BLOCK DIAGRAM **7**

3.1. GPM8F3732B 7

4. SIGNAL DESCRIPTIONS **8**

4.1. PIN DESCRIPTIONS 8

4.1.1. GPM8F3732B 8

4.2. PIN MAP 10

5. FUNCTIONAL DESCRIPTIONS **11**

5.1. CENTRAL PROCESSING UNIT 11

5.1.1. CPU Introduction 11

5.1.2. CPU Features 11

5.1.3. Arithmetic Logic Unit (ALU) 11

5.1.4. Accumulator A register 11

5.1.5. B register 11

5.1.6. Program Status Word (PSW) 11

5.1.7. Program Counter (PC) 11

5.2. MEMORY ORGANIZATION 12

5.2.1. Introduction 12

5.2.2. Program Memory Allocation 12

5.2.3. Data Memory Allocation 14

5.2.4. Memory Related SFR 18

5.2.4.1. Program write enable bit 18

5.2.4.2. Data pointer registers 18

5.2.4.3. Stack pointer 18

5.3. SPECIAL FUNCTION REGISTERS (SFR) 21

5.4. CLOCK SOURCE 25

5.5. POWER SAVING MODE 27

5.5.1. Introduction 27

5.5.2. HALT mode 27

5.5.3. SLEEP mode 28

5.6. INTERRUPT SYSTEM 34

5.6.1. Introduction 34

5.7. RESET SOURCES 52

5.7.1. Introduction 52

5.7.2. Power-On Reset (POR) 52

5.7.3. Low Voltage Reset / Low Voltage Detect (LVR/LVD) 52

5.7.4. Pad Reset (PAD_RST) 52

5.7.5. Watchdog Timer Reset (WDT_RST) 53

5.7.6. Other Reset Sources 53

5.7.7. I/O Ports 58
5.7.8. Introduction 58
5.8. TIMER MODULE 68
5.8.1. Introduction 68
5.8.2. Timer 0/1 68
5.8.2.1. Timer 0: Mode 0 (13-Bit Timer/Counter) 73
5.8.2.2. Timer 0: Mode 1 (16-Bit Timer/Counter) 73
5.8.2.3. Timer 0: Mode 2 (8-bit Timer/Counter with Auto-reload Function) 74
5.8.2.4. Timer 0: Mode 3 (Two 8-Bit Timers/Counters) 74
5.8.2.5. Timer 1: Mode 0 (13-Bit Timer/Counter) 75
5.8.2.6. Timer 1: Mode 1 (16-Bit Timer/Counter) 75
5.8.2.7. Timer 1: Mode 2 (8-Bit Timer/Counter with Auto-reload Function) 76
5.8.2.8. Timer 1: Mode 3 76
5.8.3. Timer A 76
5.8.4. Timer / Counter mode 76
5.8.4.1. Capture functions 77
5.8.4.2. Timer A Related Registers 77
5.8.5. Timer B 83
5.8.5.1. Timer / Counter mode 83
5.8.5.2. Capture functions 83
5.8.5.3. Timer B Related Registers 84
5.8.6. Timer C 89
5.8.6.1. Timer / Counter mode 89
5.8.6.2. Capture functions 89
5.8.6.3. Timer C Related Registers 90
5.9. UART0 96
5.9.1. UART0: Mode 0(Synchronous Shift register) 96
5.9.2. UART0: Mode 1(8-Bit UART, Variable Baud Rate, Timer1 Clock Source) 97
5.9.3. UART0: Mode 2(9-Bit UART, Fixed Baud Rate) 97
5.9.4. UART0: Mode 3(9-Bit UART, Variable Baud Rate, Timer1 Clock Source) 97
5.9.5. UART0 Related Registers 97
5.10. SPI 101
5.11. ADC 105
5.11.1.ADC Control 105
5.12. I2C UNIT 108
5.12.1. I2C Bus Protocol 108
5.13. MDU UNIT 112
5.14. RTC UNIT 115
5.15. LCD UNIT 116
5.16. CAPACITIVE TOUCH UNIT 123
5.16.1. Capacitance Measurement Method 123
5.17. ALPHABETICAL LIST OF INSTRUCTION SET 129

5.17.1. Arithmetic Operations 129
5.17.2. Logic Operations 129
5.17.3. Boolean Operations 130
5.17.4. Data Transfers 130
5.17.5. Program Branches 131
6. ELECTRICAL CHARACTERISTICS 132
6.1. ABSOLUTE MAXIMUM RATINGS 132
6.2. AC CHARACTERISTICS (T_A = 25℃) 132
6.3. DC CHARACTERISTICS (T_A = 25℃) 132
6.4. ADC CHARACTERISTICS (T_A = 25℃) 132
7. PACKAGE INFORMATION 134
7.1. ORDERING INFORMATION 134
7.2. PACKAGE INFORMATION 134
7.2.1. LQFP 48 134
8. DISCLAIMER 135
9. REVISION HISTORY 136

48-PIN 8-BIT MICRO-CONTROLLER WITH 32KB FLASH MEMORY

1. GENERAL DESCRIPTION

GPM8F3732B, a highly integrated microcontroller, integrates a pipelined 1T 8051 CPU, 2.5K-byte XRAM, 256-byte IDM SRAM and 32K-byte programming FLASH memory. It features maximum of 43 programmable multi-functional I/Os, Timer0/1/A/B/C, UART0, SPI (master/slaver), I2C (master/slaver), 4X31 LCD driver, up to 60-second RTC, 48MHz PLL, 16-bit X 16-bit multiplier, 32-bit / 16-bit divider, 16-channel capacitive touch sensor and one 7-channle SAR ADC with 12-bit resolution for general-purpose application. The GPM8F3732B operates over a wide voltage range of 2.4V - 5.5V with variety of clock sources. Three modes are designed in power management unit to extend battery life and there is one on-chip debug circuit with two-pin interface for in-system debug on GPM8F3732B.

2. FEATURES

- **CPU**
  - High speed & high performance 1T 8051
    - 100% software compatible with industry standard 8051
    - Pipeline RISC architecture is ten times faster than standard 8051 in executing instructions.
    - Up to 48MHz operating speed
- **Memories**
  - 2.5K bytes XRAM
  - 256 bytes internal Data Memory (IDM) SRAM
  - 32K bytes Flash memory with high endurance
    - Minimum 200,000 program/erase cycles
    - Minimum 20 years of data retention
    - 1KB page size
  - Programming read-only level for software security
- **Clock Management**
  - Internal oscillator: 16MHz±2% @ 2.4V~5.5V
  - Internal oscillator with PLL : 48MHz
- **Power Management**
  - One Sleep mode for power saving
  - One Halt mode for power saving
- **Interrupt Management**
  - 15 interrupt sources
  - Up to 6 external interrupt sources
- **Reset Management**
  - Power On Reset (POR)
  - Low Voltage Reset (LVR)
  - Pad Reset (PAD_RST)
  - Watchdog Reset (WDT_RST)
  - Software Reset (S/W_RST)
  - Flash Access Error Reset (ADDR_ERR_RST)
- **Programmable Watchdog Timer**
  - A time-base generator
  - An event timer
  - System supervisor
- **I/O Ports**
  - Max. of 43 multifunction bi-directional I/Os
  - Each incorporate with pull-up resistor, pull-down resistor, output high, output low , output driving capability and floating input which depending on programmer's settings on the corresponding registers
  - I/O ports with 12mA or 6mA current sink
  - I/O ports with 12mA or 6mA current drive
- **Two 16-bit Timer/Counter (Timer 0/1)**
  - Timer mode with selectable clock source
  - Auto reload 8-bit timers
- **Three Powerful Timers: TimerA/TimerB/TimerC with 16-bit Compare/Capture Unit**
  - Timer mode with selectable clock source
  - Auto-reloadable 16-bit timers
  - Event capture
- **UART0**
  - One synchronous mode
  - Three asynchronous modes
- **SPI (master / slaver mode)**
  - Programmable phase and polarity of master clock
  - Programmable master SPI clock frequency
  - Max SPI clock: 24MHz (F_{pll} /2) @48MHz
- **I2C (master / slaver mode)**
  - Programmable master I2C clock frequency
  - Max. I2C clock: 375KHz (F_{pll} /128) @48MHz
- **A/D Converter**
  - One 8-channel 12-bit resolution ADC
- **Built-in Low Voltage Reset**
  - Trigger level: 1.9V, 2.4V, 3.2V, 4.2V
- **Built-in Low Voltage Detect**
  - Programmable level: 2.1V, 2.6V, 3.4V, 4.4V
- **LCD driver**
  - Up to 4X31 pixels
- **MDU**
  - Built-in 16-bit X 16-bit signed multiplier
  - Built-in 32-bit / 16-bit signed divider
- **Real Time Counter**
  - Up to 60-second real time counter
- **On-chip Debug Unit**

- C-language compatible development tools

■ **Capacitive Touch sensor (CTS)**

- One 16-bit Timer (Timer C) to compute user-specified number of CTS cycle
- One 16-bit Timer (Timer B) to measure the time duration for user-specified number of CTS cycle occurrence.
- One 16-channel Capacitive Touch sensor

Product Number	GPM8F3732B
Speed (MHz)	48
Operating Voltage (V)	2.4~5.5
Flash (Kbytes)	32
XRAM (bytes)	2.5K
IDM (bytes)	256
Timer (sets)	5
UART	1
RTC	1
SPI (master / slaver)	1
I2C (master / slaver)	1
LCD Driver	4X31
8-Channel 12-bit ADC (sets)	1
Multiplier (signed)	16-bit X 16-bit
Divider (signed)	32-bit / 16-bit
IO	43
Capacitive Touch Sensor (channels)	16
Package Type	LQFP48

3. BLOCK DIAGRAM

3.1. GPM8F3732B

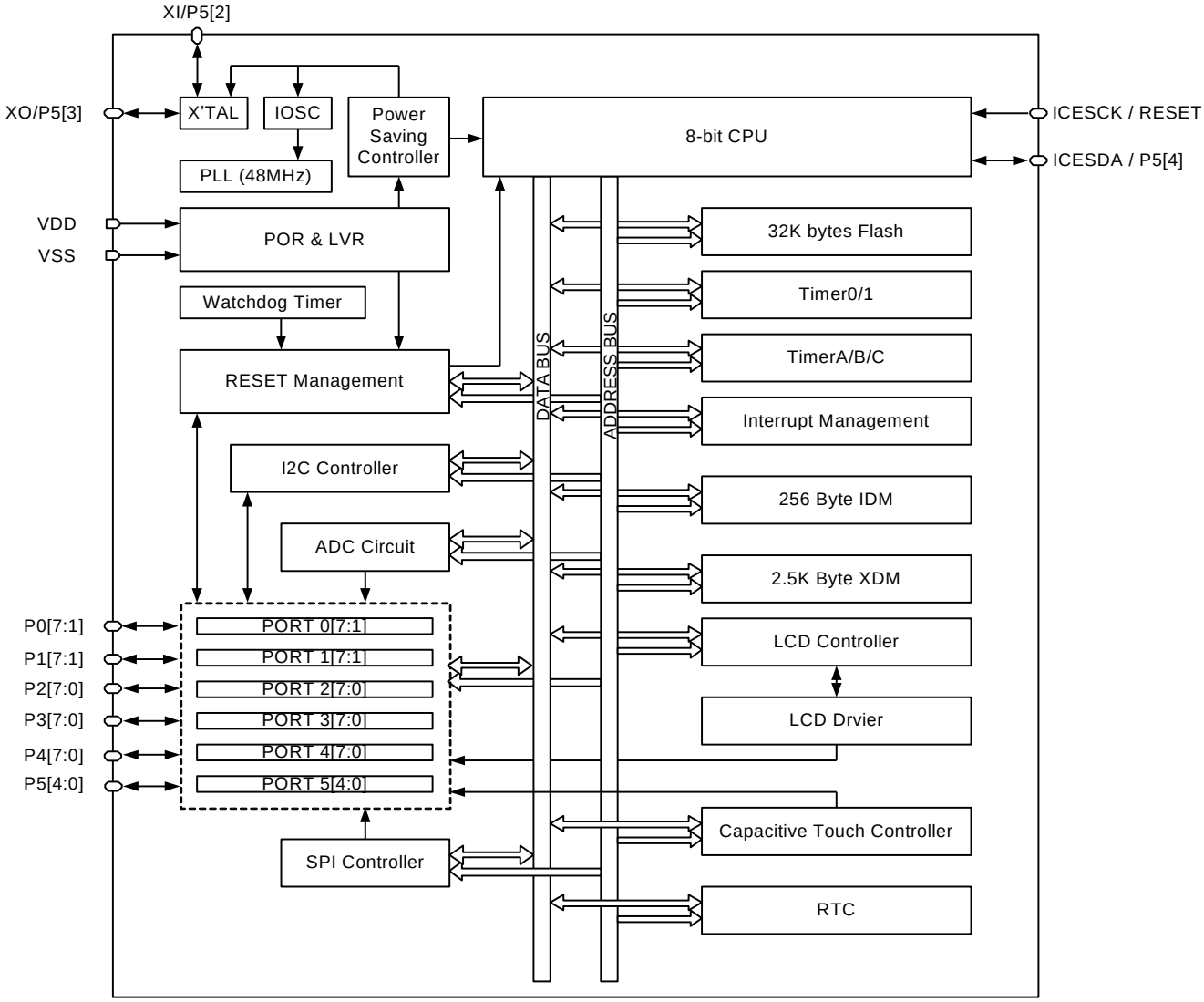


Figure 3-1 Block diagram of GPM8F3732B

4. SIGNAL DESCRIPTIONS

4.1. Pin Descriptions

4.1.1. GPM8F3732B

Type：I = Input, O = Output, S = Supply

Pin Name	LQFP48	Type	Description
VREG	1	O	Regulator out reference voltage.
P01	2	I/O	Port 0 bit 1 / AN01 (ADC0 channel 1 input) / EXT_IRQ1
P02	3	I/O	Port 0 bit 2 / AN02 (ADC0 channel 2 input)
P03	4	I/O	Port 0 bit 3 / AN03 (ADC0 channel 3 input)
P04	5	I/O	Port 0 bit 4 / AN04 (ADC0 channel 4 input)
P05	6	I/O	Port 0 bit 5 / AN05 (ADC0 channel 5 input)
P06	7	I/O	Port 0 bit 6 / AN06 (ADC0 channel 6 input) / I2CDA
P07	8	I/O	Port 0 bit 7 / AN07 (ADC0 channel 7 input) / I2CCK
ADC_VREF	9	O	ADC reference voltage.
P11	10	I/O	Port 1 bit 1 / LCD_COM0
P12	11	I/O	Port 1 bit 2 / LCD_COM1
P13	12	I/O	Port 1 bit 3 / LCD_COM2
P14	13	I/O	Port 1 bit 4 / LCD_COM3
P15	14	I/O	Port 1 bit 5 / UARTRX / LCD_SEG0
P16	15	I/O	Port 1 bit 6 / UARTTX / LCD_SEG1
P17	16	I/O	Port 1 bit 7 / LCD_SEG2
P20	17	I/O	Port 2 bit 0 / LCD_SEG3 / LED_COM0
P21	18	I/O	Port 2 bit 1 / LCD_SEG4 / LED_COM1
P22	19	I/O	Port 2 bit 2 / LCD_SEG5 / LED_COM2
P23	20	I/O	Port 2 bit 3 / LCD_SEG6 / LED_COM3
P24	21	I/O	Port 2 bit 4 / LCD_SEG7 / LED_COM4
P25	22	I/O	Port 2 bit 5 / LCD_SEG8 / LED_COM5
P26	23	I/O	Port 2 bit 6 / LCD_SEG9 / LED_COM6
P27	24	I/O	Port 2 bit 7 / LCD_SEG10 / LED_COM7
P30	25	I/O	Port 3 bit 0 / TCCAP0 / LCD_SEG11 / TH00
P31	26	I/O	Port 3 bit 1 / TCCAP1 / LCD_SEG12 / TH01
P32	27	I/O	Port 3 bit 2 / TCCAP2 / LCD_SEG13 / TH02
P33	28	I/O	Port 3 bit 3 / TCCAP3 / LCD_SEG14 / TH03
P34	29	I/O	Port 3 bit 4 / TCCAP4 / LCD_SEG15 / TH04
P35	30	I/O	Port 3 bit 5 / TCCAP5 / LCD_SEG16 / TH05
P36	31	I/O	Port 3 bit 6 / EXT_IRQ2 / LCD_SEG17 / TH06
P37	32	I/O	Port 3 bit 7 / EXT_IRQ3 / LCD_SEG18 / TH07
P40	33	I/O	Port 4 bit 0 / / TBCAP0 / LCD_SEG19 / TH08
P41	34	I/O	Port 4 bit 1 / TBCAP1 / LCD_SEG20 / TH09
P42	35	I/O	Port 4 bit 2 / TBCAP2 / LCD_SEG21 / TH10
P43	36	I/O	Port 4 bit 3 / TBCAP3 / LCD_SEG22 / TH11
P44	37	I/O	Port 4 bit 4 / TACAP0 / SPICLK / LCD_SEG23 / TH12
P45	38	I/O	Port 4 bit 5 / TACAP1 / SPICSN / LCD_SEG24 / TH13
P46	39	I/O	Port 4 bit 6 / TACAP2 / SPIRX / LCD_SEG25 / TH14
P47	40	I/O	Port 4 bit 7 / TACAP3 / SPITX / UARTTX / LCD_SEG26 / TH15
P50	41	I/O	Port 5 bit 0 / UARTRX / LCD_SEG27

Pin Name	LQFP48	Type	Description
P51	42	I/O	Port 5 bit 1 / LCD_SEG28
P54	43	I/O	Port 5 bit 4 / ICEDA (2 wire serial bus data input/output line) / UARTRX
RESET	44	I	RESET signal, high active/ ICECK (2 wire serial bus clock input line)
P52	45	I/O	Port 5 bit 2 / XTALI / I2CDA / EXT_IRQ4 / TACAP4 / LCD_SEG29
P53	46	I/O	Port 5 bit 3 / XTALO / I2CCK / EXT_IRQ5 / TACAP5 / LCD_SEG30
VDD	47	S	Power 5V input
VSS	48	S	Ground

4.2. PIN Map

Package Pin Sequence - LQFP 48 pin map

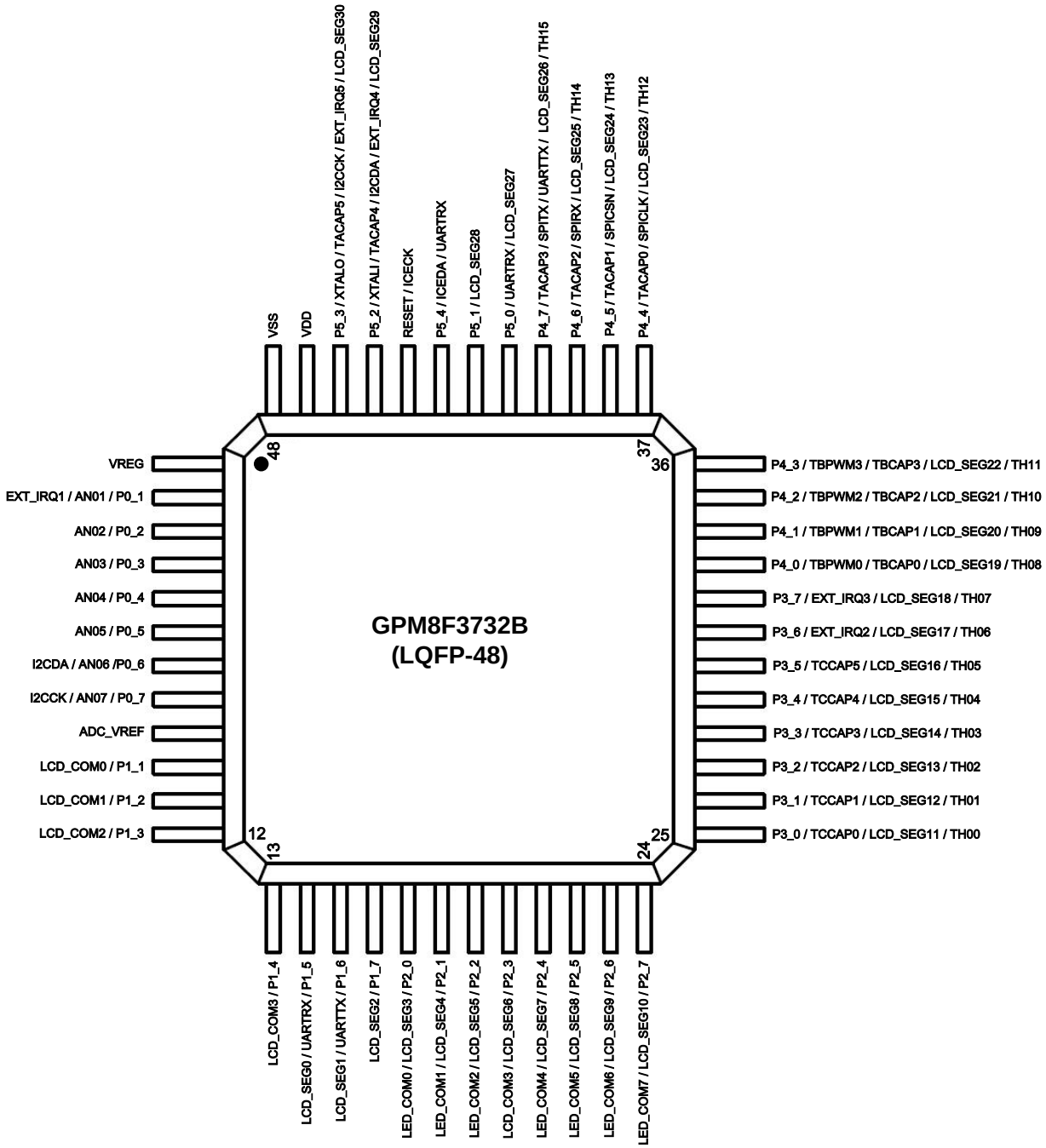


Figure 4-1 pin assignment of GPM8F3732B

5. FUNCTIONAL DESCRIPTIONS

5.1. Central Processing Unit

5.1.1. CPU Introduction

GPM8F3732B's CPU is an ultra-high performance and high speed embedded microcontroller. Pipelined architecture enables the CPU 10 times faster than standard architecture. This performance can also be exploited to great advantage in low power application where the core can be clocked over ten times slower than original implementation without performance loss.

5.1.2. CPU Features

- ❑ 100 % software compatible with industry CPU8051
- ❑ 24 times faster multiplication
- ❑ 12 times faster addition

The CPU is fully compatible with industry standard CPU8051 microcontroller, maintaining all instruction mnemonics and binary compatibility. It incorporates some great architectural enhancements, allowing the CPU instructions executing in high performance at high speed.

The arithmetic section of the processor performs extensive data manipulation and is comprised of an 8-bit arithmetic logic unit (ALU), an ACC(0xE0) register, B(0xF0) register and PSW(0xD0) register.

5.1.3. Arithmetic Logic Unit (ALU)

The ALU performs the arithmetic and logic operations during one instruction execution. Typical arithmetic operations include addition, subtraction, multiplication, and division. Additional operations such as increment, decrement, BCD-decimal-add-adjustment and comparison are also available. Within logic unit, operation such as AND, OR, Exclusive OR, complement and rotation are performed. The Boolean processor performs bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear, and move to/from carry.

5.1.4. Accumulator A register

The Accumulator register is an 8-bit general-purpose register, which can operate with data transferring, temporary saving, condition judgment, etc.

5.1.5. B register

The B register is used during multiplication and division operations. In other cases, it may be used as normal SFR.

5.1.6. Program Status Word (PSW)

The PSW contains several bits that reflect the current state of the CPU which is similar to the flag-register of general CPU.

5.1.7. Program Counter (PC)

The program counter is a 16-bit wide register. It consists of two 8-bit registers: PCH and PCL. This register indicates the address of next instruction to be executed. In Reset state, the content of 0x0000 is stored into program counter.

ACC			**Address: 0xE0**		**Accumulator A Register**			
Bit	7	6	5	4	3	2	1	0
Function	ACC[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	**Function**	**Type**	**Description**	**Condition**
7:0	ACC[7:0]	R/W	Accumulator A	

Table 5-1 The ACC register

B			**Address: 0xF0**		**B Register**			
Bit	7	6	5	4	3	2	1	0
Function	B[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	**Function**	**Type**	**Description**	**Condition**
7:0	B[7:0]	R/W	B	

Table 5-2 The B register

PSW			Address: 0xD0		Program Status Word Register			
Bit	7	6	5	4	3	2	1	0
Function	CY	AC	F0	RS1	RS0	OV	F1	P
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CY	R/W	Carry flag	
6	AC	R/W	Auxiliary carry flag	
5	F0	R/W	General purpose flag 0	
4:3	RS[1:0]	R/W	Register bank select bits RS[1:0] / Function description 00 / Bank 0, data address 0x00-0x07 01 / Bank 1, data address 0x08-0x0F 10 / Bank 2, data address 0x10-0x17 11 / Bank 3, data address 0x18-0x1F	
2	OV	R/W	Overflow flag	
1	F1	R/W	General purpose flag 1	
0	P	R/W	Parity flag	

Table 5-3 The PSW register

5.2. Memory Organization

5.2.1. Introduction

The GPM8F3732B has three separated address spaces for program memory and data memory. The program memory is an on-chip, re-programmable Flash memory containing up to 32K bytes space. The data memory is 2.5K bytes of external RAM, 256 bytes IDM with 128 bytes x 4 pages of SFR which can be read and written. The upper IDM and SFR use the same access address in different access ways which are described in figure 5-2.

5.2.2. Program Memory Allocation

The program memory size is 32KB. If system clock is set to PLL output with 48MHz PLL output frequency. CPU and peripheral will operate in 16MHz frequency and 48MHz respectively. In the code area, the address 0x008F is used for CONFIG_BYTE whose definition of each bit is described in Table 5-4. User can lock the program or content by setting CONFIG_BYTE [0]. If CONFIG_BYTE[0] is programmed to be '0', the whole memory is protected and therefore, any page erase or programming by the two-wire serial interface is not allowed. The only thing user can do is erasing the whole memory. Figure 5-1 shows the program memory map of 32KB Flash.

After each reset, CPU starts execution in the program memory at location 0x0000. Each interrupt has its own start address for service routine. The Flash memory can be programmed in-system, through the ICESCK/ICESDA interface or by software using the MOVX instruction when PWE= 1. User can refer to the example code in the programming guide for the procedure of writing and erasing operations. Flash data cannot be programmed from a '0' to '1', and only erase operation can be accepted. Therefore, flash data would typically be erased (set to 0xFF) before being programmed. The write and erase operations are executed by using Pseudo-idle mode to be automatically timed by hardware without data polling to determine the end of the write and erase operation.

For software security consideration, user can set the programmable Flash level by FLH_CTRL1 register to protect the code area being inadvertently erased or written by software; the protected region is called READONLY_PAGE.

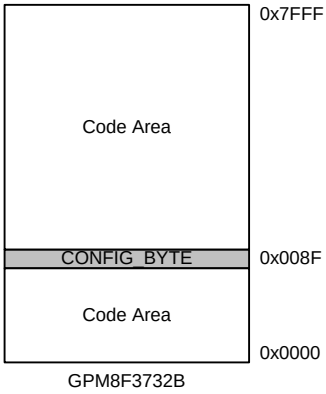


Figure 5-1 Program memory organization

CONFIG_BYTE			Address: 0x8F (Code Area)		CONFIG_BYTE Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	--	CODE Lock
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:1	--	R	Reserved	
0	CODE Lock	R	0 : CODE is locked; 1 : CODE is unlocked	

Table 5-4 The CONFIG_BYTE register

FLH_CTRL0			Address: 0xEC		Flash Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	FLH_PERASE	FLH_PROG
Default	0	0	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x51							

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1	FLH_PERASE	R/W	Flash page erase enable bit. 0: Flash page erase is disabled 1: Flash page erase is enabled	
0	FLH_PROG		Flash program enable bit. 0: Flash program is disabled 1: Flash program is enabled	

Table 5-5 The FL_LEVELLASH_CTRL0 register

FLH_CTRL1			Address: 0xED		Flash Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	FLASH_LEVEL[4:0]				
Default	0	0	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x51							

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>4:0</td><td>FLASH_LEVEL[4:0]</td><td>R/W</td><td>FLASH_LEVEL, it determines how many 1K pages are read only
<table>
<tr><td>FLASH_LEVEL</td><td>Note</td></tr>
<tr><td>0</td><td>no page is read only</td></tr>
<tr><td>1</td><td>address < 0x800 is read only</td></tr>
<tr><td>2</td><td>address < 0xC00 is read only</td></tr>
<tr><td>3</td><td>address < 0x1000 is read only</td></tr>
<tr><td>4</td><td>address < 0x1400 is read only</td></tr>
<tr><td>5</td><td>address < 0x1800 is read only</td></tr>
<tr><td>6</td><td>address < 0x1C00 is read only</td></tr>
<tr><td>7</td><td>address < 0x2000 is read only</td></tr>
<tr><td>8</td><td>address < 0x2400 is read only</td></tr>
<tr><td>9</td><td>address < 0x2800 is read only</td></tr>
<tr><td>10</td><td>address < 0x2C00 is read only</td></tr>
<tr><td>11</td><td>address < 0x3000 is read only</td></tr>
<tr><td>12</td><td>address < 0x3400 is read only</td></tr>
<tr><td>13</td><td>address < 0x3800 is read only</td></tr>
<tr><td>14</td><td>address < 0x3C00 is read only</td></tr>
<tr><td>15</td><td>address < 0x4000 is read only</td></tr>
<tr><td>16</td><td>address < 0x4400 is read only</td></tr>
<tr><td>17</td><td>address < 0x4800 is read only</td></tr>
<tr><td>18</td><td>address < 0x4C00 is read only</td></tr>
<tr><td>19</td><td>address < 0x5000 is read only</td></tr>
<tr><td>20</td><td>address < 0x5400 is read only</td></tr>
<tr><td>21</td><td>address < 0x5800 is read only</td></tr>
<tr><td>22</td><td>address < 0x5C00 is read only</td></tr>
<tr><td>23</td><td>address < 0x6000 is read only</td></tr>
<tr><td>24</td><td>address < 0x6400 is read only</td></tr>
<tr><td>25</td><td>address < 0x6800 is read only</td></tr>
<tr><td>26</td><td>address < 0x6C00 is read only</td></tr>
<tr><td>27</td><td>address < 0x7000 is read only</td></tr>
<tr><td>28</td><td>address < 0x7400 is read only</td></tr>
<tr><td>29</td><td>address < 0x7800 is read only</td></tr>
<tr><td>30</td><td>address < 0x7C00 is read only</td></tr>
<tr><td>31</td><td>address < 0x8000 is read only</td></tr>
</table>
Note 1: Only FLASH_LEVEL[4:0] is useful in GPM8F3732B</td><td></td></tr>
</table>

Table 5-6 The FLH_CTRL1 register

5.2.3. Data Memory Allocation

Data memory addresses allocates on the GPM8F3732B are divided into two parts. The first part is 2.5K bytes of external RAM and the second one is 256 byte IDM shown in figure 5-2. The lowest internal data memory (IDM) consists of four register banks with eight registers each. A bit addressable segment with 128 bits (16 bytes) begins at 0x20. The address from 0x30 to 0x7F is not defined and can be utilized freely by user. The last 128 bytes of data memory can be used by different addressing modes. With the indirect addressing mode, addresses from 0x80 to 0xFF are shared with stack space. With the direct addressing mode, the SFR addressing from 0x80 to 0xFF is accessed. The SFR memory map is shown in

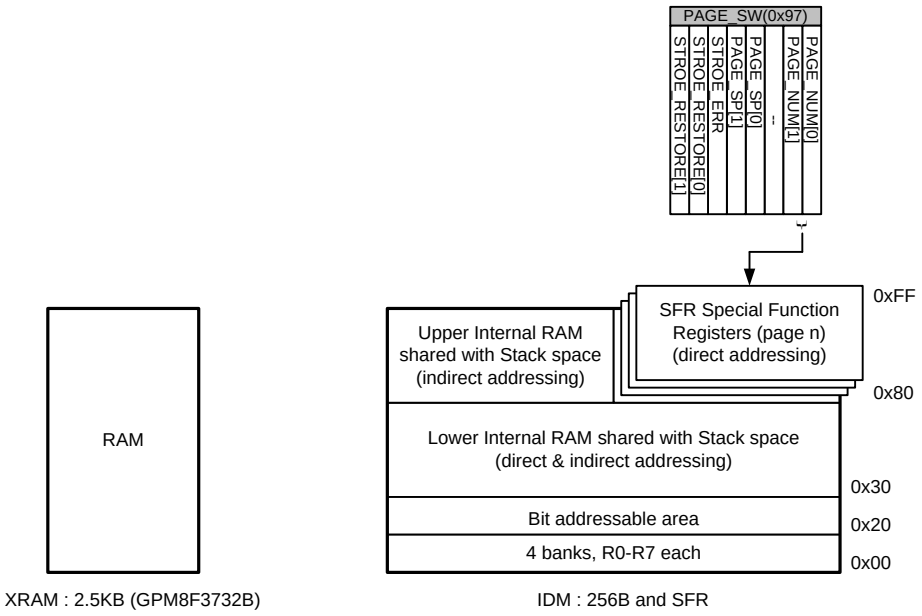


Figure 5-2 Data memory organization

Note1: Gray Area: common SFR register; White area : additional SFR register;
Note2: Switch page is unnecessary when user gray area is written.

Page0	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	EIP	SYS_CTRL0	SYS_CTRL1	SYS_CTRL2	SYS_CTRL3	SYS_CTRL4	SYS_CTRL5	SYS_CTRL6
0xF0	B							
0xE8	EIE			KEYCODE	FLH_CTRL0	FLH_CTRL1		
0xE0	ACC					EXT_INT_EN	EXT_INT_EDGE	EXT_INT_STS
0xD8	WDCON	ADC0_CTRL0	ADC0_CTRL1	ADC0_DATA_L	ADC0_DATA_H	ADC_VREF_CTRL		
0xD0	PSW	I2C_CTRL	I2C_STS	I2C_DID	I2C_DATA			
0xC8	P5	P5_ID						I2C_DEBOUNCE
0xC0	P4	P4_ID						
0xB8	IP	P1_ID	P1_DIR	P1_ATT	P1_DRV	P1_SR		
0xB0	P3	P3_ID	P3_DIR	P3_ATT	P3_DRV	P3_SR		
0xA8	IE	P0_ID	P0_DIR	P0_ATT	P0_DRV	P0_SR		
0xA0	P2	P2_ID	P2_DIR	P2_ATT	P2_DRV	P2_SR	P2_HS	
0x98	SCON0	SBUF0	SPI_CTRL	SPI_STS	SPI_TXD	SPI_RXD	BODY_ID0	BODY_ID1
0x90	P1	EIF						PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Page1	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	EIP						SYS_CTRL5	SYS_CTRL6
0xF0	B							
0xE8	EIE			KEYCODE	FLH_CTRL0	FLH_CTRL1		
0xE0	ACC							EXT_INT_STS
0xD8	WDCON	CTS_CTRL0	CTS_CTRL1	CTS_CTRL2	CTS_CTRL3	CTS_CTRL4	CTS_CTRL5	
0xD0	PSW							
0xC8	P5	P5_ID	P5_DIR	P5_ATT	P5_DRV	P5_SR		

0xC0	P4	P4_ID	P4_DIR	P4_ATT	P4_DRV	P4_SR		
0xB8	IP	P1_ID	LCD_COM3_D7_0	LCD_COM3_D15_8	LCD_COM3_D23_16	LCD_COM3_D30_24		
0xB0	P3	P3_ID	LCD_COM2_D7_0	LCD_COM2_D15_8	LCD_COM2_D23_16	LCD_COM2_D30_24		
0xA8	IE	P0_ID	LCD_COM1_D7_0	LCD_COM1_D15_8	LCD_COM1_D23_16	LCD_COM1_D30_24		
0xA0	P2	P2_ID	LCD_COM0_D7_0	LCD_COM0_D15_8	LCD_COM0_D23_16	LCD_COM0_D30_24		
0x98	SCON0	SBUF0	LCD_CTRL0	LCD_CTRL1	LCD_SEG_EN0	LCD_SEG_EN1	LCD_SEG_EN2	LCD_SEG_EN3
0x90	P1	EIF					RTC_CTRL	PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON
Page2	*0/8*	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*
0xF8	EIP						SYS_CTRL5	SYS_CTRL6
0xF0	B							
0xE8	EIE			KEYCODE	FLH_CTRL0	FLH_CTRL1		
0xE0	ACC							EXT_INT_STS
0xD8	WDCON							
0xD0	PSW	TMC_CAP4_L	TMC_CAP4_H	TMC_CAP5_L	TMC_CAP5_H			
0xC8	P5	P5_ID	TMC_CAP1_L	TMC_CAP1_H	TMC_CAP2_L	TMC_CAP2_H	TMC_CAP3_L	TMC_CAP3_H
0xC0	P4	P4_ID	TMC_CAP_CTRL1	TMC_CAP_CTRL2	TMC_CAP_INTEN	TMC_CAP_INTSTS	TMC_CAP0_L	TMC_CAP0_H
0xB8	IP	P1_ID	TMC_CTRL	TMC_PLOAD_L	TMC_PLOAD_H	TMC_L	TMC_H	TMC_CAP_CTRL0
0xB0	P3	P3_ID	TMB_CCP3_L	TMB_CCP3_H				
0xA8	IE	P0_ID	TMB_CCP0_L	TMB_CCP0_H	TMB_CCP1_L	TMB_CCP1_H	TMB_CCP2_L	TMB_CCP2_H
0xA0	P2	P2_ID	TMB_CAP_CTRL1	TMB_CAP_INTCTR				
0x98	SCON0	SBUF0	TMB_CTRL	TMB_PLOAD_L	TMB_PLOAD_H	TMB_L	TMB_H	TMB_CAP_CTRL0
0x90	P1	EIF						PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON
Page3	*0/8*	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*
0xF8	EIP						SYS_CTRL5	SYS_CTRL6
0xF0	B							
0xE8	EIE			KEYCODE	FLH_CTRL0	FLH_CTRL1		
0xE0	ACC							EXT_INT_STS
0xD8	WDCON	MDU_CTRL	MDU_DSRC_ADR0	MDU_DSRC_ADR1	MDU_DTAR_ADDR			
0xD0	PSW							
0xC8	P5	P5_ID						
0xC0	P4	P4_ID						
0xB8	IP	P1_ID	TMA_CCP4_L	TMA_CCP4_H	TMA_CCP5_L	TMA_CCP5_H		
0xB0	P3	P3_ID	TMA_CCP1_L	TMA_CCP1_H	TMA_CCP2_L	TMA_CCP2_H	TMA_CCP3_L	TMA_CCP3_H
0xA8	IE	P0_ID					TMA_CCP0_L	TMA_CCP0_H
0xA0	P2	P2_ID	TMA_CAP_CTRL1	TMA_CAP_CTRL2	TMA_CAP_INTEN	TMA_CAP_INTSTS		
0x98	SCON0	SBUF0	TMA_CTRL	TMA_PLOAD_L	TMA_PLOAD_H	TMA_L	TMA_H	TMA_CAP_CTRL0
0x90	P1	EIF						PAGE_SW
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*

Table 5-7 SFR memory map

PAGE_SW			Address: 0x97		Page Switch Register			
Bit	7	6	5	4	3	2	1	0
Function	STORE_RESTORE		STORE_ERR	PAGE_SP		--	PAGE_NUM	
Default	0	0	0	0	0	0	0	0

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:6</td><td>STORE_RESTORE</td><td>W</td><td>PAGE_NUM load or restore contorl bit.
<table>
<tr><td>STORE_RESTORE</td><td>Description</td></tr>
<tr><td>0X</td><td>The PAGE_NUM is directly updated by CPU write and PAGE_SP is inactive.</td></tr>
<tr><td>10</td><td>The latest page number is written to the PAGE_NUM. In the same time, the previous contents of PAGE_NUM are saved in the storage register which is indicated by PAGE_SP.</td></tr>
<tr><td>11</td><td>The PAGE_NUM is overwritten by the contents of the storage register which indicated by PAGE_SP and the CPU write will be ignored.</td></tr>
</table></td><td></td></tr>
<tr><td>5</td><td>STORE_ERR</td><td>R/W</td><td>This bit is used to indicate the status of PAGE_NUM store / restore function.
read:
0: page number store / restore function is normally operating.
1: page number store / restore function is abnormal because successive store or restore is over 2 times.
write:
0: clears this bit
1: no effect</td><td></td></tr>
<tr><td>4:3</td><td>PAGE_SP</td><td>R</td><td>Page number storage pointer</td><td></td></tr>
<tr><td>2</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
<tr><td>1:0</td><td>PAGE_NUM</td><td>R/W</td><td>These bits are used to indicate which SFR page is active now.
00: page 0
01: page 1
10: page 2
11: page 3</td><td></td></tr>
</table>

Table 5-8 The PAGE_SW register

5.2.4. Memory Related SFR

The following sub-sections describe program, external and internal memory relevant to SFRs of 8051 core and their functionalities. For more information about standard SFRs, please refer to appropriate peripheral section.

5.2.4.1. Program write enable bit

The Program Write Enable (PWE) bit, located in PCON register bit 4, is used during MOVX instructions. When PWE bit is set to logic 1, the MOVX @DPTR, An instruction writes data located in accumulator register into program memory addressed by DPTR register. Program memory can be read by MOVC only regardless of PWE bit.

5.2.4.2. Data pointer registers

Dual data pointer registers are implemented to speed up data block copying. DPTR0 and DPTR1 are located in four SFR addresses. Active DPTR register is selected by SEL bit (DPS[0]). If SEL=0, DPTR0 is selected, otherwise DPTR1.

5.2.4.3. Stack pointer

The 8051 has 8-bit stack pointer called SP (0x81) located in the internal RAM space. It is incremented before data is stored during PUSH and CALL execution and decremented after data is popped during POP, RET and RETI execution. In the other words, it always points to the last valid stack byte. The SP is accessed as any other SFRs. Figure 5-3 shows an example when PUSH A is executed and Figure 5-4 shows an example when POP PSW is executed.

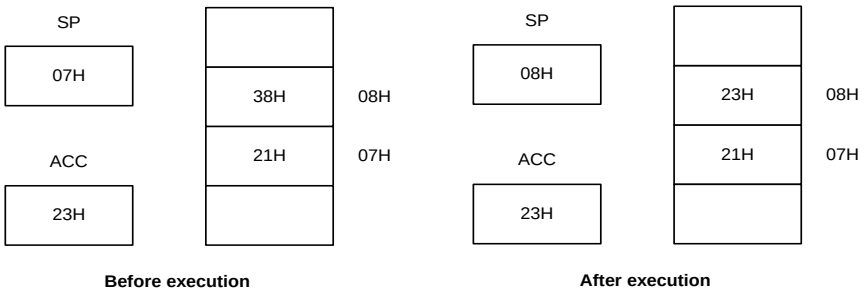


Figure 5-3 Stack byte order for PUSH A instruction

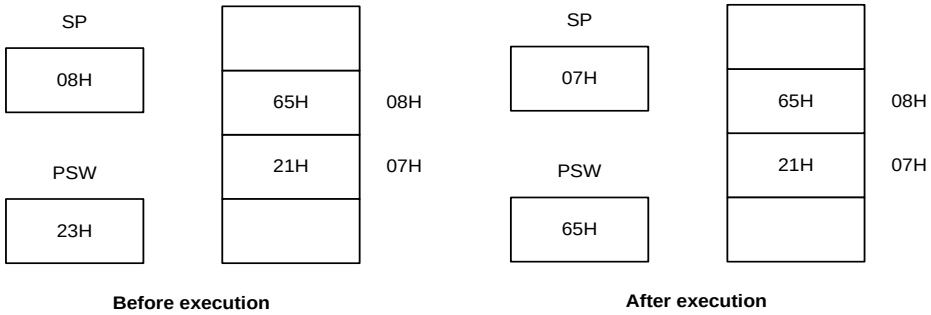


Figure 5-4 Stack byte order for POP PSW instruction

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 double baud rate bit when clocked by Timer1	
5	--	R/W	Reserved	
4	PWE	R/W	Program Write Enable (PWE)	

Bit	Function	Type	Description	Condition
			0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3:2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-9 The PCON register

DPH0			Address: 0x83		Data Pointer Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[15:8]	R/W	Data pointer register DPTR0 - high byte	

Table 5-10 The DPH0 register

DPL0			Address: 0x82		Data Pointer Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[7:0]	R/W	Data pointer register DPTR0 - low byte	

Table 5-11 The DPL0 register

DPH1			Address: 0x85		Data Pointer 1 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR1[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[15:8]	R/W	Data pointer 1 register DPTR1 - high byte	

Table 5-12 The DPH1 register

DPL1			Address: 0x84		Data Pointer 1 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[7:0]	R/W	Data pointer 1 register DPTR1 - low byte	

Table 5-13 The DPL1 register

DPS			Address: 0x86		Data Pointer Select Register			
Bit	7	6	5	4	3	2	1	0
Function	ID1	ID0	TSL	-	-	-	-	SEL
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	ID[1:0]	R/W	Increment/decrement function select. See Table 5-15	
5	TSL	R/W	Toggle selection enable bit 0: DPTR related instructions do not affect state of SEL bit 1: DPTR related instructions to toggle the SEL bit p.s. The DPTR related instructions are as below a. MOVX A,@DPTR b. MOVX @DPTR,A c. INC DPTR d. MOV DPTR,#data16 e. MOVC A,@A+DPTR	
4:1	--	R/W	Reserved	
0	SEL	R/W	Active data pointer select bit See Table 5-15	

Table 5-14 The DPS register

ID1	ID0	SEL=0	SEL=1
0	0	INC DPTR0	INC DPTR1
0	1	DEC DPTR0	INC DPTR1
1	0	INC DPTR0	DEC DPTR1
1	1	DEC DPTR0	DEC DPTR1

Table 5-15 DPTR0/DPTR1 operations

SP			Address: 0x81		Stack Pointer Register			
Bit	7	6	5	4	3	2	1	0
Function	SP[7:0]							
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:0	SP[7:0]	R/W	Stack pointer	

Table 5-16 The SP register

5.3. Special Function Registers (SFR)

GPM8F3732B has up to 185 control registers for special function registers. All of the SFRs are used by MCU and peripheral function block for controlling the desired operation. Some of the SFRs contain control and status bits for peripheral module such as Timer unit, Interrupt control unit, etc. Some bits in SFRs are read only so that writing to those bits doesn't have any effect on corresponding bits. Some SFRs have key code design that KEYCODE register must be written with correct key codes, in sequence, before writing a value to it for software security. The following table shows the summary of the SFRs. The detailed information of each SFRs are explained in each peripheral section.

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
Any	0x80	P0		0xFF	Port 0							
Any	0x81	SP		0x07	Stack Pointer							
Any	0x82	DPL0		0x00	Data pointer register DPTR0 - low byte							
Any	0x83	DPH0		0x00	Data pointer register DPTR0 - high byte							
Any	0x84	DPL1		0x00	Data pointer register DPTR1 - low byte							
Any	0x85	DPH1		0x00	Data pointer register DPTR1 - high byte							
Any	0x86	DPS		0x00	ID1	ID0	TSL	--	--	--	--	SEL
Any	0x87	PCON		0x00	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Any	0x88	TCON		0x00	TF1	TR1	TF0	TR0	ADCF	--	TAF	--
Any	0x89	TMOD		0x00	--	CT1	M11	M10	--	CT0	M01	M00
Any	0x8A	TL0		0x00	Timer 0 Load value – low byte							
Any	0x8B	TL1		0x00	Timer 1 Load value – low byte							
Any	0x8C	TH0		0x00	Timer 0 Load value – high byte							
Any	0x8D	TH1		0x00	Timer 1 Load value – high byte							
Any	0x8E	CKCON		0x07	WD1	WD0	WDFM	T1M	T0M	--	--	--
Any	0x90	P1		0xFF	Port 1							
Any	0x91	EIF		0x00	--	--	--	EXTF	LVDF	SPIF	I2CF	MDUF
Any	0x97	PAGE_SW		0x00	STORE_RESTORE[1:0]		STORE_ERR	PAGE_SP[1:0]		--	PAGE_NUM[1:0]	
Any	0x98	SCON0		N/A	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Any	0x99	SBUF0		N/A	UART 0 buffer							
Any	0xA0	P2		0xFF	Port 2							
Any	0xA1	P2_ID		0x00	Port 2 input data							
Any	0xA8	IE		0x00	EA	ETC	ETB	ES0	ET1	EADC	ET0	ETA
Any	0xA9	P0_ID		0x00	Port 0 input data							
Any	0xB0	P3		0xFF	Port 3							
Any	0xB1	P3_ID		0x00	Port 3 input data							
Any	0xB8	IP		0x00	--	PTC	PTB	PS0	PT1	PADC	PT0	PTA
Any	0xB9	P1_ID		0x00	Port 1 input data							
Any	0xC0	P4		N/A	Port 4							
Any	0xC1	P4_ID		0x00	Port 4 input data							
Any	0xC8	P5		N/A	DIV_INTF	MUL_INTF	--	Port 5[4:2]			--	--
Any	0xC9	P5_ID		0x00	--	--	--	Port 5 input data[4:2]			--	--
Any	0xD0	PSW		0x00	CY	AC	F0	RS1	RS0	OV	F1	P
Any	0xD8	WDCON		0x00	--	--	--	--	WDIF	--	EWT	RWT
Any	0xE0	ACC		0x00	ACC register							
Any	0xE7	EXT_INT_STS		0x00	--	--	EXT_INT_STS[5:0]					
Any	0xE8	EIE		0x00	--	--	EWDI	EEXT	ELVD	ESPI	EI2C	EMDU

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
Any	0xEB	KEYCODE		0x00	Key Code							
Any	0xEC	FLH_CTRL0	8F/32/51	0x00	--	--	--	--	--	--	FLH_PERASE	FLH_PROG
Any	0xED	FLH_CTRL1	8F/32/51	0x00	--	--	--	FLASH_LEVEL[4:0]				
Any	0xF0	B		0x00	B register							
Any	0xF8	EIP		0x00	--	--	PWDI	PEXT	PLVD	PSPI	PI2C	PMDU
Any	0xFE	SYS_CTRL5	8F/32/50	0xC0	TMR_CKEN	LCD_CKEN	MDU_CKEN	TH_CKEN	SPI_CKEN	UART_CKEN	I2C_CKEN	ADC_CKEN
Any	0xFF	SYS_CTRL6	8F/32/50	0x00	UART_IF_SEL[1:0]		UART_IF_EN	T01_CK_SEL	--	AERR_RSTEN	WDOG_CKEN	RTC_CKEN

Table 5-17 The common SFR register

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0	0x9A	SPI_CTRL		0x00	POLARITY	PHASE	CSB_KEEP	SPI_CLK_SEL[1:0]		SPI_EN	SPI_MODE	SPI_START
0	0x9B	SPI_STS		0x00	SPI_INTEN	--	--	--	--	--	RX_DONE	TX_DONE
0	0x9C	SPI_TXD		0x00	SPI transmission data							
0	0x9D	SPI_RXD		0x00	SPI receive data							
0	0x9E	BODY_ID0		0x00	BODY ID0							
0	0x9F	BODY_ID1		0x00	BODY ID1							
0	0xA2	P2_DIR		0x00	Port 2 direction control bit							
0	0xA3	P2_ATT		0x00	Port 2 attribute control bit							
0	0xA4	P2_DRV		0x00	Port 2 driving capability control bit							
0	0xA	P2_SR		0x00	Port 2 slew rate control bit							
0	0xA6	P2_HS		0x00	Port 2 high sink current control bit							
0	0xAA	P0_DIR		0x00	Port 0 direction control bit							
0	0xAB	P0_ATT		0x00	Port 0 attribute control bit							
0	0xAC	P0_DRV		0x00	Port 0 driving capability control bit							
0	0xAD	P0_SR		0x00	Port 0 slew rate control bit							
0	0xB2	P3_DIR		0x00	Port 3 direction control bit							
0	0xB3	P3_ATT		0x00	Port 3 attribute control bit							
0	0xB4	P3_DRV		0x00	Port 3 driving capability control bit							
0	0xB5	P3_SR		0x00	Port 3 slew rate control bit							
0	0xBA	P1_DIR		0x00	Port 1 direction control bit							
0	0xBB	P1_ATT		0x00	Port 1 attribute control bit							
0	0xBC	P1_DRV		0x00	Port 1 driving capability control bit							
0	0xBD	P1_SR		0x00	Port 1 slew rate control bit							
0	0xCF	I2C_DEBOUNCE		0x00	--	--	I2C de-bounce count[5:0]					
0	0xD1	I2C_CTRL		0x20	MST_STR	MST_STP	MST_NACK	MODE	I2C_CLK_SEL[1:0]		I2C_TRIG	I2C_EN
0	0xD2	I2C_STS		0x00	SLV_DID_OK	SLV_DAT_OK	SLV_STP_OK	ERR_SDID_IE	I2C_IF_SEL	I2C_INT_EN	NO_ACK	TS_DONE
0	0xD3	I2C_DID		0x01	I2C device ID							
0	0xD4	I2C_DATA		0x00	I2C Tx / Rx data							
0	0xD9	ADC0_CTRL0		0x00	ADC0_INTEN	ADC0_SH_CYCLE[1:0]		ADC0_CLK_SEL[1:0]			--	--
0	0xDA	ADC0_CTRL1		0x00	ADC0_START	--	--	ADC0_INTF	--	ADC0_CH_SEL[2:0]		
0	0xDB	ADC0_DATA_L		0x00	ADC0 output data – low nibble byte				--	--	--	--
0	0xDC	ADC0_DATA_H		0x00	ADC0 output data – high byte							
0	0xDD	ADC_VREF_CTRL		0x00	--	--	--	--	ADCVREF_SEL[2:0]			ADVREF_EN

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0	0xE5	EXT_INT_EN		0x00	DEBOUNCE_TIME[1:0]		EXT_INT_EN					
0	0xE6	EXT_INT_EDGE		0x00	--	--	EXT_INT_EDGE					
0	0xF9	SYS_CTRL0	8F/32/50	0x01	CK_32K_SEL	CLK_DIV[1:0]		XTAL_CAP_SEL[1:0]		XTAL_SEL[1:0]		XTAL_ENB
0	0xFA	SYS_CTRL1	8F/32/50	0x00	PLL_LOCKIN	--	PLL_N	CLK_DIV_SEL	--	CLK_SRC_SEL	PLL_CHG_EN	PLL_EN
0	0xFB	SYS_CTRL2	8F/32/50	0x01	HALT_I_SEL[2:0]			HALT_EN	V18_SEL[1:0]		IOSC32K_EN	--
0	0xFC	SYS_CTRL3	8F/32/50	0x24	--	LVD_INT_EN	LVD_SEL[1:0]		LVD_EN	LVR_SEL[1:0]		LVR_EN
0	0xFD	SYS_CTRL4	8F/32/50	0x00	MISS_CLK	WDOG_RST	SW_RST_EN	LVR_RST	LVD_INTF	LVD_STS	ADDR_ERR	ERR_WR

Table 5-18 The additional SFR register (page0)

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
1	0x96	RTC_CTRL		0x00	RTC_INTF	--	--	--	--	COUNT_SEL[1:0]		RTC_EN
1	0x9A	LCD_CTRL0		0x00	VBLK_INTEN	FR_SEL[1:0]		UP_DATE_EN	COM_MODE[1:0]		LCD_EN	LCD_BIASEN
1	0x9B	LCD_CTRL1		0x00	--	VBLK_INTF	ACT_COM[1:0]		SH_DUTY_SEL[1:0]		BIAS_DUTY_SEL[1:0]	
1	0x9C	LCD_SEG_EN0		0x00	LCD segment[7:0] enable							
1	0x9D	LCD_SEG_EN1		0x00	LCD segment[15:8] enable							
1	0x9E	LCD_SEG_EN2		0x00	LCD segment[23:16] enable							
1	0x9F	LCD_SEG_EN3		0x00	--	LCD segment[30:24] enable						
1	0xA2	LCD_C0_D7_0		0x00	LCD common-0 data[7:0]							
1	0xA3	LCD_C0_D15_8		0x00	LCD common-0 data[15:8]							
1	0xA4	LCD_C0_D23_16		0x00	LCD common-0 data[23:16]							
1	0xA5	LCD_C0_D30_24		0x00	--	LCD common-0 data[30:24]						
1	0xAA	LCD_C1_D7_0		0x00	LCD common-1 data[7:0]							
1	0xAB	LCD_C1_D15_8		0x00	LCD common-1 data[15:8]							
1	0xAC	LCD_C1_D23_16		0x00	LCD common-1 data[23:16]							
1	0xAD	LCD_C1_D30_24		0x00	--	LCD common-1 data[30:24]						
1	0xB2	LCD_C2_D7_0		0x00	LCD common-2 data[7:0]							
1	0xB3	LCD_C2_D15_8		0x00	LCD common-2 data[15:8]							
1	0xB	LCD_C2_D23_16		0x00	LCD common-2 data[23:16]							
1	0xB5	LCD_C2_D30_24		0x00	--	LCD common-2 data[30:24]						
1	0xBA	LCD_C3_D7_0		0x00	LCD common-3 data[7:0]							
1	0xBB	LCD_C3_D15_8		0x00	LCD common-3 data[15:8]							
1	0xBC	LCD_C3_D23_16		0x00	LCD common-3 data[23:16]							
1	0xBD	LCD_C3_D30_24		0x00	--	LCD common-3 data[30:24]						
1	0xC2	P4_DIR		0x00	Port 4 direction control bit							
1	0xC3	P4_ATT		0x00	Port 4 attribute control bit							
1	0xC4	P4_DRV		0x00	Port 4 driving capability control bit							
1	0xC5	P4_SR		0x00	Port 4 slew rate control bit							
1	0xCA	P5_DIR		0x00	--	--	--	Port 5 direction control bit[4:2]			--	--
1	0xCB	P5_ATT		0x00	--	--	--	Port 5 attribute control bit[4:2]			--	--
1	0xCC	P5_DRV		0x00	--	--	--	Port 5 driving capability control bit[4:2]			--	--
1	0xCD	P5_SR		0x00	--	--	--	Port 5 slew rate control bit[4:2]			--	--
1	0xD9	CTS_CTRL0		0x00	--	--	VTOPSEL[1:0]		VTOP_EN	TRIEN	CTSST	CTSEN
1	0xDA	CTS_CTRL1		0x00	CHSEL[7:0]							

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
1	0xDB	CTS_CTRL2		0x00	CHSEL[15:8]							
1	0xDC	CTS_CTRL3		0x00	LPFSEL[1:0]		VRSEL	DLSEL	CTSDC	ISEL[2:0]		
1	0xDD	CTS_CTRL4		0x00	MUPORTSEL[2:0]			MUPINSEL			MUTPOL	MUTEN
1	0xDE	CTS_CTRL5		0x00	MUTSEL_SEL[3:0]				--	--	--	TSCFG

Table 5-19 The additional SFR register (page1)

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
2	0x9A	TMB_CTRL		0x00	TMB_EDGE	ALIGN_TYPE	TMB_INTF	TMB_INTEN	CLK_SRC_SEL[2:0]			TMB_EN
2	0x9B	TMB_PLOAD_L		0x00	Timer B pre-load data– low byte							
2	0x9C	TMB_PLOAD_H		0x00	Timer B pre-load data – high byte							
2	0x9D	TMB_L		0x00	Timer B – low byte							
2	0x9E	TMB_H		0x00	Timer B – high byte							
2	0x9F	TMB_CAP_CTRL0		0x00	--	--	--	--	Timer B capture enable			
2	0xA2	TMB_CAP_CTRL1		0x00	TMB_CAP3_EDGE[1:0]		TMB_CAP2_EDGE[1:0]		TMB_CAP1_EDGE[1:0]		TMB_CAP0_EDGE[1:0]	
2	0xA3	TMB_CAP_INTCR		0x00	TMB_CAP_STS[3:0]				TMB_CAP_INTEN[3:0]			
2	0xAA	TMB_CCP0_L		0x00	Timer B CCP0 – low byte							
2	0xAB	TMB_CCP0_H		0x00	Timer B CCP0 – high byte							
2	0xAC	TMB_CCP1_L		0x00	Timer B CCP1 – low byte							
2	0xAD	TMB_CCP1_H		0x00	Timer B CCP1 – high byte							
2	0xAE	TMB_CCP2_L		0x00	Timer B CCP2 – low byte							
2	0xAF	TMB_CCP2_H		0x00	Timer B CCP2 – high byte							
2	0xB2	TMB_CCP3_L		0x00	Timer B CCP3 – low byte							
2	0xB3	TMB_CCP3_H		0x00	Timer B CCP3 – high byte							
2	0xBA	TMC_CTRL		0x00	--	--	TMC_INTF	TMC_INTEN	CLK_SRC_SEL[2:0]			TMC_EN
2	0xBB	TMC_PLOAD_L		0x00	Timer C pre-load data – low byte							
2	0xBC	TMC_PLOAD_H		0x00	Timer C pre-load data – high byte							
2	0xBD	TMC_L		0x00	Timer C – low byte							
2	0xBE	TMC_H		0x00	Timer C – high byte							
2	0xBF	TMC_CAP_CTRL0		0x00	--	--	Timer C capture enable					
2	0xC2	TMC_CAP_CTRL1		0x00	TMC_CAP3_EDGE[1:0]		TMC_CAP2_EDGE[1:0]		TMC_CAP1_EDGE[1:0]		TMC_CAP0_EDGE[1:0]	
2	0xC3	TMC_CAP_CTRL2		0x00	--	--	--	--	TMC_CAP5_EDGE[1:0]		TMC_CAP4_EDGE[1:0]	
2	0xC4	TMC_CAP_INTEN		0x00	--	--	Timer C capture interrupt enable					
2	0xC5	TMC_CAP_INTSTS		0x00	--	--	Timer C capture interrupt status flag					
2	0xC6	TMC_CAP0_L		0x00	TMC_CAP0 – low byte							
2	0xC7	TMC_CAP0_H		0x00	TMC_CAP0 – high byte							
2	0xCA	TMC_CAP1_L		0x00	TMC_CAP1 – low byte							
2	0xCB	TMC_CAP1_H		0x00	TMC_CAP1 – high byte							
2	0xCC	TMC_CAP2_L		0x00	TMC_CAP2 – low byte							
2	0xCD	TMC_CAP2_H		0x00	TMC_CAP2 – high byte							
2	0xCE	TMC_CAP3_L		0x00	TMC_CAP3 – low byte							
2	0xCF	TMC_CAP3_H		0x00	TMC_CAP3 – high byte							
2	0xD1	TMC_CAP4_L		0x00	TMC_CAP4 – low byte							
2	0xD2	TMC_CAP4_H		0x00	TMC_CAP4 – high byte							

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
2	0xD3	TMC_CAP5_L		0x00	TMC_CAP5 – low byte							
2	0xD4	TMC_CAP5_H		0x00	TMC_CAP5 – high byte							

Table 5-20 The additional SFR register (page2)

Page	Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
3	0x9A	TMA_CTRL		0x00	--	--	TMA_INTF	TMA_INTEN	CLK_SRC_SEL[2:0]			TMA_EN
3	0x9B	TMA_PLOAD_L		0x00	Timer A pre-load data– low byte							
3	0x9C	TMA_PLOAD_H		0x00	Timer A pre-load data – high byte							
3	0x9D	TMA_L		0x00	Timer A – low byte							
3	0x9E	TMA_H		0x00	Timer A – high byte							
3	0x9F	TMA_CAP_CTRL0		0x00	--	--	Timer A capture enable					
3	0xA2	TMA_CAP_CTRL1		0x00	TMA_CAP3_EDGE[1:0]		TMA_CAP2_EDGE[1:0]		TMA_CAP1_EDGE[1:0]		TMA_CAP0_EDGE[1:0]	
3	0xA 3	TMA_CAP_CTRL2		0x00	--	--	--	--	TMA_CAP5_EDGE[1:0]		TMA_CAP4_EDGE[1:0]	
3	0xA4	TMA_CAP_INTEN		0x00	--	--	Timer A capture interrupt enable					
3	0xA5	TMA_CAP_INTSTS		0x00	---	--	Timer A capture interrupt status flag					
3	0xAE	TMA_CCP0_L		0x00	Timer A CCP0 – low byte							
3	0xAF	TMA_CCP0_H		0x00	Timer A CCP0 – high byte							
3	0xB2	TMA_CCP1_L		0x00	Timer A CCP1 – low byte							
3	0xB3	TMA_CCP1_H		0x00	Timer A CCP1 – high byte							
3	0xB4	TMA_CCP2_L		0x00	Timer A CCP2 – low byte							
3	0xB5	TMA_CCP2_H		0x00	Timer A CCP2 – high byte							
3	0xB6	TMA_CCP3_L		0x00	Timer A CCP3 – low byte							
3	0xB7	TMA_CCP3_H		0x00	Timer A CCP3 – high byte							
3	0xBA	TMA_CCP4_L		0x00	Timer A CCP4 – low byte							
3	0xBB	TMA_CCP4_H		0x00	Timer A CCP4 – high byte							
3	0xBC	TMA_CCP5_L		0x00	Timer A CCP5 – low byte							
3	0xBD	TMA_CCP5_H		0x00	Timer A CCP5 – high byte							
3	0xD9	MDU_CTRL		0x00	SAVE_R_EN	DIV_ERR	DIV_INTF	MUL_INTF	DIV_INTEN	MUL_INTEN	DIV_EN	MUL_EN
3	0xDA	MDU_DSRC_ADR0		0x00	MDU DMA source address 0							
3	0xDB	MDU_DSRC_ADR1		0x00	MDU DMA source address 1							
3	0xDC	MDU_DTAR_ADDR		0x00	MDU DMA target address							

Table 5-21 The additional SFR register (page3)

5.4. Clock Source

GPM8F3732B has two clock sources including internal oscillator (16MHz) and internal PLL clock source. These two clocks are chosen to be system clock source by controlling CLK_DIV_SEL and CLK_SRC_SEL bits of SYS_CTRL1 register. In addition, a clock divisor for the system clock source is contained to obtain different frequency options. There are total of four selections which can be controlled by CLK_DIV[1:0] bits of SYS_CTRL0 register. The block diagram of clock source and detailed description of SYS_CTRL0 and SYS_CTRL1 register are shown in Figure 5-5, Table 5-22 and Table 5-23, respectively.

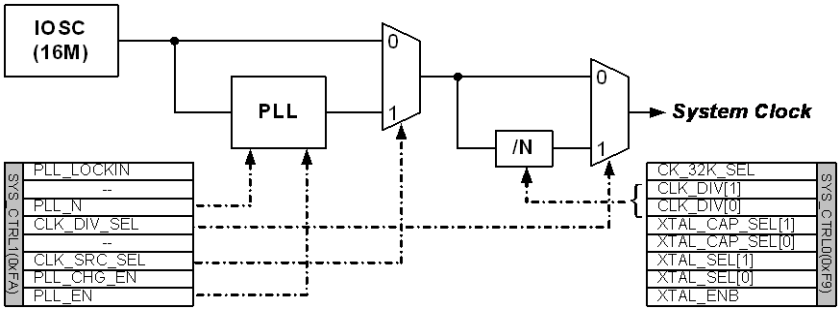


Figure 5-5 The block diagram of clock sources

SYS_CTRL0			Page : 0 / Address: 0xF9		System Control-0 Register			
Bit	7	6	5	4	3	2	1	0
Function	CK_32K_SEL	CLK_DIV[1 :0]		XTAL_CAP_SEL[1 :0]		XTAL_SEL[1 :0]		XTAL_ENB
Default	0	0	0	0	0	0	0	1
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description
7	CK_32K_SEL	R/W	32KHz clock source select signal. 0 : IOSC_32k 1 : 32768Hz X'tal output
6:5	CLK_DIV[1 :0]	R/W	System Clock divider. This function will be disabled automatically if CLK_SRC_SEL[1] of SYS_CTRL1 register is set to 1. CLK_DIV / System Divider 00 / Clock Source / 2 01 / Clock Source / 4 10 / Clock Source / 8 11 / Clock Source / 16
4:3	XTAL_CAP_SEL[1:0]	R/W	XTAL PAD embedded capacitor select signal. XTAL_CAP_SEL / Capacity 00 / No effect 01 / 1pf 10 / 1pf 11 / 2pf
2:1	XTAL_SEL[1 :0]	R/W	The 32768Hz XTAL operating mode control bit (XTAL_ENB of SYS_CTRL0 register needs to be 0). XTAL_SEL[1:0] / Operating Mode 00 / 32768 strong mode 01 / 32768 enhance mode 10 / 32768 normal mode 11 / 32768 green mode
0	XTAL_ENB	R/W	32768Hz Crystal PAD enable signal. 0 : enabled 1 : disabled

Table 5-22 The SYS_CTRL0 register

SYS_CTRL1			Page : 0 / Address: 0xFA		System Control-1 Register			
Bit	7	6	5	4	3	2	1	0
Function	PLL_LOCKIN	--	PLL_N	CLK_DIV_SEL	--	CLK_SRC_SEL	PLL_CHG_EN	PLL_EN
Default	0	0	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7	PLL_LOCKIN	R	PLL lock-in flag. 0 : PLL is tracking or PLL is disable 1 : PLL is locked-in	
6	--	--	Reserved	
5	PLL_N	R/W	PLL frequency select signals. ***User must to set CLK_DIV_SEL of SYS_CTRL1 register to 1 before set PLL_N to 1. After this setting, system clock is active in 36MHz / N , where N is depended on the setting value of CLK_DIV of SYS_CTRL0 register.*** PLL_N: 0 → PLL Output Frequency: 48MHz; 1 → 36MHz	
4	CLK_DIV_SEL	R/W	System clock select signal. 0 : system clock = input clock source 1 : system clock = input clock source / N	
3	--	R/W	Reserved	
2	CLK_SRC_SEL	R/W	Clock input source select signals. CLK_SRC_SEL: 0 → Clock Source: 16M IOSC clock; 1 → 36 / 48M PLL clock	
1	PLL_CHG_EN	R/W	PLL_N change enable signal. This bit must be set when updating PLL_N or 1st PLL enable. That will be cleared by H/W automatic. 0 : disabled 1 : enabled	
0	PLL_EN	R/W	Embedded PLL enable signal. 0 : disabled 1 : enabled	

Table 5-23 SYS_CTRL1 register

5.5. Power Saving Mode

5.5.1. Introduction

Although GPM8F3732B is a high-speed microcontrollers designed for maximum performance, it also provides Power Management Unit (PMU) with two advanced power conservation modes. These modes are HALT mode and SLEEP mode. In order to reduce the current consumption when system does not need to be active, SLEEP mode can be utilized. For more information about these two modes, please see the following section. Table 5-24 show the three operating modes in GPM8F3732B. In addition, user can save power consumption by reducing core power voltage by setting SYS_CTRL2.

5.5.2. HALT mode

The HALT Mode reduces power consumption by turning off the clock provided to the microcontroller and other unused peripheral besides RTC and LCD interface, resulting in MCU stops executing the following instruction. The HALT mode operation flow is shown as figure 5-6.

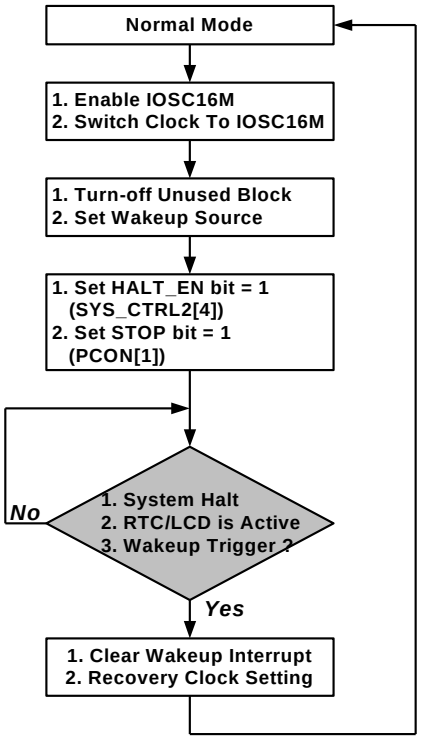


Figure 5-6 The Halt mode operating flow

5.5.3. SLEEP mode

SLEEP mode is the lowest power consumption state that the microcontroller can enter. It is achieved by cutting-off frequency provided to system clock, resulting in a fully static condition. Processor operation will be postponed on the instruction that sets the STOP bit. SLEEP mode can be exited by a Non-clocked interrupt such as the external interrupts EXT_IRQ0 to EXT_IRQ5. Clocked interrupts such as the watchdog timer and serial ports do not operate in SLEEP mode. After wakeup source trigger, processor operation will resume with the fetching of the interrupt vector associated with the interrupt that caused the exit from SLEEP mode. When the interrupt service routine is completed, RETI returns the program to the instruction immediately following the one that invoked the SLEEP mode. When EXT_IRQ0/1 or EXT_IRQ4/5 are used for wakeup source, EXT_INT_EN and EXT_INT_EDGE register must be set as shown in Table 5-26, Table 5-27 and Table 5-28. The SLEEP mode operation flow is shown as Figure 5-7.

In order to reduce power consumption when system operating in normal mode. User can switch-off clock of unused block by register setting independent. These register description are shown in Table 5-29 and Table 5-30

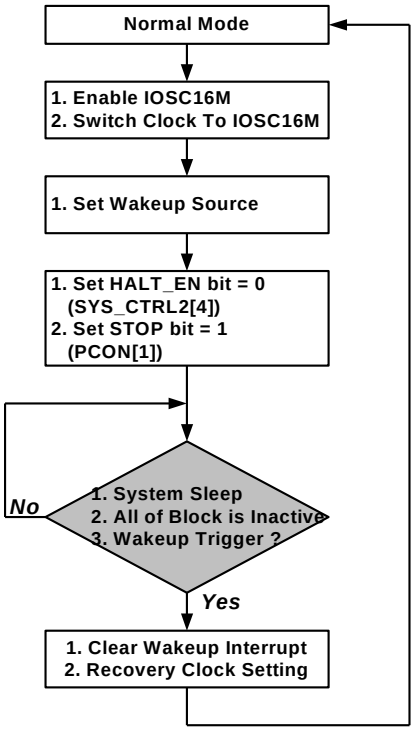


Figure 5-7 The SLEEP mode operating flow

	CPU clock	Peripheral clock	RTC & LCD clock	Wakeup source	After wakeup
Normal Mode	ON	Register setting	Register setting	--	--
HALT Mode	OFF	OFF	Register setting	1. Watch Dog interrupt 2. External Interrupt 3. RTC interrupt	Next instruction state
SLEEP Mode	OFF	OFF	OFF	1. External Interrupt	Next instruction state

Table 5-24 The two operation modes for GPM8F3732B

PCON			**Address: 0x87**		**Power Configuration Register**			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 double baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 double baud rate bit when clocked by Timer1	
5	--	R/W	Reserved	
4	PWE	R/W	Program Write Enable (PWE) 0: Disables Flash write activity during MOVX instruction 1: Enables Flash write activity during MOVX instruction	
3:2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-25 The PCON register

EXT_INT_EN			Page : 0 / Address : 0xE5		External Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	DEBOUNCE_TIME[1 :0]		EXT_INT5_EN	EXT_INT4_EN	EXT_INT3_EN	EXT_INT2_EN	EXT_INT1_EN	-
Default	0	0	0	0	0	0	0	-

Bit	Function	Type	Description	Condition
7:6	DEBOUNCE_TIME	R/W	External interrupt de-bounce time select signal DEBOUNCE_TIME[1 :0] / Clock Cycle 00 / 4 01 / 37 10 / 72 11 / 142	
5	EXT_INT5_EN	R/W	External interrupt 5 enable signal that is mapped to P5_3. 0 : disabled 1 : enable	
4	EXT_INT4_EN	R/W	External interrupt 4 enable signal that is mapped to P5_2. 0 : disabled 1 : enabled	
3	EXT_INT3_EN	R/W	External interrupt 3 enable signal that is mapped to P3_7. 0 : disabled 1 : enabled	
2	EXT_INT2_EN	R/W	External interrupt 2 enable signal that is mapped to P3_6. 0 : disabled 1 : enabled	
1	EXT_INT1_EN	R/W	External interrupt 1 enable signal that is mapped to P0_1. 0 : disabled 1 : enabled	

Table 5-26 The EXT_INT_EN register

EXT_INT_EDGE			Page : 0 / Address : 0xE6		External Interrupt Edge Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	EXT_INT5_EDGE	EXT_INT4_EDGE	EXT_INT3_EDGE	EXT_INT2_EDGE	EXT_INT1_EDGE	-
Default	0	0	0	0	0	0	0	-

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	EXT_INT5_EDGE	R/W	External interrupt 5 trigger edge control signal 0 : falling edge 1 : rising edge	
4	EXT_INT4_EDGE	R/W	External interrupt 4 trigger edge control signal 0 : falling edge 1 : rising edge	
3	EXT_INT3_EDGE	R/W	External interrupt 3 trigger edge control signal 0 : falling edge 1 : rising edge	
2	EXT_INT2_EDGE	R/W	External interrupt 2 trigger edge control signal 0 : falling edge 1 : rising edge	
1	EXT_INT1_EDGE	R/W	External interrupt 1 trigger edge control signal 0 : falling edge 1 : rising edge	

Table 5-27 The EXT_INT_EDGE register

EXT_INT_STS			**Address : 0xE7**		**External Interrupt Status Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	EXT_INT5_STS	EXT_INT4_STS	EXT_INT3_STS	EXT_INT2_STS	EXT_INT1_STS	-
Default	0	0	0	0	0	0	0	-

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	EXT_INT5_STS	R/W	External interrupt 5 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clears this bit 1 : no effect	
4	EXT_INT4_STS	R/W	External interrupt 4 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clears this bit 1 : no effect	
3	EXT_INT3_STS	R/W	External interrupt 3 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clears this bit	

Bit	Function	Type	Description	Condition
			1 : no effect	
2	EXT_INT2_STS	R/W	External interrupt 2 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clears this bit 1 : no effect	
1	EXT_INT1_STS	R/W	External interrupt 1 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clears this bit 1 : no effect	

Table 5-28 The EXT_INT_STS register

SYS_CTRL5	Address : 0xFE			System Control-5 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMR_CKEN	LCD_CKEN	MDU_CKEN	TH_CKEN	SPI_CKEN	UART_CKEN	I2C_CKEN	ADC_CKEN
Default	1	1	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7	TMR _CKEN	R/W	Timer controller clock enable signal. 0 : disabled 1 : enabled	
6	LCD_CKEN	R/W	LCD controller clock enable signal. 0 : disabled 1 : enabled	
5	MDU_CKEN	R/W	MDU controller clock enable signal. 0 : disabled 1 : enabled	
4	TH_CKEN	R/W	Capacitive touch controller clock enable signal. 0 : disabled 1 : enabled	
3	SPI_CKEN	R/W	SPI controller clock enable signal. 0 : disabled 1 : enabled	
2	UART_CKEN	R/W	UART controller clock enable signal. 0 : disabled 1 : enabled	
1	I2C_CKEN	R/W	I2C controller clock enable signal. 0 : disabled 1 : enabled	
0	ADC_CKEN	R/W	ADC controller clock enable signal.	

Bit	Function	Type	Description	Condition
			0 : disabled 1 : enabled	

Table 5-29 The SYS_CTRL5 register

SYS_CTRL6			Address : 0xFF		System Control-6 Register			
Bit	7	6	5	4	3	2	1	0
Function	UART_IF_SEL		UART_IF_EN	T01_CK_SEL	--	AERR_RSTEN	WDOG_CKEN	RTC_CKEN
Default	1	1	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7:6	UART_IF_SEL[1:0]	R/W	UART IO interface select signal UART_IF_SEL[1 :0] / UART_TX / UART_RX 0X / P1[6] / P1[5] 10 / P4[7] / P5[0] 11 / P4[7] / P5[4]	
5	UART_IF_EN	R/W	UART interface enable signal. 0 : disabled 1 : enabled	
4	T01_CK_SEL	R/W	Timer0/1 clock source select signal.This bit is used combining with T0M/T1M of CKCON(0x8E). T0M /T1M / T01_CK_SEL / Timer0/1 Clock 0 / 0 / System Clock / 8 0 / 1 / System Clock / 2 1 / 0 / System Clock / 4 1 / 1 / System Clock / 1	
3	--	R/W	Reserved	
2	AERR_RSTEN	R/W	Flash address over range reset enable 0 : disabled 1 : enabled	
1	WDOG_CKEN	R/W	Watch dog controller clock enable control bit 0 : disabled 1 : enabled	
0	RTC_CKEN	R/W	RTC controller clock enable signal. 0 : disabled 1 : enabled	

Table 5-30 The SYS_CTRL6 register

SYS_CTRL2			Page : 0 / Address: 0xFB		System Control 2 Register			
Bit	7	6	5	4	3	2	1	0
Function	HALT_I_SEL[2:0]			HALT_EN	V18_SEL[1:0]		IOSC32K_EN	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	HALT_I_SEL	R/W	Regulator operating current selection during halt mode	

Bit	Function	Type	Description	Condition
			HALT_EN / HALT_I_SEL[2:0] / Imax of VCC_18 0 / XXX / 30mA 1 / 000 / 3uA 1 / 001 / 4uA 1 / 010 / 5uA 1 / 011 / 6uA 1 / 100 / 7uA 1 / 101 / 8uA 1 / 110 / 10uA 1 / 111 / 12uA	
4	HALT_EN	R/W	Halt mode enable signal. 0 : system operating in sleep mode when PCON[1] is set to 1 1 : system operating in halt mode when PCON[1] is set to 1	
3:2	V18_SEL	R/W	1.8V power domain select bit. V18_SEL[1:0] / Voltage of V18 00 / 2.0V 01 / prohibit 10 / 1.9V 11 / 2.1V	
1	IOSC32K_EN	R/W	Internal 32K oscillator enable bit 0 : disabled 1 : enabled	
0	--	R/W	Reserved	

Table 5-31 SYS_CTRL2 register

5.6. Interrupt System

5.6.1. Introduction

The GPM8F3732B provides 15 types of interrupt sources with two levels interrupt priority control which tabled in Table 5-32. For standard 8051 interrupt sources, each interrupt can be in high or low level priority group by setting or clearing a bit in the IP(0xB8) and EIP(0xF8) registers. IE0 has the top priority in default state and user can choose the related interrupt source to be the top priority by IP register. Interrupt requests are sampled each system clock at the rising edge of clock control. Each interrupt vector can be individually enabled or disabled by setting or clearing a corresponding bit in the IE(0xA8), EIE(0xE8). The IE contains global interrupt system disable(0) / enable(1) bit called EA.

In general, once an interrupt event occurs, the corresponding flag bit will be set. The related registers of interrupt flag are described as below.

If the related interrupt control bit is set to enable interrupt, an interrupt request signal will be generated and then CPU executes service routine. If the related interrupt control bit is disabled, programmer still can observe the corresponding flag bit, but no interrupt request signal will be generated. The interrupt flag bits must be cleared in the interrupt service routine to prevent program from deadlock in interrupt service routine. With any instruction, interrupts pending during the previous instruction is served. Before entering interrupt service routine, the system saves the current PC address into top of stack pointer and jumps to corresponding vector to execute the interrupt service. After finishing the interrupt service, the system abstract the return PC address from the top of the stack to execute the following instruction.

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Vector number	Priority
TAF	Timer A Interrupt	--	Software(cleared by 0)	0x03	0	1
TF0	Timer 0 Interrupt	--	Hardware	0x0B	1	2
ADC0F	ADC0 Interrupt	--	Software(cleared by 0)	0x13	2	3

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Vector number	Priority
TF1	Timer 1 Interrupt	--	Hardware	0x1B	3	4
TI0 & RI0	UART0 Interrupt	--	Software(cleared by 0)	0x23	4	5
TBF	Timer B Interrupt	--	Software(cleared by 0)	0x2B	5	6
TCF	Timer C Interrupt	--	Software(cleared by 0)	0x33	6	7
MDUF	MDU / RTC	--	Software(cleared by 0)	0x3B	7	8
I2CF/LCDF	I2C / LCD	--	Software(cleared by 0)	0x43	8	9
SPIF	SPI	--	Software(cleared by 0)	0x4B	9	10
LVDF	LVD	--	Software(cleared by 0)	0x53	10	11
EXTF	External Interrupt	Rising/Falling	Software(cleared by 0)	0x5B	11	12
WDIF	Watchdog Interrupt	--	Software(cleared by 0)	0x63	12	13

Table 5-32 Summaries of all interrupt sources

IP			Address: 0xB8		Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	-	PTC	PTB	PS0	PT1	PADC	PT0	PTA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	PTC	R/W	Timer C interrupt priority level control (1: high level)	
5	PTB	R/W	Timer B interrupt priority level control (1: high level)	
4	PS0	R/W	UART0 interrupt priority level control (1: high level)	
3	PT1	R/W	Timer 1 interrupt priority level control (1: high level)	
2	PADC	R/W	ADC0 interrupt priority level control (1: high level)	
1	PT0	R/W	Timer 0 interrupt priority level control (1: high level)	
0	PTA	R/W	Timer A interrupt priority level control (1: high level)	

Table 5-33 IP register

EIP			Address: 0xF8		Extended Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	PWDI	PEXT	PLVD	PSPI	PI2C	PMDU
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	--	R/W	Reserved	
5	PWDI	R/W	Watchdog interrupt priority level control (1: high level)	
4	PEXT	R/W	External interrupt priority level control (1: high level)	
3	PLVD	R/W	LVD interrupt priority level control (1: high level)	
2	PSPI	R/W	SPI interrupt priority level control (1: high level)	
1	PI2C	R/W	I2C/LCD interrupt priority level control (1: high level)	
0	PMDU	R/W	MDU/RTC interrupt priority level control (1: high level)	

Table 5-34 EIP register

IE			Address: 0xA8		Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EA	ETC	ETB	ES0	ET1	EADC	ET0	ETA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EA	R/W	Enables global interrupts	
6	ETC	R/W	Enables Timer C interrupt	
5	ETB	R/W	Enables Timer B interrupt	
4	ES0	R/W	Enables UART0 interrupt	
3	ET1	R/W	Enables Timer 1 interrupt	
2	EADC	R/W	Enables ADC0 interrupt	
1	ET0	R/W	Enables Timer 0 interrupt	
0	ETA	R/W	Enables Timer A interrupt	

Table 5-35 IE register

EIE			Address: 0xE8		Extended Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	-	-	EWDI	EEXT	ELVD	ESPI	EI2C	EMDU
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	--	R/W	Reserved	
5	EWDI	R/W	Enables watchdog interrupt	
4	EEXT	R/W	Enables External interrupts	
3	ELVD	R/W	Enables LVD interrupts	
2	ESPI	R/W	Enables SPI interrupts	
1	EI2C	R/W	Enables I2C / LCD interrupts	
0	EMDU	R/W	Enables MDU / RTC interrupts	

Table 5-36 EIE register

TCON			Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	ADCF	--	TAF	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: disabled ; 1: enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	
4	TR0	R/W	Timer 0 run control bit 0: disabled ; 1: enabled	
3	ADCF	R/W	ADC0 interrupt flag	
2	--	R/W	Reserved	

Bit	Function	Type	Description	Condition
1	TAF	R/W	Timer A interrupt flag	
0	--	R/W	Reserved	

Table 5-37 TCON register

WDCON			Address: 0xD8		Watchdog Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	WDIF	--	EWT	RWT
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3	WDIF	R/W	Watchdog interrupt flag	
2	--	R/W	Reserved	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disabled; 1: Enabled	
0	RWT	R/W	Reset watchdog timer 0: NA; 1: Reset	

Table 5-38 WDCON register

SCON0			Address: 0x98		UART0 configuration register			
Bit	7	6	5	4	3	2	1	0
Function	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
7:6	SM0[1:0]	R/W	Mode and baud rate setting	
5	SM02	R/W	Enables a multiprocessor communication feature	
4	REN0	R/W	Enables serial reception.	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0, this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received.	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-39 SCON0 register

EIF			Address: 0x91		Extended interrupt flag			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	EXTF	LVDF	SPIF	I2CF	MDUF
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	EXTF	R/W	External interrupt flag	
3	LVDF	R/W	LVD interrupt flag	

Bit	Function	Type	Description	Condition
2	SPIF	R/W	SPI interrupt flag	
1	I2CF	R/W	I2C / LCD interrupt flag	
0	MDUF	R/W	MDU / RTC interrupt flag	

Table 5-40 EIF register

TMA_CTRL			Page : 3 / Address: 0x9A		Timer A Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_INTF	TMA_INTEN	CLK_SRC_SEL			TMA_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	TMA_INTF	R/W	Timer A interrupt flag. read : 0 : idle / busy 1 : timer A interrupt trigger write : 0 : clears this bit 1 : no effect	
4	TMA_INTEN	R/W	Timer A interrupt enable signal 0 : disabled 1 : enabled	
3:1	CLK_SRC_SEL[2:0]	R/W	Timer A input clock source select signal. CLK_SRC_SEL[2:0] / Clock Source 000 / System clock 001 / System clock / 2 010 / System clock / 4 011 / System clock / 8 100 / System clock / 16 101 / System clock / 32 110 / IOSC_16M 111 / 32K (IOSC_32K or XTAL)	
0	TMA_EN	R/W	Timer A enable signal. 0 : disabled 1 : enabled	

Table 5-41 TMA_CTRL register

TMA_CAP_INTEN			Page : 3 / Address: 0xA4		Timer A Capture Mode Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_CAP_INTEN[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMA_CAP_INTEN[5:0]	R/W	Timer A capture mode interrupt enable signals. These are	

Bit	Function	Type	Description	Condition
			mapping to CAP0 ~ CAP5 respectively. 0 : disabled 1 : enabled	

Table 5-42 TMA_CAP_INTEN register

TMA_CAP_INTSTS			Page : 3 / Address: 0xA5		Timer A Capture Mode Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_CAP_INTSTS[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMA_CAP_INTSTS[5:0]	R/W	Timer A capture mode interrupt flag. These are mapping to CAP0 ~ CAP5 respectively. read : 0 : no capture signal triggered 1 : capture signal triggered write : 0 : clears this bit 1 : no effect	

Table 5-43 TMA_CAP_INTSTS register

TMB_CTRL			Page : 2 / Address: 0x9A		Timer B Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMB_INTF	TMB_INTEN	CLK_SRC_SEL[2:0]			TMB_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	TMB_INTF	R/W	Timer B interrupt flag. read : 0 : idle / busy 1 : timer B interrupt trigger write : 0 : clears this bit 1 : no effect	
4	TMB_INTEN	R/W	Timer B interrupt enable signal 0 : disabled 1 : enabled	
3:1	CLK_SRC_SEL[2:0]	R/W	Timer B input clock source select signal. CLK_SRC_SEL[2:0] : Clock Source 000 : System clock 001 : System clock / 2 010 : System clock / 4 011 : System clock / 8 100 : System clock / 16	

Bit	Function	Type	Description	Condition
			101 System clock / 32 110 IOSC_16M 111 32K (IOSC_32K or XTAL	
0	TMB_EN	R/W	Timer B enable signal. 0 : disabled 1 : enabled	

Table 5-44 TMB_CTRL register

TMB_CAP_INTCTR			Page : 2 / Address: 0xA3		Timer B Capture Mode Interrupt Control Register			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CAP_INTSTS[3:0]				TMB_CAP_INTEN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	TMB_CAP_INTSTS[3:0]	R/W	Timer B capture mode interrupt flag. These are mapping to CAP0 ~ CAP3 respectively. read : 0 : no capture signal triggered 1 : capture signal triggered write : 0 : clears this bit 1 : no effect	
3:0	TMB_CAP_INTEN[5:0]	R/W	Timer B capture mode interrupt enable signals. These are mapping to CAP0 ~ CAP3 respectively. 0 : disabled 1 : enabled	

Table 5-45 TMA_CAP_INTEN register

TMC_CTRL			Page : 2 / Address: 0xBA		Timer C Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_INTF	TMC_INTEN	CLK_SRC_SEL[2:0]			TMC_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R	Reserved	
5	TMC_INTF	R/W	Timer C interrupt flag. read : 0 : idle / busy 1 : timer C interrupt trigger write : 0 : clears this bit 1 : no effect	
4	TMC_INTEN	R/W	Timer C interrupt enable signal 0 : disabled 1 : enabled	
3:1	CLK_SRC_SEL[2:0]	R/W	Timer C input clock source select signal.	

Bit	Function	Type	Description	Condition
			CLK_SRC_SEL[2:0] Clock Source 000 System clock 001 System clock / 2 010 System clock / 4 011 System clock / 128 100 System clock / 256 101 System clock / 512 110 System clock / 1024 111 Prohibit	
0	TMC_EN	R/W	Timer C enable signal. 0 : disabled 1 : enabled	

Table 5-46 TMC_CTRL register

TMC_CAP_INTEN			Page : 2 / Address: 0xC4		Timer C Capture Mode Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_CAP_INTEN[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMC_CAP_INTEN[5:0]	R/W	Timer C capture mode interrupt enable signals. These are mapping to CAP0 ~ CAP5 respectively. 0 : disabled 1 : enabled	

Table 5-47 TMC_CAP_INTEN register

TMC_CAP_INTSTS			Page : 2 / Address: 0xC5		Timer C Capture Mode Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_CAP_INTSTS[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMC_CAP_INTSTS[5:0]	R/W	Timer C capture mode interrupt flag. These are mapping to CAP0 ~ CAP5 respectively. read: 0 : no capture signal triggered 1 : capture signal triggered write: 0 : clears this bit 1 : no effect	

Table 5-48 TMC_CAP_INTSTS register

ADC0_CTRL0			Page : 0 / Address: 0xD9		ADC0 Control 0 register			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_INTEN	ADC0_SH_CYCLE		ADC0_CLK_SEL			--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC0_INTEN	R/W	ADC0 interrupt enable control bit. 0 : disabled 1 : enabled	
6:5	ADC0_SH_CYCLE	R/W	ADC0 sample and hold cycle selection control bit. ADC0_SH_CYCLE: Cycle (ADC0_CLK) 00: 2 01: 4 10: 8 11: 16	
4:2	ADC0_CLK_SEL	R/W	ADC0 clock selection control bit ADC0_CLK_SEL: ADC0_CLK 000: System clock / 2 001: System clock / 4 010: System clock / 8 011: System clock / 12 100: System clock / 16 101: System clock / 20 110: System clock / 24 111: System clock / 28	
1:0	-	R/W	Reserved	

Table 5-49 ADC0_CTRL0 register

ADC0_CTRL1			Page : 0 / Address: 0xDA		ADC0 Control 1 register			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_START	--	--	ADC0_INTF	--	ADC0_CH_SEL[2:0]		
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC0_START	R/W	ADC0 start transfer control bit 0: idle 1: start transfer	
6:5	-	R/W	Reserved	
4	ADC0_INTF	R/W	ADC0 interrupt flag. read : 0 : idle / converting 1 : conversion ready write : 0 : clears this bit 1 : no effect	
3	-	R/W	Reserved	

Bit	Function	Type	Description	Condition
2:0	ADC0_CH_SEL	R/W	ADC0 channel selection control bit ADC0_CH_SEL: ADC0_CLK 000: Prohibit 001: ADC0_CH1 (P0[1]) 010: ADC0_CH2 (P0[2]) 011: ADC0_CH3 (P0[3]) 100: ADC0_CH4 (P0[4]) 101: ADC0_CH5 (P0[5]) 110: ADC0_CH6 (P0[6]) 111: ADC0_CH7 (P0[7])	

Table 5-50 ADC0_CTRL1 register

MDU_CTRL			Page : 3 / Address: 0xD9		Multiplier / Divider Control Register			
Bit	7	6	5	4	3	2	1	0
Function	SAVE_R_EN	DIV_ERR	DIV_INTF	MUL_INTF	DIV_INTEN	MUL_INTEN	DIV_EN	MUL_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SAVE_R_EN	R/W	Remainder save to SRAM enable 0 : disabled 1 : enabled	
6	DIV_ERR	R	Divisor error flag. read : 0: divisor is a nonzero value. 1: divisor is zero. This flag will be cleared automatic when divisor is updated to nonzero value.	
5	DIV_INTF	R/W	Divider interrupts flag. read : 0 : idle / busy 1 : Divider interrupt trigger write : 0 : clears this bit 1 : no effect	
4	MUL_INTF	R/W	Multiplier interrupts flag. read : 0 : idle / busy 1 : Multiplier interrupt trigger write : 0 : clears this bit 1 : no effect	
3	DIV_INTEN	R/W	Divider interrupt enable signal. 0 : disabled 1 : enabled	
2	MUL_INTEN	R/W	Multiplier interrupt enable signal. 0 : disabled 1 : enabled	

Bit	Function	Type	Description	Condition
1	DIV_EN	R/W	Divider enable control bit. 0 : disabled 1 : enabled	
0	MUL_EN	R/W	Multiplier enable control bit. 0 : disabled 1 : enabled	

Table 5-51 MDU_CTRL register

P5			Address: 0xC8		Port5 Register			
Bit	7	6	5	4	3	2	1	0
Function	DIV_INTF	MUL_INTF	--	P54	P53	P52	P51	P50
Default	0	0	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
7	DIV_INTF	R	Divider interrupts flag. 0 : idle / busy 1 : Divider interrupt trigger	
6	MUL_INTF	R	Multiplier interrupts flag. 0 : idle / busy 1 : Multiplier interrupt trigger	
4:0	P5[4:2]	R/W	P5 is used to set IO output data only. Otherwise, it can also be used to configure the Port5 function.	

Table 5-52 P5 register

I2C_STS			Page : 0 / Address: 0xD2		I2C Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	SLV_DID_OK	SLV_DAT_OK	SLV_STP_OK	ERR_SDID_IE	I2C_IF_SEL	I2C_INT_EN	NO_ACK	TS_DONE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SLV_DID_OK	R/W	This bit indicates device ID has been received by I2C controller. This is for slaver mode only. read: 0 : device ID is not asserted 1 : device ID is asserted write: 0 : clears this bit 1 : no effect	
6	SLV_DAT_OK	R/W	This bit indicates data was received or transmitted by I2C controller. This is for slaver mode only. read: 0 : data is transmitting or idle now 1 : data is transmission complete write: 0 : clears this bit 1 : no effect	

Bit	Function	Type	Description	Condition
5	SLV_STP_OK	R/W	This bit indicates stop command was received by I2C controller. This is for slaver mode only. read: 0 : stop command is not assert 1 : stop command is asserted write: 0 : clears this bit 1 : no effect	
4	ERR_SDID_IE	R/W	Device ID error interrupt enable of slaver mode. 0 : disabled 1 : enabled	
3	I2C_IF_SEL	R/W	I2C interface select signal 0 : P0_6 = SDA / P0_7 = SCL 1 : P5_2 = SDA / P5_3 = SCL	
2	I2C_INT_EN	R/W	I2C interrupt enable control bit. 0 : disabled 1 : enabled	
1	NO_ACK	R/W	I2C has not yet received acknowledging signal. read : 0 : acknowledge 1 : no acknowledge write : 0 : clears this bit 1 : no effect	
0	TS_DONE	R/W	I2C transmission complete flag. read: 0 : I2C is idle or on going 1 : I2C is finished data transmission write: 0 : clears this bit 1 : no effect	

Table 5-53 I2C_STS register

SPI_STS			**Page : 0 / Address: 0x9B**		**SPI Status Register**			
Bit	7	6	5	4	3	2	1	0
Function	SPI_INTEN	--	--	--	--	--	RX_DONE	TX_DONE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SPI_INTEN	R/W	SPI interrupt enable 0 : disabled 1 : enabled	
6:2	--	R/W	Reserved	
1	RX_DONE	R	SPI finished data receiving with slaver mode. 0: Idle / Busy 1:Done	

Bit	Function	Type	Description	Condition
0	TX_DONE	R	SPI finished data transmission with master mode. 0: Idle / Busy 1:Done	

Table 5-54 SPI_STS register

SYS_CTRL3			Page : 0 / Address: 0xFC		System Control 3 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	LVD_INT_EN	LVD_SEL[1:0]		LVD_EN	LVR_SEL[1:0]		LVR_EN
Default	0	0	1	0	0	1	0	0
Key Code	0x8F, 0x32, 0x50							

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	LVD_INT_EN	R/W	LVD interrupt enable 0 : disabled 1 : enabled	
5:4	LVD_SEL[1:0]	R/W	LVD voltage selection bits LVD_SEL[1:0] / Voltage 00 / 2.1V 01 / 2.6V 10 / 3.4V 11 / 4.4V	
3	LVD_EN	R/W	LVD enable control 0: disables LVD function 1: enables LVD function	
2:1	LVR_SEL[1:0]	R/W	LVR voltage selection bits LVR_SEL[1:0] / Voltage 00 / 1.9V 01 / 2.4V 10 / 3.2V 11 / 4.2V	
0	LVR_EN	R/W	LVR enable control 0: disables LVR function 1: enables LVR function	

Table 5-55 SYS_CTRL3 register

SYS_CTRL4			Page : 0 / Address: 0xFD		System Control 4 Register			
Bit	7	6	5	4	3	2	1	0
Function	MISS_CLK	WDOG_RST	SW_RST_EN	LVR_RST	LVD_INTF	LVD_STS	ADDR_ERR	ERR_WR
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	MISS_CLK	R	Miss XTAL clock indicate flag 0 : XTAL is normally work 1 : miss xtal clock	

Bit	Function	Type	Description	Condition
6	WDOG_RST	R/W	Watchdog reset indicated flag read: 0 : Watchdog reset is inactive 1 : Watchdog reset is active Write: 0 : clears this bit 1 : no effect	
5	SW_RST_EN	R/W	Software reset enable signal 0 : disables software reset 1 : enables software reset	
4	LVR_RST	R/W	LVR indicated flag read: 0 : LVR is inactive 1 : LVR is active Write: 0 : clears this bit 1 : no effect	
3	LVD_INTF	R/W	LVD interrupt flag read: 0 : LVD is inactive 1 : LVD is active Write: 0 : clears this bit 1 : no effect	
2	LVD_STS	R	LVD status flag. 0 : LVD is inactive 1 : LVD is active	
1	ADDR_ERR	R/W	Flash access address over range flag. read: 0 : flash access address is not over range 1 : flash access address is over range Write: 0 : clears this bit 1 : no effect	
1	ERR_WR	R/W	Flash is illegal programming or erasing flag. This flag will be set to high when a programming or erasing is out of space or among lock_level range. read: 0 : legal programming or erasing 1 : illegal programming or erasing Write: 0 : clears this bit 1 : no effect	

Table 5-56 SYS_CTRL4 register

EXT_INT_EN			Page : 0 / Address : 0xE5		External Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	
Function	DEBOUNCE_TIME[1 :0]		EXT_INT5_EN	EXT_INT4_EN	EXT_INT3_EN	EXT_INT2_EN	EXT_INT1_EN	-
Default	0	0	0	0	0	0	0	-

Bit	Function	Type	Description	Condition
7:6	DEBOUNCE_TIME	R/W	External interrupt de-bounce time select signal DEBOUNCE_TIME[1 :0] / Clock Cycle 00 / 4 01 / 37 10 / 72 11 / 142	
5	EXT_INT5_EN	R/W	External interrupt 5 enable signal that is mapped to P5_3 0 : disabled 1 : enabled	
4	EXT_INT4_EN	R/W	External interrupt 4 enable signal that is mapped to P5_2. 0 : disabled 1 : enabled	
3	EXT_INT3_EN	R/W	External interrupt 3 enable signal that is mapped to P3_7. 0 : disabled 1 : enabled	
2	EXT_INT2_EN	R/W	External interrupt 2 enable signal that is mapped to P3_6. 0 : disabled 1 : enabled	
1	EXT_INT1_EN	R/W	External interrupt 1 enable signal that is mapped to P0_1. 0 : disabled 1 : enabled	

Table 5-57 The EXT_INT_EN register

EXT_INT_EDGE			Page : 0 / Address : 0xE6		External Interrupt Edge Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	EXT_INT5_EDGE	EXT_INT4_EDGE	EXT_INT3_EDGE	EXT_INT2_EDGE	EXT_INT1_EDGE	-
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	EXT_INT5_EDGE	R/W	External interrupt 5 trigger edge control signal 0 : falling edge 1 : rising edge	
4	EXT_INT4_EDGE	R/W	External interrupt 4 trigger edge control signal 0 : falling edge 1 : rising edge	
3	EXT_INT3_EDGE	R/W	External interrupt 3 trigger edge control signal 0 : falling edge 1 : rising edge	

Bit	Function	Type	Description	Condition
2	EXT_INT2_EDGE	R/W	External interrupt 2 trigger edge control signal 0 : falling edge 1 : rising edge	
1	EXT_INT1_EDGE	R/W	External interrupt 1 trigger edge control signal 0 : falling edge 1 : rising edge	

Table 5-58 The EXT_INT_EDGE register

EXT_INT_STS			**Address : 0xE7**		**External Interrupt Status Register**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	EXT_INT5_STS	EXT_INT4_STS	EXT_INT3_STS	EXT_INT2_STS	EXT_INT1_STS	-
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	EXT_INT5_STS	R/W	External interrupt 5 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clears this bit 1 : no effect	
4	EXT_INT4_STS	R/W	External interrupt 4 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clears this bit 1 : no effect	
3	EXT_INT3_STS	R/W	External interrupt 3 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clear this bit 1 : no effect	
2	EXT_INT2_STS	R/W	External interrupt 2 status flag. read: 0 : external interrupt is not occurred 1 : external interrupt is occurred write: 0 : clears this bit 1 : no effect	
1	EXT_INT1_STS	R/W	External interrupt 1 status flag. read: 0 : external interrupt is not occurred	

Bit	Function	Type	Description	Condition
			1 : external interrupt is occurred write: 0 : clears this bit 1 : no effect	

Table 5-59 The EXT_INT_STS register

RTC_CTRL			Page : 1 / Address: 0x96		Real Time Counter Control Register			
Bit	7	6	5	4	3	2	1	0
Function	RTC_INTF	--	--	--	--	COUNT_SEL[1:0]		RTC_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	RTC_INTF	R/W	RTC interrupt flag. read : 0 : interrupt is inactived 1 : interrupt is actived write : 0 : clears this bit 1 : no effect	
6:3	--	R/W	Reserved	
3:2	COUNT_SEL[1:0]	R/W	RTC interrupt interval select signals 00 : 0.5 Sec 01 : 1Sec 10 : 30Sec 11 : 60Sec	
0	RTC_EN	R/W	RTC enable signal 0 : disabled 1 : enabled	

Table 5-60 RTC_CTRL register

LCD_CTRL			Page : 1 / Address: 0x9A		LCD Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	VBLK_INTEN	FR_SEL[1:0]		UP_DATE_EN	COM_MODE[1:0]		LCD_EN	LCD_BIASEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	VBLK_INTEN	R/W	V-Blank interrupt enable 0 : disabled 1 : enabled	
6:5	FR_SEL	R/W	Frame select signal FR_SEL[1:0] / Frame Rate 00 / 110Hz 01 / 95Hz 10 / 85Hz 11 / 75Hz	
4	UP_DATE_EN	R/W	LCD display content update enable signal. Hardware will update	

Bit	Function	Type	Description	Condition
			LCD content when V-syn is arrived and this bit is enabled. 0 : disabled 1 : enabled	
3:2	COM_MODE	R/W	LCD common signal selection bit COM_MODE / COM # 00 / COM0 01 / COM0 ~ COM1 10 / COM0 ~ COM2 11 / COM0 ~ COM3	
1	LCD_EN	R/W	LCD enable control bit. 0 : disabled 1 : enabled	
0	LCD_BIASEN	R/W	LCD bias enable control bit. 0 : disabled 1 : enabled	

Table 5-61 LCD_CTRL register

LCD_CTRL1			Page : 1 / Address: 0x9B		LCD Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	VBLK_INTF	ACT_COM		SH_DUTY_SEL		BIAS_DUTY_SEL	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	VBLK_INTF	R/W	LCD V-blanking interrupts flag. Read: 0 : inactive 1 : active Write : 0 : clears this bit 1 : no effect	
5:4	ACT_COM	R	These bits are used to indicate which COM is scanning. ACT_COM / COM # 00 / 0 01 / 1 10 / 2 11 / 3	
3:2	SH_DUTY_SEL	R	LCD segment bias select signal. SH_DUTY_SEL / Duty Cycle 00 / 0.5/384 01 / 0.5/512 10 / 0.5/640 11 / Always On	
1:0	BIAS_DUTY_SEL	R	LCD common bias select signal. BIAS_DUTY_SEL / Duty Cycle 00 / 1/384	

Bit	Function	Type	Description		Condition
			01	1/512	
			10	1/640	
			11	Always On	

Table 5-62 LCD_CTRL1 register

5.7. Reset Sources

5.7.1. Introduction

There are six types of reset sources for the GPM8F3732B including Power-On Reset (POR), Low Voltage Reset (LVR), Pad Reset (RAD_RST), Watchdog Timer Reset (WDT_RST), Software Reset (S/W_RST) and Flash Error Reset (ADDR_ERR_RST). Figure 5-8 shows the block diagram of each reset source.

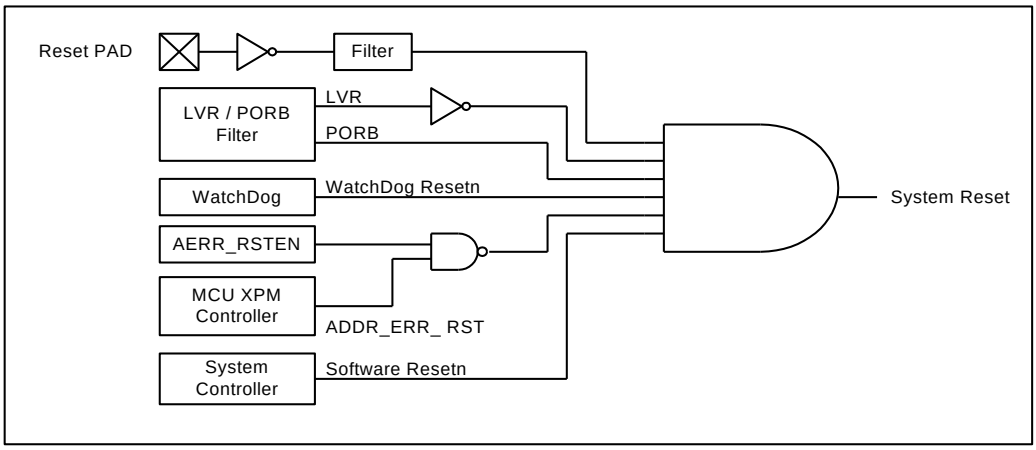


Figure 5-8 Reset sources

5.7.2. Power-On Reset (POR)

A POR is generated when VDD is rising from 0v. When VDD rises to an acceptable level (~1.5V), the power on reset circuit will starts a power-on sequence. After that, the system starts to activate and will operate in target speed. The POR will reset whole chip and registers.

5.7.3. Low Voltage Reset / Low Voltage Detect (LVR/LVD)

The on-chip Low Voltage Reset (LVR) circuitry forces the system entering reset state when power supplying voltage falls below the specific LVR trigger voltage. This function prevents MCU from working at an invalid operating voltage range.

To enable or disable this function, SYS_CTRL3[0] can be set. If this function is enabled, the LVR circuit will monitor power level while chip is operating. And the LVR voltage level can be 1.9V, 2.4V, 3.2V or 4.2V by setting SYS_CTRL3[2:1]. If the power is lower than the specific level for a specific period, the system reset will take place and go to initial state.

In order to allow software to early notify that a power failure is about to occur, the LVD flag bit can be monitored. Built-in voltage detection circuit controls the LVD flag. The LVD flag is set while VDD supply is below LVD voltage and is cleared when the VDD supply is over LVD voltage. The LVD voltage can be 2.1V, 2.6V, 3.4V or 4.4V by setting SYS_CTRL3[5:4] bits.

5.7.4. Pad Reset (PAD_RST)

The GPM8F3732B provides an external pin to force the system returning to its initial status. The RESET pin is high active as shown in figure 5-9. When the RESET pin equals to VDD over 120us, system will be forced to enter reset state, execute instruction from address 0x0000 and all registers go to default state.

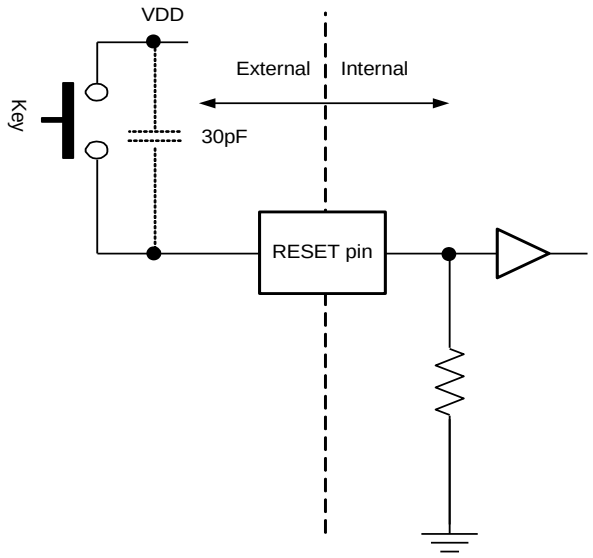


Figure 5-9 Pad reset circuit

5.7.5. Watchdog Timer Reset (WDT_RST)

On-chip watchdog circuitry makes the device entering reset state when MCU goes into unknown state and has no watchdog cleared information. This function prevents the MCU to be stuck in an abnormal condition. The WDT can be enabled or disabled through WDCON register bit 1. At any time prior to reaching its user selected terminal value, software can set the Reset Watchdog Timer (WDCON[0]) bit. If RWT is set before the timeout is reached, the timer will start over. If timeout is reached without RWT being set, the watchdog will reset the CPU. Hardware will automatically clear RWT after software sets it. When the reset occurs, the Watchdog Timer Reset Flag (SYSCON_CTRL4[6]) will automatically be set to indicate the cause of the reset, however software must clear this bit manually.

WDCON register is a timed access register that prevent it from accidental writes. KEYCODE is located at 0xEB. Correct sequence, 0xAA and 0x55, is required before write to WDCON register. Reading from such register is not protected.

The Watchdog has four timeout selections based on the internal 32K clock frequency. The selections are a pre-selected number of clocks and can be set by CKCON[7:6]. In addition, CKCON[5] can be used to set these four timeout selections in fast mode or not. Figure 5-10 shows the block diagram of Watchdog timer.

5.7.6. Other Reset Sources

Other reset sources includes Software Reset and Flash Address Error Reset. Software Reset is occurred when writing KEY code to KEYCODE register(0xEB). The key codes are 0x8F, 0x32 and 0x50. The timing does not matter, but the key codes must be written in order before SW reset is take place. Flash Address Error Reset is the reset when flash access addresses is out of flash space and AERR_RSTEN(SYS_CTRL6[2]) is set to 1.

In GPM8F3732B, system supports four reset status flag can be monitored by SYS_CTRL4 register which is shown as table 5-68.

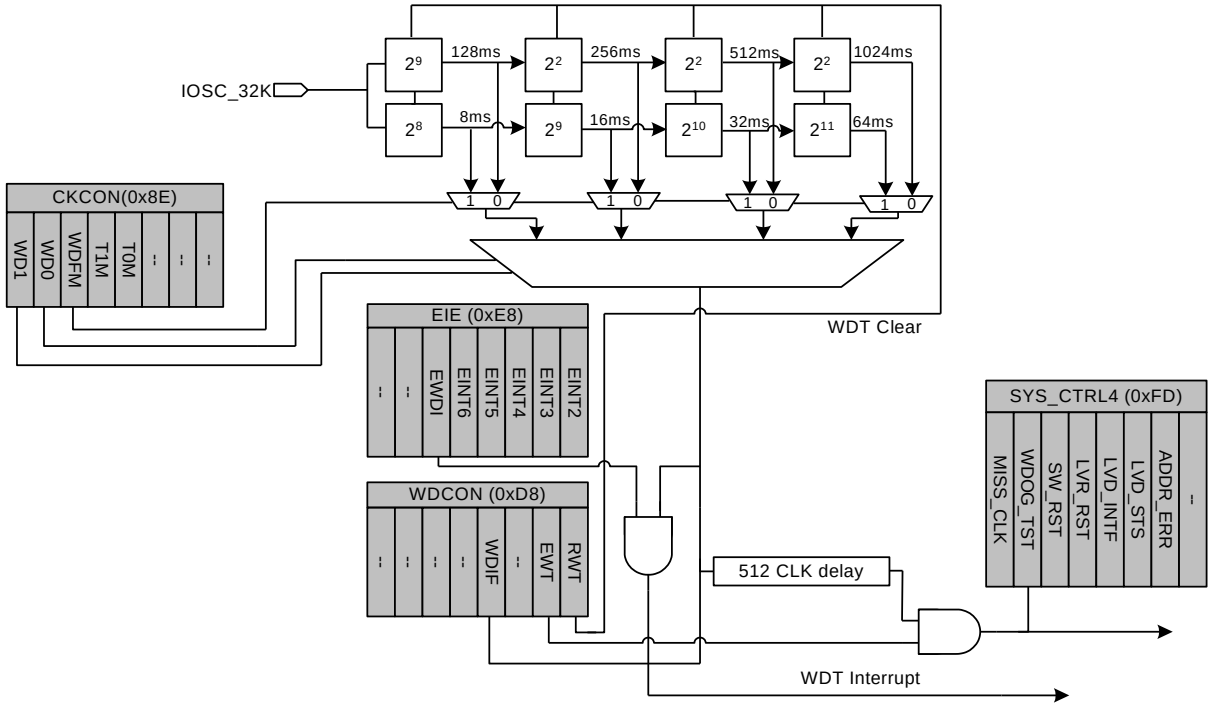


Figure 5-10 The block diagram of Watchdog timer

SYS_CTRL3			Page : 0 / Address: 0xFC		System Control 3 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	LVD_INT_EN	LVD_SEL[1:0]		LVD_EN	LVR_SEL[1:0]		LVR_EN
Default	0	0	1	0	0	1	0	0
Key Code	0x8F, 0x32, 0x50							

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	LVD_INT_EN	R/W	LVD interrupt enable 0 : disabled 1 : enabled	
5:4	LVD_SEL[1:0]	R/W	LVD voltage selection bits LVD_SEL[1:0] / Voltage 00 / 2.1V 01 / 2.6V 10 / 3.4V 11 / 4.4V	
3	LVD_EN	R/W	LVD enable control 0: disables LVD function 1: enables LVD function	
2:1	LVR_SEL[1:0]	R/W	LVR voltage selection bits LVR_SEL[1:0] / Voltage 00 / 1.9V 01 / 2.4V 10 / 3.2V 11 / 4.2V	
0	LVR_EN	R/W	LVR enable control 0: disables LVR function 1: enables LVR function	

Table 5-63 SYS_CTRL3 register

WDCON			Address: 0xD8		Watchdog Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	WDIF	--	EWT	RWT
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3	WDIF	R/W	Watchdog interrupt flag	
2	--	R/W	Reserved	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disabled 1: Enabled	
0	RWT	R/W	Reset watchdog timer 0: NA 1: Reset	

Table 5-64 WDCON register

KEYCODE			Address: 0xEB		KEYCODE Register			
Bit	7	6	5	4	3	2	1	0
Function	KC7	KC6	KC5	KC4	KC3	KC2	KC1	KC0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	KEYCODE[7:0]	R/W	KEYCODE register	

Note 1: Some protected registers are needed to write correct key code to KEYCODE register before write data to them.

Note 2: User must turn-off global interrupt enable before using KEYCODE function.

Table 5-65 KEYCODE register

CKCON			Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	1	1	1

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:6</td><td>WD[1:0]</td><td>R/W</td><td>Watchdog timeout selection bits
If WDFM=0:
<table><tr><th>WD[1:0]</th><th>Timeout</th></tr><tr><td>00</td><td>128ms</td></tr><tr><td>01</td><td>256ms</td></tr><tr><td>10</td><td>512ms</td></tr><tr><td>11</td><td>1024ms</td></tr></table>If WDFM=1:
<table><tr><th>WD[1:0]</th><th>Timeout</th></tr><tr><td>00</td><td>8ms</td></tr><tr><td>01</td><td>16ms</td></tr><tr><td>10</td><td>32ms</td></tr><tr><td>11</td><td>64ms</td></tr></table></td><td></td></tr>
<tr><td>5</td><td>WDFM</td><td>R/W</td><td>Watchdog fast mode selection bit
0: watchdog fast mode is disabled
1: watchdog fast mode is enabled</td><td></td></tr>
<tr><td>4</td><td>T1M</td><td>R/W</td><td>Timer 1 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF).
<table><tr><th>T1M</th><th>T01_CK_SEL</th><th>Timer1 Clock</th></tr><tr><td>0</td><td>0</td><td>System Clock / 8</td></tr><tr><td>0</td><td>1</td><td>System Clock / 2</td></tr><tr><td>1</td><td>0</td><td>System Clock / 4</td></tr><tr><td>1</td><td>1</td><td>System Clock / 1</td></tr></table></td><td></td></tr>
<tr><td>3</td><td>T0M</td><td>R/W</td><td>Timer 0 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF).
<table><tr><th>T0M</th><th>T01_CK_SEL</th><th>Timer0 Clock</th></tr><tr><td>0</td><td>0</td><td>System Clock / 8</td></tr><tr><td>0</td><td>1</td><td>System Clock / 2</td></tr><tr><td>1</td><td>0</td><td>System Clock / 4</td></tr></table></td><td></td></tr>
</table>

Bit	Function	Type	Description	Condition
			1 1 System Clock / 1	
2:0	--	R/W	Reserved	

Table 5-66 CKCON register

SYS_CTRL6			Address : 0xFF		System Control-6 Register			
Bit	7	6	5	4	3	2	1	0
Function	UART_IF_SEL		UART_IF_EN	T01_CK_SEL	--	AERR_RSTEN	WDOG_CKEN	RTC_CKEN
Default	1	1	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7:6	UART_IF_SEL[1:0]	R/W	UART IO interface select signal UART_IF_SEL[1 :0] / UART_TX / UART_RX 0X / P1[6] / P1[5] 10 / P4[7] / P5[0] 11 / P4[7] / P5[4]	
5	UART_IF_EN	R/W	UART interface enable signal. 0 : disabled 1 : enabled	
4	T01_CK_SEL	R/W	Timer0/1 clock source select signal.This bit is used combining with T0M/T1M of CKCON(0x8E). T0M /T1M / T01_CK_SEL / Timer0/1 Clock 0 / 0 / System Clock / 8 0 / 1 / System Clock / 2 1 / 0 / System Clock / 4 1 / 1 / System Clock / 1	
3	--	R/W	Reserved	
2	AERR_RSTEN	R/W	Flash address over range reset enable 0 : disabled 1 : enabled	
1	WDOG_CKEN	R/W	Watch dog controller clock enable control bit 0 : disabled 1 : enabled	
0	RTC_CKEN	R/W	RTC controller clock enable signal. 0 : disabled 1 : enabled	

Table 5-67 The SYS_CTRL6 register

SYS_CTRL4			Page : 0 / Address: 0xFD		System Control 4 Register			
Bit	7	6	5	4	3	2	1	0
Function	MISS_CLK	WDOG_RST	SW_RST_EN	LVR_RST	LVD_INTF	LVD_STS	ADDR_ERR	ERR_WR
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	MISS_CLK	R	Miss XTAL clock indicate flag	

Bit	Function	Type	Description	Condition
			0 : XTAL is normally work 1 : miss xtal clock	
6	WDOG_RST	R/W	Watch dog reset indicated flag read: 0 : Watchdog reset is inactive 1 : Watchdog reset is active Write: 0 : clears this bit 1 : no effect	
5	SW_RST_EN	R/W	Software reset enable signal 0 : disables software reset 1 : enables software reset	
4	LVR_RST	R/W	LVR indicated flag read: 0 : LVR is inactive 1 : LVR is active Write: 0 : clears this bit 1 : no effect	
3	LVD_INTF	R/W	LVD interrupt flag read: 0 : LVD is inactive 1 : LVD is active Write: 0 : clears this bit 1 : no effect	
2	LVD_STS	R	LVD status flag.: 0 : LVD is inactive 1 : LVD is active	
1	ADDR_ERR	R/W	Flash access address over range flag. read: 0 : flash access address is not over range 1 : flash access address is over range Write: 0 : clears this bit 1 : no effect	
1	ERR_WR	R/W	Flash is illegal programming or erasing flag. This flag will be set to high when a programming or erasing is out-of space or among lock_level range. read: 0 : legal programming or erasing 1 : illegal programming or erasing Write: 0 : clears this bit 1 : no effect	

Table 5-68 SYS_CTRL4 register

5.7.7. I/O Ports

5.7.8. Introduction

The GPM8F3732B has six I/O ports, including standard Port 0, Port 1, Port 2, Port 3 and additional Port 4, Port5. These port pins may be multiplexed with an alternate function for the peripheral features on the device. In general, when an initial reset state occurs, all ports are used as a general purpose input floating port function. All the input ports can be programmable pull high/low by DIR, ATT and Px registers. The P0, P0_ID, P0_DIR nd P0_ATT registers of Port 0 are controlled by 0x80, 0xA9 and SFRs 0xAA, 0xAB registers of page-0. The P1, P1_ID, P1_DIR and P1_ATT registers of Port 1 are controlled by 0x90, 0xB9 and SFRs 0xBA, 0xBB registers of page-0. The P2, P2_ID, P2_DIR and P2_ATT registers of Port 2 are controlled by 0xA0, 0xA1 and SFRs 0xA2, 0xA3 registers of page-0. The P3, P3_ID, P3_DIR and P3_ATT registers of Port 3 are controlled by 0xB0, 0xB1 and SFRs 0xB2, 0xB3 registers of page-0. The P4, P4_ID, P4_DIR and P4_ATT registers of Port 4 are controlled by 0xC0, 0xC1 and SFRs 0xC2, 0xC3 registers of page-1. The P5, P5_ID, P5_DIR and P5_ATT registers of Port 5 are controller by 0xC8, 0xC9 and SFRs 0xCA, 0xCB registers of page-1. The writing output data to the I/O port are performed via their corresponding SFRs P0(0x80), P1(0x90), P2(0xA0), P3(0xB0), P4(0xC0) and P5(0xC8). The reading data from the I/O port are performed via their corresponding SFRs P0_ID(0xA9), P1_ID(0xB9), P2_ID(0xA1), P3_ID(0xB1), P4_ID(0xC1) and P5_ID(0xC9). It is necessary that setting PX, PX_ATT, and PX_DIR register to ensure I/O State before using IO. Table 5-69 to table 5-72 are shows the truth table of analog pad and digital pad respectively. In GPM8F3732B, all of the GPIO port can be program to analog pad for special function. The detail descriptions of analog function are in corresponding sections. The built-in pull high/low resistor is 50KΩ. In addition to, there is a register for slew rate control (Px_SR) of each port. The default state of Px_SR register is '0x00' without slew rate control function. Figure 5-11, figure 5-13 show the block diagrams of the general purpose I/O.

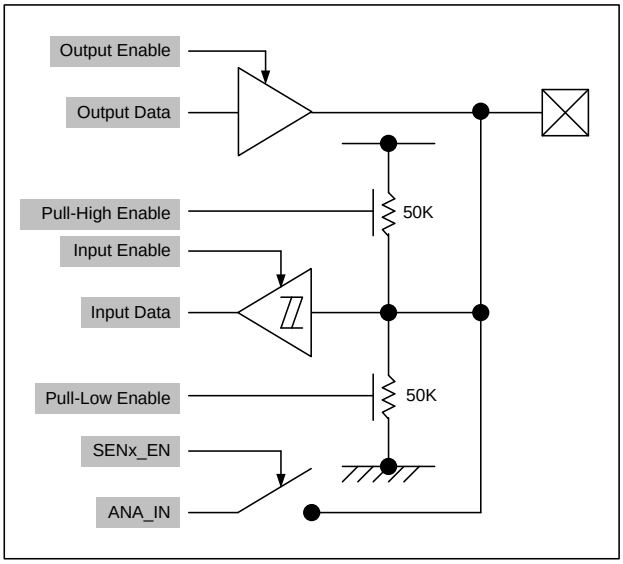


Figure 5-11 The block diagram of Port0_0 to Port1_0

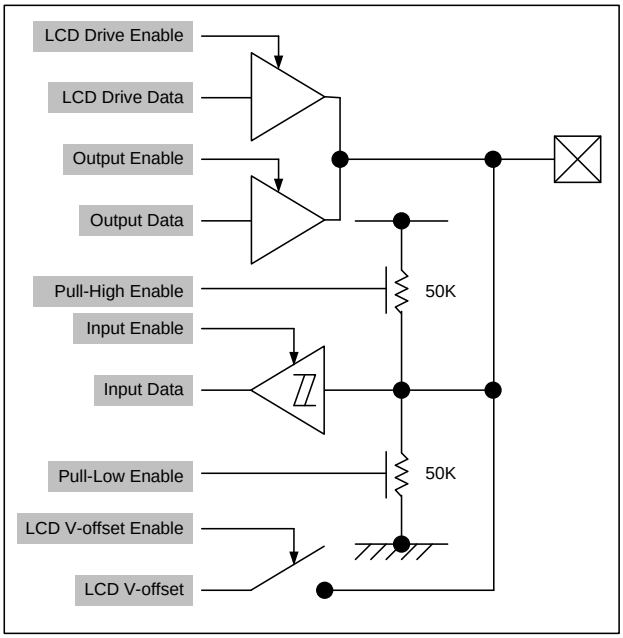


Figure 5-12 The block diagram of Port1_5 to Port1_7 and Port5

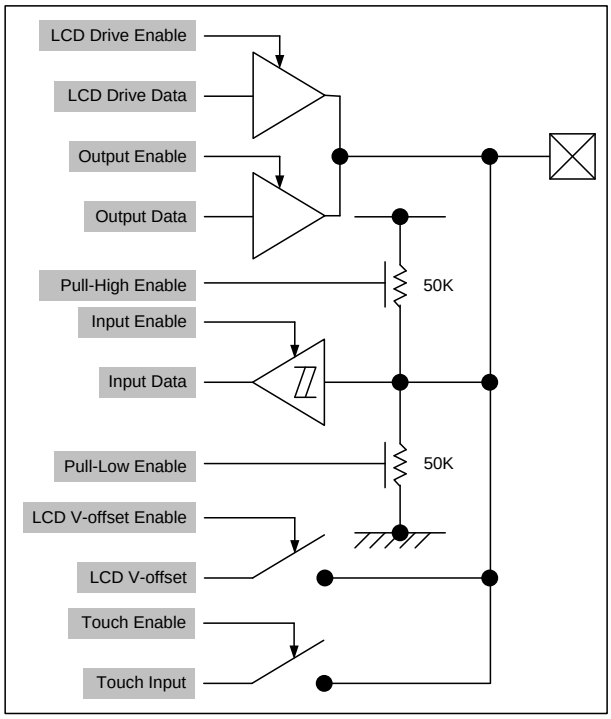


Figure 5-13 The block diagram of Port3_0 to Port4_7

DIR	ATT	Px	Function	Description
0	0	0	Floating	Float (High Impendence)
0	0	1	Floating	Float (High Impendence)
0	1	0	Pull Low*	Input with pull low
0	1	1	Pull High	Input with pull high
1	0	0	Output High	Output with buffer (inverted -content of buffer register)
1	0	1	Output Low	Output with buffer (inverted -content of buffer register)
1	1	0	Output Low	Output with buffer
1	1	1	Output High	Output with buffer

Table 5-69 The truth table of analog pad (for Port0_0 to Port1_0)

DIR	ATT	Px	LCD_COMX_EN	Function	Description
0	0	0	0	Floating	Float (High Impendence)
0	0	1	0	Floating	Float (High Impendence)
0	1	0	0	Pull Low*	Input with pull low
0	1	1	0	Pull High	Input with pull high
1	0	0	0	Output High	Output with buffer (inverted -content of buffer register)
1	0	1	0	Output Low	Output with buffer (inverted -content of buffer register)
1	1	0	0	Output Low	Output with buffer
1	1	1	0	Output High	Output with buffer
X	X	X	1	Floating	Analog interface

Table 5-70 The truth table of analog pad (for Port1_1 to Port1_4)

DIR	ATT	Px	LCD_SEGX_EN	Function	Description
0	0	0	0	Floating	Float (High Impendence)
0	0	1	0	Floating	Float (High Impendence)
0	1	0	0	Pull Low*	Input with pull low
0	1	1	0	Pull High	Input with pull high
1	0	0	0	Output High	Output with buffer (inverted -content of buffer register)
1	0	1	0	Output Low	Output with buffer (inverted -content of buffer register)
1	1	0	0	Output Low	Output with buffer
1	1	1	0	Output High	Output with buffer
X	X	X	1	Floating	Analog interface

Table 5-71 The truth table of analog pad (for Port1_5 to Port1_7 and Port5)

DIR	ATT	Px	LCD_SEGX_EN	TCH_EN	Function	Description
0	0	0	0	0	Floating	Float (High Impendence)
0	0	1	0	0	Floating	Float (High Impendence)
0	1	0	0	0	Pull Low*	Input with pull low
0	1	1	0	0	Pull High	Input with pull high
1	0	0	0	0	Output High	Output with buffer (inverted -content of buffer register)
1	0	1	0	0	Output Low	Output with buffer (inverted -content of buffer register)
1	1	0	0	0	Output Low	Output with buffer
1	1	1	0	0	Output High	Output with buffer
X	X	X	1	0	Floating	Analog interface
X	X	X	0	1	Floating	Analog interface

Table 5-72 The truth table of analog pad (for Port3_0 to Port3_7)

P0			Address: 0x80		Port0 Register			
Bit	7	6	5	4	3	2	1	0
Function	P07	P06	P05	P04	P03	P02	P01	--
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:1	P0[7:1]	R/W	P0 is used to set IO output data only. Otherwise, that also can be used to configure the Port0 function.	
0	--	R/W	Reserved	

Table 5-73 P0 register

P1			Address: 0x90		Port1 Register			
Bit	7	6	5	4	3	2	1	0
Function	P17	P16	P15	P14	P13	P12	P11	-
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:1	P1[7:1]	R/W	P1 is used to set IO output data only. Otherwise, that also can be used to configure the Port1 function.	
0	--	R/W	Reserved	

Table 5-74 P1 register

P2			Address: 0xA0		Port2 Register			
Bit	7	6	5	4	3	2	1	0
Function	P27	P26	P25	P24	P23	P22	P21	P20
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P2[7:0]	R/W	P2 is used to set IO output data only. Otherwise, that also can be used to configure the Port2 function.	

Table 5-75 P2 register

P3			Address: 0xB0		Port3 Register			
Bit	7	6	5	4	3	2	1	0
Function	P37	P36	P35	P34	P33	P32	P31	P30
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P3[7:0]	R/W	P3 is used to set IO output data only. Otherwise, that also can be used to configure the Port3 function.	

Table 5-76 P3 register

P4			Address: 0xC0		Port4 Register			
Bit	7	6	5	4	3	2	1	0
Function	P47	P46	P45	P44	P43	P42	P41	P40
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
7:0	P4[7:0]	R/W	P4 is used to set IO output data only. Otherwise, that also can be used to configure the Port4 function.	

Table 5-77 P4 register

P5			Address: 0xC8		Port5 Register			
Bit	7	6	5	4	3	2	1	0
Function	DIV_INTF	MUL_INTF	--	P54	P53	P52	P51	P50
Default	0	0	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
7	DIV_INTF	R	Divider interrupts flag. 0 : idle / busy 1 : Divider interrupt trigger	
6	MUL_INTF	R	Multiplier interrupts flag. 0 : idle / busy 1 : Multiplier interrupt trigger	
4:0	P5[4:0]	R/W	P5 is used to set IO output data only. Otherwise, that also can be used to configure the Port5 function.	

Table 5-78 P5 register

P0_ID			Address: 0xA9		Port0 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_ID[7:1]							--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	P0_ID[7:1]	R/W	P0_ID is used to read-back I/O input state only.	
0	--	R/W	Reserved	

Table 5-79 P0_ID register

P1_ID			Address: 0xB9		Port1 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_ID[7:1]							--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	P1_ID[7:1]	R/W	P1_ID is used to read-back I/O input state only.	
0	--	R/W	Reserved	

Table 5-80 P1_ID register

P2_ID			Address: 0xA1		Port2 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_ID[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_ID[7:0]	R/W	P2_ID is used to read-back I/O input state only.	

Table 5-81 P2_ID register

P3_ID			Address: 0xB1		Port3 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P3_ID[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P3_ID[7:0]	R/W	P3_ID is used to read-back I/O input state only.	

Table 5-82 P3_ID register

P4_ID			Address: 0xC1		Port4 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	P4_ID[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P4_ID[7:0]	R/W	P4_ID is used to read-back I/O input state only.	

Table 5-83 P4_ID register

P5_ID			Address: 0xC9		Port5 Input Data Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P5_ID[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P5_ID[4:0]	R/W	P5_ID is used to read-back I/O input state only.	

Note: If P0_PU and P0_PD are setting to '1' simultaneously, P0 will be output mode

Table 5-84 P5_ID register

P0_DIR			Page : 0 / Address: 0xAA		Port0 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_DIR[7:1]							--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	P0_DIR[7:1]	R/W	P0_DIR is use to configure the Port0 function. That indicates direction of corresponding I/O.	
0	--	R/W	Reserved	

Table 5-85 P0_DIR register

P1_DIR			Page : 0 / Address: 0xBA		Port1 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_DIR[7:1]							--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	P1_DIR[7:1]	R/W	P1_DIR is use to configure the Port1 function. That indicates direction of corresponding I/O.	
0	--	R/W	Reserved	

Table 5-86 P1_DIR register

P2_DIR			Page : 0 / Address: 0xA2		Port2 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_DIR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_DIR[7:0]	R/W	P2_DIR is use to configure the Port2 function. That indicates direction of corresponding I/O.	

Table 5-87 P2_DIR register

P3_DIR			Page : 0 / Address: 0xB2		Port3 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P3_DIR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P3_DIR[7:0]	R/W	P3_DIR is use to configure the Port3 function. That indicates direction of corresponding I/O.	

Table 5-88 P3_DIR register

P4_DIR			Page : 1 / Address: 0xC2		Port4 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P4_DIR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P4_DIR[7:0]	R/W	P4_DIR is use to configure the Port4 function. That indicates direction of corresponding I/O.	

Table 5-89 P4_DIR register

P5_DIR			Page : 1 / Address: 0xCA		Port5 Direction Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P5_DIR[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P5_DIR[4:0]	R/W	P5_DIR is use to configure the Port5 function. That indicates direction of corresponding I/O.	

Table 5-90 P5_DIR register

P0_ATT			Page : 0 / Address: 0xAB		Port0 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_ATT[7:1]							--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	P0_ATT[7:1]	R/W	P0_ATT can use to configure the Port0 function.	
0	--	R/W	Reserved	

Table 5-91 P0_ATT register

P1_ATT			Page : 0 / Address: 0xBB		Port1 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_DIR[7:1]							--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	P1_ATT[7:1]	R/W	P1_ATT can use to configure the Port1 function.	
0	--	R/W	Reserved	

Table 5-92 P1_ATT register

P2_ATT			Page : 0 / Address: 0xA3		Port2 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_ATT[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_ATT[7:0]	R/W	P2_ATT can use to configure the Port2 function.	

Table 5-93 P2_ATT register

P3_ATT			Page : 0 / Address: 0xB3		Port3 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	P3_ATT[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P3_ATT[7:0]	R/W	P3_ATT can use to configure the Port3 function.	

Table 5-94 P3_ATT register

P4_ATT			Page : 1 / Address: 0xC3		Port4 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	P4_ATT[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P4_ATT[7:0]	R/W	P4_ATT can use to configure the Port4 function.	

Table 5-95 P4_ATT register

P5_ATT			Page : 1 / Address: 0xCB		Port5 Attribute Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P5_ATT[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P5_ATT[4:0]	R/W	P5_ATT can use to configure the Port5 function.	

Table 5-96 P5_ATT register

P0_DRV			Page : 0 / Address: 0xAC		Port0 Driving Capability Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_DRV[7:1]							--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	P0_DRV[7:1]	R/W	P0_DRV can use to configure the Port0 driving capability.	
0	--	R/W	Reserved	

Table 5-97 P0_DRV register

P1_DRV			Page : 0 / Address: 0xBC		Port1 Driving Capability Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_DRV[7:1]							--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	P1_DRV[7:1]	R/W	P1_DRV can use to configure the Port1 driving capability.	
0	--	R/W	Reserved	

Table 5-98 P1_DRV register

P2_DRV			Page : 0 / Address: 0xA4		Port2 Driving Capability Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_DRV[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_DRV[7:0]	R/W	P2_DRV can use to configure the Port2 driving capability.	

Table 5-99 P2_DRV register

P3_DRV			Page : 0 / Address: 0xB4		Port3 Driving Capability Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P3_DRV[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P3_DRV[7:0]	R/W	P3_DRV can use to configure the Port3 driving capability.	

Table 5-100 P3_DRV register

P4_DRV			Page : 1 / Address: 0xC4		Port4 Driving Capability Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P4_DRV [7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P4_DRV [7:0]	R/W	P4_DRV can use to configure the Port4 driving capability.	

Table 5-101 P4_DRV register

P5_DRV			Page : 1 / Address: 0xCC		Port5 Driving Capability Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P5_DRV[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P5_DRV[4:0]	R/W	P5_DRV can use to configure the Port5 driving capability.	

Table 5-102 P5_DRV register

P0_SR			Page : 0 / Address: 0xAD		Port0 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_SR[7:1]							--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	P0_SR[7:1]	R/W	P0_SR can use to configure the Port0 output slew rate,	
0	--	R/W	Reserved	

Table 5-103 P0_SR register

P1_SR			Page : 0 / Address: 0xBD		Port1 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P1_SR[7:1]							--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	P1_SR[7:1]	R/W	P1_SR can use to configure the Port1 output slew rate,	
0	--	R/W	Reserved	

Table 5-104 P1_SR register

P2_SR			Page : 0 / Address: 0xA5		Port2 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_SR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_SR[7:0]	R/W	P2_SR can use to configure the Port2 output slew rate,	

Table 5-105 P2_SR register

P3_SR			Page : 0 / Address: 0xB5		Port3 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P3_SR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P3_SR[7:0]	R/W	P3_SR can use to configure the Port3 output slew rate,	

Table 5-106 P3_SR register

P4_SR			Page : 1 / Address: 0xC5		Port4 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P4_SR [7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P4_SR [7:0]	R/W	P4_SR can use to configure the Port4 output slew rate,	

Table 5-107 P4_SR register

P5_SR			Page : 1 / Address: 0xCD		Port5 Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P5_SR[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P5_SR[4:0]	R/W	P5_SR can use to configure the Port5 output slew rate,	

Table 5-108 P5_SR register

P2_HS			Page : 0 / Address: 0xA6		Port2 High Sink Current Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P2_HS[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P2_HS[7:0]	R/W	P2_HS can use to configure the Port2 to high sinking current mode (24mA).	

Table 5-109 P2_HS register

5.8. Timer Module

5.8.1. Introduction

GPM8F3732B is equipped with five timers. They are Timer 0, Timer 1, Timer A, Timer B and Timer C respectively. In addition, Timer B also features Compare/Capture function.

Timer A, Timer C features Capture function. The Timer 0 and Timer 1 are up-count timers with 16-bit resolution. The Timer A, Timer B, Timer C are down-count timers and with 16-bit resolution. Each timer's function is described in the following sections.

5.8.2. Timer 0/1

Timer 0 and Timer 1 are fully compatible with the standard 8051 timers. Each timer consists of two 8-bit registers TH0(0x8C), TL0(0x8A), TH1(0x8D), TL1(0x8B). Timer 0 and Timer 1 work in the same three modes except for mode 3 and the related control registers are TMOD(0x89), TCON(0x88) and CKCON(0x8E) registers. In the timer mode, timer registers are incremented every 1/2/4/8 SYSCLK periods depends on CKCON(0x8E) and SYS_CTRL6(0xFF) setting, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on theirs corresponding input pins: T0 or T1. The input pins are sampled every CLK period.

TH0			Address: 0x8C		Timer0 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH0[7:0]	R/W	Timer 0 Load value – high byte	

Table 5-110 TH0 register

TL0			Address: 0x8A		Timer0 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL0[7:0]	R/W	Timer 0 Load value – low byte	

Table 5-111 TL0 register

TH1			Address: 0x8D		Timer1 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH1[7:0]	R/W	Timer 1 Load value – high byte	

Table 5-112 TH1 register

TL1			Address: 0x8B		Timer1 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL1[7:0]	R/W	Timer 1 Load value – low byte	

Table 5-113 TL1 register

TMOD			Address: 0x89		Timer0/1 Control Mode Register			
Bit	7	6	5	4	3	2	1	0
Function	--	CT1	M11	M10	--	CT0	M01	M00
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	CT1	R/W	Counter or timer select bit 0: Timer mode, internally clocked	

Bit	Function	Type	Description	Condition
			1: Counter mode, Timer 1 clock source is from 32KHz XTAL source	
5:4	M1[1:0]	R/W	Mode select bits of timer 1, which is tabled as Table 5-115	
3	--	R/W	Reserved	
2	CT0	R/W	Counter or timer select bit 0: Timer mode, internally clocked 1: Counter mode, Timer 0 clock source is from 32KHz XTAL source	
1:0	M0[1:0]	R/W	Mode select bits of timer 0, which is tabled as Table 5-115	

Table 5-114 TMOD register

M1	M0	Mode	Function description
0	0	0	TH0/1 operates as 8-bit timer/counter with a divide by 32 pre-scaler served by lower 5-bit of TL0/1.
0	1	1	16-bit timer/counter. TH0/1 and TL0/1 are cascaded
1	0	2	TL0/1 operates as 8-bit timer/counter with 8-bit auto-reload by TH0/1
1	1	3	TL0 is configured as 8-bit timer/counter controlled by the standard Timer 0 bits. TH0 is an 8-bit timer controlled by the Timer 1 controls bits. Timer 1 holds its count.

Table 5-115 Four modes of Timer 0 and Timer 1

TCON			Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	ADCF	--	TAF	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: disabled ; 1: enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	
4	TR0	R/W	Timer 0 run control bit 0: disabled ; 1: enabled	
3	ADCF	R/W	ADC0 interrupt flag	
2	--	R/W	Reserved	
1	TAF	R/W	Timer A interrupt flag	
0	--	R/W	Reserved	

Table 5-116 TCON register

CKCON			Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits If WDFM=0:	

Bit	Function	Type	Description	Condition
			WD[1:0] / Timeout 00 / 128ms 01 / 256ms 10 / 512ms 11 / 1024ms If WDFM=1: WD[1:0] / Timeout 00 / 8ms 01 / 16ms 10 / 32ms 11 / 64ms	
5	WDFM	R/W	Watchdog fast mode selection bit 0: watchdog fast mode is disabled 1: watchdog fast mode is enabled	
4	T1M	R/W	Timer 1 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF). T1M / T01_CK_SEL / Timer1 Clock 0 / 0 / System Clock / 8 0 / 1 / System Clock / 2 1 / 0 / System Clock / 4 1 / 1 / System Clock / 1	
3	T0M	R/W	Timer 0 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF). T0M / T01_CK_SEL / Timer0 Clock 0 / 0 / System Clock / 8 0 / 1 / System Clock / 2 1 / 0 / System Clock / 4 1 / 1 / System Clock / 1	
2:0	--	R/W	Reserved	

Table 5-117 CKCON register

SYS_CTRL6			Address : 0xFF		System Control-6 Register			
Bit	7	6	5	4	3	2	1	0
Function	UART_IF_SEL		UART_IF_EN	T01_CK_SEL	--	AERR_RSTEN	WDOG_CKEN	RTC_CKEN
Default	1	1	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7:6	UART_IF_SEL[1:0]	R/W	UART IO interface select signal UART_IF_SEL[1 :0] / UART_TX / UART_RX 0X / P1[6] / P1[5] 10 / P4[7] / P5[0] 11 / P4[7] / P5[4]	
5	UART_IF_EN	R/W	UART interface enable signal.	

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td></td><td></td><td></td><td>0 : disabled
1 : enabled</td><td></td></tr>
<tr><td>4</td><td>T01_CK_SEL</td><td>R/W</td><td>Timer0/1 clock source select signal.This bit is used combining with T0M/T1M of CKCON(0x8E).
<table>
<tr><th>T0M /T1M</th><th>T01_CK_SEL</th><th>Timer0/1 Clock</th></tr>
<tr><td>0</td><td>0</td><td>System Clock / 8</td></tr>
<tr><td>0</td><td>1</td><td>System Clock / 2</td></tr>
<tr><td>1</td><td>0</td><td>System Clock / 4</td></tr>
<tr><td>1</td><td>1</td><td>System Clock / 1</td></tr>
</table></td><td></td></tr>
<tr><td>3</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
<tr><td>2</td><td>AERR_RSTEN</td><td>R/W</td><td>Flash address over range reset enable
0 : disabled
1 : enabled</td><td></td></tr>
<tr><td>1</td><td>WDOG_CKEN</td><td>R/W</td><td>Watch dog controller clock enable control bit
0 : disabled
1 : enabled</td><td></td></tr>
<tr><td>0</td><td>RTC_CKEN</td><td>R/W</td><td>RTC controller clock enable signal.
0 : disabled
1 : enabled</td><td></td></tr>
</table>

Table 5-118 The SYS_CTRL6 register

5.8.2.1. Timer 0: Mode 0 (13-Bit Timer/Counter)

In this mode, Timer 0 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 0 interrupt flag TF0 is set. The counted input is enabled to the Timer 0 when TR0(TCON[4]) = 1 and the input source is 32KHz clock. The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Figure 5-14 shows the block diagram of Timer 0 for Mode 0.

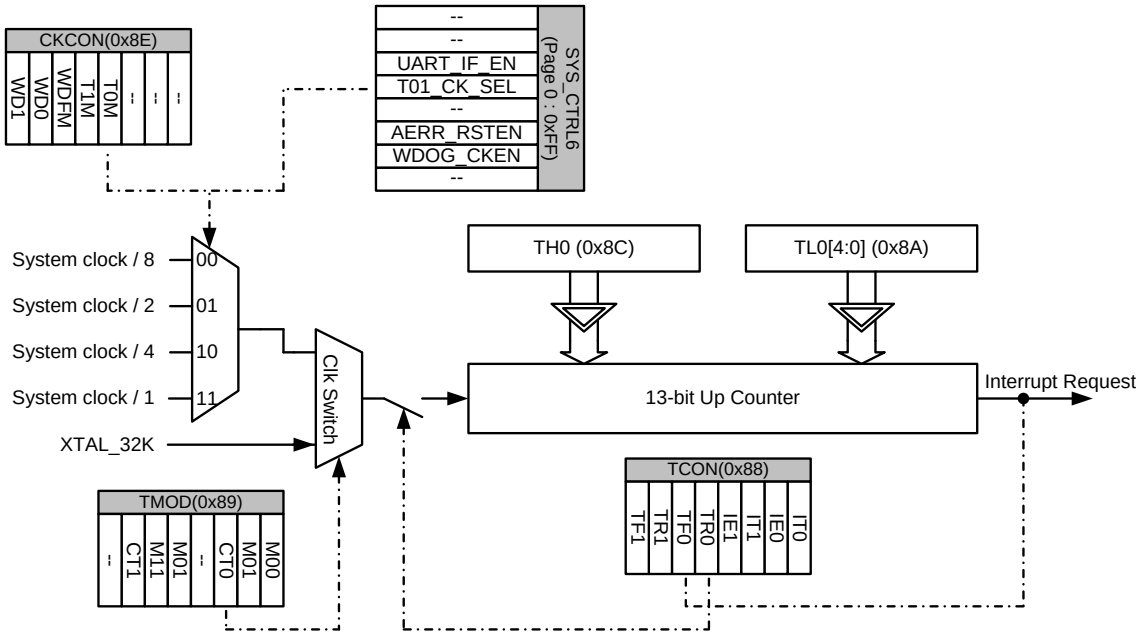


Figure 5-14 The block diagram of Timer 0 for Mode 0

5.8.2.2. Timer 0: Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in figure 5-15.

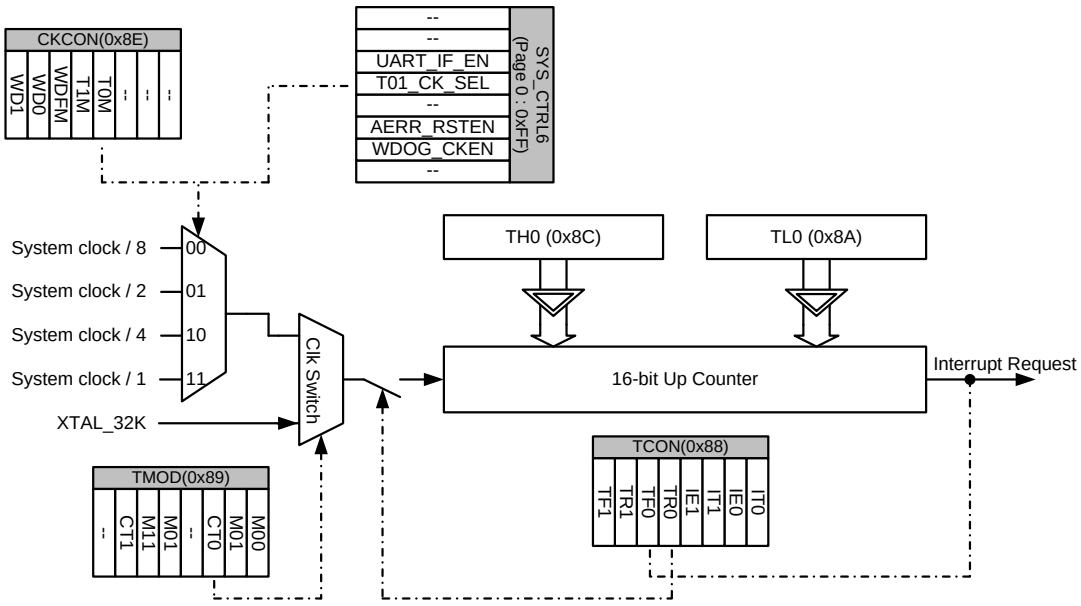


Figure 5-15 The block diagram of Timer 0 for Mode 1

5.8.2.3. Timer 0: Mode 2 (8-bit Timer/Counter with Auto-reload Function)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reloads, as shown in figure 5-16. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is loaded by software. The reload leaves TH0 unchanged.

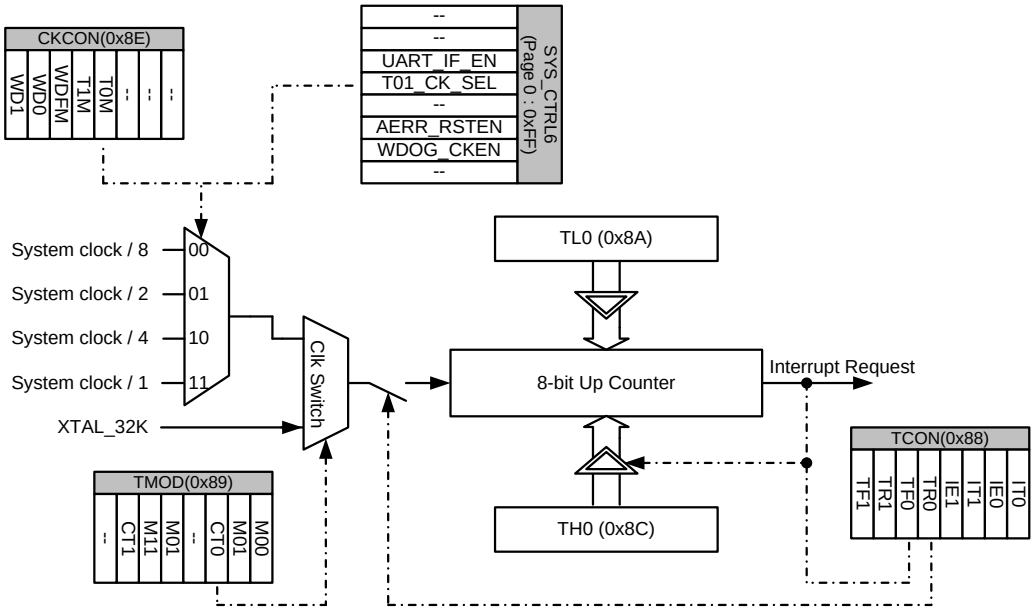


Figure 5-16 The block diagram of Timer 0 for Mode 2

5.8.2.4. Timer 0: Mode 3 (Two 8-Bit Timers/Counters)

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The block diagram for Mode 3 on Timer 0 is shown in figure 5-17. TL0 uses the Timer 0 control bits: CT0, GATE0, TR0, and TF0. TH0 is locked into a timer function and uses the TR1 and TF1 flags from Timer 1 and controls Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer/counter. When Timer 0 is in Mode 3, Timer 1 can be turned off by switching it into its own Mode 3, or can still be used by the serial channel as a baud rate generator, or in any application where interrupt from Timer 1 is not required.

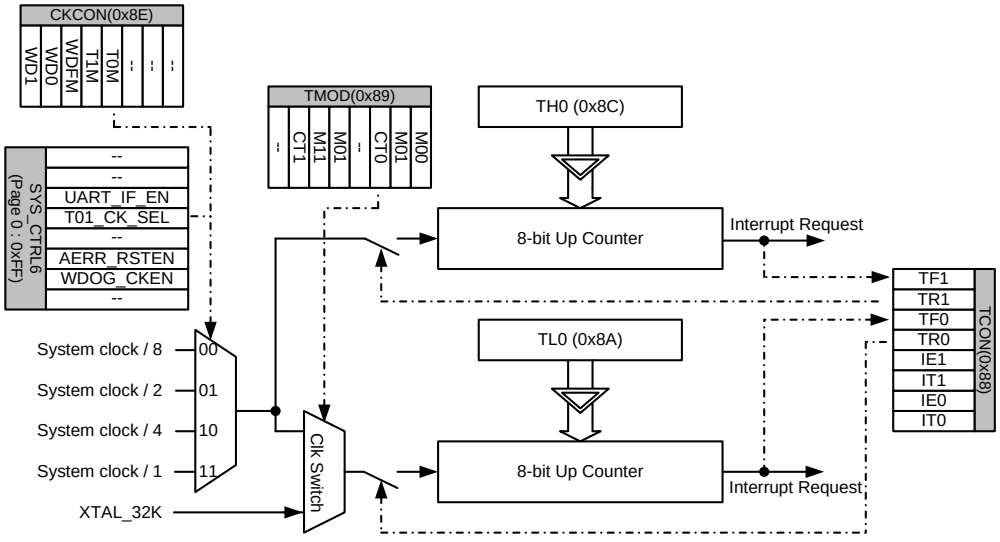


Figure 5-17 The block diagram of Timer 0 for Mode 3

5.8.2.5. Timer 1: Mode 0 (13-Bit Timer/Counter)

In this mode, the Timer 1 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 1 interrupt flag TF1 is set. The counted input is enabled to the Timer1 when TR1(TCON[6]) = 1 and the input source is 32KHz clock. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Figure 5-18 shows the block diagram of Timer1 for Mode 0

.

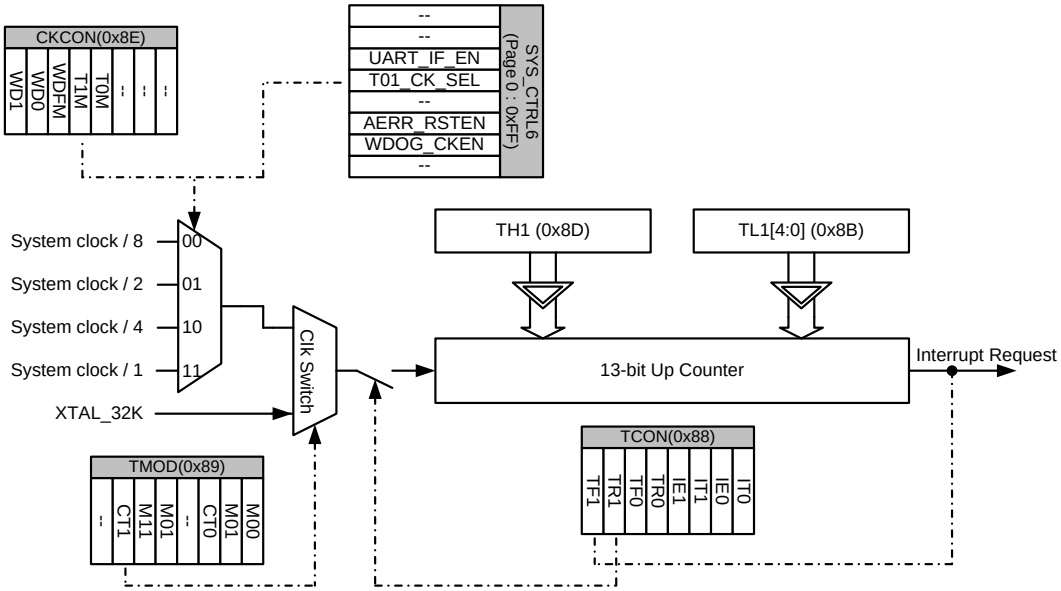


Figure 5-18 The block diagram of Timer 1 for Mode 0

5.8.2.6. Timer 1: Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in figure 5-19.

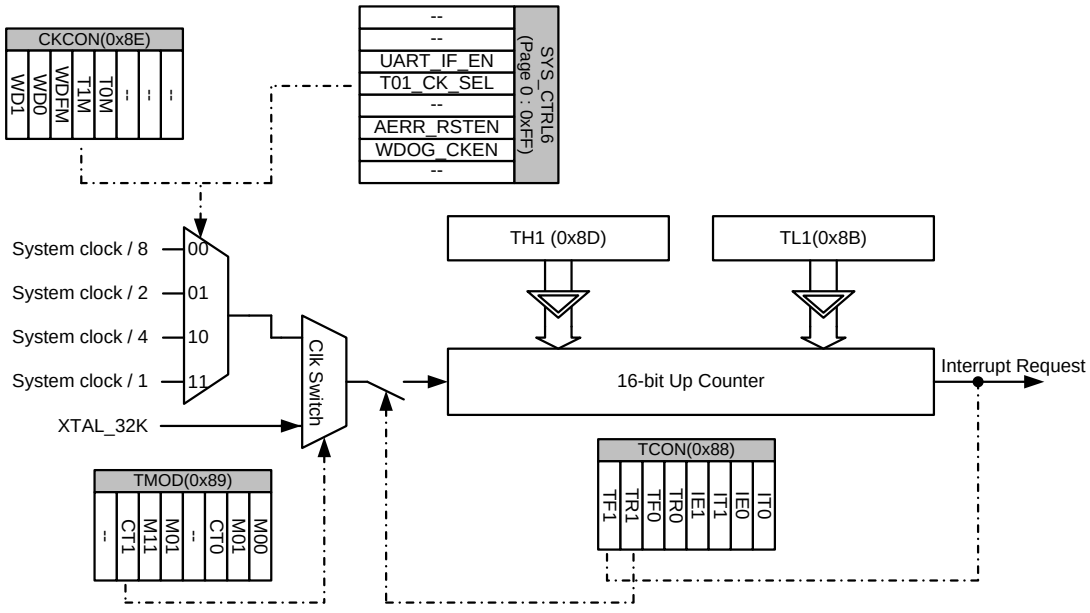


Figure 5-19 The block diagram of Timer 1 for Mode 1

5.8.2.7. Timer 1: Mode 2 (8-Bit Timer/Counter with Auto-reload Function)

Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reloads, as shown in figure 5-20. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is loaded by software. The reload leaves TH1 unchanged.

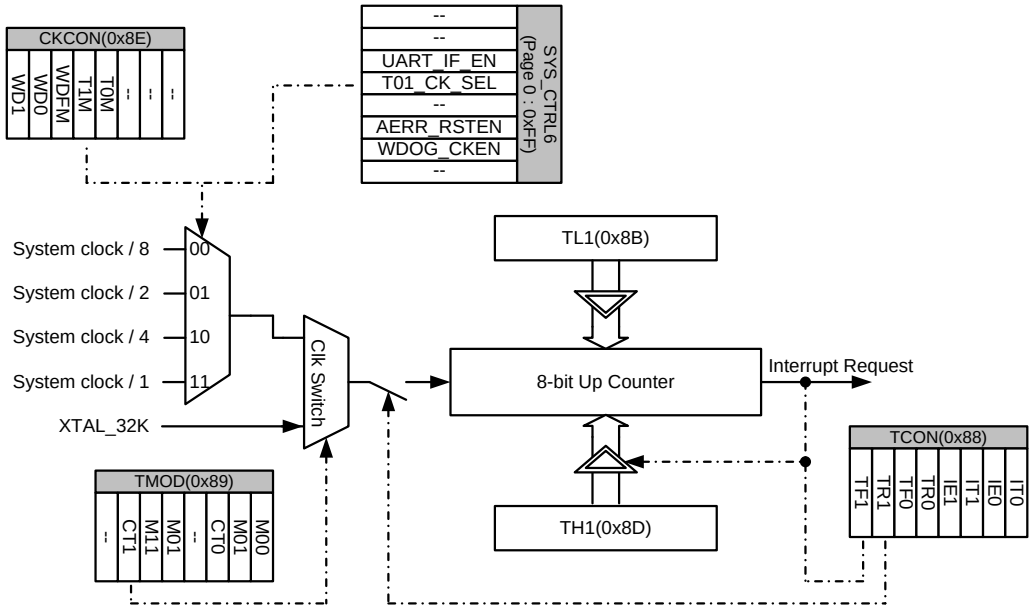


Figure 5-20 The block diagram of Timer 1 for Mode 2

5.8.2.8. Timer 1: Mode 3

Timer 1 in Mode 3 is has no timer function. The effect is the same as setting TR1=0.

5.8.3. Timer A

The Timer A, which is a 16-bit-wide register, can operate as timer. The additional Counter/Capture feature is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc.

5.8.4. Timer / Counter mode

In timer / counter function, that have up to 8 clock source can be selected. Thus, the 16-bit timer register is decremented in every clock periods. The figure 5-21 shows the block diagram of counter / timer function for Timer A. When Timer A rolls over from pre-load data (TMA_PLOAD_H/L) to 0, not only TMA_INTF is set but also Timer A registers is loaded with the 16-bit value from TMA_PLOAD_H/L register. Required TMA_PLOAD_H/L value can be preset by software.

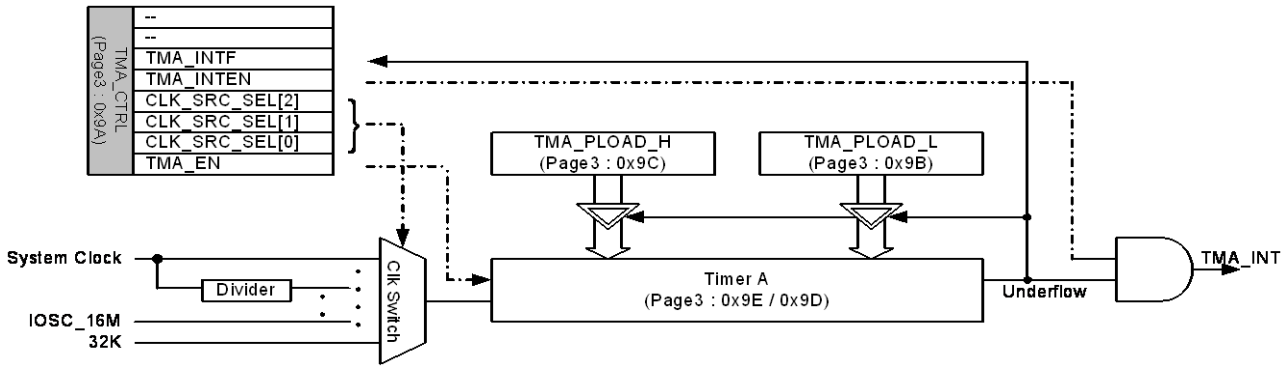


Figure 5-21 The block diagram of counter / timer function for Timer A

5.8.4.1. Capture functions

Each of capture registers can be used to latch the current 16-bit value of the Timer A registers (TMA_H and TMA_L) when an external event is triggered.

Figure 5-22 shows functional diagrams of the Timer A capture function.

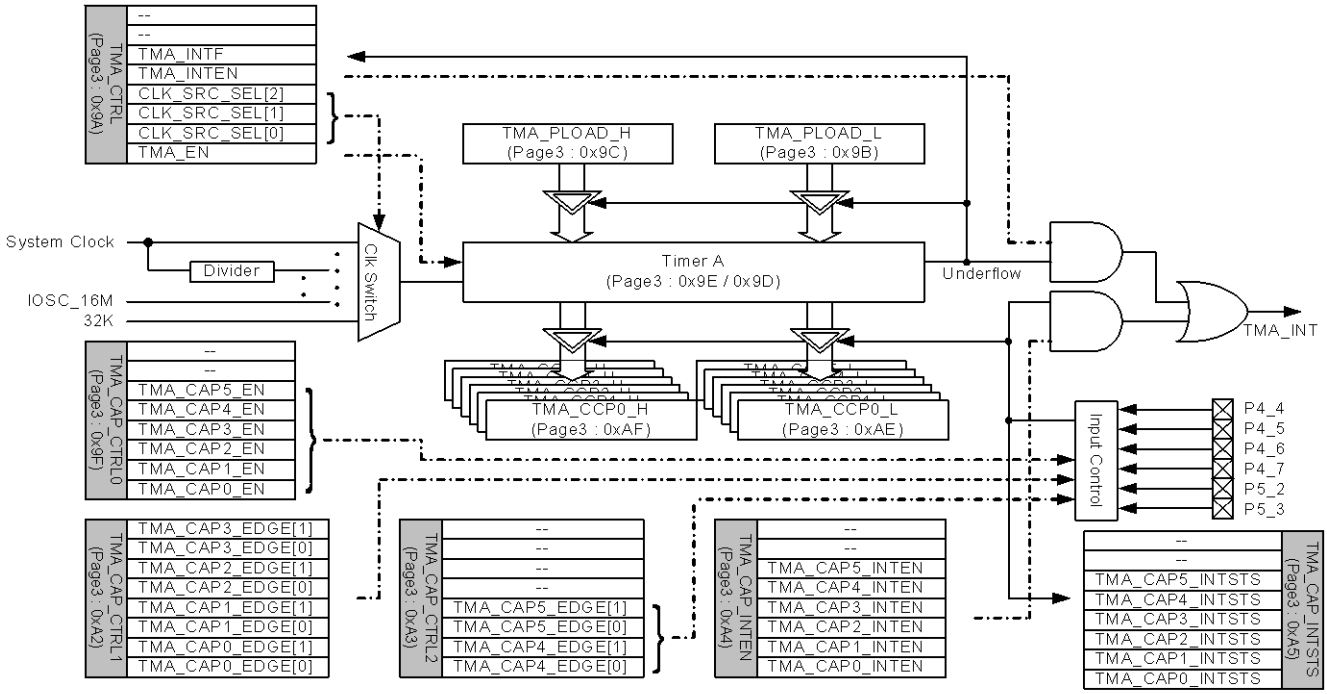


Figure 5-22 The block diagram of Timer A capture mode

5.8.4.2. Timer A Related Registers

TMA_CTRL			Page : 3 / Address: 0x9A		Timer A Control1 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_INTF	TMA_INTEN	CLK_SRC_SEL[2:0]			TMA_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	TMA_INTF	R/W	Timer A interrupt flag. read : 0 : idle / busy 1 : timer A interrupt trigger write : 0 : clears this bit 1 : no effect	
4	TMA_INTEN	R/W	Timer A interrupt enable control bit 0 : disabled 1 : enabled	
3:1	CLK_SRC_SEL	R/W	Timer A input clock source selection control bit CLK_SRC_SEL[2:0] | Clock Source 000 | System clock	

Bit	Function	Type	Description	Condition
			001 System clock / 2 010 System clock / 4 011 System clock / 8 100 System clock / 16 101 System clock / 32 110 IOSC_16M 111 32K (IOSC_32K or XTAL)	
0	TMA_EN	R/W	Timer A enable control bit. 0 : disabled 1 : enabled	

Table 5-119 TMA_CTRL register

TMA_PLOAD_L			Page : 3 / Address: 0x9B		Timer A Pre-Load Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PLOAD_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PLOAD_L[7:0]	R/W	Timer A pre-load data register – low byte	

Table 5-120 TMA_PLOAD_L register

TMA_PLOAD_H			Page : 3 / Address: 0x9C		Timer A Pre-Load Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_PLOAD_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_PLOAD_H[7:0]	R/W	Timer A pre-load data register – high byte	

Table 5-121 TMA_PLOAD_H register

TMA_L			Page : 3 / Address: 0x9D		Timer A Counter Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_L[7:0]	R/W	Timer A counter register – low byte	

Table 5-122 TMA_L register

TMA_H			Page : 3 / Address: 0x9E		Timer A Counter Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_H[7:0]	R/W	Timer A counter register – high byte	

Table 5-123 TMA_H register

TMA_CAP_CTRL0			Page : 3 / Address: 0x9F		Timer A Capture Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_CAPx_EN[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
1:0	TMA_CAPx_EN[5:0]	R/W	Timer A capture mode enable control bit. All of the trigger source are from external I/O. Following table is the trigger source mapping table. TMA_CAPx_EN / Mapping I/O TMA_CAP0_EN / P4[4] TMA_CAP1_EN / P4[5] TMA_CAP2_EN / P4[6] TMA_CAP3_EN / P4[7] TMA_CAP4_EN / P5[2] TMA_CAP5_EN / P5[3] 0: disabled 1: enabled	

Table 5-124 TMA_CAP_CTRL0 register

TMA_CAP_CTRL1			Page : 3 / Address: 0xA2		Timer A Capture Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CAP3_EDGE[1:0]		TMA_CAP2_EDGE[1:0]		TMA_CAP1_EDGE[1:0]		TMA_CAP0_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	TMA_CAP3_EDGE[7:6]	R/W	Timer A capture 3 sample edge selection bit 00: falling edge 01: rising edge 1x: both edges	
5:4	TMA_CAP2_EDGE[5:4]	R/W	Timer A capture 2 sample edge selection bit 00: falling edge 01: rising edge 1x: both edges	
3:2	TMA_CAP1_EDGE[3:2]	R/W	Timer A capture 1 sample edge selection bit 00: falling edge 01: rising edge 1x: both edges	
1:0	TMA_CAP0_EDGE[1:0]	R/W	Timer A capture 0 sample edge selection bit 00: falling edge 01: rising edge 1x: both edges	

Table 5-125 TMA_CAP_CTRL1 register

TMA_CAP_CTRL2			Page : 3 / Address: 0xA3		Timer A Capture Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMA_CAP5_EDGE[1:0]		TMA_CAP4_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:2	TMA_CAP5_EDGE[3:2]	R/W	Timer A capture 5 sample edge selection bit 00: falling edge 01: rising edge 1x: both edges	
1:0	TMA_CAP4_EDGE[1:0]	R/W	Timer A capture 4 sample edge selection bit 00: falling edge 01: rising edge 1x: both edges	

Table 5-126 TMA_CAP_CTRL2 register

TMA_CAP_INTEN			Page : 3 / Address: 0xA4		Timer A Capture Mode Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_CAPx_INTEN[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
1:0	TMA_CAPx_INTEN[5:0]	R/W	Timer A capture mode interrupt enable control bits. These are map to CAP0 ~ CAP5 respectively. 0: disabled 1: enabled	

Table 5-127 TMA_CAP_INTEN register

TMA_CAP_INTSTS			Page : 3 / Address: 0xA5		Timer A Capture Mode Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMA_CAPx_INTSTS[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
1:0	TMA_CAPx_INTSTS[5:0]	R/W	Timer A capture mode interrupt status register. These are map to CAP0 ~ CAP5 respectively. read : 0 : no capture triggered 1 : capture triggered write : 0 : clears this bit 1 : no effect	

Table 5-128 TMA_CAP_INTSTS register

TMA_CCP0_L			Page : 3 / Address: 0xAE		Timer A Counter / Capture 0 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP0_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP0_L[7:0]	R/W	Timer A Counter / Capture 0 register – low byte	

Table 5-129 TMA_CCP0_L register

TMA_CCP0_H			Page : 3 / Address: 0xAF		Timer A Counter / Capture 0 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP0_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP0_H[7:0]	R/W	Timer A Counter / Capture 0 register – high byte	

Table 5-130 TMA_CCP0_H register

TMA_CCP1_L			Page : 3 / Address: 0xB2		Timer A Counter / Capture 1 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP1_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP1_L[7:0]	R/W	Timer A Counter / Capture 1 register – low byte	

Table 5-131 TMA_CCP1_L register

TMA_CCP1_H			Page : 3 / Address: 0xB3		Timer A Counter / Capture 1 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP1_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP1_H[7:0]	R/W	Timer A Counter / Capture 1 register – high byte	

Table 5-132 TMA_CCP1_H register

TMA_CCP2_L			Page : 3 / Address: 0xB4		Timer A Counter / Capture 2 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP2_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP2_L[7:0]	R/W	Timer A Counter / Capture 2 register – low byte	

Table 5-133 TMA_CCP2_L register

TMA_CCP2_H			Page : 3 / Address: 0xB5		Timer A Counter / Capture 2 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP2_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP2_H[7:0]	R/W	Timer A Counter / Capture 2 register – high byte	

Table 5-134 TMA_CCP2_H register

TMA_CCP3_L			Page : 3 / Address: 0xB6		Timer A Counter / Capture 3 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP3_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP3_L[7:0]	R/W	Timer A Counter / Capture 3 register – low byte	

Table 5-135 TMA_CCP3_L register

TMA_CCP3_H			Page : 3 / Address: 0xB7		Timer A Counter / Capture 3 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP3_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP3_H[7:0]	R/W	Timer A Counter / Capture 3 register – high byte	

Table 5-136 TMA_CCP3_H register

TMA_CCP4_L			Page : 3 / Address: 0xBA		Timer A Counter / Capture 4 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP4_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP4_L[7:0]	R/W	Timer A Counter / Capture 4 register – low byte	

Table 5-137 TMA_CCP4_L register

TMA_CCP4_H			Page : 3 / Address: 0xBB		Timer A Counter / Capture 4 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP4_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP4_H[7:0]	R/W	Timer A Counter / Capture 4 register – high byte	

Table 5-138 TMA_CCP4_H register

TMA_CCP5_L			Page : 3 / Address: 0xBC		Timer A Counter / Capture 5 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP5_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP5_L[7:0]	R/W	Timer A Counter / Capture 5 register – low byte	

Table 5-139 TMA_CCP5_L register

TMA_CCP5_H			Page : 3 / Address: 0xBD		Timer A Counter / Capture 5 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMA_CCP5_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMA_CCP5_H[7:0]	R/W	Timer A Counter / Capture 5 register – high byte	

Table 5-140 TMA_CCP5_H register

5.8.5. Timer B

The Timer B, which is a 16-bit-wide register, can operate as timer. The additional Counter/Capture feature is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc.

5.8.5.1. Timer / Counter mode

In timer / counter function, that have up to 8 clock source can be selected. Thus, the 16-bit timer register is decremented in every clock periods. The figure5-23 shows the block diagram of counter / timer function for Timer B. When Timer B rolls over from pre-load data (TMB_PLOAD_H/L) to 0, not only TMB_INTF is set but also Timer B registers is loaded with the 16-bit value from TMB_PLOAD_H/L register. Required TMB_PLOAD_H/L value can be preset by software.

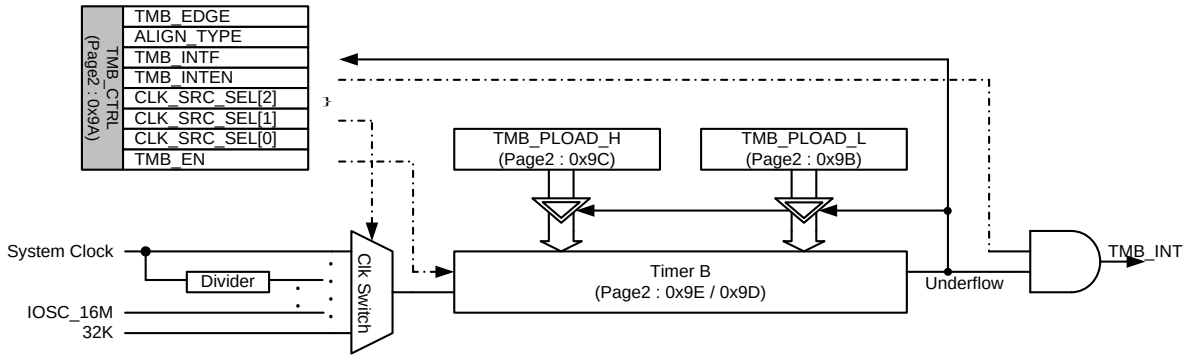


Figure 5-23 The block diagram of counter / timer function for Timer B

5.8.5.2. Capture functions

Each of capture registers can be used to latch the current 16-bit value of the Timer B registers (TMB_H and TMB_L) when an external event is triggered.

Figure 5-24 shows functional diagrams of the Timer B capture function.

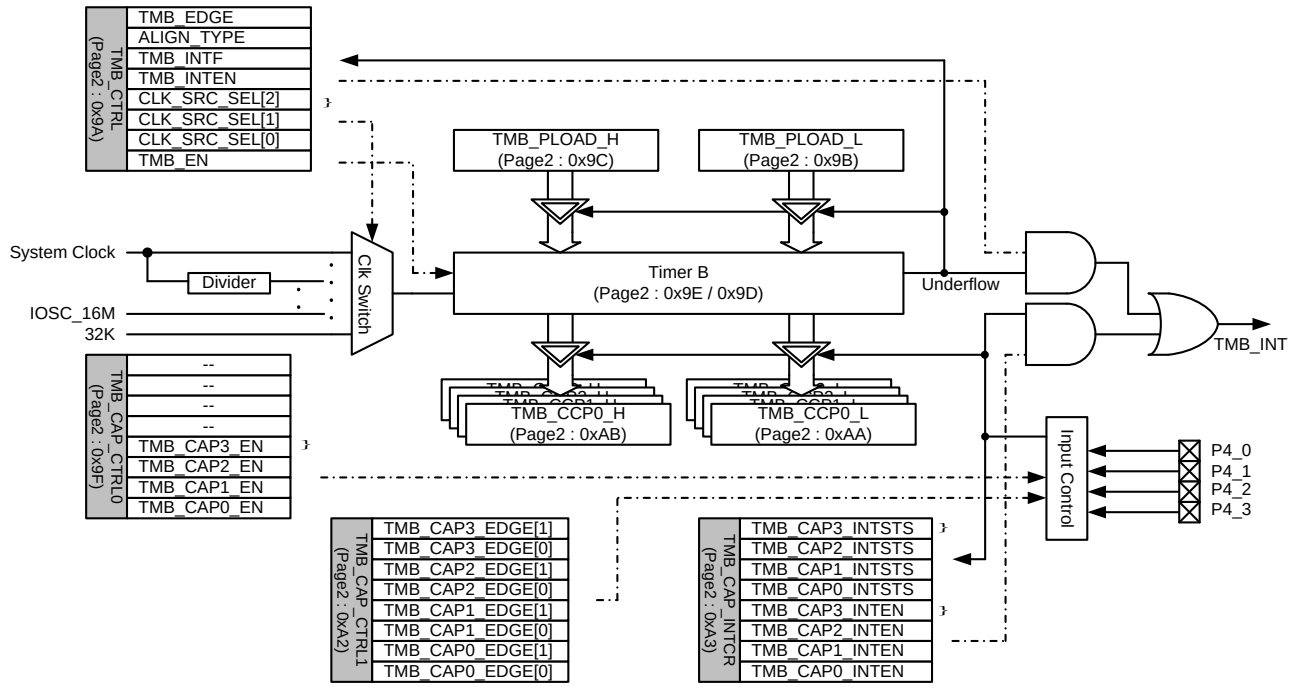


Figure 5-24 The block diagram of Timer B capture mode

5.8.5.3. Timer B Related Registers

TMB_CTRL			Page : 2 / Address: 0x9A		Timer B Control1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMB_EDGE	ALIGN_TYPE	TMB_INTF	TMB_INTEN	CLK_SRC_SEL[2:0]			TMB_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TMB_EDGE	R	Timer B up/down count edge indication. 0 : falling edge 1 : rising edge	
6	ALIGN_TYPE	R/W	0 : edge align 1 : center align	
5	TMB_INTF	R/W	Timer B interrupt flag. read : 0 : idle / busy 1 : timer B interrupt trigger write : 0 : clears this bit 1 : no effect	
4	TMB_INTEN	R/W	Timer B interrupt enable control bit 0 : disabled 1 : enabled	
3:1	CLK_SRC_SEL	R/W	Timer B input clock source selection control bit CLK_SRC_SEL[2:0] | Clock Source 000 | System clock 001 | System clock / 2	

Bit	Function	Type	Description	Condition
			010 System clock / 4 011 System clock / 8 100 System clock / 16 101 System clock / 32 110 IOSC_16M 111 32K (IOSC_32K or XTAL)	
0	TMB_EN	R/W	Timer B enable control bit. 0 : disabled 1 : enabled	

Table 5-141 TMB_CTRL register

TMB_PLOAD_L			Page : 2 / Address: 0x9B		Timer B Pre-Load Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_PLOAD_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_PLOAD_L[7:0]	R/W	Timer B pre-load data register – low byte	

Table 5-142 TMB_PLOAD_L register

TMB_PLOAD_H			Page : 2 / Address: 0x9C		Timer B Pre-Load Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_PLOAD_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_PLOAD_H[7:0]	R/W	Timer B pre-load data register – high byte	

Table 5-143 TMB_PLOAD_H register

TMB_L			Page : 2 / Address: 0x9D		Timer B Counter Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_L[7:0]	R/W	Timer B counter register – low byte	

Table 5-144 TMB_L register

TMB_H			Page : 2 / Address: 0x9E		Timer B Counter Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_H[7:0]	R/W	Timer B counter register – high byte	

Table 5-145 TMB_H register

TMB_CAP_CTRL0			Page : 2 / Address: 0x9F		Timer B Capture Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMB_CAPx_EN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	TMB_CAPx_EN[3:0]	R/W	Timer B capture mode enable control bit. All of the trigger source are from external I/O. Following table is the trigger source mapping table. TMB_CAPx_EN / Mapping I/O TMB_CAP0_EN / P4[0] TMB_CAP1_EN / P4[1] TMB_CAP2_EN / P4[2] TMB_CAP3_EN / P4[3] 0 : disabled 1 : enabled	

Table 5-146 TMB_CAP_CTRL0 register

TMB_CAP_CTRL1			Page : 2 / Address: 0xA2		Timer B Capture Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CAP3_EDGE[1:0]		TMB_CAP2_EDGE[1:0]		TMB_CAP1_EDGE[1:0]		TMB_CAP0_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	TMB_CAP3_EDGE[7:6]	R/W	Timer B capture 3 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edges	
5:4	TMB_CAP2_EDGE[5:4]	R/W	Timer B capture 2 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edges	
3:2	TMB_CAP1_EDGE[3:2]	R/W	Timer B capture 1 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edges	
1:0	TMB_CAP0_EDGE[1:0]	R/W	Timer B capture 0 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edges	

Table 5-147 TMB_CAP_CTRL1 register

TMB_CAP_INTCTRL			Page : 2 / Address: 0xA3		Timer B Capture Mode Interrupt Control Register			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CAP_INTSTS[3:0]				TMB_CAP_INTEN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	TMB_CAP_INTSTS[3:0]	R/W	Timer B capture mode trigger flag. These are map to CAP0 ~ CAP3 respectively. read : 0 : no capture signal triggered 1 : capture signal triggered write : 0 : clears this bit 1 : no effect	
3:0	TMB_CAP_INTEN	R/W	Timer B capture mode interrupt enable control bits. These are map to CAP0 ~ CAP3 respectively. 0 : disabled 1 : enabled	

Table 5-148 TMB_CAP_INTCTRL registers

TMB_CCP0_L			Page : 2 / Address: 0xAA		Timer B Counter / Capture 0 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP0_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP0_L[7:0]	R/W	Timer B Counter / Capture 0 register – low byte	

Table 5-152 TMB_CCP0_L register

TMB_CCP0_H			Page : 2 / Address: 0xAB		Timer B Counter / Capture 0 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP0_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP0_H[7:0]	R/W	Timer B Counter / Capture 0 register – high byte	

Table 5-153 TMB_CCP0_H register

TMB_CCP1_L			Page : 2 / Address: 0xAC		Timer B Counter / Capture 1 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP1_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP1_L[7:0]	R/W	Timer B Counter / Capture 1 register – low byte	

Table 5-154 TMB_CCP1_L register

TMB_CCP1_H			Page : 2 / Address: 0xAD		Timer B Counter / Capture 1 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP1_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP1_H[7:0]	R/W	Timer B Counter / Capture 1 register – high byte	

Table 5-155 TMA_CCP1_H register

TMB_CCP2_L			Page : 2 / Address: 0xAE		Timer B Counter / Capture 2 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP2_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP2_L[7:0]	R/W	Timer B Counter / Capture 2 register – low byte	

Table 5-156 TMB_CCP2_L register

TMB_CCP2_H			Page : 2 / Address: 0xAF		Timer B Counter / Capture 2 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP2_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP2_H[7:0]	R/W	Timer B Counter / Capture 2 register – high byte	

Table 5-157 TMB_CCP2_H register

TMB_CCP3_L			Page : 2 / Address: 0xB2		Timer B Counter / Capture 3 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP3_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP3_L[7:0]	R/W	Timer B Counter / Capture 3 register – low byte	

Table 5-158 TMB_CCP3_L register

TMB_CCP3_H			Page : 2 / Address: 0xB3		Timer B Counter / Capture 3 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_CCP3_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_CCP3_H[7:0]	R/W	Timer B Counter / Capture 3 register – high byte	

Table 5-159 TMB_CCP3_H register

5.8.6. Timer C

The Timer C, which is a 16-bit-wide register, can operate as timer. The additional Counter/Capture feature is one of the most powerful peripheral units of the core. It can be used for all kinds of event capturing.

5.8.6.1. Timer / Counter mode

In timer / counter function, it has up to 7 clock source options. Thus, the 16-bit timer register is decremented in every clock period. The figure 5-32 shows the block diagram of counter / timer function for Timer C. When Timer C rolls over from pre-load data (TMC_PLOAD_H/L) to 0, not only TMC_INTF is set but also Timer C registers is loaded with the 16-bit value from TMC_PLOAD_H/L register. Required TMC_PLOAD_H/L value can be preset by software.

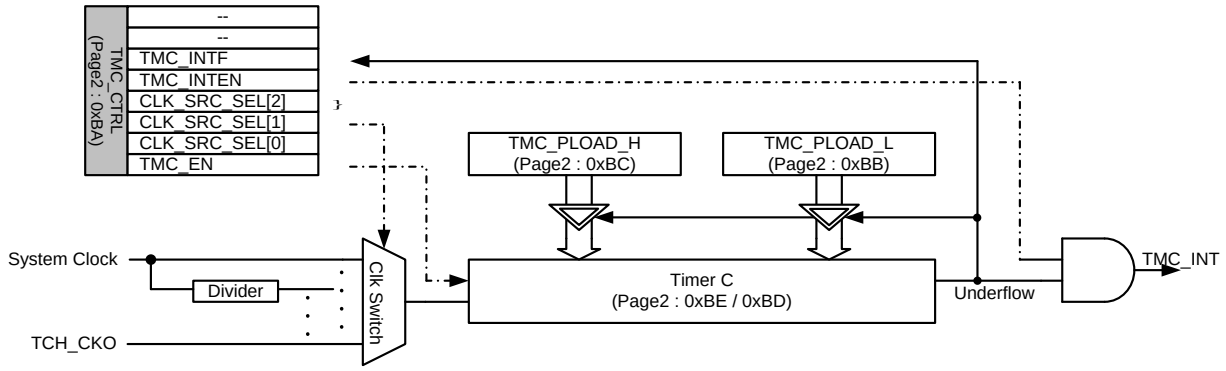


Figure 5-32 The block diagram of counter / timer function for Timer C

5.8.6.2. Capture functions

Each of capture registers can be used to latch the current 16-bit value of the Timer C registers (TMC_H and TMC_L) when an external event is triggered.

Figure 5-33 shows functional diagrams of the Timer C capture function.

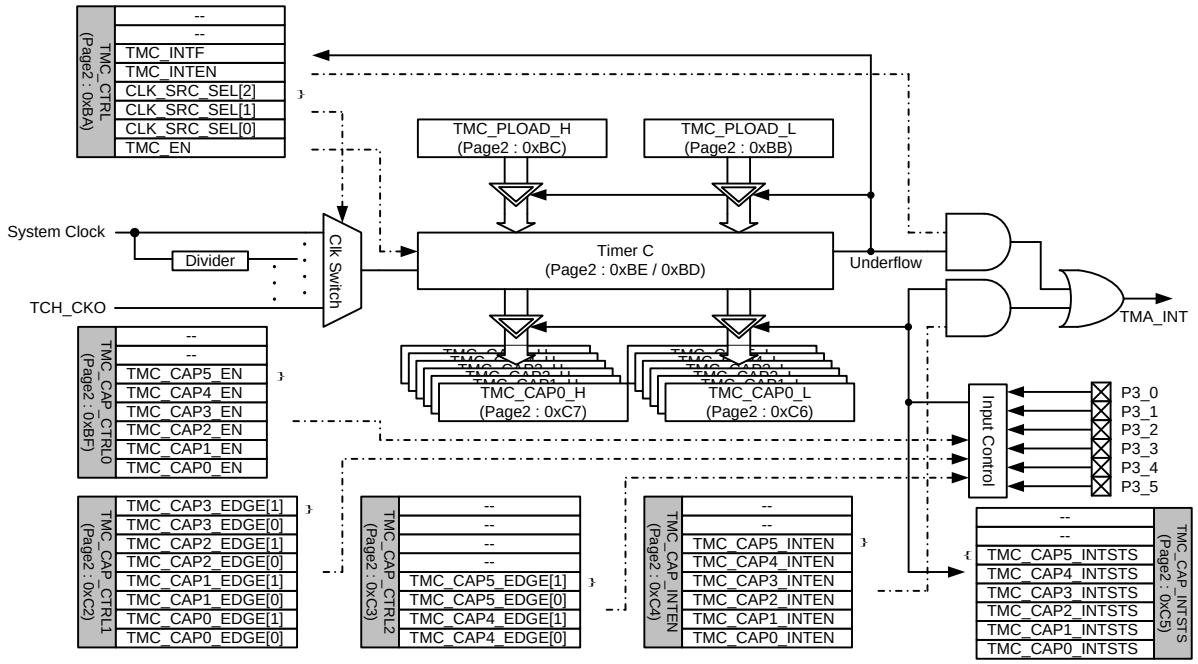


Figure 5-33 The block diagram of Timer A capture mode

5.8.6.3. Timer C Related Registers

TMC_CTRL			Page : 2 / Address: 0xBA		Timer C Control1 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_INTF	TMC_INTEN	CLK_SRC_SEL[2:0]			TMC_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R	Reserved	
5	TMC_INTF	R/W	Timer C interrupt flag. read : 0 : idle / busy 1 : timer C interrupt trigger write : 0 : clears this bit 1 : no effect	
4	TMC_INTEN	R/W	Timer C interrupt enable control bit 0 : disabled 1 : enabled	
3:1	CLK_SRC_SEL	R/W	Timer C input clock source selection control bit CLK_SRC_SEL[2:0] / Clock Source 000 / System clock 001 / System clock / 2 010 / System clock / 4 011 / System clock / 128 100 / System clock / 256 101 / System clock / 512 110 / System clock / 1024 111 / TCH_CKO	
0	TMC_EN	R/W	Timer C enable control bit. 0 : disabled 1 : enabled	

Table 5-160 TMC_CTRL register

TMC_PLOAD_L			Page : 2 / Address: 0xBB		Timer C Pre-Load Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_PLOAD_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_PLOAD_L[7:0]	R/W	Timer C pre-load data register – low byte	

Table 5-161 TMC_PLOAD_L register

TMC_PLOAD_H			Page : 2 / Address: 0xBC		Timer C Pre-Load Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_PLOAD_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_PLOAD_H[7:0]	R/W	Timer C pre-load data register – high byte	

Table 5-162 TMC_PLOAD_H register

TMC_L			Page : 2 / Address: 0xBD		Timer C Counter Register - Low Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_L[7:0]	R/W	Timer C counter register – low byte	

Table 5-163 TMC_L register

TMC_H			Page : 2 / Address: 0xBE		Timer B Counter Register - High Byte			
Bit	7	6	5	4	3	2	1	0
Function	TMB_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMB_H[7:0]	R/W	Timer B counter register – high byte	

Table 5-164 TMB_H register

TMC_CAP_CTRL0			Page : 2 / Address: 0xBF		Timer C Capture Control 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_CAPx_EN[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMC_CAPx_EN[5:0]	R/W	Timer C capture mode enable control bit. All of the trigger source are from external I/O. Following table is the trigger source mapping table. TMC_CAPx_EN / Mapping I/O TMC_CAP0_EN / P3[0] TMC_CAP1_EN / P3[1] TMC_CAP2_EN / P3[2] TMC_CAP3_EN / P3[3] TMC_CAP4_EN / P3[4] TMC_CAP5_EN / P3[5] 0: disabled 1: enabled	

Table 5-165 TMC_CAP_CTRL0 register

TMC_CAP_CTRL1			Page : 2 / Address: 0xC2		Timer C Capture Control 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP3_EDGE[1:0]		TMC_CAP2_EDGE[1:0]		TMC_CAP1_EDGE[1:0]		TMC_CAP0_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	TMC_CAP3_EDGE[7:6]	R/W	Timer C capture 3 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edges	
5:4	TMC_CAP2_EDGE[5:4]	R/W	Timer C capture 2 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edges	
3:2	TMC_CAP1_EDGE[3:2]	R/W	Timer C capture 1 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edges	
1:0	TMC_CAP0_EDGE[1:0]	R/W	Timer C capture 0 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edges	

Table 5-166 TMC_CAP_CTRL1 register

TMC_CAP_CTRL2			Page : 2 / Address: 0xC3		Timer C Capture Control 2 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	TMC_CAP5_EDGE[1:0]		TMC_CAP4_EDGE[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:2	TMC_CAP5_EDGE[3:2]	R/W	Timer C capture 5 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edges	
1:0	TMC_CAP4_EDGE[1:0]	R/W	Timer C capture 4 sample edge selection bit 00 : falling edge 01 : rising edge 1x : both edges	

Table 5-167 TMC_CAP_CTRL2 register

TMC_CAP_INTEN			Page : 2 / Address: 0xC4		Timer C Capture Mode Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_CAPx_INTEN[7:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMC_CAPx_INTEN[5:0]	R/W	Timer C capture mode interrupt enable control bits. These are mapping to CAP0 ~ CAP5 respectively. 0 : disabled 1 : enabled	

Table 5-168 TMC_CAP_INTEN register

TMC_CAP_INTSTS			Page : 2 / Address: 0xC5		Timer C Capture Mode Interrupt Status Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	TMC_CAPx_INTSTS[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	TMC_CAPx_INTSTS[5:0]	R/W	Timer C capture mode interrupt status register. These are mapping to CAP0 ~ CAP5 respectively. read : 0 : no capture triggered 1 : capture triggered write : 0 : clears this bit 1 : no effect	

Table 5-169 TMC_CAP_INTSTS register

TMC_CAP0_L			Page : 2 / Address: 0xC6		Timer C Capture 0 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP0_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP0_L[7:0]	R/W	Timer C Capture 0 register – low byte	

Table 5-170 TMC_CAP0_L register

TMC_CAP0_H			Page : 2 / Address: 0xC7		Timer C Capture 0 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP0_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP0_H[7:0]	R/W	Timer C Capture 0 register – high byte	

Table 5-171 TMC_CAP0_H register

TMC_CAP1_L			Page : 2 / Address: 0xCA		Timer C Capture 1 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP1_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP1_L[7:0]	R/W	Timer C Capture 1 register – low byte	

Table 5-172 TMC_CAP1_L register

TMC_CAP1_H			Page : 2 / Address: 0xCB		Timer C Capture 1 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP1_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP1_H[7:0]	R/W	Timer C Capture 1 register – high byte	

Table 5-173 TMC_CAP1_H register

TMC_CAP2_L			Page : 2 / Address: 0xCC		Timer C Capture 2 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP2_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP2_L[7:0]	R/W	Timer C Capture 2 register – low byte	

Table 5-174 TMC_CAP2_L register

TMC_CAP2_H			Page : 2 / Address: 0xCD		Timer C Capture 2 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP2_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP2_H[7:0]	R/W	Timer C Capture 2 register – high byte	

Table 5-175 TMC_CAP2_H register

TMC_CAP3_L			Page : 2 / Address: 0xCE		Timer C Capture 3 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP3_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP3_L[7:0]	R/W	Timer C Capture 3 register – low byte	

Table 5-176 TMC_CAP3_L register

TMC_CAP3_H			Page : 2 / Address: 0xCF		Timer C Capture 3 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP3_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP3_H[7:0]	R/W	Timer C Capture 3 register – high byte	

Table 5-177 TMC_CAP3_H register

TMC_CAP4_L			Page : 2 / Address: 0xD1		Timer C Capture 4 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP4_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAPC4_L[7:0]	R/W	Timer C Capture 4 register – low byte	

Table 5-178 TMC_CAP4_L register

TMC_CAP4_H			Page : 2 / Address: 0xD2		Timer C Capture 4 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP4_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP4_H[7:0]	R/W	Timer C Capture 4 register – high byte	

Table 5-179 TMC_CAP4_H register

TMC_CAP5_L			Page : 2 / Address: 0xD3		Timer C Capture 5 Register – low byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP5_L[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP5_L[7:0]	R/W	Timer C Capture 5 register – low byte	

Table 5-180 TMC_CAP5_L register

TMC_CAP5_H			Page : 2 / Address: 0xD4		Timer C Capture 5 Register – high byte			
Bit	7	6	5	4	3	2	1	0
Function	TMC_CAP5_H[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TMC_CAP5_H[7:0]	R/W	Timer C Capture 5 register – high byte	

Table 5-181 TMC_CAP5_H register

5.9. UART0

UART0 has the same functionality as a standard 8051 UART. The serial port is full duplex, meaning it can transmit and receive concurrently. It is reception with double-buffer, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. Figure 5-34 shows the block diagram of UART module. The serial port can operate in 4 modes: one synchronous and three asynchronous modes. Mode 2 and 3 has a special feature for multiprocessor communications. This feature is enabled by setting SM02 bit in SCON0 register. The master processor first sends out an address byte, which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM02 = 1, no slave will be interrupted by a data byte. An address byte will interrupt all slaves. The addressed slave will clear its SM02 bit and prepare to receive the data bytes that will be coming. The slaves that are not being addressed leave their SM02 set and ignoring the incoming data.

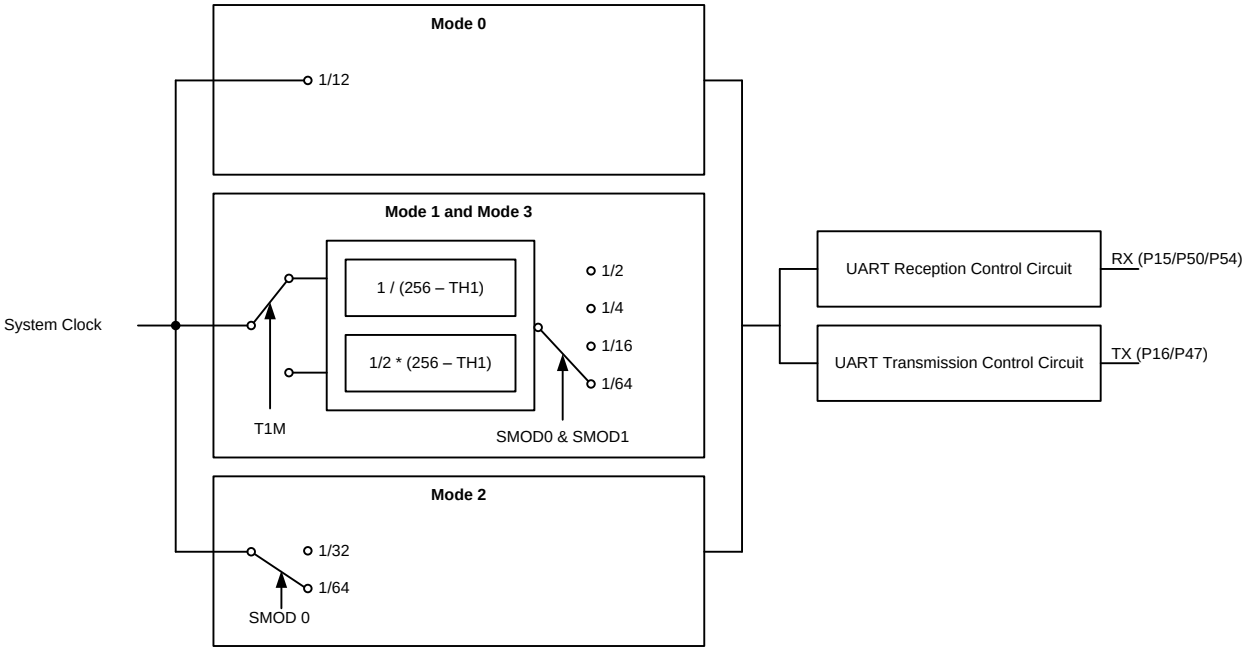


Figure 5-34 The block diagram of UART module

5.9.1. UART0: Mode 0(Synchronous Shift register)

This mode is used as shift register IO control, and not for real communication application. The baud rate is fixed at 1/12 of the system clock frequency and TX output is a shift clock. Eight bits are transmitted with LSB first. Reception is initialized by setting the flags in SCON0 as follows: RI0 =0 and REN0 =1. Figure 5-35 shows the timing diagram of UART0 transmission mode 0.

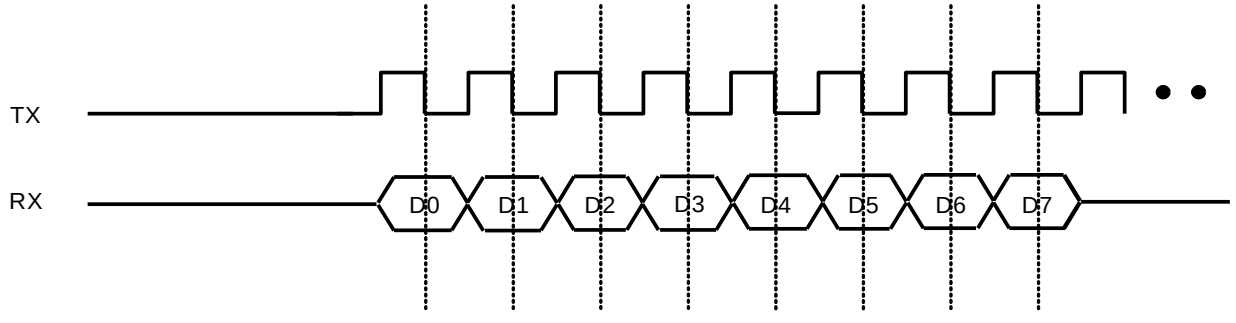


Figure 5-35 The timing diagram of UART0 transmission mode 0

5.9.2. UART0: Mode 1(8-Bit UART, Variable Baud Rate, Timer1 Clock Source)

In mode 1, TX serves as serial output. Total of 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receiving, a start bit synchronizes the reception, 8 data bits are available by reading SBUF0 and stop bit sets the flag RB08 in the SFR SCON0. The baud rate is variable and depends from Timer 1 mode. The SMOD0 and SMOD1 bits of PCON (0x87) are used to set the baud rate as $T1_{ov}/2$ or $T1_{ov}/4$ or $T1_{ov}/16$ or $T1_{ov}/64$. Figure 5-36 shows the format of UART0 transmission mode 1.



Figure 5-36 The format of UART0 transmission mode 1

5.9.3. UART0: Mode 2(9-Bit UART, Fixed Baud Rate)

This mode is similar to Mode 1 with two differences. The baud rate is fixed at 1/32 or 1/64 of system clock frequency, and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the UART0 interface: at transmission, bit TB08 in SCON0 is output as the 9th bit, and at receive, the 9th bit affects RB08 in SCON0. Figure 5-37 shows the format of UART0 transmission mode 2.

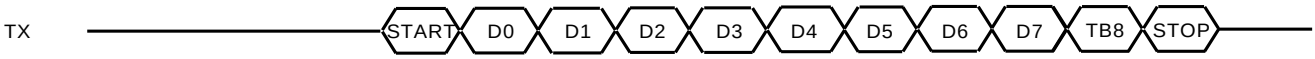


Figure 5-37 The format of UART0 transmission mode 2

5.9.4. UART0: Mode 3(9-Bit UART, Variable Baud Rate, Timer1 Clock Source)

The only difference between Mode 2 and Mode 3 is that the baud rate is a variable in Mode 3. When REN0 =1 data receiving is enabled. The baud rate is variable and depends from Timer 1 mode. The SMOD0 and SMOD1 bits of PCON (0x87) are used to set the baud rate as $T1_{ov}/2$ or $T1_{ov}/4$ or $T1_{ov}/16$ or $T1_{ov}/64$. Figure 5-38 shows the format of UART0 transmission mode 1.

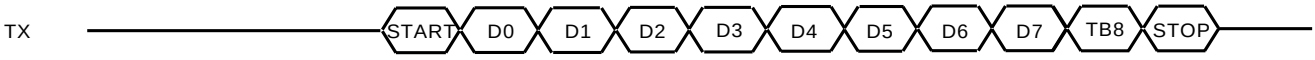


Figure 5-38 The format of UART0 transmission mode 3

5.9.5. UART0 Related Registers

The UART0 related registers are: SBUF0(0x99), SCON0(0x98), PCON(0x87), IE(0xA8) and IP(0xB8). The UART0 data buffer (SBUF0) consists of two separate registers: transmit and receive registers. A data written into SBUF0 sets this data in UART0 output register and starts a transmission. A data read from SBUF0, reads data from the UART0 receive register.

SBUF0			**Address: 0x99**		**UART0 Buffer Register**			
Bit	7	6	5	4	3	2	1	0
Function	SBUF0[7:0]							
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	**Function**	**Type**	**Description**	**Condition**
2:0	SBUF0[7:0]	R/W	UART 0 buffer	

Table 5-182 SBUF0 register

SCON0			**Address: 0x98**		**UART0 Configuration Register**			
Bit	7	6	5	4	3	2	1	0
Function	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
7:6	SM0[1:0]	R/W	Mode and baud rate setting which described as below table	
5	SM02	R/W	Enables a multiprocessor communication feature	
4	REN0	R/W	Enables serial reception.	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0 this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-183 SCON0 register

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	--	PWE	--	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 baud rate bit when clocked by Timer1	
5	--	R/W	Reserved	
4	PWE	R/W	Program Write Enable (PWE) 0: Disables Flash write activity during MOVX instruction 1: Enables Flash write activity during MOVX instruction	
3:2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-184 PCON register

SYS_CTRL6			Address : 0xFF		System Control-6 Register			
Bit	7	6	5	4	3	2	1	0
Function	UART_IF_SEL		UART_IF_EN	T01_CK_SEL	--	AERR_RSTEN	WDOG_CKEN	RTC_CKEN
Default	1	1	0	0	0	0	0	0
Key Code	0x8F, 0x32 , 0x50							

Bit	Function	Type	Description	Condition
7:6	UART_IF_SEL[1:0]	R/W	UART IO interface select signal UART_IF_SEL[1 :0] / UART_TX / UART_RX 0X / P1[6] / P1[5] 10 / P4[7] / P5[0] 11 / P4[7] / P5[4]	
5	UART_IF_EN	R/W	UART interface enable signal. 0 : disabled	

Bit	Function	Type	Description	Condition
			1 : enabled	
4	T01_CK_SEL	R/W	Timer0/1 clock source select signal.This bit is used combining with T0M/T1M of CKCON(0x8E). T0M /T1M | T01_CK_SEL | Timer0/1 Clock 0 | 0 | System Clock / 8 0 | 1 | System Clock / 2 1 | 0 | System Clock / 4 1 | 1 | System Clock / 1	
3	--	R/W	Reserved	
2	AERR_RSTEN	R/W	Flash address over range reset enable 0 : disabled 1 : enabled	
1	WDOG_CKEN	R/W	Watchdog controller clock enable control bit 0 : disabled 1 : enabled	
0	RTC_CKEN	R/W	RTC controller clock enable signal. 0 : disabled 1 : enabled	

Table 5-185 The SYS_CTRL6 register

CKCON			Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits If WDFM=0: WD[1:0] | Timeout 00 | 128ms 01 | 256ms 10 | 512ms 11 | 1024ms If WDFM=1: WD[1:0] | Timeout 00 | 8ms 01 | 16ms 10 | 32ms 11 | 64ms	
5	WDFM	R/W	Watchdog fast mode selection bit 0: watchdog fast mode is disabled 1: watchdog fast mode is enabled	

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>4</td><td>T1M</td><td>R/W</td><td>Timer 1 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF).
<table>
<tr><th>T1M</th><th>T01_CK_SEL</th><th>Timer1 Clock</th></tr>
<tr><td>0</td><td>0</td><td>System Clock / 8</td></tr>
<tr><td>0</td><td>1</td><td>System Clock / 2</td></tr>
<tr><td>1</td><td>0</td><td>System Clock / 4</td></tr>
<tr><td>1</td><td>1</td><td>System Clock / 1</td></tr>
</table></td><td></td></tr>
<tr><td>3</td><td>T0M</td><td>R/W</td><td>Timer 0 clock source select signal.This bit is used combining with T01_CK_SEL of SYS_CTRL6(0xFF).
<table>
<tr><th>T0M</th><th>T01_CK_SEL</th><th>Timer0 Clock</th></tr>
<tr><td>0</td><td>0</td><td>System Clock / 8</td></tr>
<tr><td>0</td><td>1</td><td>System Clock / 2</td></tr>
<tr><td>1</td><td>0</td><td>System Clock / 4</td></tr>
<tr><td>1</td><td>1</td><td>System Clock / 1</td></tr>
</table></td><td></td></tr>
<tr><td>2:0</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
</table>

Table 5-186 CKCON register

SM00	SM01	Mode	Function	Baud rate
0	0	0	Shift register	SYSCLK/12
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	SYSCLK/32(SMOD0=0) SYSCLK/64(SMOD0=1)
1	1	3	9-bit UART	variable

❑ variable: in Mode1 and Mode 3(T1M=0)

SMOD1	SMOD0	Baud rate
0	0	T1ov/64(T1ov=SYSCLK/(256-TH1))
0	1	T1ov/16(T1ov=SYSCLK/(256-TH1))
1	0	T1ov/4(T1ov=SYSCLK/(256-TH1))
1	1	T1ov/2(T1ov=SYSCLK/(256-TH1))

❑ Baud rate setting example (SYSCLK = 48MHz, T1M =1, T01_CK_SEL=1)

Bit rate	Baud rate	Timer reload setting (TH1)	Actual rate	Error deviation (%)
4800	T1ov/64	0x64(100)	4807.69	0.16%
9600	T1ov/64	0xB2(178)	9615.38	0.16%
19200	T1ov/16	0x64(100)	19230.77	0.16%
38400	T1ov/16	0xB2(178)	38461.54	0.16%
57600	T1ov/4	0x30(48)	57692.31	0.016%
115200	T1ov/2	0x30(48)	115384.62	0.16%

❑ Baud rate setting example (SYSCLK = 8MHz, T1M=1, T01_CK_SEL=1)

Bit rate	Baud rate	Timer reload setting (TH1)	Actual rate	Error deviation (%)
4800	T1ov/16	0x98(152)	4807.69	0.16%
9600	T1ov/4	0x30(48)	9615.38	0.16%

Bit rate	Baud rate	Timer reload setting (TH1)	Actual rate	Error deviation (%)
19200	T1ov/2	0x30(48)	19230.77	0.16%
38400	T1ov/2	0x98(152)	38461.54	0.16%
57600	T1ov/2	0xBB(187)	57971.01	0.64%
115200	T1ov/2	0xDD(221)	114285.71	-0.79%

IE			Address: 0xA8		Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EA	ETC	ETB	ES0	ET1	EADC	ET0	ETA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EA	R/W	Enable global interrupts	
6	ETC	R/W	Enable Timer C interrupt	
5	ETB	R/W	Enable Timer B interrupt	
4	ES0	R/W	Enable UART0 interrupt	
3	ET1	R/W	Enable Timer 1 interrupt	
2	EADC	R/W	Enable ADC0 interrupt	
1	ET0	R/W	Enable Timer 0 interrupt	
0	ETA	R/W	Enable Timer A interrupt	

Table 5-187 IE register

IP			Address: 0xB8		Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	PTC	PTB	PS0	PT1	PADC	PT0	PTA
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	PTC	R/W	Timer C interrupt priority level control (1: high level)	
5	PTB	R/W	Timer B interrupt priority level control (1: high level)	
4	PS0	R/W	UART0 interrupt priority level control (1: high level)	
3	PT1	R/W	Timer 1 interrupt priority level control (1: high level)	
2	PADC	R/W	ADC0 interrupt priority level control (1: high level)	
1	PT0	R/W	Timer 0 interrupt priority level control (1: high level)	
0	PTA	R/W	Timer A interrupt priority level control (1: high level)	

Table 5-188 IP register

5.10. SPI

A Serial Peripheral Interface (SPI) controller is built in GPM8F3732B to facilitate communicating with other devices and components. The SPI controller includes four master modes and one slaver mode. There are four control signals on SPI including SPI_CSB, SPI_CLK, SPI_TX, and SPI_RX, these four signals are shared with P4[7:4]. While SPI module is enabled by corresponding control bit, these four pins cannot be GPIOs. In other words, any setting on corresponding GPIO control register will have no effect. The SPI provides following features.

- ❑ Programmable phase and polarity of master clock
- ❑ Programmable master SPI_CLK clock frequency

In master mode, the shifting clock (SPI_CLK) is generated by SPI block. There are two control bits to control the clock phase and polarity. The transmission starts immediately after SPI_START is

set(SPI_CTRL[0]=1, Page0 / 0x9A). The SPI shifts the 8-bit data from MSB to LSB through the SPI_TX pin during 8 SPI_CLK cycles. Programmer can read SPI data from SPI_RXD control register. The following four diagrams depict the timing scheme on SPI master mode for different operation types (polarity control bit equals “1” or “0”, phase control bit equals “1” or “0”). The related registers are SPI_CTRL register, SPI_STS register, SPI_TXD register and SPI_RXD registers which are tabled as Table 5-189 to Table 5-192. Figure 5-39 is the block diagram of SPI controller.

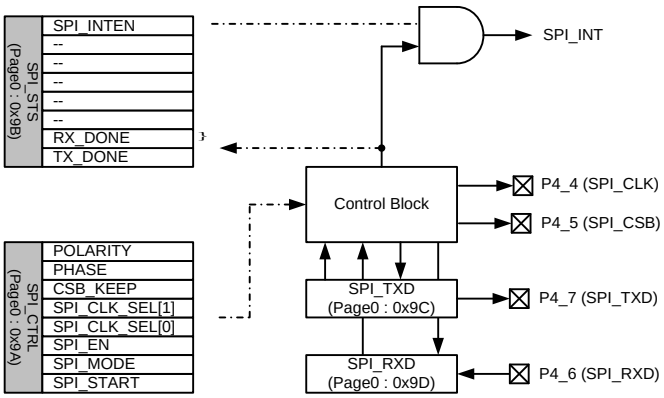


Figure 5-39 The block diagram of SPI controller

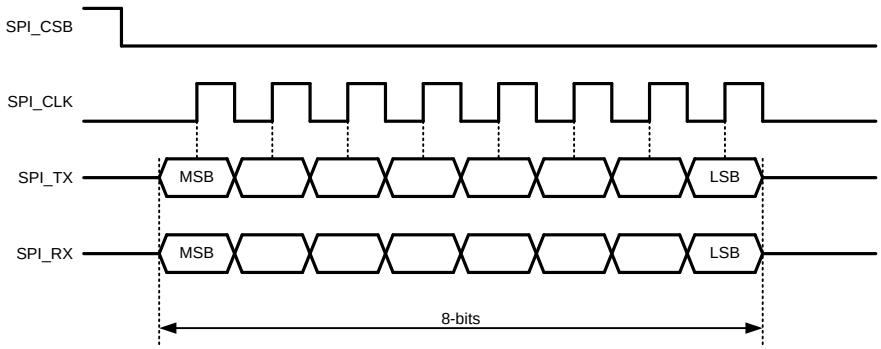


Figure 5-40 Master / Slaver Mode, POLARITY=0, PHASE=0

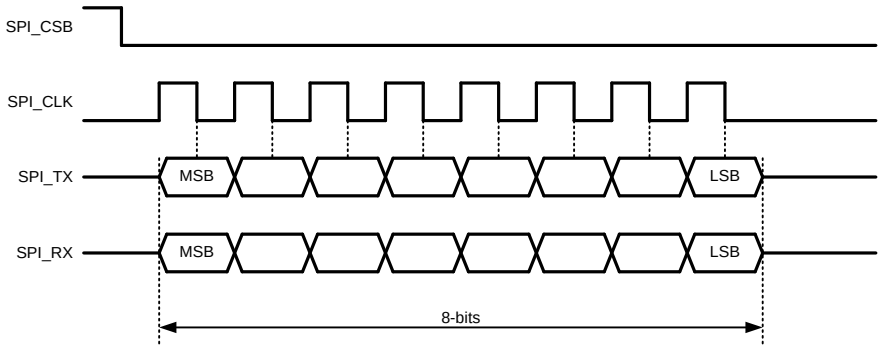


Figure 5-41 Master Mode, POLARITY=0, PHASE=1

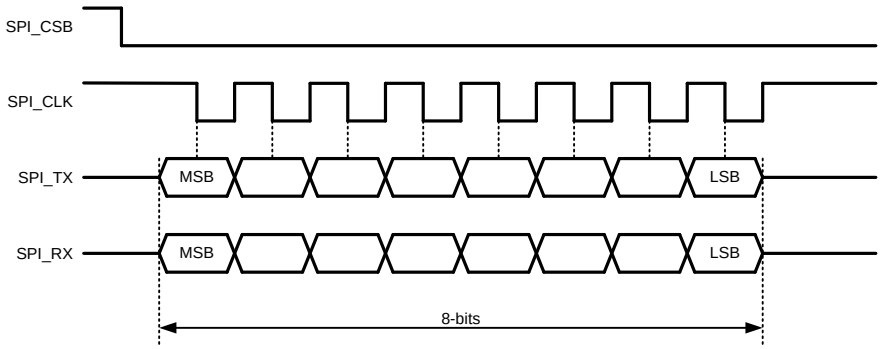


Figure 5-42 Master Mode, POLARITY=1, PHASE=0

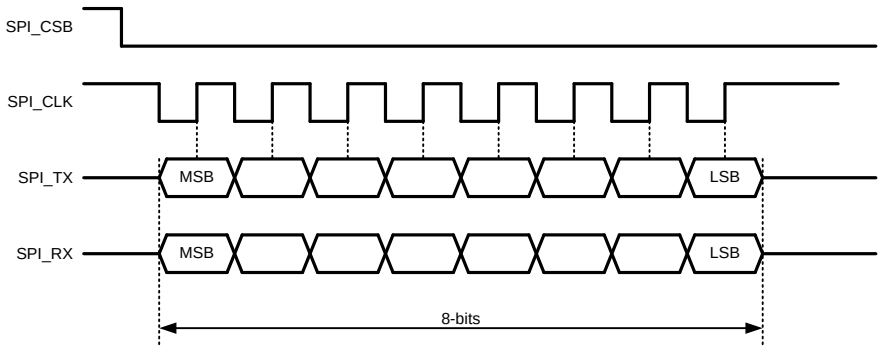


Figure 5-43 Master Mode, POLARITY=1, PHASE=1

SPI_CTRL			**Page : 0 / Address: 0x9A**		**SPI Control Register**			
Bit	7	6	5	4	3	2	1	0
Function	POLARITY	PHASE	CSB_KEEP	SPI_CLK_SEL[1:0]		SPI_EN	SPI_MODE	SPI_START
Default	0	0	0	0	0	0	0	0
Key Code	FF,00							

Bit	Function	Type	Description	Condition
7	POLARITY	R/W	SPI CLK initial state 0: low state 1: high state	
6	PHASE	R/W	SPI CLK type control 0: 1st edge sample 1: 2nd edge sample	
5	CSB_KEEP	R/W	SPI CSB keep low control	
4:3	SPI_CLK_SEL[1:0]	R/W	SPI Clock output selection: 00: system clock / 2 01: system clock / 4 10: system clock / 8 11: system clock / 16	
2	SPI_EN	R/W	SPI signals forward to P4[7:4] enable P4[4] : SPI_CLK P4[5] : SPI_CSB P4[6] : SPI_RX P4[7] : SPI_TX	
1	SPI_MODE	R/W	SPI operation mode.	

Bit	Function	Type	Description	Condition
			0: Master 1:Slaver	
0	SPI_START	R/W	SPI enable(W)/SPI busy flag(R)	

Table 5-189 SYSCON1 register

SPI_STS			Page : 0 / Address: 0x9B		SPI Status Register			
Bit	7	6	5	4	3	2	1	0
Function	SPI_INTEN	--	--	--	--	--	RX_DONE	TX_DONE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SPI_INTEN	R/W	SPI interrupt enable 0: disabled 1: enabled	
6:2	-	R/W	Reserved	
1	RX_DONE	R/W	SPI finished data receiving with slaver mode. read: 0: Idle / Busy 1:Done write: 0: clears this bit 1: no effect	
0	TX_DONE	R/W	SPI finished data transmission with master mode. 0: Idle / Busy 1:Done write: 0: clears this bit 1: no effect	

Table 5-190 SPI_STS register

SPI_TXD			Page : 0 / Address: 0x9C		SPI Transmission Data Register			
Bit	7	6	5	4	3	2	1	0
Function	SPI_TXD[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	SPI_TXD[7:0]	R/W	SPI transmission data	

Table 5-191 SPI_TXD register

SPI_RXD			Page : 0 / Address: 0x9D		SPI Receive Data Register			
Bit	7	6	5	4	3	2	1	0
Function	SPI_RXD[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	SPI_RXD	R/W	SPI receive data	

Table 5-192 SPI_RXD register

5.11. ADC

There is one Analog-to-Digital-Converter (ADC) embedded in GPM8F3732B. It provides general purpose usages such as any other analog functions.

- ❑ 7 Channels, 12-bit resolution (11-bit no-missing code) ADC
- ❑ Supports programming sample hold and ADC clock function

5.11.1. ADC Control

Seven channels of 12-bit SAR ADC are built in GPM8F3732B. They are defined as general-purpose line input P01 … P07. These eight channels are very suitable for system voltage detection and other general-purpose usages. Figure 5-44 and Figure 5-45 shows the related timing and block diagrams.

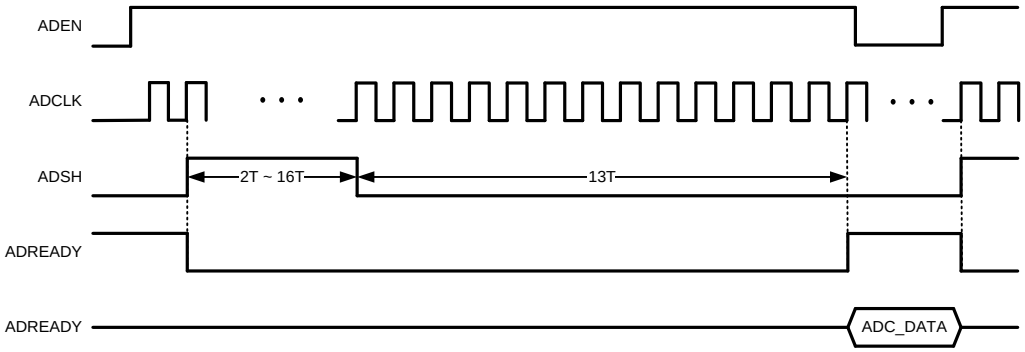


Figure 5-44 The timing diagram of ADC control

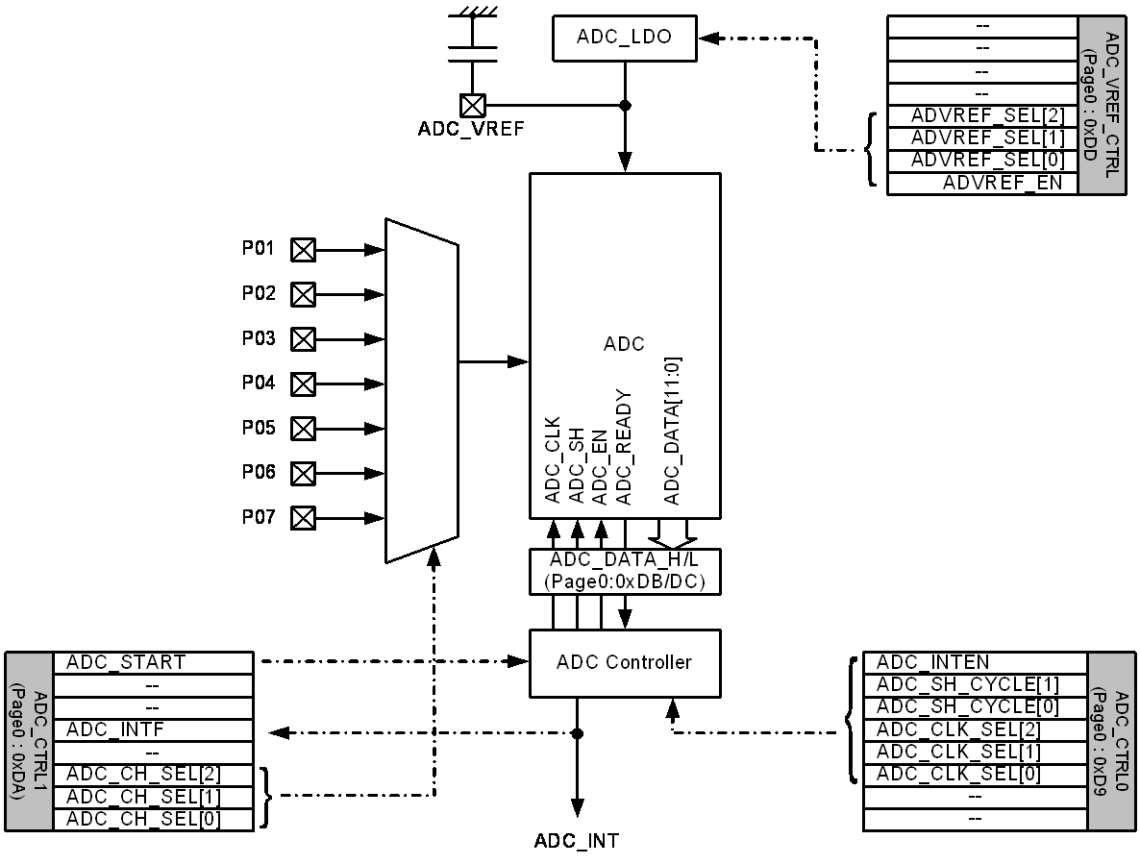


Figure 5-45 The block diagram of ADC

ADC Related Register

ADC0_CTRL0			**Page : 0 / Address: 0xD9**		**ADC0 Control 0 Register**			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_INTEN	ADC0_SH_CYCLE[1:0]		ADC0_CLK_SEL[2:0]			--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC0_INT_EN	R/W	ADC0 interrupt enable control bit. 0: disabled 1: enabled	
6:5	ADC0_SH_CYCLE	R/W	ADC0 sample and hold cycle selection control bit. ADC0_SH_CYCLE: Cycle (ADC0_CLK) 00: 2 01: 4 10: 8 11: 16	
4:2	ADC0_CLK_SEL	R/W	ADC0 clock selection control bit ADC0_CLK_SEL: ADC0_CLK 000: System clock / 2 001: System clock / 4 010: System clock / 8 011: System clock / 12 100: System clock / 16 101: System clock / 20 110: System clock / 24 111: System clock / 28	
1:0	--	R/W	Reserved	

Table 5-193 ADC0_CTRL0 register

ADC0_CTRL1			**Page : 0 / Address: 0xDA**		**ADC0 Control 1 Register**			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_START	--	--	ADC0_INTF	--	ADC0_CH_SEL[2:0]		
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ADC0_START	R/W	ADC0 start transfer control bit 0: idle 1: starts transfer	
6:5	-	R/W	Reserved	
4	ADC0_INTF	R/W	ADC0 interrupt flag. read : 0 : idle / converting 1 : conversion ready write : 0 : clears this bit 1 : no effect	
3	--	R/W	Reserved	

Bit	Function	Type	Description	Condition
2:0	ADC0_CH_SEL	R/W	ADC0 channel selection control bit ADC0_CH_SEL: ADC0_Channel 001: ADC0_CH1 (P0[1]) 010: ADC0_CH2 (P0[2]) 011: ADC0_CH3 (P0[3]) 100: ADC0_CH4 (P0[4]) 101: ADC0_CH5 (P0[5]) 110: ADC0_CH6 (P0[6]) 111: ADC0_CH7 (P0[7])	

Table 5-194 ADC0_CTRL1 register

ADC0_DATA_L			Page : 0 / Address: 0xDB		ADC0 Data Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_DATA[3:0]				--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	ADC0_DATA[3:0]	R	ADC0 output data[3:0]	
3:0	-	R/W	Reserved	

Table 5-195 ADC0_DATA_L register

ADC0_DATA_H			Page : 0 / Address: 0xDC		ADC0 Data Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	ADC0_DATA[11:4]							
Default	0	0	0	0				

Bit	Function	Type	Description	Condition
7:0	ADC0_DATA[11:4]	R	ADC0 output data[11:4]	

Table 5-196 ADC0_DATA_H register

ADC_VREF_CTRL			Page : 0 / Address: 0xDD		ADC Reference Voltage Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	ADCVREF_SEL[2:0]			ADC_VREF_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	-	R/W	Reserved	
3:1	ADCVREF_SEL[2:0]	R/W	ADC reference voltage selection control bit ADC_VREF_SEL: Voltage 000: 1.8V 001: 2.0V 010: 2.4V 011: 2.2V 100: 3.0V 101: 3.2V	

Bit	Function	Type	Description	Condition
			110 3.4V 111 VDD	
0	ADC_VREF_EN	R/W	ADC reference voltage regulator enable 0 : disabled 1 : enabled	

Table 5-197 ADC_VREF_CTRL register

5.12. I2C Unit

An I2C Interface (I2C) is equipped in GPM8F3732B. Only two wires (SCK and SDA) are needed to implement the protocol. To avoid all possibilities of confusion, data loss and blockage of information, the master and slave devices must have a defined protocol. The master that initiates a data transfer over the I2C-bus is responsible for terminating the transfer.

5.12.1. I2C Bus Protocol

A Start condition can transfer a one-byte serial data over the SDA line, and a stop condition can terminate the data transfer. A "Start" condition is a high-to-low transition of SDA line while SCK is high. A "Stop" condition is a Low-to-High transition of the SDA line while SCK is high. Start and Stop conditions are always generated by the master. The I2C-bus is busy when a Start condition is generated. A few clocks after a Stop condition, the I2C-bus will be free, again. Figure 5-46 shows Start and Stop conditions.

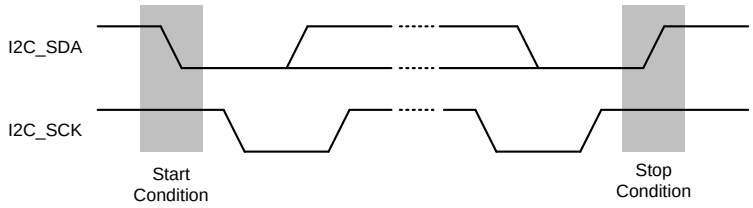


Figure 5-46 Start and Stop conditions

When a master initiates a Start condition, it should send a slave address to notify the slave device. The one byte of address field consists of a 7-bit address and a 1-bit transfer direction indicator (that is, writes or read). If bit 8 is 0, it indicates a write operation (transmit operation); if bit 8 is 1, it indicates a request for data read (receive operation). Every byte placed on the SDA line should be eight bits in length. The number of bytes which can be transmitted per transfer is unlimited. The first byte following a Start condition should have the address field. The address field can be transmitted by the master when the I2C-bus is operating in master mode. Each byte should be followed by an acknowledgement (ACK) bit. The MSB bit of the serial data and addresses are always sent first. To finish a one-byte transfer operation completely, the receiver should send an ACK bit to the transmitter. The ACK pulse should occur at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The master should generate the clock pulse required to transmit the ACK bit. Figure 5-47 and Figure 5-48 shows the format of I2C master mode with data transmission.

In the master mode, after the data is transferred, the I2C-bus interface will issue an interrupt if interrupt is enabled. After the CPU receives the interrupt request, it should write a new data into I2C_DATA register before clear the interrupt. In the receive mode, after a data is received, the I2C controller will issue an interrupt if interrupt is enabled. After the CPU receives the interrupt request, it should read the data from I2C_DATA before clear the interrupt.

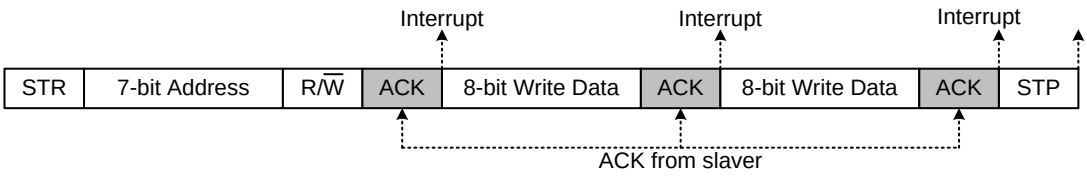


Figure 5-47 I2C master mode with data write

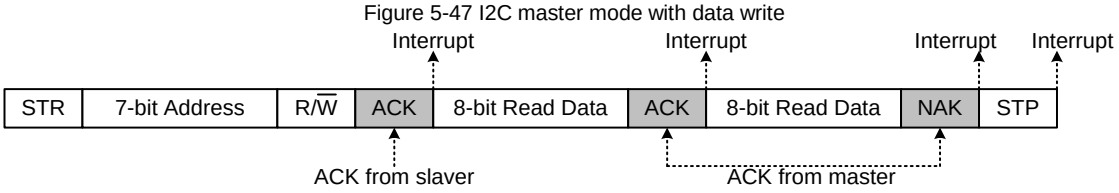


Figure 5-48 I2C master mode with data read

Figure 5-49 and Figure 5-50 shows the format of I2C slaver mode with data transmission.

In the slaver mode, after the data is recovered (which consist of address transfer), the I2C-bus interface will issue an interrupt if interrupt is enabled. After the CPU receives the interrupt request, it should read the data from I2C_DATA before clear the interrupt. During slaver mode data reading, after the CPU receives the interrupt request, I2C controller should write a new data into I2C_DATA register before clear the interrupt.

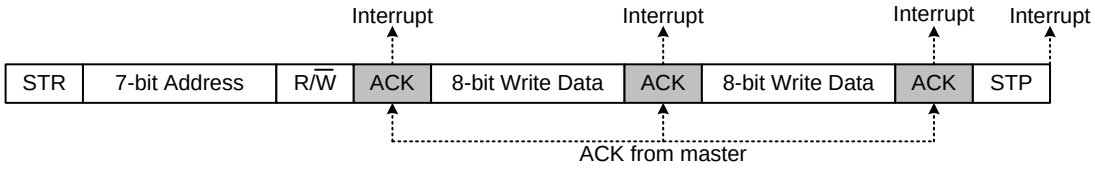


Figure 5-49 I2C slaver mode with data write

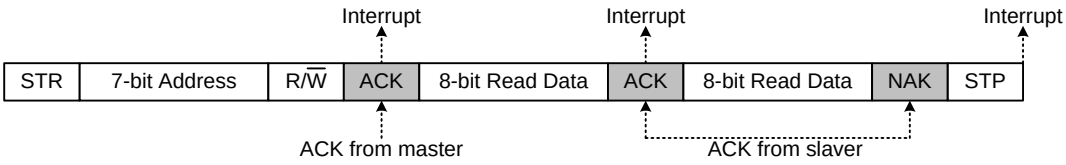


Figure 5-50 I2C slaver mode with data read

I2C Related Register

I2C_DEBOUNCE			Page : 0 / Address: 0xCF		I2C De-bounce Count Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	I2C_DB_CNT[5:0]					
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:0	I2C_DEBOUNCE	R/W	I2C input SCL and SDA de-bounce count.	

Table 5-198 I2C_DEBOUNCE register

I2C_CTRL			Page : 0 / Address: 0xD1		I2C Control Register			
Bit	7	6	5	4	3	2	1	0
Function	MST_STR	MST_STP	MST_NACK	MODE	I2C_CLK_SEL[1:0]		I2C_TRIGGER	I2C_EN
Default	0	0	1	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	MST_STR	R/W	I2C issue start command with divice address enable bit. This bit will be auto cleared by hardware when this transfer is finished.	

Bit	Function	Type	Description	Condition
			0 : disabled 1 : enabled	
6	MST_STP	R/W	I2C issue stop command enable bit. This bit will be auto cleared by hardware when this transfer is finished. 0 : disabled 1 : enabled	
5	MST_NACK	R/W	I2C issue non-acknowledge enable bit. This bit will be auto cleared by hardware when this transfer is finished. 0 : master respond acknowledge 1 : master respond non-acknowledge	
4	MODE	R/W	I2C operating mode selection control bit. 0: master 1: slaver	
3:2	I2C_CLK_SEL[1:0]	R/W	I2C clock selection control bit 00 : I2C clock is system clock / 128 01 : I2C clock is system clock / 256 10 : I2C clock is system clock / 768 11 : I2C clock is system clock / 1024	
1	I2C_TRIGGER	R/W	I2C start transmission trigger bit. This bit is for master mode only. The I2C master will begin to transmit or receive data when I2C_EN is set to 1. After data transmitted this bit will be cleared by H/W automatically. 0 : disabled 1 : enabled	
0	I2C_EN	R/W	I2C enable control bit. 0 : disabled 1 : enabled	

Table 5-199 I2C_CTRL register

I2C_STS			**Page : 0 / Address: 0xD2**		**I2C Status Register**			
Bit	7	6	5	4	3	2	1	0
Function	SLV_DID_OK	SLV_DAT_OK	SLV_STP_OK	ERR_SDID_IE	I2C_IF_SEL	I2C_INT_EN	NO_ACK	TS _DONE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SLV_DID_OK	R/W	This bit indicates device ID has been received by I2C controller. This is for slaver mode only. read: 0 : device ID is not asserted 1 : device ID is asserted write: 0 : clears this bit 1 : no effect	
6	SLV_DAT_OK	R/W	This bit indicates data was received or transmitted by I2C controller. This is for slaver mode only. read:	

Bit	Function	Type	Description	Condition
			0 : data is transmitting or idle now 1 : data is transmission complete write: 0 : clears this bit 1 : no effect	
5	SLV_STP_OK	R/W	This bit indicates stop command has been received by I2C controller. This is for slaver mode only. read: 0 : stop command is not assert 1 : stop command is asserted write: 0 : clears this bit 1 : no effect	
4	ERR_SDID_IE	R/W	Device ID error interrupt enable of slaver mode. 0 : disabled 1 : enabled	
3	I2C_IF_SEL	R/W	I2C interface select signal 0 : P0_6 = SDA / P0_7 = SCL 1 : P5_2 = SDA / P5_3 = SCL	
2	I2C_INT_EN	R/W	I2C interrupt enable control bit. 0 : disabled 1 : enabled	
1	NO_ACK	R/W	I2C not have received acknowledging signal. read : 0 : acknowledge 1 : no acknowledge write : 0 : clears this bit 1 : no effect	
0	TS_DONE	R/W	I2C transmission complete flag. read: 0 : I2C is idle or on going 1 : I2C is finished data transmission write: 0 : clears this bit 1 : no effect	

Table 5-200 I2C_STS register

I2C_DID			Page : 0 / Address: 0xD3		I2C Device ID Register			
Bit	7	6	5	4	3	2	1	0
Function	DEV_ID							R_W
Default	0	0	0	0	0	0	0	1

Bit	Function	Type	Description	Condition
7:1	DEV_ID[6:0]	R/W	I2C device ID register. In master mode, device ID is used to inform which slaver will be connected. In slaver mode, this is	

Bit	Function	Type	Description	Condition
			used to identify the received ID which is sanded from external maser controller.	
0	R_W	R/W	I2C read / write control signal, this register is shared between master and slaver mode.	

Table 5-201 I2C_DID register

I2C_DATA			Page : 0 / Address: 0xD4		I2C Data Register			
Bit	7	6	5	4	3	2	1	0
Function	I2C_DATA[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	I2C_DATA	R/W	I2C read / write Data Register. This register is shared between master and slaver mode.	

Table 5-202 I2C_DATA register

5.13. MDU Unit

The GPM8F3732B has embedded a MDU controller. That supports sign operation with 16 X 16 multiplier and 32/16 divider. In multiplier mode, user store multiplicand and multiplier into internal data memory and write related address in MDU_DSRC_ADDR0 / MDU_DSRC_ADDR1 register. Next, user must write the target address in MDU_DTAR_ADDR in order to index the storage address for saving calculation result. Then, enable the multiplier and get the calculation result after 17 system clock cycle ago. In divider mode, user stores dividend and divisor into internal data memory and write related address in MDU_DSRC_ADDR0 / MDU_DSRC_ADDR1 register. Next, user must write the target address in MDU_DTAR_ADDR in order to index the storage address for saving calculation result. Then, enable the divider and get the calculation result after 33 system clock cycle ago. Figure 5-51 is the block diagram of MDU controller

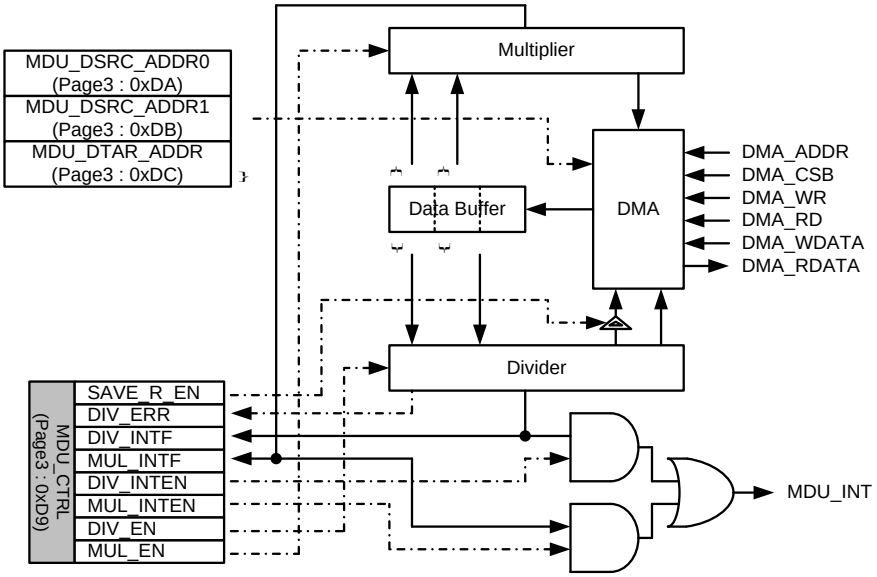


Figure 5-51 The block diagram of MDU controller

MDU Related Register

MDU_CTRL			**Page : 3 / Address: 0xD9**		**Multiplier / Divider Control Register**			
Bit	7	6	5	4	3	2	1	0
Function	SAVE_R_EN	DIV_ERR	DIV_INTF	MUL_INTF	DIV_INTEN	MUL_INTEN	DIV_EN	MUL_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SAVE_R_EN	R/W	Remainder save to internal SRAM enable 0 : disabled 1 : enabled	
6	DIV_ERR	R	Divisor error flag. read : 0: divisor is a suitable value (non-zero). 1: divisor is a unsuitable value (zero). This flag will be cleared automatic when divisor is updated to non-zero value.	
5	DIV_INTF	R/W	Divider interrupts flag. read : 0 : idle / busy 1 : Divider interrupt trigger write : 0 : clears this bit 1 : no effect	
4	MUL_INTF	R/W	Multiplier interrupts flag. read : 0 : idle / busy 1 : Multiplier interrupt trigger write : 0 : clears this bit 1 : no effect	
3	DIV_INTEN	R/W	Divider interrupt enable control bit. 0 : disabled 1 : enabled	
2	MUL_INTEN	R/W	Multiplier interrupt enable control bit. 0 : disabled 1 : enabled	
1	DIV_EN	R/W	Divider enable control bit. 0 : disabled 1 : enabled	
0	MUL_EN	R/W	Multiplier enable control bit. 0 : disabled 1 : enabled	

Table 5-203 MDU_CTRL register

MDU_DSRC_ADR0			**Page : 3 / Address: 0xDA**		**MDU DMA Source Address 0 Register**			
Bit	7	6	5	4	3	2	1	0
Function	MDU_DSRC_ADR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	MDU_DSRC_ADR0	R/W	***Multiplicand*** and ***Dividend*** DMA source address register. These address cover all-off internal data memory only. The arrangement of internal content as below table.	

MDU_DSRC_ADR0	***Multiplicand***	***Dividend***
ADDR	Multiplicand[15 : 8]	Dividend[31 : 24]
ADDR+1	Multiplicand[7 : 0]	Dividend[23 : 16]
ADDR+2	--	Dividend[15 : 8]
ADDR+3	--	Dividend[7 : 0]

Table 5-204 MDU_DSRC_ADR0 register

MDU_DSRC_ADR1			**Page : 3 / Address: 0xDB**		**MDU DMA Source Address 1 Register**			
Bit	7	6	5	4	3	2	1	0
Function	MDU_DSRC_ADR1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	MDU_DSRC_ADR1	R/W	***Multiplier*** and ***Divisor*** DMA source address register. These address cover all-off internal data memory only. The arrangement of internal content as below table.	

MDU_DSRC_ADR1	***Multiplier***	***Divisor***
ADDR	Multiplier[15 : 8]	Divisor [15 : 8]
ADDR+1	Multiplier[7 : 0]	Divisor [7 : 0]

Table 5-205 MDU_DSRC_ADR1 register

MDU_DTAR_ADDR			**Page : 3 / Address: 0xDC**		**MDU DMA Target Address Register**			
Bit	7	6	5	4	3	2	1	0
Function	MDU_DTAR_ADDR[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	MDU_DTAR_ADDR	R/W	***Multiplier*** and ***Divider*** DMA target address register. These address cover all-off internal data memory only. The arrangement of internal content as below table.	

MDU_DTAR_ADDR	***Multipilier***	***Divider***
ADDR	Product[31: 24]	Quotient[31 : 24]
ADDR+1	Product[23 : 16]	Quotient[23 : 16]
ADDR+2	Product[15 : 8]	Quotient[15 : 8]
ADDR+3	Product[7 : 0]	Quotient[7 : 0]
ADDR+4	-	Remainder[15 : 8]
ADDR+5	-	Remainder[7 : 0]

Table 5-206 MDU_DTAR_ADDR register

P5			Address: 0xC8		Port5 Register			
Bit	7	6	5	4	3	2	1	0
Function	DIV_INTF	MUL_INTF	--	P54	P53	P52	P51	P50
Default	0	0	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Function	Type	Description	Condition
7	DIV_INTF	R	Divider interrupts flag. 0: idle / busy 1 : Divider interrupt trigger	
6	MUL_INTF	R	Multiplier interrupts flag. 0: idle / busy 1: Multiplier interrupt trigger	
5	--	R/W	Reserved	
4:0	P5[4:0]	R/W	P5 is used to set IO output data only. Otherwise, that also can be used to configure the Port5 function.	

Table 5-207 P5 register

5.14. RTC Unit

The GPM8F3732B has embedded a RTC counter. That supports up to 60-sec time-piece function. Before enable RTC function, user must enable 32K clock first. Moreover, the RTC provide 4 interrupt trigger point that consist of 0.5sec/1sec/30sec/60sec etc. User can choice anyone to trigger system. Figure 5-52 is the block diagram of RTC block.

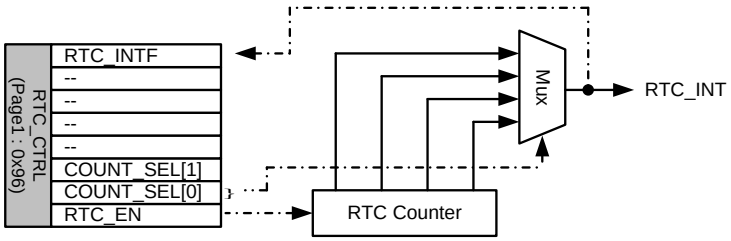


Figure 5-52 The block diagram of RTC block

RTC Related Register

RTC_CTRL			Page : 1 / Address: 0x96		Real Time Counter Control Register			
Bit	7	6	5	4	3	2	1	0
Function	RTC_INTF	--	--	--	--	COUNT_SEL[1:0]		RTC_EN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	RTC_INTF	R/W	RTC interrupt flag. read : 0 : interrupt is inactived 1 : interrupt is actived write : 0 : clears this bit 1 : no effect	
6:3		R/W	Reserved	
2:1	COUNT_SEL	R/W	RTC interrupt interval select signals	

Bit	Function	Type	Description	Condition
			00 : 0.5 Sec 01 : 1Sec 10 : 30Sec 11 : 60Sec	
0	RTC_EN	R/W	RTC enable signal 0 : disabled 1 : enabled	

Table 5-208 RTC_CTRL register

5.15. LCD Unit

A LCD Interface is equipped in GPM8F3732B. That supports 4 X 31 pixels resolution with 1/3 voltage bias. For satisfaction difference application, user cans choice m COM X n SEG randomly. In addition, user wills turn-off the system clock in order to decrease power consumption. Then, LCD controller is still providing display scanning with low power disputation. Figure 5-53 is the block diagram of LCD controller.

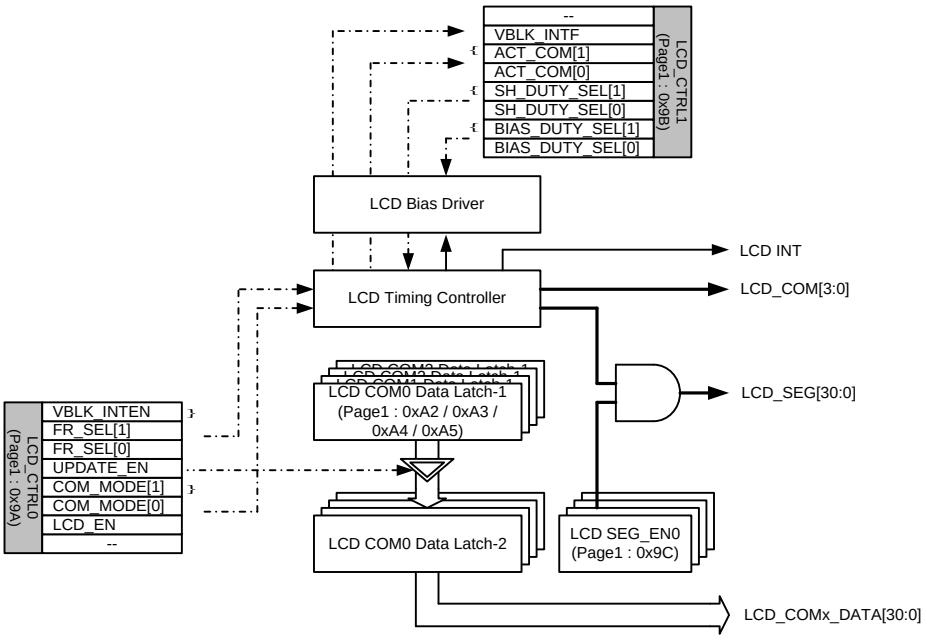


Figure 5-53 The block diagram of LCD controller

LCD Related Register

LCD_CTRL0			Page : 1 / Address: 0x9A		LCD Control Register - 0			
Bit	7	6	5	4	3	2	1	0
Function	VBLK_INTEN	FR_SEL[1:0]		UPDATE_EN	COM_MODE[1:0]		LCD_EN	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	VBLK_INTEN	R/W	V-Blank interrupt enable 0 : disabled 1 : enabled	
6:5	FR_SEL[1:0]	R/W	Frame select signal	

Bit	Function	Type	Description	Condition
			FR_SEL[1:0] / Frame Rate 00 / 110Hz 01 / 95Hz 10 / 85Hz 11 / 75Hz	
4	UPDATE_EN	R/W	LCD display content update enable signal. Hardware will update LCD content when V-syn is arrived and this bit is enabled. 0 : disabled 1 : enabled	
3:2	COM_MODE[1:0]	R/W	LCD common signal selection bit COM_MODE[1:0] / COM # 00 / COM0 01 / COM0 ~ COM1 10 / COM0 ~ COM2 11 / COM0 ~ COM3	
1	LCD_EN	R/W	LCD enable control bit. 0 : disabled 1 : enabled	
0	--	R/W	Reserved	

Table 5-209 LCD_CTRL0 register

LCD_CTRL1			**Page : 1 / Address: 0x9B**		**LCD Control Register -** 1			
Bit	7	6	5	4	3	2	1	0
Function	--	VBLK_INTF	ACT_COM[1:0]		SH_DUTY_SEL[1:0]		BIAS_DUTY_SEL[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	VBLK_INTF	R/W	LCD V-blanking interrupts flag. Read: 0 : inactive 1 : active Write : 0 : clears this bit 1 : no effect	
5:4	ACT_COM[1:0]	R	These bits are used to indicate which COM is scanning. ACT_COM / COM # 00 / 0 01 / 1 10 / 2 11 / 3	
3:2	SH_DUTY_SEL[1:0]	R/W	LCD segment bias select signal. SH_DUTY_SEL / Duty Cycle 00 / 0.5/384 01 / 0.5/512	

Bit	Function	Type	Description	Condition
			10 0.5/640 11 Always On	
1:0	BIAS_DUTY_SEL[1:0]	R/W	LCD common bias select signal. BIAS_DUTY_SEL / Duty Cycle 00 1/384 01 1/512 10 1/640 11 Always On	

Table 5-210 LCD_CTRL1 register

LCD_SEG_EN0			Page : 1 / Address: 0x9C		LCD Segment Enable Control Register - 0			
Bit	7	6	5	4	3	2	1	0
Function	LCD_SEG_EN[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_SEG_EN[7:0]	R/W	LCD segment[7:0] enable control bit. The relate PAD will operate in other factions when LCD_SEG_EN[x] is set to 0. 0 : disabled 1 : enabled	

Table 5-211 LCD_SEG_EN0 register

LCD_SEG_EN1			Page : 1 / Address: 0x9D		LCD Segment Enable Control Register - 1			
Bit	7	6	5	4	3	2	1	0
Function	LCD_SEG_EN[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_SEG_EN[15:8]	R/W	LCD segment[15:8] enable control bit. The relate PAD will operate in other factions when LCD_SEG_EN[x] is set to 0. 0 : disabled 1 : enabled	

Table 5-212 LCD_SEG_EN1 register

LCD_SEG_EN2			Page : 1 / Address: 0x9E		LCD Segment Enable Control Register - 2			
Bit	7	6	5	4	3	2	1	0
Function	LCD_SEG_EN[23:16]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_SEG_EN[23:16]	R/W	LCD segment[23:16] enable control bit. The relate PAD will operate in other factions when LCD_SEG_EN[x] is set to 0. 0 : disabled 1 : enabled	

Table 5-213 LCD_SEG_EN2 register

LCD_SEG_EN3			Page : 1 / Address: 0x9F		LCD Segment Enable Control Register - 3			
Bit	7	6	5	4	3	2	1	0
Function	--	LCD_SEG_EN[30:24]						
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6:0	LCD_SEG_EN[30:24]	R/W	LCD segment[30:24] enable control bit. The relate PAD will operate in other factions when LCD_SEG_EN[x] is set to 0. 0 : disabled 1 : enabled	

Table 5-214 LCD_SEG_EN3 register

LCD_COM0_D7_0			Page : 1 / Address: 0xA2		LCD Common 0 Data 7-0 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM0_D[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM0_D[7:0]	R/W	LCD common 0 data[7:0]. 0 : pixel off 1 : pixel on	

Table 5-215 LCD_COM0_D7_0 register

LCD_COM0_D15_8			Page : 1 / Address: 0xA3		LCD Common 0 Data 15:8 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM0_D[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM0_D[15:8]	R/W	LCD common 0 data[15:8]. 0 : pixel off 1 : pixel on	

Table 5-216 LCD_COM0_D15_8 register

LCD_COM0_D23_16			Page : 1 / Address: 0xA4		LCD Common 0 Data 23-16 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM0_D[23:16]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM0_D[23:16]	R/W	LCD common 0 data[23:16]. 0 : pixel off 1 : pixel on	

Table 5-217 LCD_COM0_D23_16 register

LCD_COM0_D30_24			Page : 1 / Address: 0xA5		LCD Common 0 Data 30-24 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	LCD_COM0_D[30:24]						
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6:0	LCD_COM0_D[30:24]	R/W	LCD common 0 data[30:24]. 0 : pixel off 1 : pixel on	

Table 5-218 LCD_COM0_D30_24 register

LCD_COM1_D7_0			Page : 1 / Address: 0xAA		LCD Common 1 Data 7-0 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM1_D[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM1_D[7:0]	R/W	LCD common 1 data[7:0]. 0 : pixel off 1 : pixel on	

Table 5-219 LCD_COM1_D7_0 register

LCD_COM1_D15_8			Page : 1 / Address: 0xAB		LCD Common 1 Data 15:8 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM1_D[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM1_D[15:8]	R/W	LCD common 1 data[15:8]. 0 : pixel off 1 : pixel on	

Table 5-220 LCD_COM1_D15_8 register

LCD_COM1_D23_16			Page : 1 / Address: 0xAC		LCD Common 1 Data 23-16 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM1_D[23:16]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM1_D[23:16]	R/W	LCD common 1 data[23:16]. 0 : pixel off 1 : pixel on	

Table 5-221 LCD_COM1_D23_16 register

LCD_COM1_D30_24			Page : 1 / Address: 0xAD		LCD Common 1 Data 30-24 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	LCD_COM1_D[30:24]						
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6:0	LCD_COM1_D[30:24]	R/W	LCD common 1 data[30:24]. 0 : pixel off 1 : pixel on	

Table 5-222 LCD_COM1_D30_24 register

LCD_COM2_D7_0			Page : 1 / Address: 0xB2		LCD Common 2 Data 7-0 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM2_D[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM2_D[7:0]	R/W	LCD common 2 data[7:0]. 0 : pixel off 1 : pixel on	

Table 5-223 LCD_COM2_D7_0 register

LCD_COM2_D15_8			Page : 1 / Address: 0xB3		LCD Common 2 Data 15:8 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM2_D[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM2_D[15:8]	R/W	LCD common 2 data[15:8]. 0 : pixel off 1 : pixel on	

Table 5-224 LCD_COM2_D15_8 register

LCD_COM2_D23_16			Page : 1 / Address: 0xB4		LCD Common 2 Data 23-16 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM2_D[23:16]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM2_D[23:16]	R/W	LCD common 2 data[23:16]. 0 : pixel off 1 : pixel on	

Table 5-225 LCD_COM2_D23_16 register

LCD_COM2_D30_24			Page : 1 / Address: 0xB5		LCD Common 2 Data 30-24 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	LCD_COM2_D[30:24]						
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6:0	LCD_COM2_D[30:24]	R/W	LCD common 2 data[30:24]. 0 : pixel off 1 : pixel on	

Table 5-226 LCD_COM2_D30_24 register

LCD_COM3_D7_0			Page : 1 / Address: 0xBA		LCD Common 3 Data 7-0 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM3_D[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM3_D[7:0]	R/W	LCD common 3 data[7:0]. 0 : pixel off 1 : pixel on	

Table 5-227 LCD_COM3_D7_0 register

LCD_COM3_D15_8			Page : 1 / Address: 0xBB		LCD Common 3 Data 15:8 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM3_D[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM3_D[15:8]	R/W	LCD common 3 data[15:8]. 0 : pixel off 1 : pixel on	

Table 5-228 LCD_COM3_D15_8 register

LCD_COM3_D23_16			Page : 1 / Address: 0xBC		LCD Common 3 Data 23-16 Register			
Bit	7	6	5	4	3	2	1	0
Function	LCD_COM3_D[23:16]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	LCD_COM3_D[23:16]	R/W	LCD common 3 data[23:16]. 0 : pixel off 1 : pixel on	

Table 5-229 LCD_COM3_D23_16 register

LCD_COM3_D30_24			Page : 1 / Address: 0xBD		LCD Common 3 Data 30-24 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	LCD_COM3_D[30:24]						
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6:0	LCD_COM3_D[30:24]	R/W	LCD common 3 data[30:24]. 0 : pixel off 1 : pixel on	

Table 5-230 LCD_COM3_D30_24 register

5.16. Capacitive Touch Unit

In GPM8F3732B, there are two timers, timer B and timer C for Capacitive Touch sensor. They are 16-bit down counter. It provides the ability to perform capacitive sensing, decision making, responsive actions and other duties pertinent to the system as well.

5.16.1. Capacitance Measurement Method

The capacitance measurement method based on the relaxation oscillator methodology. It produces an oscillating voltage signal for measurement, at a frequency dependent on the capacitance of an object connected to the module. The basic concept is as follows:

• The capacitive sensing structure oscillates at some frequency, dependent on the capacitance of a connected sensing electrode.

•The capacitive sensing structure frequency changes when a touch is introduced near the sensing electrode because the touch changes the total capacitance presented by the electrode.

•The capacitive sensing structure frequency change is used as an indication of a touch condition. Figure 5-54 to Figure 5-57 show the related timing and block diagram.

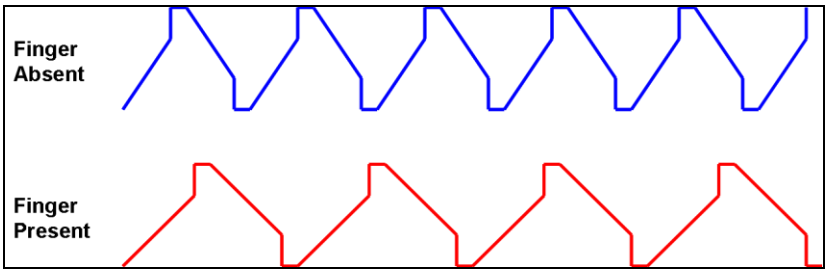


Figure 5-54 The timing show the status of Finger Absent and Finger Present.

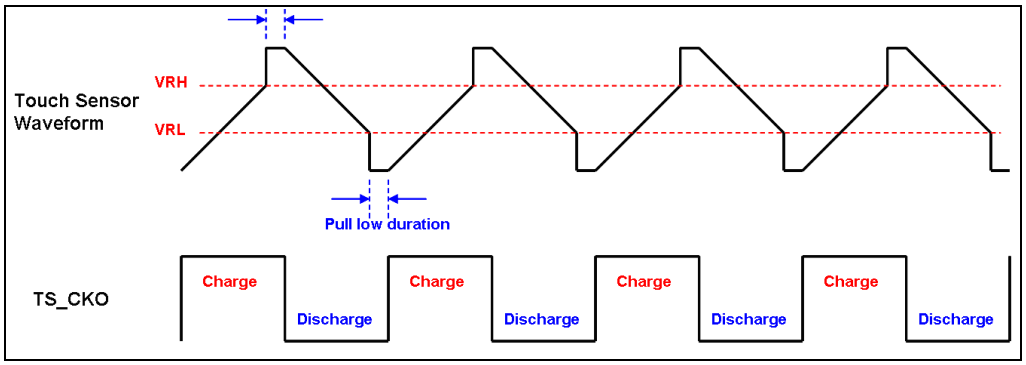


Figure 5-55 The timing shows the capacitive sensing structure output frequency (EN_TRI = “0”)

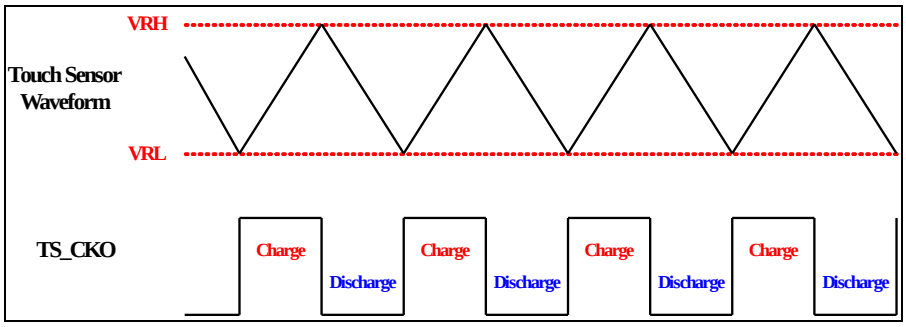


Figure 5-56 The timing shows the capacitive sensing structure output frequency (EN_TRI = "1")

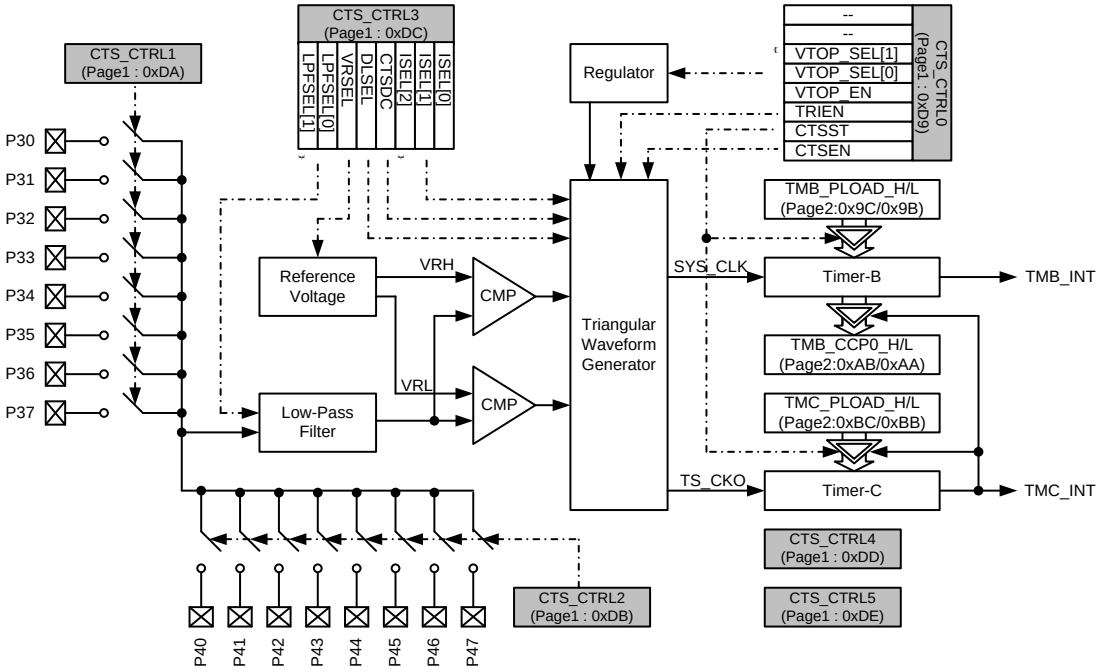


Figure 5-57 The capacitive sensing structure block diagrams.

The capacitive sensing structure provides two applications, the self-capacitance and mutual-capacitance. A simplified application diagram is shown in Figure 5-.

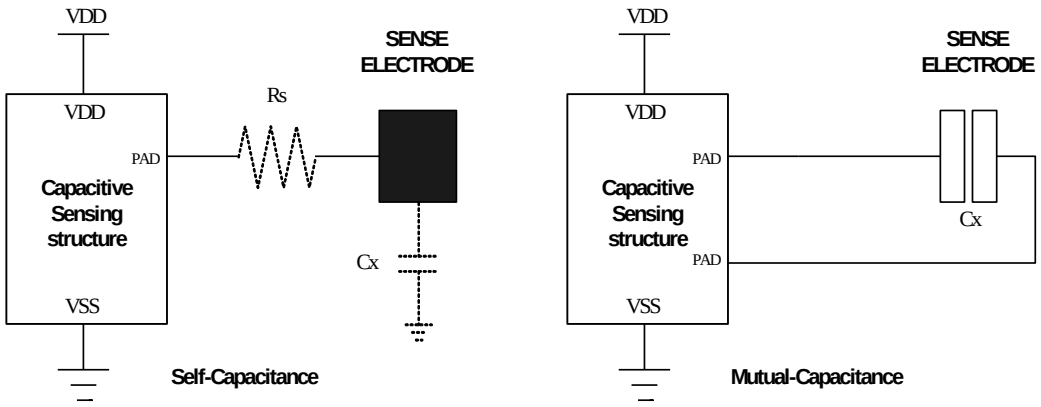


Figure 5-58 The self-capacitance and mutual-capacitance.

CTS_CTRL0			Page : 1 / Address: 0xD9		Capacitive Touch Sensor Control Register – 0			
Bit	7	6	5	4	3	2	1	0
Function	--	--	VTOPSEL[1:0]		VTOP_EN	TRIEN	CTSST	CTSEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	-	R/W	Reserved	
5:4	VTOPSEL[1:0]	R/W	Regulator Output Voltage for touch sensing VDD voltage, VTOPSEL[1:0] – gTouch VDD 00 – 2.2V 01 – 2.7V 10 – 3.0V 11 – 4.5V	
3	VTOPEN	R/W	gTouch regulator enable 0 : disabled 1 : enabled	
2	TRIEN	R/W	0 : Disables triangular waveform mode 1 : Enables triangular waveform mode	
1	CTSST	R/W	Touch sensor start transfer control 0 : disabled 1 : enabled	
0	CTSEN	R/W	Capacitive touch sensor enable bit 0: Disabled 1: Enabled	

Table 5-231 The CTS_CTRL0 register

CTS_CTRL1			Page : 1 / Address: 0xDA		Capacitive Touch Sensor Control Register – 1			
Bit	7	6	5	4	3	2	1	0
Function	CHSEL[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CHSEL[7:0]	R/W	Touch channel selection CHSEL[7:0] – Touch Channel 0000_0001 – P30 is selected 0000_0010 – P31 is selected 0000_0100 – P32 is selected 0000_1000 – P33 is selected 0001_0000 – P34 is selected 0010_0000 – P35 is selected 0100_0000 – P36 is selected 1000_0000 – P37 is selected	

Table 5-232 The CTS_CTRL1 register

CTS_CTRL2			Page : 1 / Address: 0xDB		Capacitive Touch Sensor Control Register – 2			
Bit	7	6	5	4	3	2	1	0
Function	CHSEL[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CHSEL[15:8]	R/W	Touch channel selection CHSEL[15:8] — Touch Channel 0000_0001 — P40 is selected 0000_0010 — P41 is selected 0000_0100 — P42 is selected 0000_1000 — P43 is selected 0001_0000 — P44 is selected 0010_0000 — P45 is selected 0100_0000 — P46 is selected 1000_0000 — P47 is selected	

Table 5-233 The CTS_CTRL2 register

CTS_CTRL3			Page : 1 / Address: 0xDC		Capacitive Touch Sensor Control Register – 3			
Bit	7	6	5	4	3	2	1	0
Function	LPFSEL[1:0]		VRSEL	DLSEL	CTSDC	ISEL[2:0]		
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	LPFSEL[1:0]	R/W	Noise Filter for Comparator(1st order RC filter) LPFSEL[1:0] — Bandwidth 00 — 10MHz 01 — 2MHz 10 — 1MHz 11 — 0.5MHz	
5	VRSEL	R/W	Voltage Reference Selection for Comparator (VDD=2.2V) VRSEL — VRH — VRL 0 — 1.47V — 0.73V 1 — 2.02V — 0.18V Voltage Reference Selection for Comparator (VDD=2.7V) VRSEL — VRH — VRL 0 — 1.8V — 0.9V 1 — 2.475V — 0.225V Voltage Reference Selection for Comparator (VDD=3.0V) VRSEL — VRH — VRL 0 — 2.0V (2/3 VDD) — 1.0V (1/3 VDD) 1 — 2.75V (11/12 VDD) — 0.25V (1/12 VDD) Voltage Reference Selection for Comparator (VDD=4.5V)	

Bit	Function	Type	Description	Condition
			VRSEL / VRH / VRL 0 / 3.0V / 1.5V 1 / 4.125V / 0.375V	
4	DLSEL	R/W	Pull High/Pull Low Duration {CTSDC , DLSEL} / Delay Time 00 / 260ns 01 / 128ns 10 / 142ns 11 / 70ns	
3	CTSDC	R/W	Charge/ Discharge double current selection 0: Disabled 1: Enabled	
2:0	ISEL	R/W	Charge/Discharge current selection {CTSDC , ISEL} / Charge / Discharge Current 0_000 / 0uA 0_001 / 2.5uA 0_010 / 5uA 0_011 / 10uA 0_100 / 25uA 0_101 / 50uA 0_110 / 100uA 0_111 / 150uA	

Table 5-234 The CTS_CTRL3 register

CTS_CTRL4			Page : 1 / Address: 0xDD		Capacitive Touch Sensor Control Register - 4			
Bit	7	6	5	4	3	2	1	0
Function	MUPORTSEL[2:0]			MUPINSEL[2:0]			MUTPOL	MUTEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	MUPORTSEL	R/W	Select Mutual-capacitance IO port mapping MUPORTSEL[2:0] / Port Number 000 / IO port P0 001 / IO port P1 010 / IO port P2 011 / IO port P3 100 / IO port P4 101 / IO port P5 110 / prohibit 11 / prohibit	
4:2	MUPINSEL	R/W	Select Mutual-capacitance IO pin mapping MUPORTSEL[2:0] / Port Number 000 / IO Port x Pin 0 001 / IO Port x Pin 1 010 / IO Port x Pin 2	

Bit	Function	Type	Description	Condition
			011 IO Port x Pin 3 100 IO Port x Pin 4 101 IO Port x Pin 5 110 IO Port x Pin 6 11 IO Port x Pin 7	
1	MUTPOL	R/W	Adjustment of the mutual-capacitance output waveform of the polarity 0 : negative polarity 1 : positive polarity	
0	MUTEN	R/W	Mutual capacitance function control 0 : Disabled 1 : Enabled	

Table 5-235 The CTS_CTRL4 register

CTS_CTRL5			Page : 1 / Address: 0xDE		Capacitive Touch Sensor Control Register 5			
Bit	7	6	5	4	3	2	1	0
Function	MUTDEL_SEL[3:0]				--	--	--	TSCFG
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	MUTDEL_SEL	R/W	Mutual capacitance output PAD delay timing control with TS_CKO waveform MUTDEL_SEL[3:0] Delay cycle 0000 Prohibit 0001 delay 1 system clock cycle. 0010 delay 2 system clock cycle. 0011 delay 4 system clock cycle. 0100 delay 6 system clock cycle. 0101 delay 8 system clock cycle. 0110 delay 10 system clock cycle. 0111 delay 12 system clock cycle. 1000 delay 14 system clock cycle. 1001 delay 16 system clock cycle. 1010 delay 18 system clock cycle. 1011 delay 20 system clock cycle. 1100 delay 22 system clock cycle. 1101 delay 24 system clock cycle. 1110 delay 26 system clock cycle. 1111 delay 28 system clock cycle.	
3:1	-	R/W	Reserved	
0	TSCGF	R	Read TS_CKO signal waveform	

Table 5-236 The CTS_CTRL5 register

5.17. Alphabetical List of Instruction Set

5.17.1. Arithmetic Operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A,direct	Add direct byte to accumulator	0x25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A,#data	Add immediate data to accumulator	0x24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A,#data	Add immediate data to A with carry flag	0x34	2	2
SUBB A,Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	1	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	2	3
INC DPTR	Increment data pointer	0xA3	1	1
MUL A,B	Multiply A and B	0xA4	1	2
DIV A,B	Divide A by B	0x84	1	6
DA A	Decimal adjust accumulator	0xD4	1	3

5.17.2. Logic Operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A,direct	AND direct byte to accumulator	0x55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A,#data	AND immediate data to accumulator	0x54	2	2
ANL direct,A	AND accumulator to direct byte	0x52	2	3
ANL direct,#data	AND immediate data to direct byte	0x53	3	3
ORL A,Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A,direct	OR direct byte to accumulator	0x45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A,#data	OR immediate data to accumulator	0x44	2	2
ORL direct,A	OR accumulator to direct byte	0x42	2	3
ORL direct,#data	OR immediate data to direct byte	0x43	3	3
XRL A,Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A,#data	Exclusive OR immediate data to accumulator	0x64	2	2

Mnemonic	Description	Code	Bytes	Cycles
XRL direct,A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	1

5.17.3. Boolean Operations

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C,bit	AND direct bit to carry flag	0x82	2	2
ANL C,/bit	AND complement of direct bit to carry	0xB0	2	2
ORL C,bit	OR direct bit to carry flag	0x72	2	2
ORL C,/bit	OR complement of direct bit to carry	0xA0	2	2
MOV C,bit	Move direct bit to carry flag	0xA2	2	2
MOV bit,C	Move carry flag to direct bit	0x92	2	3

5.17.4. Data Transfers

Mnemonic	Description	Code	Bytes	Cycles
MOV A,Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A,direct	Move direct byte to accumulator	0xE5	2	2
MOV A,@Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A,#data	Move immediate data to accumulator	0x74	2	2
MOV Rn,A	Move accumulator to register	0xF8-0xFF	1	1
MOV Rn,direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn,#data	Move immediate data to register	0x78-0x7F	2	2
MOV direct,A	Move accumulator to direct byte	0xF5	2	2
MOV direct,Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1,direct2	Move direct byte to direct byte	0x85	3	3
MOV direct,@Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct,#data	Move immediate data to direct byte	0x75	3	3
MOV @Ri,A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri,direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri,#data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR,#data16	Load 16-bit constant into active DPH and DPL in LARGE mode	0x90	3	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator	0x93	1	5
MOVC A,@A+PC	Move code byte relative to PC to accumulator	0x83	1	4

Mnemonic	Description		Code	Bytes	Cycles
MOVX A,@Ri	Move external RAM (8-bit address) to A	XDM	0xE2-0xE3	1	3*
		SXDM			3
MOVX A,@DPTR	Move external RAM (16-bit address) to A	XDM	0xE0	1	2*
		SXDM			2
MOVX @Ri,A	Move A to external XDM (8-bit address)	ODE inside ROM/RAM	0xF2-0xF3	1	4*
		Other cases			5*
	Move A to external SXDM (8-bit address)	All cases			3
MOVX @DPTR,A	Move A to external XDM (16-bit address)	CODE inside ROM/RAM	0xF0	1	3*
		Other cases			4*
	Move A to external SXDM (16-bit address)	All cases			2
PUSH direct	Push direct byte onto IDM stack		0xC0	2	3
POP direct	Pop direct byte from IDM stack		0xD0	2	2
XCH A,Rn	Exchange register with accumulator		0xC8-0xCF	1	2
XCH A,direct	Exchange direct byte with accumulator		0xC5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator		0xC6-0xC7	1	3
XCHD A,@Ri	Exchange low-order nibble indirect RAM with A		0xD6-0xD7	1	3

5.17.5. Program Branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	0x11-0xF1	2	4
LCALL addr16	Long subroutine call	0x12	3	4
RET	Return from subroutine	0x22	1	4
RETI	Return from interrupt	0x32	1	4
AJMP addr11	Absolute jump	0x01-0xE1	2	3
LJMP addr16	Long jump	0x02	3	4
SJMP rel	Short jump (relative address)	0x80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	0x73	1	5
JZ rel	Jump if accumulator is zero	0x60	2	4
JNZ rel	Jump if accumulator is not zero	0x70	2	4
JC rel	Jump if carry flag is set	0x40	2	3
JNC	Jump if carry flag is not set	0x50	2	3
JB bit,rel	Jump if direct bit is set	0x20	3	5
JNB bit,rel	Jump if direct bit is not set	0x30	3	5
JBC bit,direct rel	Jump if direct bit is set and clear bit	0x10	3	5
CJNE A,direct rel	Compare direct byte to A and jump if not equal	0xB5	3	5
CJNE A,#data rel	Compare immediate to A and jump if not equal	0xB4	3	4
CJNE Rn,#data rel	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4
CJNE @Ri,#data rel	Compare immediate to ind. and jump if not equal	0xB6-0xB7	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	0xD8-0xDF	2	4
DJNZ direct,rel	Decrement direct byte and jump if not zero	0xD5	3	5
NOP	No operation	0x00	1	1

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	-0.3V ~ 6.0V
Input Voltage Range	V_{IN}	-0.3V to V_+ + 0.3V
Operating Temperature	T_A	-40℃ to +85℃
VDD Total MAX Current	I_{VDDM}	30mA
VSS Total MAX Current	I_{VSSM}	30mA

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
IOSC Frequency	F_{OSC}	8.0×(1-2%)	8.0	8.0×(1+2%)	MHz	±2% at 2.4V~5.5V
PLL Frequency	F_{PLL}	48.0×(1-2%)	48.0	48.0×(1+2%)	MHz	±2% at 2.4V~5.5V

6.3. DC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	-	5.5	V	
Operating Current	I_{OP}	-	-	15.0	mA	SYSCLK= 48MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	10.0	uA	VDD = 5.5V
Input High Level	V_{IH}	0.7*VDD	-	-	V	VDD = 5.0V(with Schmitt trigger)
Input Low Level	V_{IL}	-	-	0.3*VDD	V	VDD = 5.0V(with Schmitt trigger)
Output High Level	V_{OH}	0.8*VDD	-	-	V	I_{OH} = -8mA at VDD = 5.0V
Output Low Level	V_{OL}	-	-	0.2*VDD	V	I_{OL} = 20mA at VDD = 5.0V
Input Pull High Resistor 1	R_{PH1}	30	50	70	KΩ	VDD = 5.0V
Input Pull High Resistor 1	R_{PL1}	30	50	70	KΩ	VDD = 5.0V
Low Voltage Reset 1	V_{LVR1}	1.9×(1-5%)	2.2	1.9×(1+5%)	V	SYS_CTRL3[2:1]=00
Low Voltage Reset 2	V_{LVR2}	2.4×(1-5%)	2.4	2.4×(1+5%)	V	SYS_CTRL3[2:1]=01
Low Voltage Reset 3	V_{LVR3}	3.2×(1-5%)	3.2	3.2×(1+5%)	V	SYS_CTRL3[2:1]=10
Low Voltage Reset 4	V_{LVR4}	4.2×(1-5%)	4.2	4.2×(1+5%)	V	SYS_CTRL3[2:1]=11

6.4. ADC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	V_{LVR}	-	5.5	V	
ADC Input Voltage Range	V_{ADCIN}	0	-	VDD	V	
ADC Clock Period	T_{AD}	-	-	-	us	Depended on system clock
Input Channel		-	-	16	channel	
Resolution		12			Bit	
No Missing Code		10			bits	
ADC Conversion Time	T_{CON}	-	-	-	us	ADCLK * 15

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Integral Linearity Error	E_{INL}	-	±2	±3	LSB	
Differential Linearity Error	E_{DNL}	-	-1~+2	-1~+3	LSB	

7. PACKAGE INFORMATION

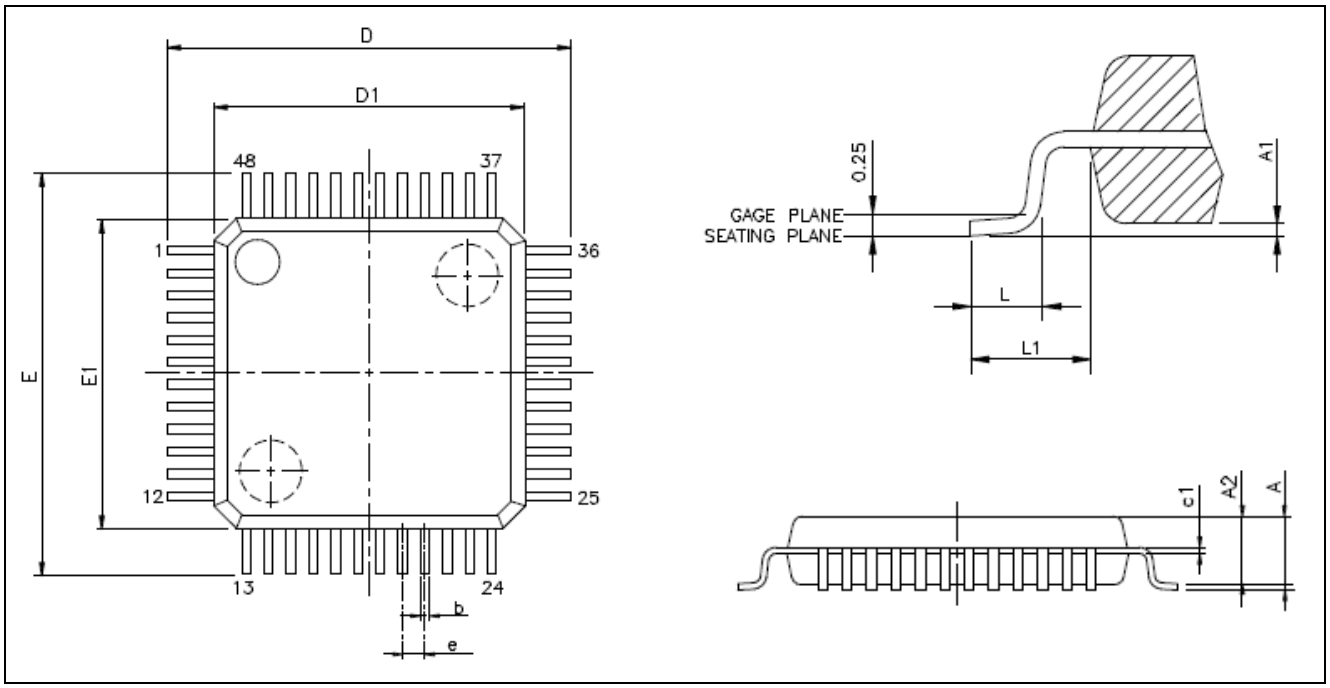
7.1. Ordering Information

Product Number	Package Type
GPM8F3732B – QL23x	Halogen Free Package

Note1: Package form number (x = 1 - 9, serial number).

7.2. Package Information

7.2.1. LQFP 48



Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	-	1.45
c1	0.09	-	0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
b	0.17	-	0.27
L	0.45	-	0.75
L1	1.00 REF		

8.DISCLAIMER

The information appearing in this publication is believed to be accurate.

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9. REVISION HISTORY

Date	Revision #	Description	Page
Aug. 14, 2017	0.4	Modify LCD pixel number from 4x32 pixels to 4x31 pixels.	5, 6, 9, 10, 16, 23, 116,119, 120,121, 122,123
May 17, 2016	0.3	add PX register definition	58
Jul. 03, 2015	0.2	1. Modify IOSC clock source in Figure 5-5 2.Modify wrong spelling 3. Modify Figure 5-21	
Dec. 11, 2014	0.1	Original	146