256×8 bit electrically erasable PROM

BR24L02-W / BR24L02F-W / BR24L02FJ-W
BR24L02FV-W / BR24L02FVM-W

The BR24L02-W series is 2-wire (I^2C BUS type) serial EEPROMs which are electrically programmable.

∗ I^2C BUS is a registered trademark of Philips.

●Applications

General purpose

●Features

1) 256 registers × 8 bits serial architecture.
2) Single power supply (1.8V to 5.5V).
3) Two wire serial interface.
4) Self-timed write cycle with automatic erase.
5) 8 byte page write mode.
6) Low power consumption.
   Write (5V) : 1.2mA (Typ.)
   Read (5V) : 0.2mA (Typ.)
   Standby (5V) : 0.1μA (Typ.)
7) DATA security
   Write protect feature (WP pin) .
   Inhibit to WRITE at low V_{CC}.
8) Small package - - - DIP8 / SOP8 / SOP-J8 / SSOP-B8 / MSOP-8
9) High reliability EEPROM with Double-Cell structure
10) High reliability fine pattern CMOS technology.
11) Endurance : 1,000,000 erase / write cycles
12) Data retention : 40 years
13) Filtered inputs in SCL•SDA for noise suppression.
14) Initial data FFh in all address.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	−0.3 to +6.5	V
Power dissipation	Pd	800 (DIP8) ∗1	mW
		450 (SOP8) ∗2	
		450 (SOP-J8) ∗3	
		300 (SSOP-B8) ∗4	
		310 (MSOP8) ∗5	
Storage temperature	Tstg	−65 to +125	°C
Operating temperature	Topr	−40 to +85	°C
Terminal voltage	−	−0.3 to V_{CC}+0.3	V

∗1 Degradation is done at 8.0mW/°C for operation above 25°C.
∗2, 3 Degradation is done at 4.5mW/°C for operation above 25°C.
∗4 Degradation is done at 3.0mW/°C for operation above 25°C.
∗5 Degradation is done at 3.1mW/°C for operation above 25°C.

● **Recommended operating conditions**

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	1.8 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V

● **DC operating characteristics** (Unless otherwise specified Ta=–40 to 85°C, VCC=1.8 to 5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
"HIGH" input volatge 1	V_{IH1}	0.7V_{CC}	–	–	V	2.5V≤V_{CC}≤5.5V
"LOW" input volatge 1	V_{IL1}	–	–	0.3V_{CC}	V	2.5V≤V_{CC}≤5.5V
"HIGH" input volatge 2	V_{IH2}	0.8V_{CC}	–	–	V	1.8V≤V_{CC}≤2.5V
"LOW" input volatge 2	V_{IL2}	–	–	0.2V_{CC}	V	1.8V≤V_{CC}≤2.5V
"LOW" output volatge 1	V_{OL1}	–	–	0.4	V	I_{OL}=3.0mA, 2.5V≤V_{CC}≤5.5V, (SDA)
"LOW" output volatge 2	V_{OL2}	–	–	0.2	V	I_{OL}=0.7mA, 1.8V≤V_{CC}≤5.5V, (SDA)
Input leakage current	I_{LI}	–1	–	1	μA	V_{IN}=0V to V_{CC}
Output leakage current	I_{LO}	–1	–	1	μA	V_{OUT}=0V to V_{CC}
Operating current	I_{CC1}	–	–	2.0	mA	V_{CC}=5.5V, f_{SCL}=400kHz, t_{WR}=5ms, Byte Write, Page Write
	I_{CC2}	–	–	0.5	mA	V_{CC}=5.5V, f_{SCL}=400kHz Random Read, Current Read, Sequential Read
Standby current	I_{SB}	–	–	2.0	μA	V_{CC}=5.5V, SDA·SCL=V_{CC}, A0, A1, A2=GND, WP=GND

○ This product is not designed for protection against radioactive rays.

●**Dimension**

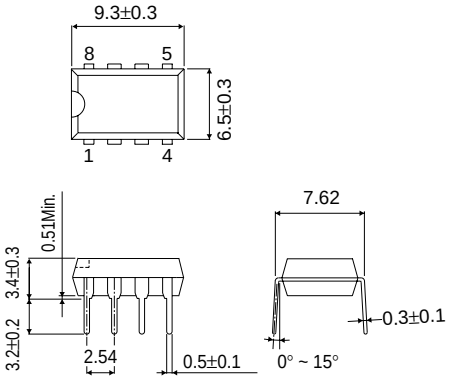


Fig.1(a) PHYSICAL DIMENSION (Units : mm)
DIP8 (BR24L02-W)

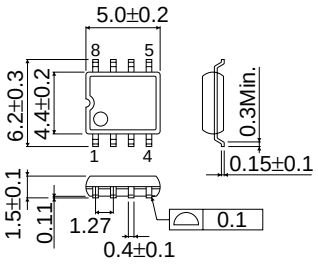


Fig.1(b) PHYSICAL DIMENSION (Units : mm)
SOP8 (BR24L02F-W)

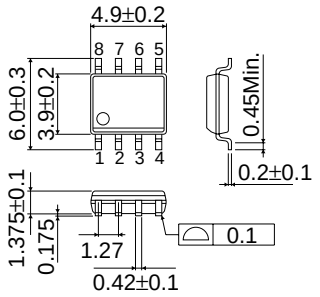


Fig.1(c) PHYSICAL DIMENSION (Units : mm)
SOP-J8 (BR24L02FJ-W)

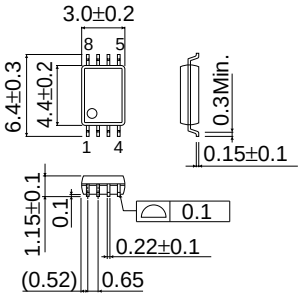


Fig.1(d) PHYSICAL DIMENSION (Units : mm)
SSOP-B8 (BR24L02FV-W)

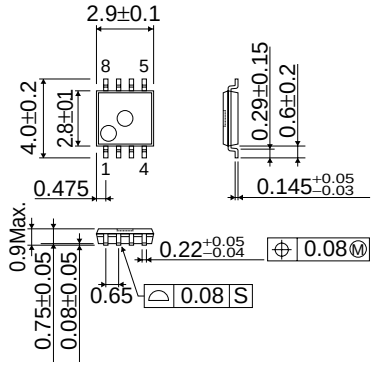


Fig.1(e) PHYSICAL DIMENSION (Units : mm)
MSOP8 (BR24L02FVM-W)

●**Block diagram**

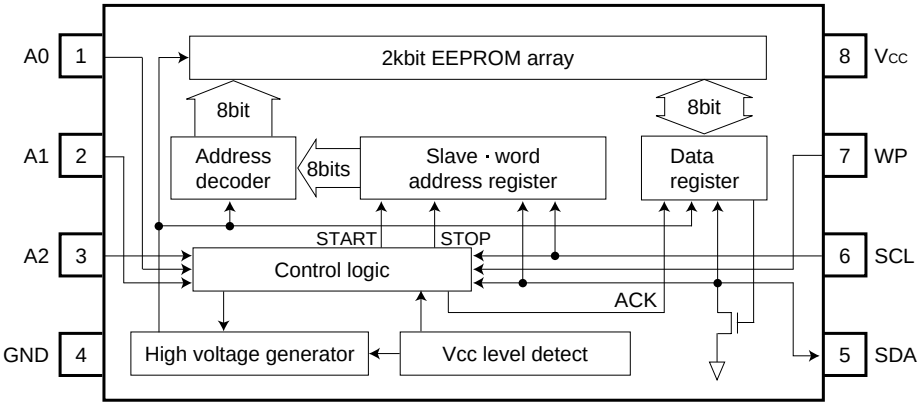


Fig.2 BLOCK DIAGRAM

●**Pin configuration**

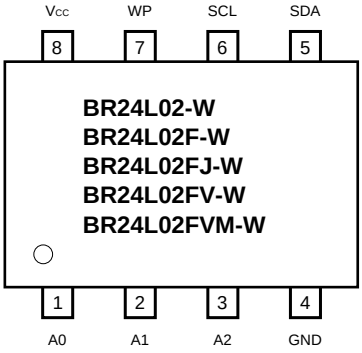


Fig.3 PIN LAYOUT

●**Pin name**

Pin name	I / O	Function
Vcc	–	Power supply
GND	–	Ground (0V)
A0, A1, A2	IN	Slave address set
SCL	IN	Serial clock input
SDA	IN / OUT	Slave and word address, serial data input, serial data output ∗1
WP	IN	Write protect input

∗1 An open drain output requires a pull-up resistor.

● **AC operating characteristics** (Unless otherwise specified Ta=–40 to 85°C, VCC=1.8 to 5.5V)

Parameter	Symbol	Fast-mode 2.5V ≤ Vcc ≤ 5.5V			Standard-mode 1.8V ≤ Vcc ≤ 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock frequency	fSCL	–	–	400	–	–	100	kHz
Data clock "HIGH" period	tHIGH	0.6	–	–	4.0	–	–	µs
Data clock "LOW" period	tLOW	1.2	–	–	4.7	–	–	µs
SDA and SCL rise time ∗1	tR	–	–	0.3	–	–	1.0	µs
SDA and SCL fall time ∗1	tF	–	–	0.3	–	–	0.3	µs
Start condition hold time	tHD:STA	0.6	–	–	4.0	–	–	µs
Start condition setup time	tSU:STA	0.6	–	–	4.7	–	–	µs
Input data hold time	tHD:DAT	0	–	–	0	–	–	ns
Input data setup time	tSU:DAT	100	–	–	250	–	–	ns
Output data delay time	tPD	0.1	–	0.9	0.2	–	3.5	µs
Output data hold time	tDH	0.1	–	–	0.2	–	–	µs
Stop condition setup time	tSU:STO	0.6	–	–	4.7	–	–	µs
Bus free time	tBUF	1.2	–	–	4.7	–	–	µs
Write cycle time	tWR	–	–	5	–	–	5	ms
Noise spike width (SDA and SCL)	tI	–	–	0.1	–	–	0.1	µs
WP hold time	tHD:WP	0	–	–	0	–	–	ns
WP setup time	tSU:WP	0.1	–	–	0.1	–	–	µs
WP high period	tHIGH:WP	1.0	–	–	1.0	–	–	µs

∗1 Not 100% tested.

●**Synchronous data timing**

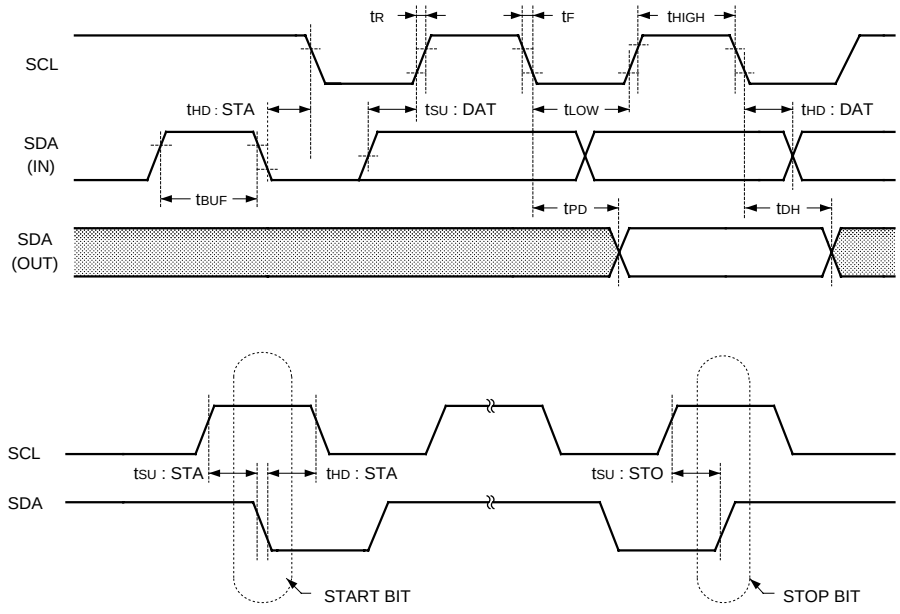


Fig.4 SYNCHRONOUS DATA TIMING

- SDA data is latched into the chip at the rising edge of SCL clock.
- Output data toggles at the falling edge of SCL clock.

●**Write cycle timing**

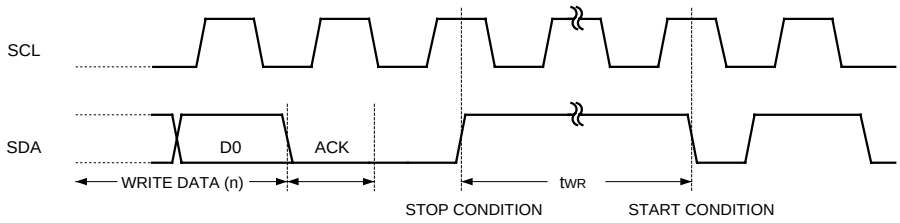


Fig.5 WRITE CYCLE TIMING

●WP timing

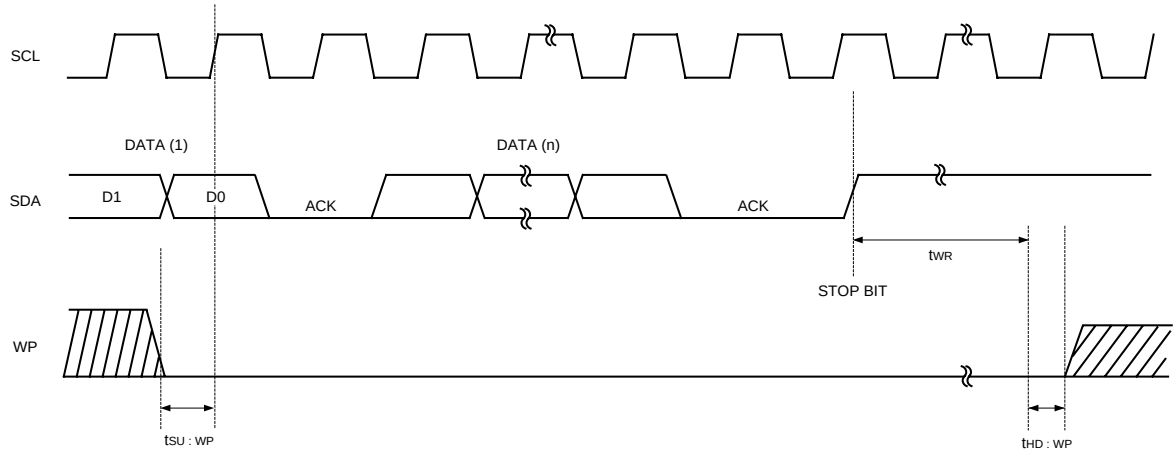


Fig.6(a) WP TIMING OF THE WRITE OPERATION

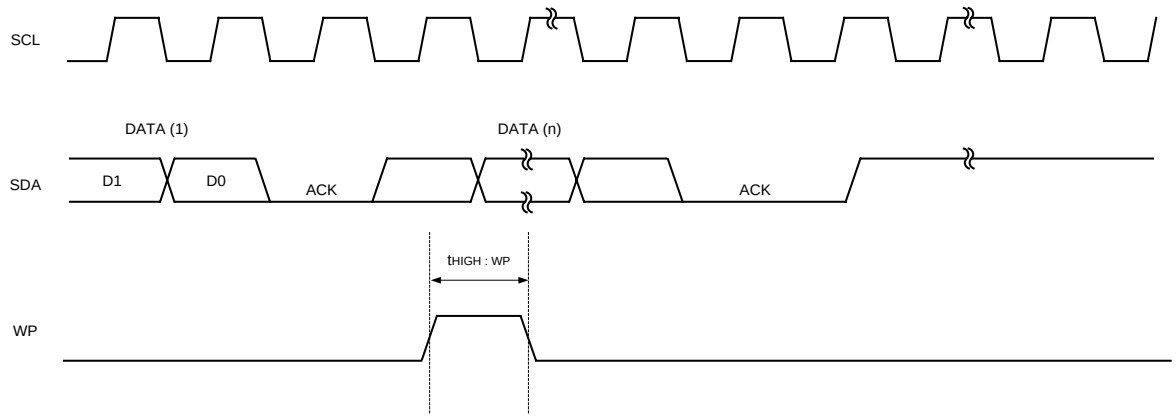


Fig.6(b) WP TIMING OF THE WRITE CANCEL OPERATION

- For the WRITE operation, WP must be “LOW” during the period of time from the rising edge of the clock which takes in D0 of first byte until the end of t_{WR}. (See Fig.6 (a))
  During this period, WRITE operation is canceled by setting WP “HIGH”. (See Fig.6 (b))
- In the case of setting WP “HIGH” during t_{WR}, WRITE operation is stopped in the middle and the data of accessing address is not guaranteed. Please write correct data again in the case.

●Device operation

1) Start condition (Recognition of start bit)

- All commands are proceeded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH.
- The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. (See Fig.4 SYNCHRONOUS DATA TIMING)

2) Stop condition (Recognition of stop bit)

- All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. (See Fig.4 SYNCHRONOUS DATA TIMING)

3) Notice about write command

- In the case that stop condition is not executed in WRITE mode, transferred data will not be written in a memory.

4) Device addressing

- Following a START condition, the master output the slave address to be accessed.
- The most significant four bits of the slave address are the “device type identifier”, for this device it is fixed as “1010”.
- The next three bit (device address) identify the specified device on the bus.
  The device address is defined by the state of A0, A1 and A2 input pins. This IC works only when the device address inputted from SDA pin correspond to the state of A0, A1 and A2 input pins. Using this address scheme, up to eight device may be connected to the bus. The last bit of the stream (R/$\overline{W}$ - - - READ / $\overline{WRITE}$) determines the operation to the performed.
- The last bit of the stream (R/$\overline{W}$ - - - READ / $\overline{WRITE}$) determines the operation to be performed. When set to “1”, a read operation is selected ; when set to “0”, a write operation is selected.

  R / $\overline{W}$ set to “0” - - - - - - WRITE (including word address input of Random Read)
  R / $\overline{W}$ set to “1” - - - - - - READ

1010	A2	A1	A0	R / $\overline{W}$

5) Write protect (WP)

When WP pin set to Vcc (H level), write protect is set for 256 words (all address).
When WP pin set to GND (L level), enable to write 256 words (all address).
Either control this pin or connect to GND (or Vcc). It is inhibited from being left unconnected.

6) Acknowledge

- Acknowledge is a software convention used to indicate successful data transfers.
  The transmitter device will release the bus after transmitting eight bits.
  (When inputting the slave address in the write or read operation, transmitter is μ-COM. When outputting the data in the read operation, it is this device.)
- During the ninth clock cycle, the receiver will pull the SDA line LOW to Acknowledge that the eight bits of data has been received.
  (When inputting the slave address in the write or read operation, receiver is this device. When outputting the data in the read operation, it is μ-COM.)
- The device will respond with an Acknowledge after recognition of a START condition and its slave address (8bit).
- In the WRITE mode, the device will respond with an Acknowledge, after the receipt of each subsequent 8-bit word (word address and write data).
- In the READ mode, the device will transmit eight bit of data, release the SDA line, and monitor the line for an Acknowledge.
- If an Acknowledge is detected, and no STOP condition is generated by the master, the device will continue to transmit the data. If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode. (See Fig.7 ACKNOWLEDGE RESPONSE FROM RECEIVER)

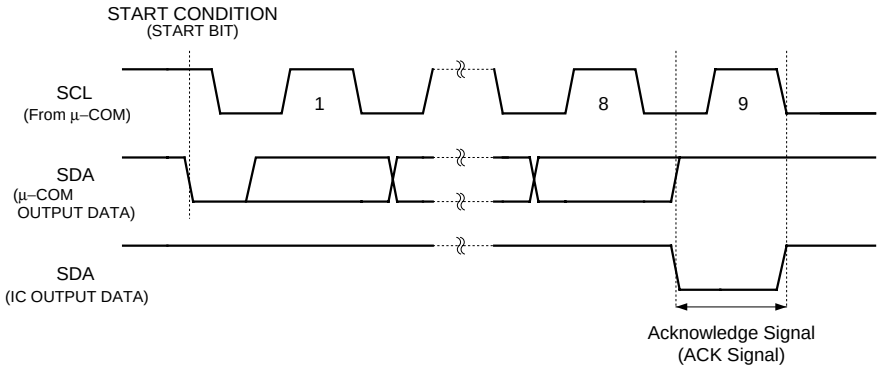


Fig.7 ACKNOWLEDGE RESPONSE FROM RECEIVER

●**Byte write**

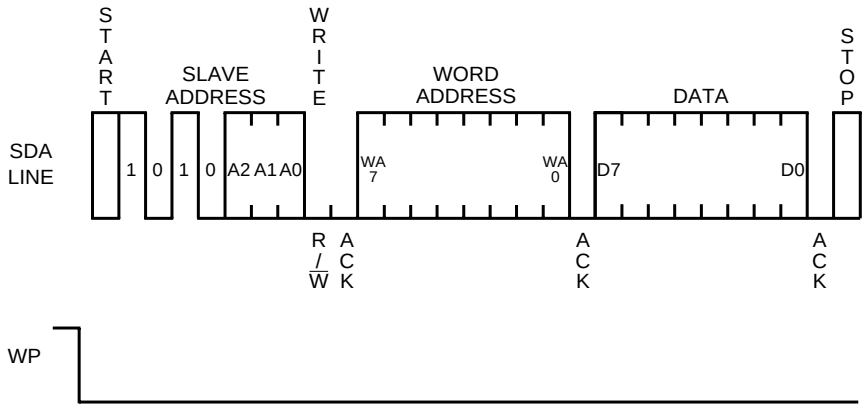


Fig.8 BYTE WRITE CYCLE TIMING

- By using this command, the data is programmed into the indicated word address.
- When the master generates a STOP condition, the device begins the internal write cycle to the nonvolatile memory array.

●**Page write**

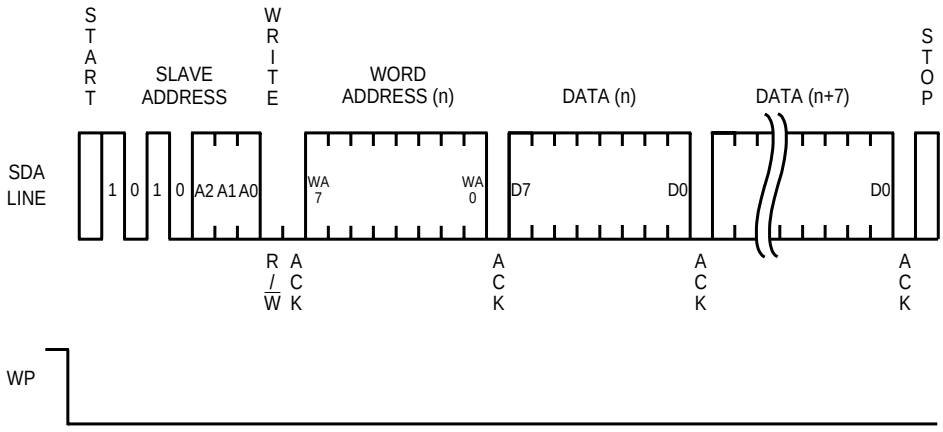


Fig.9 PAGE WRITE CYCLE TIMING

- This device is capable of eight byte page write operation.
- When two or more byte data are inputted, the three low order address bits are internally incremented by one after the receipt of each word. The five higher order bits of the address (WA7 to WA3) remain constant.
- If the master transmits more than eight words, prior to generating the STOP condition, the address counter will "roll over", and the previous transmitted data will be overwritten.

●Current read

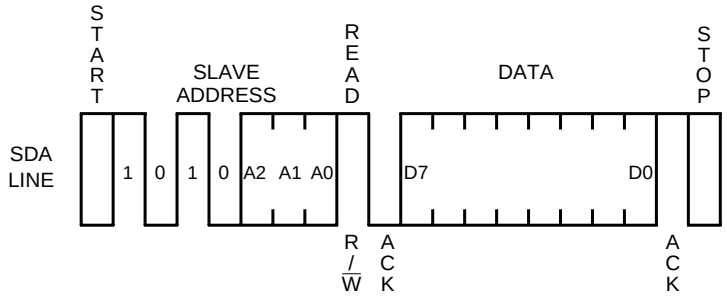


Fig.10 CURRENT READ CYCLE TIMING

- In case that the previous operation is Random or Current Read (which includes Sequential Read respectively), the internal address counter is increased by one from the last accessed address (n).
  Thus Current Read outputs the data of the next word address (n+1).
  If the last command is Byte or Page Write, the internal address counter stays at the last address (n).
  Thus Current Read outputs the data of the word address (n).
- If an Acknowledge is detected, and no STOP condition is generated by the master (μ-COM), the device will continue to transmit the data. [It can transmit all data (2kbit 256word)]
- If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode.

Note) If an Acknowledge is detected with “Low” level, not “High” level, command will become Sequential Read.
So the device transmits the next data, Read is not terminated. In the case of terminating Read, input Acknowledge with “High” always, then input stop condition.

●Random read

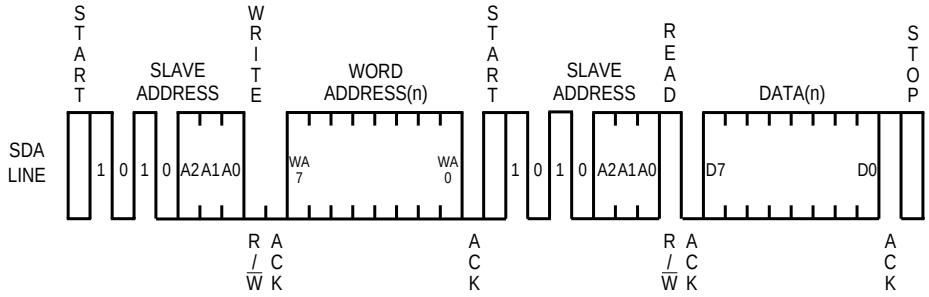


Fig.11 RANDOM READ CYCLE TIMING

- Random read operation allows the master to access any memory location indicated word address.
- If an Acknowledge is detected, and no STOP condition is generated by the master (μ-COM), the device will continue to transmit the data. [It can transmit all data (2kbit 256word)]
- If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode.

Note) If an Acknowledge is detected with “Low” level, not “High” level, command will become Sequential Read.
So the device transmits the next data, Read is not terminated. In the case of terminating Read, input Acknowledge with “High” always, then input stop condition.

● **Sequential read**

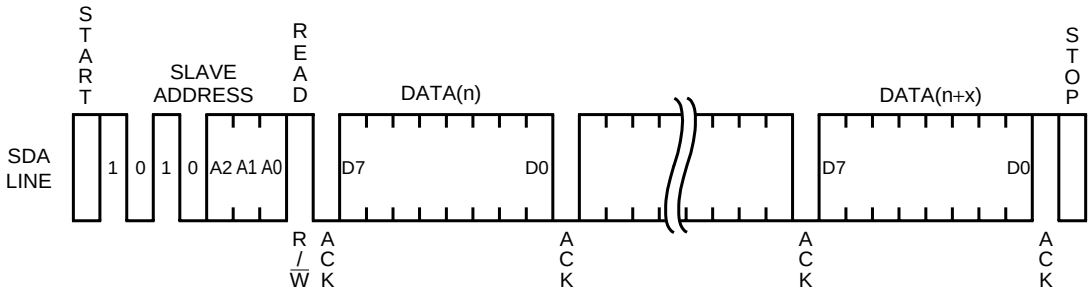


Fig.12 SEQUENTIAL READ CYCLE TIMING
(Current Read)

- If an Acknowledge is detected, and no STOP condition is generated by the master (μ-COM), the device will continue to transmit the data. [It can transmit all data (2kbit 256word)]
- If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode.
- The Sequential Read operation can be performed with both Current Read and Random Read.

Note) If an Acknowledge is detected with “Low” level, not “High” level, command will become Sequential Read. So the device transmits the next data, Read is not terminated. In the case of terminating Read, input Acknowledge with “High” always, then input stop condition.

● **Application**

1) WP effective timing

WP is fixed to “H” or “L” usually. But in case of controlling WP to cancel the write command, please pay attention to [WP effective timing] as follows.

During write command input, write command is canceled by controlling WP “H” within the WP cancellation effective period.

The period from the start condition to the rising edge of the clock which take in D0 of the data (the first byte of the data for Page Write) is the cancellation invalid period. WP input is don’t care during the period. Setup time for rising edge for the SCL which takes in D0 must be more than 100ns.

The period from the rising edge of SCL which takes in D0 to the end of internal write cycle (t_{WR}) is the cancellation effective period. In case of setting WP to “H” during t_{WR}, WRITE operation is stopped in the middle and the data of accessing address is not guaranteed, so that write correct data again please.

It is not necessary waiting t_{WR} (5msmax.) after stopping command by WP, because the device is stand by state.

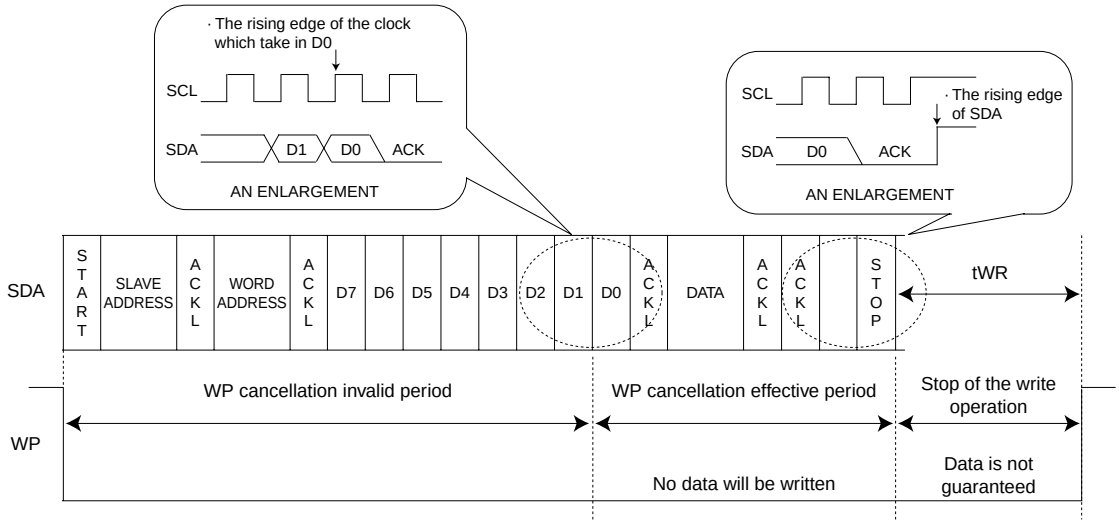


Fig.13 WP EFFECTIVE TIMING

2) Software reset

Please execute software reset in case that the device is an unexpected state after power up and / or the command input need to be reset.

There are some kinds of software reset. Here we show three types of example as follows.

During dummy clock, please release SDA bus (tied to V_{CC} by pull up resistor).

During that time, the device may pull the SDA line LOW for Acknowledge or outputting or read data.

If the master controls the SDA line HIGH, it will conflict with the device output LOW then it makes a current overload.

It may cause instantaneous power down and may damage the device.

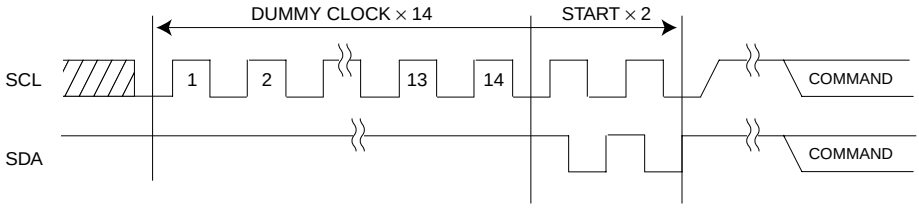


Fig.14-(a) DUMMY CLOCK × 14 + START + START

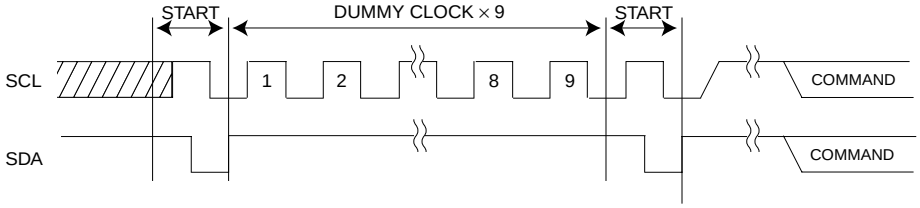


Fig.14-(b) START+ DUMMY CLOCK × 9 + START

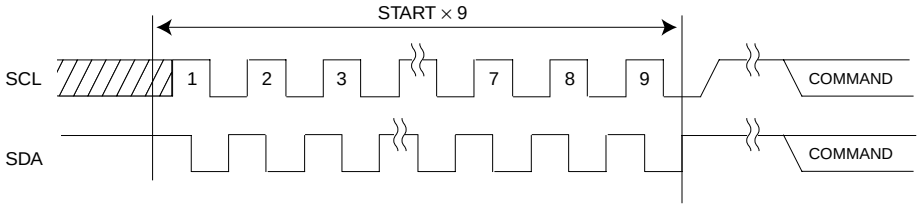


Fig.14-(c) START × 9

∗ COMMAND starts with start condition.

3) Acknowledge polling

Since the device ignore all input commands during the internal write cycle, no ACK will be returned.
When the master send the next command after the wire command, if the device returns the ACK, it means that the program is completed. If no ACK id returned, it means that the device is still busy.
By using Acknowledge polling, the waiting time is minimized less than t_{WR}=5ms.
In case of operating Write or Current Read right after Write, first, send the slave address (R / $\overline{W}$ is "HIGH" or "LOW" respectively). After the device returns the ACK, continue word address input or data output respectively.

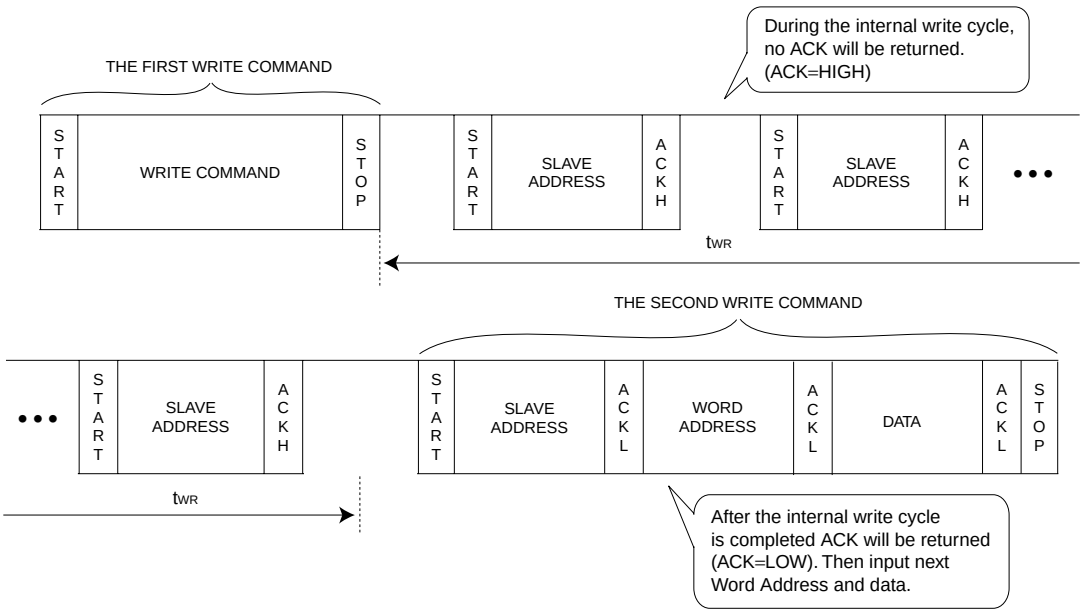


Fig.15 SUCCESSIVE WRITE OPERATION BY ACKNOWLEDGE POLLING

4) Command cancellation by start and stop condition

During a command input, it is canceled by the successive inputs of start condition and stop condition. (Fig.4)
But during ACK or data output, the device may output the SDA line LOW. In such cases, operation of start and stop condition is impossible, so that the reset can't work. Execute the software reset in the cases. (See Page14)
Operating the command cancel by start and stop condition during the command of Random Read or Sequential Read or Current Read, internal address counter is not confirmed.
Therefore operation of Current Read after this in not valid. Operate a Random Read in this case.

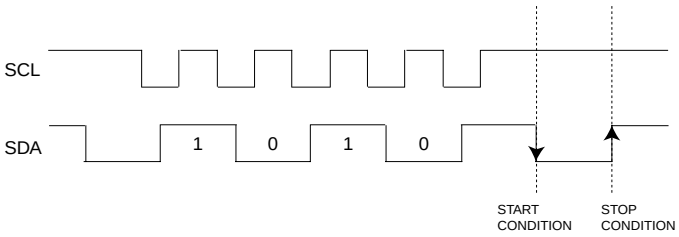
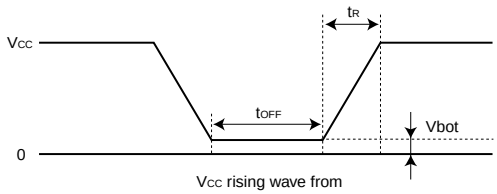


Fig.16 COMMAND CANCELLATION BY START AND STOP CONDITION DURING THE INPUT OF SLAVE ADDRESS

5) Notes for power supply

Vcc rises through the low voltage region in which internal circuit of IC and the controller are unstable, so that device may not work properly due to an incomplete reset of internal circuit.
To prevent this, the device has the feature of P.O.R. and LVcc.
In the case of power up, keep the following conditions to ensure functions of P.O.R and LVcc.

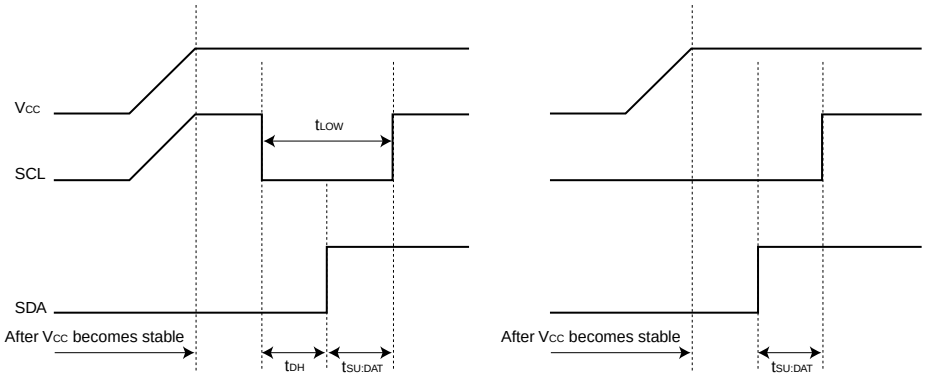
(1) It is necessary to be "SDA=H" and "SCL='L' or 'H' ".
(2) Follow the recommended conditions of tR, tOFF, Vbot for the function of P.O.R. durning power up.



Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

(3) Prevent SDA and SCL from being "Hi-Z".
In case that condition 1. and / or 2. cannot be met, take following actions.
A) Unable to keep condition 1. (SDA is "LOW" during power up.)
→Control SDA, SCL to be "HIGH" as figure below.



a) SCL="H" and SDA="L"

b) SCL="L" and SDA="L"

B) Unable to keep condition 2.
→After power becomes stable, execute software reset. (See page14)

C) Unable to keep condition 1 and 2.
→Follow the instruction A first, then the instruction B.

• LVCC circuit

LVCC circuit inhibit write operation at low voltage, and prevent an inadvertent write. Below the LVCC voltage (Typ.=1.2V), write operation is inhibited.

6) I / O circuit

• Pull up resister of SDA pin

The pull up resister is needed because SDA is NMOS open drain. Decide the value of this resister (R_{PU}) properly, by considering V_{IL}, I_L characteristics of a controller which control the device and V_{OH}, I_{OL} characteristics of the device. If large R_{PU} is chosen, clock frequency need to be slow. In case of small R_{PU}, the operating current increases.

• Maximum of R_{PU}

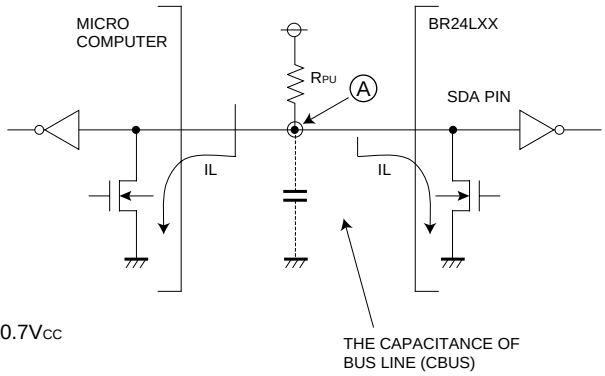
Maximum of R_{PU} is determined by following factor.

① SDA rise time determined by R_{PU} and the capacitance of bus line (CBUS) must be less than T_R.
And the other timing must keep the conditions of AC spec.

② When SDA bus is HIGH, the voltage (A) of SDA bus determined by a total input leak (I_L) of the all devices connected to the bus and R_{PU} must be enough higher than input HIGH level of a controller and the device, including noise margin 0.2 V_{CC}.

$$V_{CC} - I_L R_{PU} - 0.2V_{CC} \geq V_{IH}$$

$$\therefore\ R_{PU} \leq \frac{0.8V_{CC} - V_{IH}}{I_L}$$



Examples : When V_{CC}=3V I_L=10μA V_{IH}=0.7V_{CC}

According to ②

$$R_{PU} \leq \frac{0.8\times3-0.7\times3}{10\times10^{-6}}$$

$$\leq 300\ [k\Omega]$$

- The minimum value R_{PU}

The minimum value of R_{PU} is determined by following factors.

① Meet the condition that V_{OLMAX}=0.4V, I_{OLMAX}=3mA when the device output low on SDA line.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leq I_{OL}$$

$$\therefore R_{PU} \geq \frac{V_{CC} - V_{OL}}{I_{OL}}$$

② V_{OLMAX} (=0.4V) must be lower than the input LOW level of the controller and the EEPROM including recommended noise margin (0.1 V_{CC}).

$$V_{OLMAX} \leq V_{IL} - 0.1V_{CC}$$

Examples : V_{CC}=3V, V_{OL}=0.4V, I_{OL}=3mA, the V_{IL} of the controller and the EEPROM is V_{IL}=0.3V_{CC}

According to ① $R_{PU} \geq \frac{3-0.4}{3\times10^{-3}}$

≥ 867 [Ω]

and V_{OL}=0.4[V]
V_{IL} =0.3×3
=0.9[V]

so that condition ② is met

- Pull up resister of SCL pin

In the case that SCL is controlled by CMOS output, the pull up resister of SCL is not needed.
But in the case that there is a timing at which SCL is Hi-Z, connect SCL to V_{CC} with pull up resister.
Several ~ several dozen kΩ is recommended as a pull up resister, which is considered with the driving ability of the output port of the controller.

7) Connections of A0, A1, A2, WP pin

- Connections of device address pin (A0, A1, A2)

The state of device address PIN are compared with the device address send by the master, then one of the devices which are connected to the identical bus is selected. Pull up or down these pins, or connect them to V_{CC} or GND.
Pins which is not used as device address (N.C. PIN) may be either HIGH, LOW, and Hi-Z.

The type of the device which have N.C. PIN	BR24L16 / F / FJ / FV / FVM-W	A0, A1, A2
	BR24L08 / F / FJ / FV / FVM-W	A0, A1
	BR24L04 / F / FJ / FV / FVM-W	A0

- Connections of WP pin

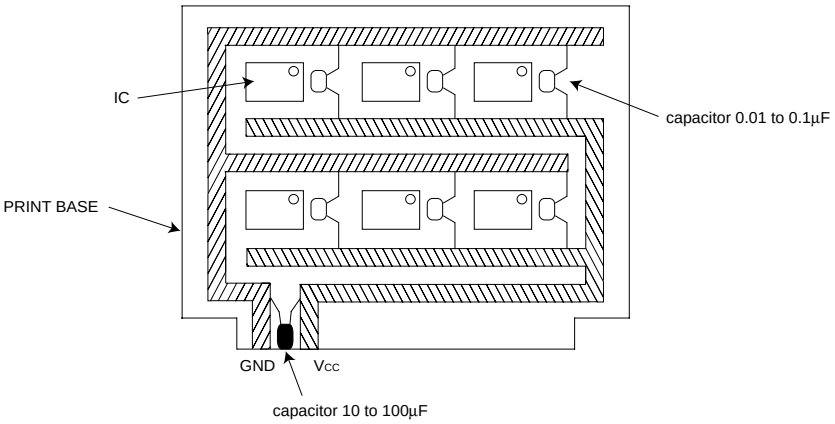
The WP input allows or inhibits write operations. When WP is HIGH, only READ is available and WRITE to any address is inhibited. Both Read and Write are available when WP is LOW.
In the case that the device is used as a ROM, it is recommended that WP is pulled up or connected to V_{CC}.
In the case that both READ and WRITE are operated, WP pin must be pulled down or connected to GND or controlled.

8) Notes for noise on V_{CC}

- About bypass capacitor

  Noise and surges on power line may cause the abnormal function. It is recommended that the bypass capacitors (0.1µF) are attached on the V_{CC} and GND line beside the device.

  The attachment of bypass capacitors on the board near by connector is also recommended.

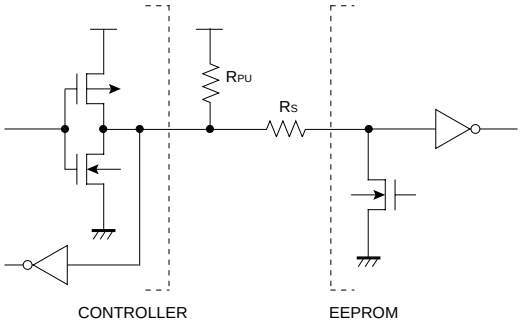


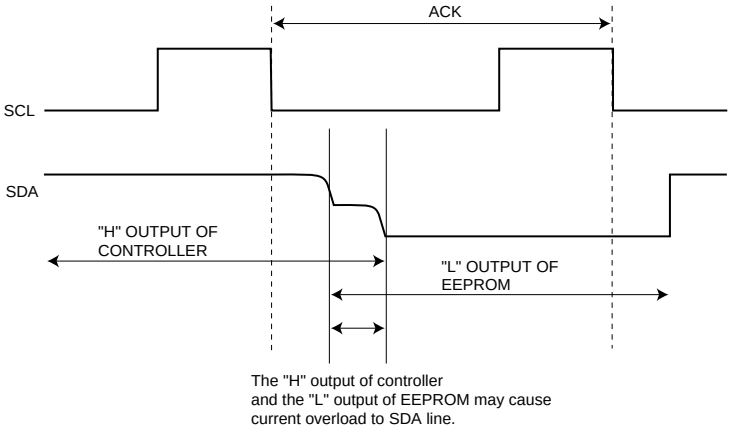
9) The notice about the connection of controller

- About R_S

  The open drain interface is recommended for SDA port in I^2CBUS. But, in the case that Tri-state CMOS interface is applied to SDA, insert a series resister R_S between SDA pin of the device and a pull up resister R_{PU}. It limits the current from PMOS of controller to NMOS of EEPROM.

  R_S also protects SDA pin from surges. Therefore, R_S is able to be used though SDA port is open drain.





The "H" output of controller
and the "L" output of EEPROM may cause
current overload to SDA line.

• The maximum value of R_S

The maximum value of R_S is determined by following factors.

① SDA rise time determined by R_{PU} and the capacitance of bus line (CBUS) of SDA must be less than t_R. And the other timing must also keep the conditions of the AC timing.

② When the device outputs LOW on SDA line, the voltage of the bus Ⓐ determined by R_{PU} and R_S must be lower than the inputs LOW level of the controller, including recommended noise margin ($0.1V_{CC}$).

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leq V_{IL}$$

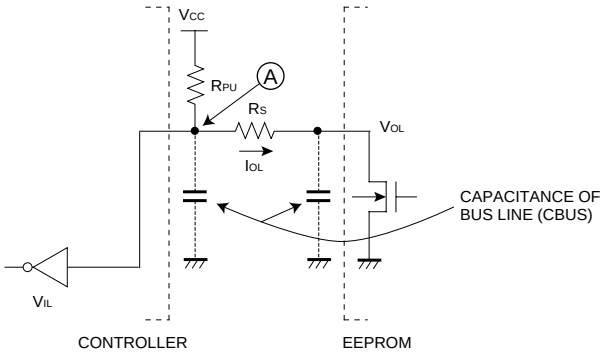
$$\therefore\ R_S \leq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Examples : when V_{CC}=3V, V_{IL}=0.3V_{CC}, V_{OL}=0.4V, R_{PU}=20kΩ

According to ②

$$R_S \leq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leq 1.67\ [k\Omega]$$



• The minimum value of R_S

The minimum value of R_S is determined by the current overload due to the conflict on the bus.

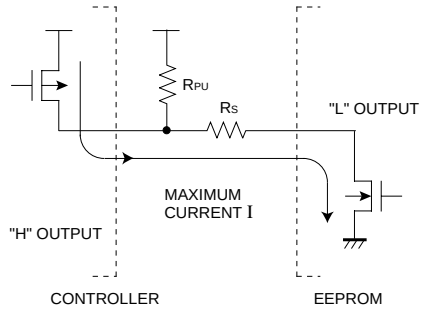
The current overload may cause noise on the power line and instantaneous power down.

The following conditions must be met, where I is the maximum permissible current.

The maximum permissible current depends on V_{CC} line impedance and so on. It need to be less than 10mA for EEPROM.

$$\frac{V_{CC}}{R_S} \leq I$$

$$\therefore\ R_S \geq \frac{V_{CC}}{I}$$



Examples : When V_{CC}=3V, I=10mA

$$R_S \geq \frac{3}{10\times10^{-3}}$$

$$\geq 300\ [\Omega]$$

10) The special character DATA

The following characteristic data are typ value.

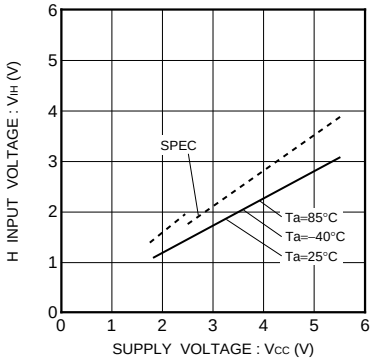


Fig.17 High input voltage V_{IH} (A0,A1,A2,SCL,SDA,WP)

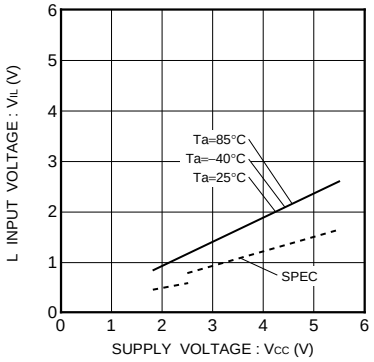


Fig.18 Low input voltage V_{IL} (A0,A1,A2,SCL,SDA,WP)

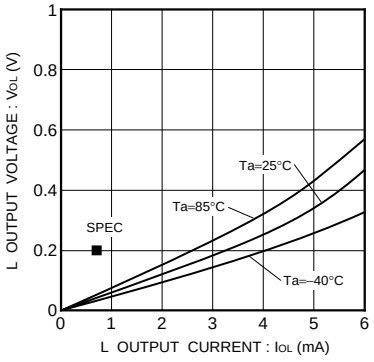


Fig.19 Low output voltage V_{OL}–I_{OL} (V_{CC}=1.8V)

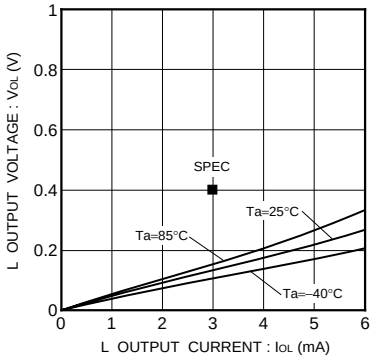


Fig.20 Low output voltage V_{OL}–I_{OL} (V_{CC}=2.5V)

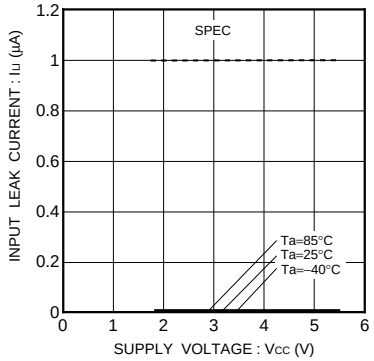


Fig.21 Input leakage current I_{LI} (A0,A1,A2,SCL,WP)

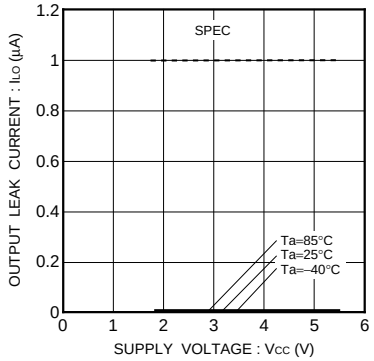


Fig.22 Output leakage current I_{LO}(SDA)

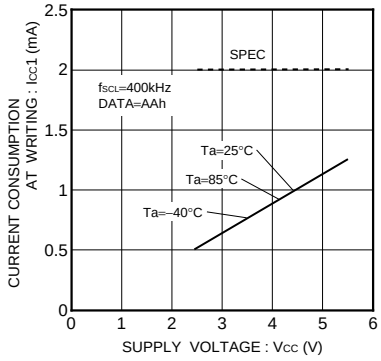


Fig.23 Write operating current I_{CC1} (f_{SCL}=400kHz)

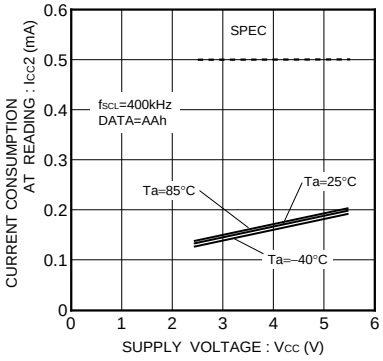


Fig.24 Read operating current I_{CC2} (f_{SCL}=400kHz)

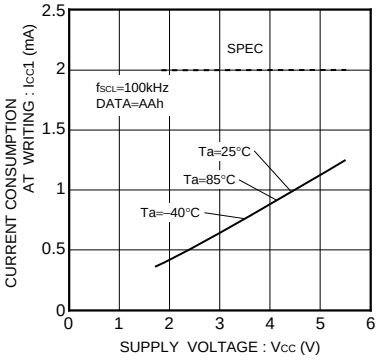


Fig.25 Write operating current I_{CC1} (f_{SCL}=100kHz)

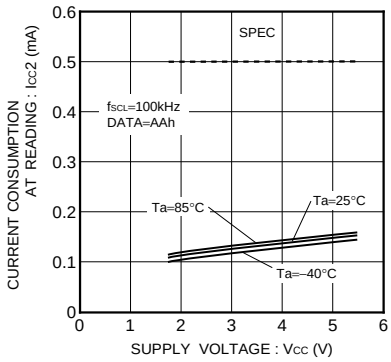


Fig.26 Read operating current
$I_{CC}2$ (f_{SCL}=100kHz)

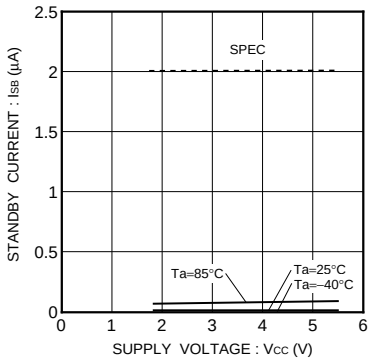


Fig.27 Standby current I_{SB}

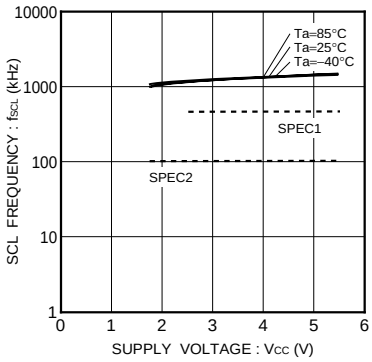


Fig.28 Clock frequency f_{SCL}

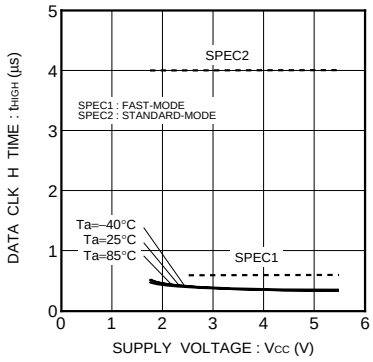


Fig.29 Data clock "H" period t_{HIGH}

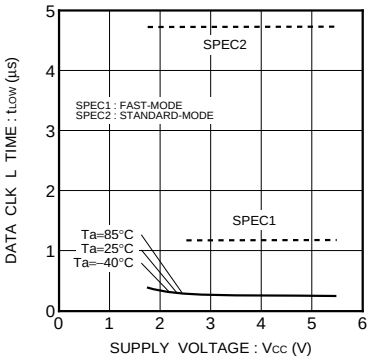


Fig.30 Data clock "L" period t_{LOW}

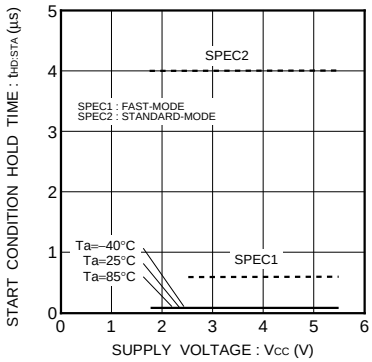


Fig.31 Start condition hold time
$t_{HD:STA}$

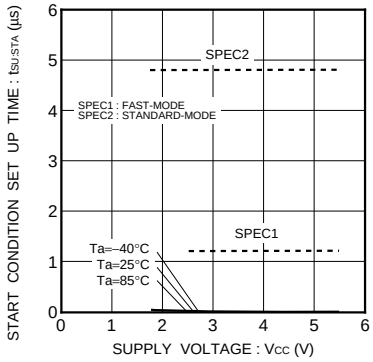


Fig.32 Start condition setup time
$t_{SU:STA}$

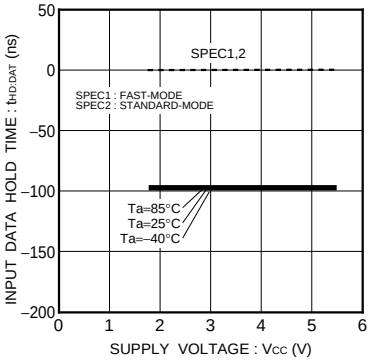


Fig.33 Input data hold time
$t_{HD:DAT}$(HIGH)

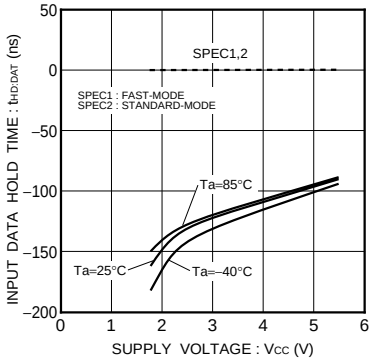


Fig.34 Input data hold time
$t_{HD:DAT}$(LOW)

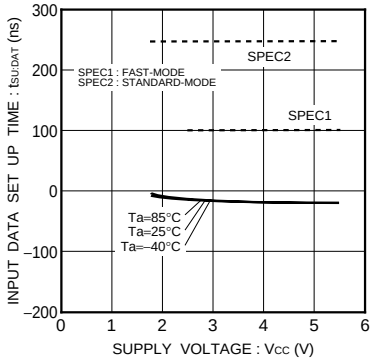


Fig.35 Input data setup time $t_{SU:DAT}$(HIGH)

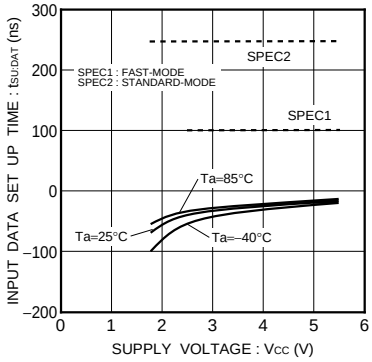


Fig.36 Input data setup time $t_{SU:DAT}$(LOW)

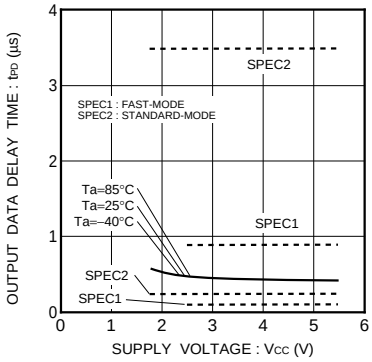


Fig.37 Output data delay time $t_{PD}0$

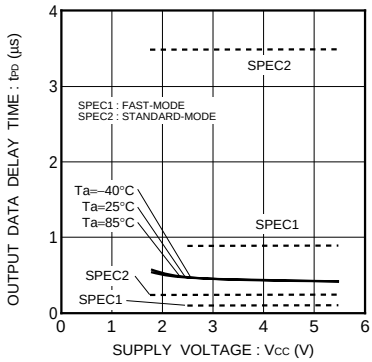


Fig.38 Output data delay time $t_{PD}1$

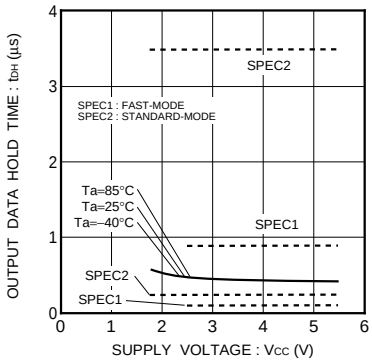


Fig.39 Output data hold time $t_{DH}0$

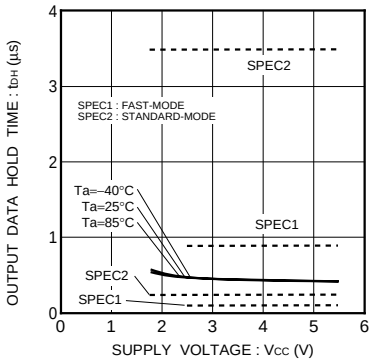


Fig.40 Output data hold time $t_{DH}1$

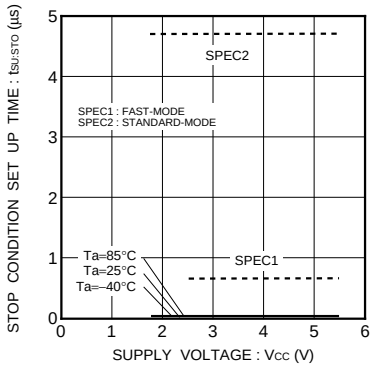


Fig.41 Stop condition setup time $t_{SU:STO}$

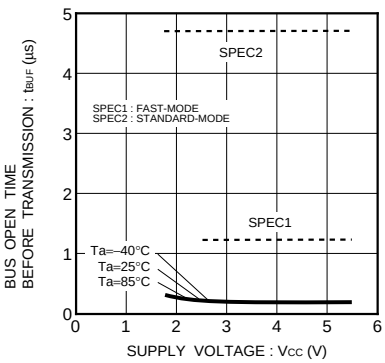


Fig.42 BUS free time t_{BUF}

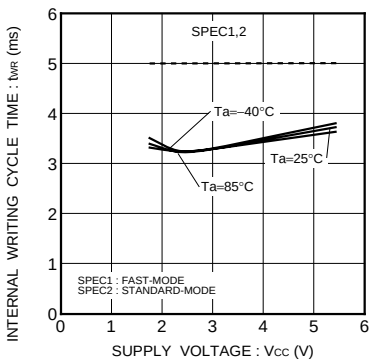


Fig.43 Write cycle time t_{WR}

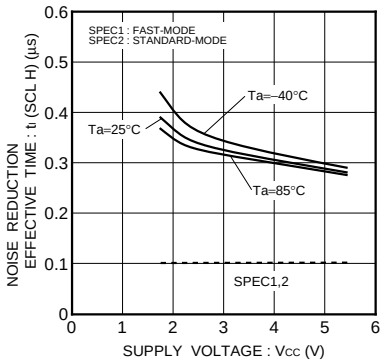


Fig.44 Noise spike width
tl (SCL H)

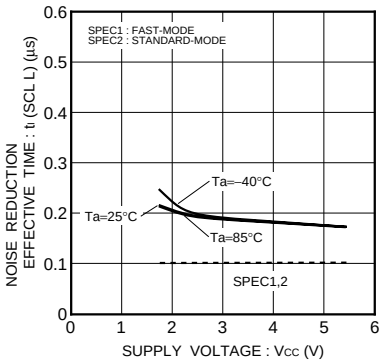


Fig.45 Noise spike width
tl (SCL L)

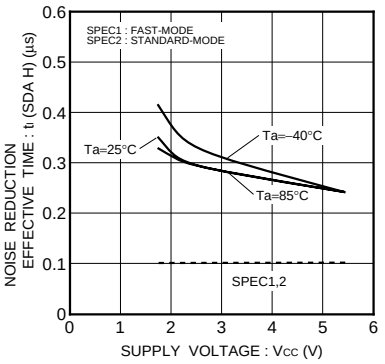


Fig.46 Noise spike width
tl (SDA H)

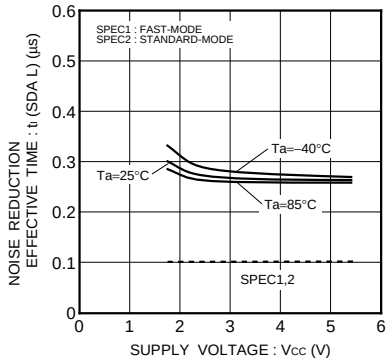


Fig.47 Noise spike width
tl (SDA L)

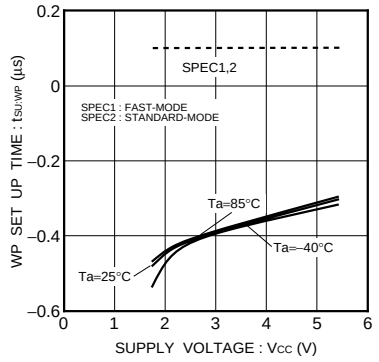


Fig.48 WP setup time $t_{SU:WP}$

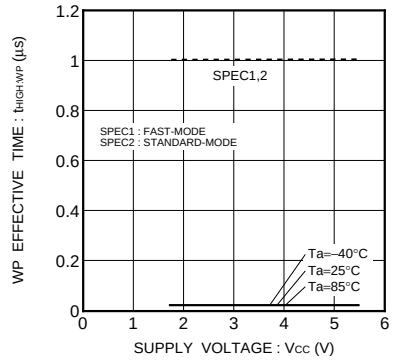


Fig.49 WP high period $t_{HIGH:WP}$

Notes

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