AK8855
NTSC/PAL Digital Video Decoder

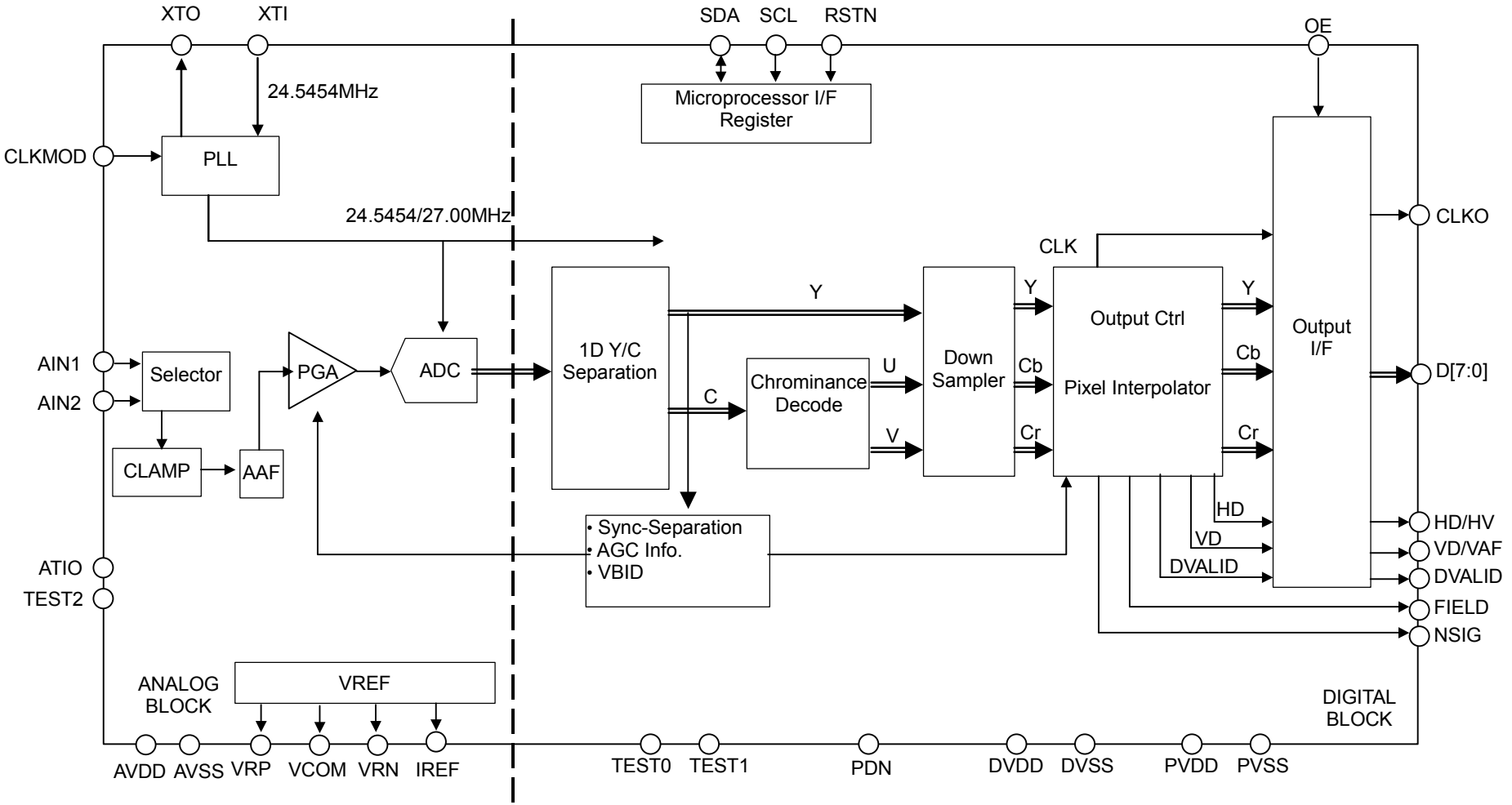
General Description

The AK8855 decodes the NTSC, PAL Composite Video signal into Digital code.
Outputs are ITU-R BT. 601 Level compatible Y, Cb and Cr signals.
Decoded results are scaled to QVGA/CIF sizes etc..
Output interface is camera-interface in ITU-R BT.656-alike output format.
When such information as Closed Caption, VBID, WSS are encoded on the Video signal, each code can be read
out externally.
When the Macrovision signal is super-imposed, its information can also externally be read out.

Features

- NTSC-M / PAL- B, D, G, H, I Composite signal decoding process
- 2-CH input acceptable (selector is integrated on-chip)
- On-chip 10 Bit ADC (operation at 24.5454 MHz or 27 MHz)
- Fixed clock Sampling
- On-chip PLL (27 MHz clock generation from 24.5454 MHz)
- On-chip Quartz Crystal Oscillator circuit
- Pixel Position Correction function
- Selectable Picture sizes (QVGA / VGA / QCIF / CIF / 601)
  - Rotated Picture Mode output available (ex. QVGA : 240 X 180)
- Selectable Output rate
  (525 : 30 / 15 / 7.5 625 : 25 / 12.5 / 6.25 [frames / sec])
- On-chip Anti-Aliasing Filter
- On-chip PGA (0 dB ~ 12 dB)
- Auto Color Control (ACC) function
- Adaptive Auto Gain Control (AGC) function
- Primary YC Separation
- Output Interface
  - ITU-R BT.656-alike output format (4:2:2 8 Bit parallel output with EAV / SAV) *
  * depending on the input signal quality, ITU-R BT. 656 compatible output may not be available.
  - Camera Interface
  - Interface by HD / VD / DVALID signals
- Closed Caption decoding function (to be output by register setting)
- VBID (CGMS-A) decoding function (CRCC decode)
  (to be output by register setting)
- WSS decoding function (to be output by register setting)
- Macrovision signal detect function
- Power-down function
- I2C Control compatible
- Internal operating power supply 2.7 V ~ 3.3 V
- supplying I / F Power Supply (1.6 V ~ 2.0 V or 2.7 V ~ 3.3 V)
- Package 57 FBGA

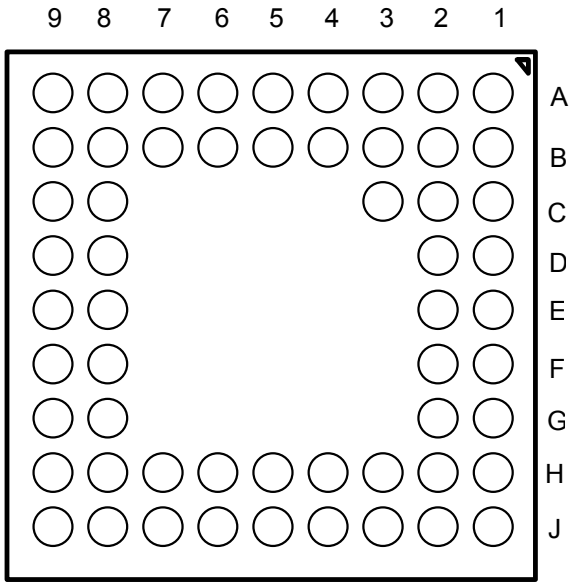
Total Functional Block Diagram



Ordering Guide

AK8855VG 57 pin FBGA

Pin Layout Drawing



Bottom View

	1	2	3	4	5	6	7	8	9
A	NC	VRN	VRP	ATIO	XTI	XTO	DVDD	FIELD	NC
B	VCOM	IREF	TEST2	BVSS	CLKMOD	DVSS	BVSS	NSIG	DVALID
C	AIN1	AVSS	NC					HD	VD
D	AVDD	BVSS						PVSS	PVDD
E	AIN2	DVSS						D1	D0
F	TEST0	DVDD						DVSS	DVDD
G	SCL	TEST1						BVSS	D2
H	SDA	PDN	RSTN	PVSS	DVSS	D5	D4	CLKO	D3
J	NC	OE	PVDD	DVDD	D7	D6	PVDD	PVSS	NC

TOP View

Pin Functional Description

Pin#	Pin Name	I/O	Functional Outline
A5	XTI	I	Quartz crystal resonator connecting pin (to be grounded to Digital ground via a 18 pF capacitor in the recommended circuit). - 24.5454 MHz crystal resonator should be used. - input from 24.5454 MHz crystal oscillator is connected to this pin.
A6	XTO	O	Quartz crystal resonator connecting pin (to be grounded to Digital ground via a 22 pF capacitor in the recommended circuit). - 24.5454 MHz crystal resonator should be used. - This pin outputs DVSS level at PDN = L. - when a crystal resonator is not used, this pin is left open (NC) or connected to DVSS.
B5	CLKMOD	I	Clock mode setting pin. Connect to either DVDD or DVSS. DVSS grounding : crystal resonator is used DVDD connection : crystal oscillator is used
J2	OE	I	Output enable pin L : output pins are put into Hi-Z condition H : data is output
H1	SDA	I/O	I2C data pin This pin is pulled-up to PVDD.
G1	SCL	I	I2C clock input pin Input level of lower-than-PVDD should be input.
H3	RSTN	I	Reset signal input pin L : reset H : normal operation Output pin conditions are in Hi-Z when RSTN pin is at low.
H2	PDN	I	power-down control pin L : power-down H : normal operation
H8	CLKO	O	Data clock output pin for output I/ F
J5	D7	O	Data output pin Video decode data is output (MSB) (note)
J6	D6	O	Data output pin (note)
H6	D5	O	Data output pin (note)
H7	D4	O	Data output pin (note)
H9	D3	O	Data output pin (note)
G9	D2	O	Data output pin (note)
E8	D1	O	Data output pin (note)
E9	D0	O	Data output pin (LSB) (note)
C8	HD/HV	O	HD / HV timing signal output pin (note)
C9	VD/VAF	O	VD / VAF timing signal output pin (pin)
B9	DVALID	O	pin to indicate a valid Video interval (note)
A8	FIELD	O	FIELD signal output pin (note)
B8	NSIG	O	to show a status at no signal input condition (note) L : with input signal H : no signal input

C1	AIN1	I	Analog input pin (1)
E1	AIN2	I	Analog input pin (2)
B2	IREF	O	Reference current setting pin Connect this pin to Analog ground via a 4.7 kohm (<= 1 % accuracy) resistor. This pin becomes Hi-Z output at power-down mode.
A2	VRN	O	internal negative reference voltage for AD converter - connect this pin to Analog ground via a 0.1 uF or larger capacitor. - there is a case when this pin becomes Hi-Z output at power-down. - Do not use this as a reference voltage source for external circuit(s).
A3	VRP	O	O internal positive reference voltage for AD converter - connect this pin to Analog ground via a 0.1 uF or larger capacitor. - there is a case when this pin becomes Hi-Z output at power-down. - do not use this as a reference voltage source for external circuit(s).
B1	VCOM	O	internal common voltage for AD converter - connect this pin to Analog ground via a 0.1 uF or larger capacitor. - there is a case when this pin becomes Hi-Z output at power-down. - do not use this as a reference voltage source for external circuit(s).
B6	DVSS	G	ground pin for crystal oscillator circuit
A7	DVDD	P	power supply pin for crystal oscillator circuit
D1	AVDD	P	Analog power supply pin
C2	AVSS	G	Analog ground pin
F2, J4, F9	DVDD	P	Digital power supply pins
E2, H5, F8	DVSS	G	Digital ground pins
D2, G8, B7, B4	BVSS	G	Substrate ground pins Connect those pins to Analog ground.
J3, J7, D9	PVDD	P	power supply pins for interface Interface power supply for CLKO, OE, PDN, RSTN, D [7:0], FIELD, HD, VD, NSIG, DVALID, SDA, SCL
H4, D8, J8	PVSS	G	Ground pins for interface power supply
A4	ATIO	I	Analog test pin Connect this pin to AVDD for normal operation
F1	TEST0	I/O	Test mode setting pin. Connect this pin to DVSS
G2	TEST1	I/O	Test mode setting pin. Connect this pin to DVSS
B3	TEST2	O	connect this pin to AVSS
A1	NC	NC	NC pin to be connected to AVSS
C3	NC	NC	pin to be connected to AVSS (index pin)
J1	NC	NC	pin to be connected to DVSS
J9	NC	NC	pin to be connected to DVSS
A9	NC	NC	pin to be connected to DVSS

I : input pin
O : output pin
I/O : input / output pin
P : power supply pin
G : ground pin
note) the AK8855 starts to output after it is reset.
When no signal is input, Black level data (Y = 0x10, Cb/Cr = 0x80) is output.

Electrical Characteristics

(1) Absolute Maximum Ratings

Parameter	Min	Max	Units	Note
Supply voltage DVDD, AVDD, PVDD	-0.3	4.5	V	
Analog Input pin voltage (VinA)	-0.3	AVDD + 0.3	V	AIN1, AIN2
Clock input voltage (Vckin)	-0.3	DVDD + 0.3	V	XTI
Digital Input pin voltage (VinD)	-0.3	PVDD + 0.3	V	OE, PDN,RSTN, SDA, SCL
Input pin current (Iin)	-10	10	mA	
Storage temperature	-40	125	°C	

Power supply voltages are values where each ground pin (DVSS = AVSS = PVSS) is at 0 V (voltage reference).All power supply ground pins DVSS, AVSS and PVSS should be at same potential.
When to connect to Data bus such digital output pins as CLKO, D[7:0], FIELD, HD, VD, NSIG, DVALID, Data bus operating voltage must be within the input pin voltage range as described above.

(2) Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units	Conditions
Supply voltage * AVDD,DVDD	*2.7*	3.0	3.3	V	AVDD = DVDD
interface power supply PVDD	*1.6*	1.8	2.0	V	
	2.7	3.0	3.3	V	PVDD = DVDD
Operating temperature (Ta)	*-30*		85	°C	

* power supply voltages are values where each ground pin (PVSS = AVSS = PVSS) is at 0 V (voltage reference).All power supply ground pins DVSS, AVSS and PVSS should be at same potential.

(3) DC Characteristics

< operating voltage : DVDD 2.7V~3.3V / PVDD 2.7V~3.3V / PVDD 1.6 V~2.0 V , temperature -30~+85°C >

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Digital input H voltage (VIH)	VIH1	0.7PVDD			V	PVDD = 2.7~3.3V
	VIH2	0.8PVDD				PVDD =1.6~2.0V
	VIH3	0.7DVDD			V	
Digital input L voltage (VIL)	VIL1			0.3PVDD	V	PVDD = 2.7~3.3V
	VIL2			0.2PVDD		PVDD =1.6~2.0V
	VIL3			0.3DVDD	V	
Digital input leak current	IL			+/-10	*u*A	
Digital output H voltage (VOH)	VOH1	2.2			V	*IOH =-1mA* PVDD = 2.7~3.3V
	VOH2	1.3			V	*IOH =-600uA* PVDD = 1.6~2.0V
Digital output L voltage (VOL)	VOL1			0.4	V	IOL = 2m*A* PVDD = 2.7~3.3V
	VOL2			0.4	V	IOL = 1m*A* PVDD =1.6~2.0V
I2C (SDA) L output	VOLC			0.4	V	IOLC = 3mA

note)
Digital output pins refer to CLKO, D[7:0], FIELD, HD/HV, VD/VAF, NSIG and DVALID pin outputs in general term.
Digital inputs which are specified by VIH1, VIH2, VIL1 and VIL2 refer to OE, PDN, RSTN,SCL and SDA pin inputs in general term.
Digital input which is specified by VIH3 and VIL3 means XTI input.
SDA pin output is not included in digital output pin unless otherwise noted.

(4) AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Digital output maximum allowable load capacitance	CL			15	pF	PVDD =1.6~2.0V
				30	pF	PVDD = 2.7~3.3V

(5) Analog Characteristics < AVDD = 3.0 V, temperature 25 °C >

Selector Clamp

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Maximum input range	VIMX			1	V_{PP}	
Clamp level	VYCP		0.9		V	
Clamp current	CLPI		150		uA	

PGA

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Resolution			7		bit	
Minimum gain	GMN		0		dB	
Maximum gain	GMX		12		dB	
Gain step	GST		0.094		dB	

AD Converter

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Resolution	RES		10		bits	
operating clock frequency	FS		24.5454 27		MHz	
Integral non-linearity error	INL		2.0	4.0	LSB	fs = 27MHz
Differential non-linearity error	DNL		1.0	2.0	LSB	fs = 27MHz
S/N	SN		54		dB	fin = 1MHz Ain = -1dB fs = 27MHz
S/(N+D)	SND		51		dB	fin = 1MHz Ain = -1dB fs = 27MHz
ADC internal common voltage	VCOM		1.3		V	
ADC ADC internal positive-side VREF voltage	VRP		1.7		V	
ADC internal negative-side VREF voltage	VRN		0.9		V	

(6) Current consumption < DVDD = AVDD = PVDD = 3.0 V, Ta = -30 ~ +85°C >

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Operating power supply current						note1)
Total			66	86	mA	When an external clock source is input
Analog part power supply (AVDD)	Idda		24		mA	
Digital part power supply (DVDD)	Iddd		28		mA	When an external clock source is input
			(30)		mA	(when a crystal resonator is connected)
Interface part power supply (PVDD)	Iddp		14		mA	CL = 30pF
Power-down current						
Total power-down current			1	100	uA	
Analog part power supply (AVDD)			≦ 1		uA	
Digital part power supply (DVDD)			≦ 1		uA	
Interface part power supply (PVDD)			≦ 1		uA	note2),note3)

note 1) when to decode color bar signal during 601 output mode (internal system clock at 27 MHz operation).
note 2) output bus potential of data output pin is fixed at PVDD when to measure power-down current. Input level of digital input pins (PDN, RSTN, OE) and input level of I2C pins (SCLK, SDA) are fixed to either PVSS or PVDD.
note 3) set digital output pins to PVDD potential, or set OE pin high in power-down setting mode.

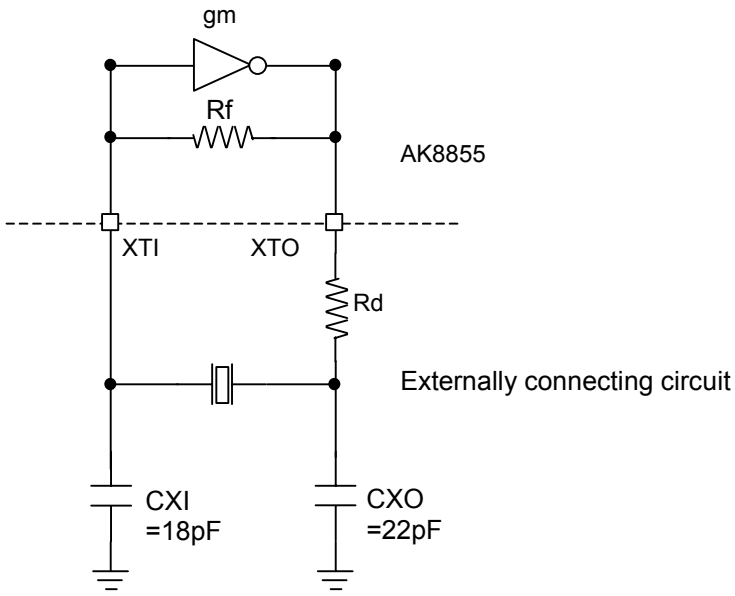
(7) Quartz Crystal Oscillator circuit

Quartz crystal resonator and externally connecting load capacitance

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Oscillating frequency	f0		24.5454		[MHz]	
Frequency accuracy	delta f / f			+/-100	[ppm]	
load capacitance	CL		15		[pF]	
effective equivalent resistance	Re			100	[Ω]	note1)
Parallel capacitance	C0			0.85	[pF]	
XTI pin externally connecting load capacitance	CXI		18		[pF]	
XTLO pin externally connecting load capacitance	CXO		22		[pF]	

note 1) effective equivalent resistance is generally given as :
Re = R1 x (1 + CO / CL) square
Where R1 : serial equivalent resistance of crystal resonator
CO : parallel capacitance of crystal resonator

Circuit connection example

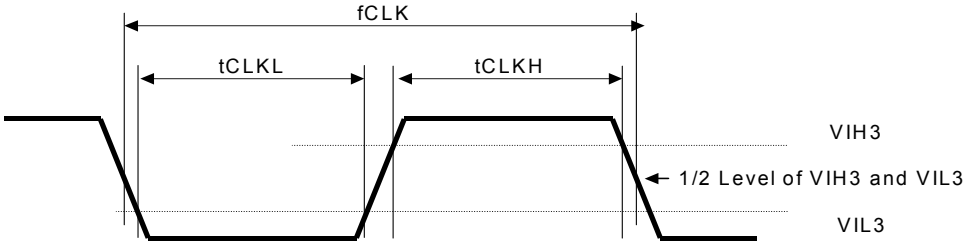


Note) Rd : as for the necessity of limiting resistor and its value, refer to the quartz crystal resonator specification which is to be used.

AC Timing

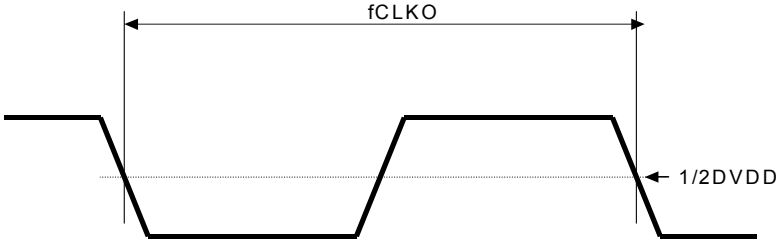
(DVDD 2.7 V ~ 3.3 V / PVDD 1.6 V ~ 2.0 V or PVDD 2.7 V ~ 3.3 V, Ta at –30 ~ +85 °C)
loading condition : CL = 30 pF (at 3.0 V I / F)
CL = 15 pF (at 1.8 V I / F)

(1) Clock Input (XTI input)



Parameter	Symbol	Min.	Typ.	Max	Unit
CLK	fCLK		24.5454		MHz
CLK duty ratio	pCLKD	40		60	%
Frequency stability				+/-100	ppm

(2) CLKO Output

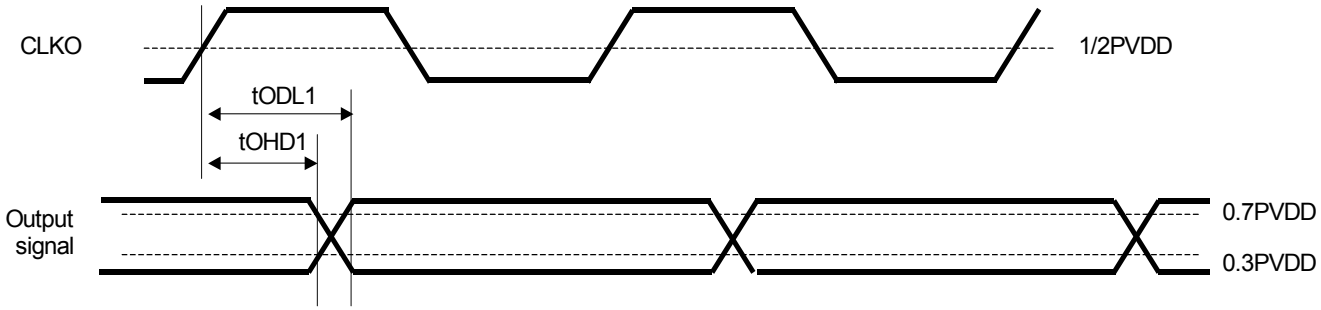


Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions
CLKO	fCLKO		6.75		MHz	QCIF
			12.2727			QVGA / Rotated QVGA / Rotated CIF
			13.5			CIF(PAL)
			24.5454			VGA
			27			CIF(NTSC)/601

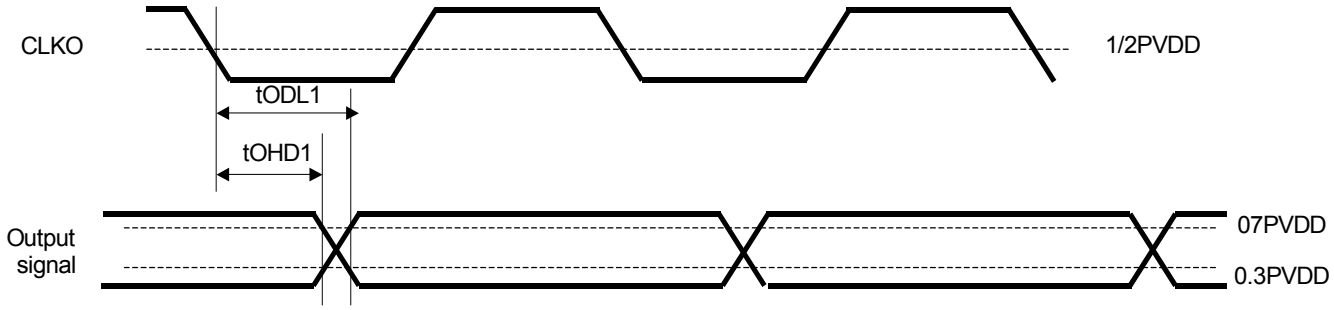
(3) Output Data Timing

(3-1) All digital output signals except for NSIG output (VGA / 601 / CIF (NTSC))

CLKINV-bit = 0 (by register setting)



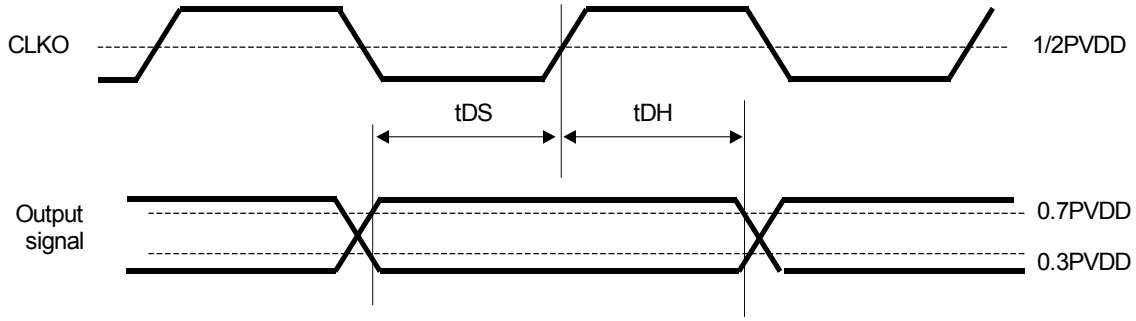
CLKINV-bit = High (by register setting)



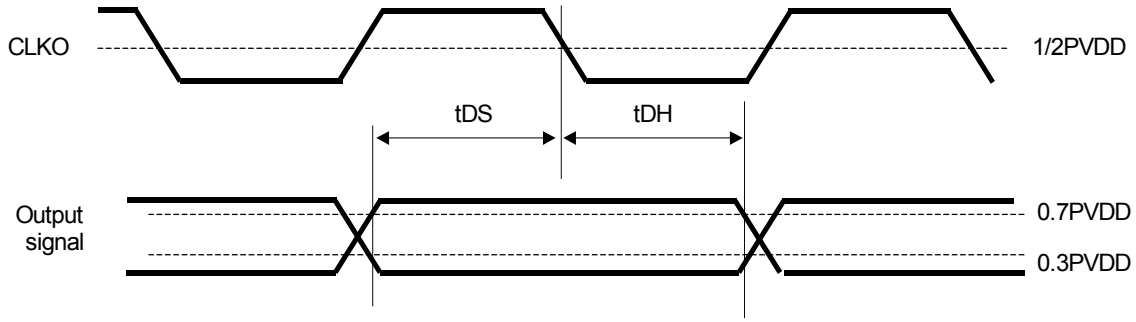
Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions
Output Data Delay Time	tODL1			28	nsec	
Output Data Hold Time	tOHD1	3				

(3-2) All output signals except for NSIG output (QVGA / QCIF / CIF (PAL) / Rotated QVGA / Rotated CIF)

CLKINV-bit = 0 (by register setting)

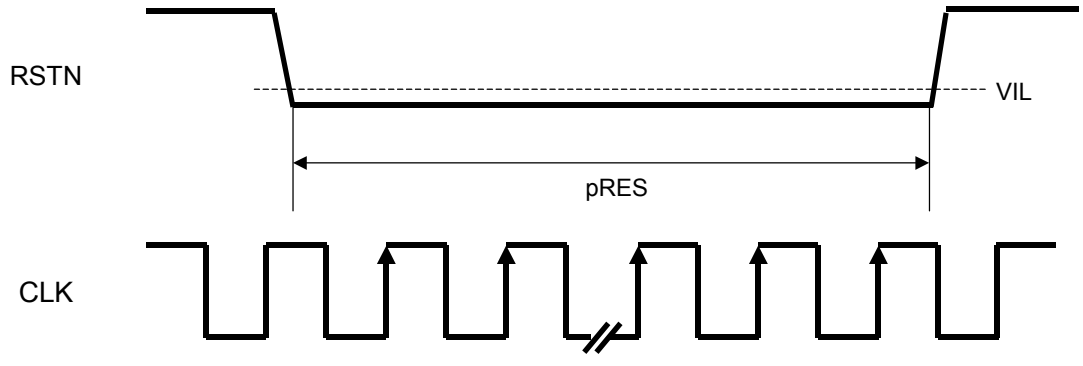


CLKINV-bit = 1 (by register setting)



Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions
Output Data Setup Time	tDS	8			nsec	
Output Data Hold Time	tDH	8			nsec	

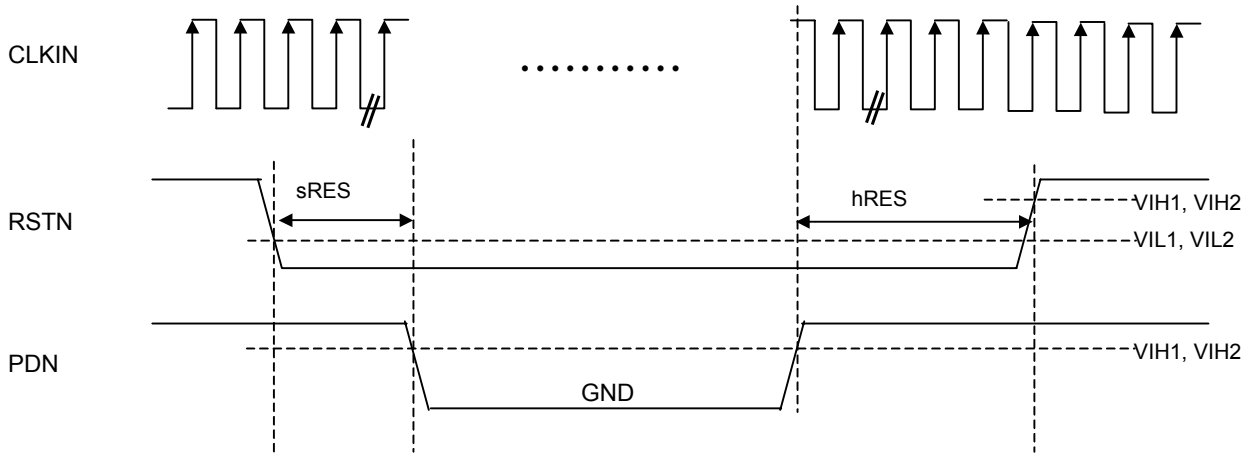
(4) Reset Timing



Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions
RSTN pulse width	pRES	100			CLK	Rising Clock Edge

note)
Clock input is required for reset. Set RSTN pin to low after clock is fed.
Output pins are in Hi-Z condition during RSTN pin at low.
After reset is finished, decoded result is output if OE pin is at high (Black level is output if no input is fed).

(5) Power-down Sequence , Reset Sequence after the power-down release
Activate reset for longer-than-512 clock time before setting PDN (PDN to low).
Activate reset after the PDN release (PDN to high).

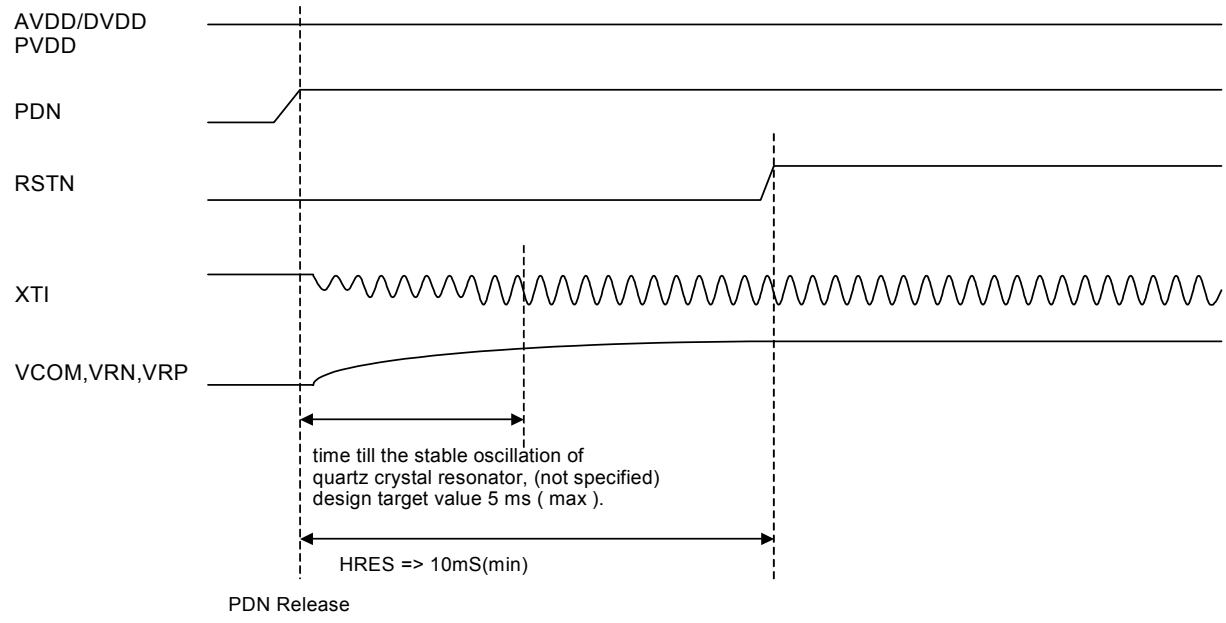


Parameter	Symbol	Min.	Typ.	Max	Unit
RSTN pulse width	sRES	512			SYSCLK
time from PDN to high to RSTN to high	hRES	10			msec

At power-down, all control signals must be surely connected to either the selected power supply or ground level, and not to ViH / ViL levels.
When to turn off power supplies (AVDD / DVDD) other than PVDD, set the device into the power-down condition after executing power-down sequence and then, the power should be turned off.
It is recommended to set all digital output pins to PVDD potential or set OE pin high, in power-down mode setting.

note) clock input is required for reset operation. During reset sequence, output pins become Hi-Z condition (it does not depend on OE pin state).

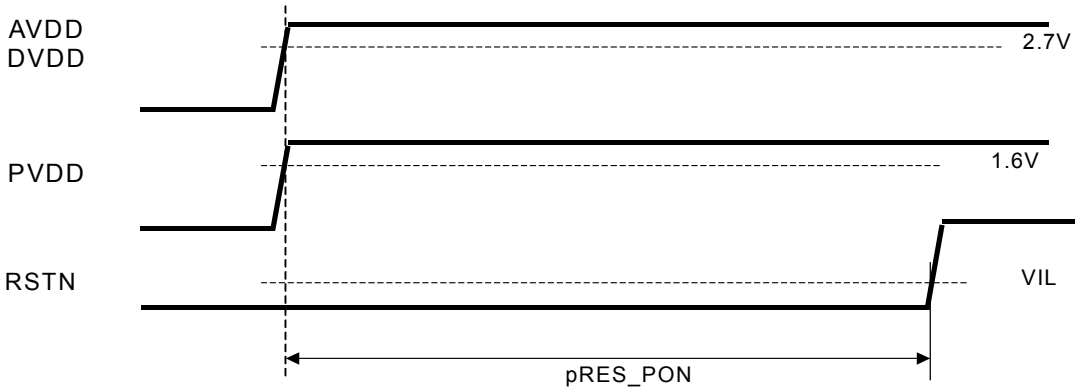
Power-down release sequence when crystal resonator is connected, is shown as follows.



6) Power-On-Reset

At power-on, reset must be enabled for a duration time till the Analog Reference Voltage & Current are stabilized.

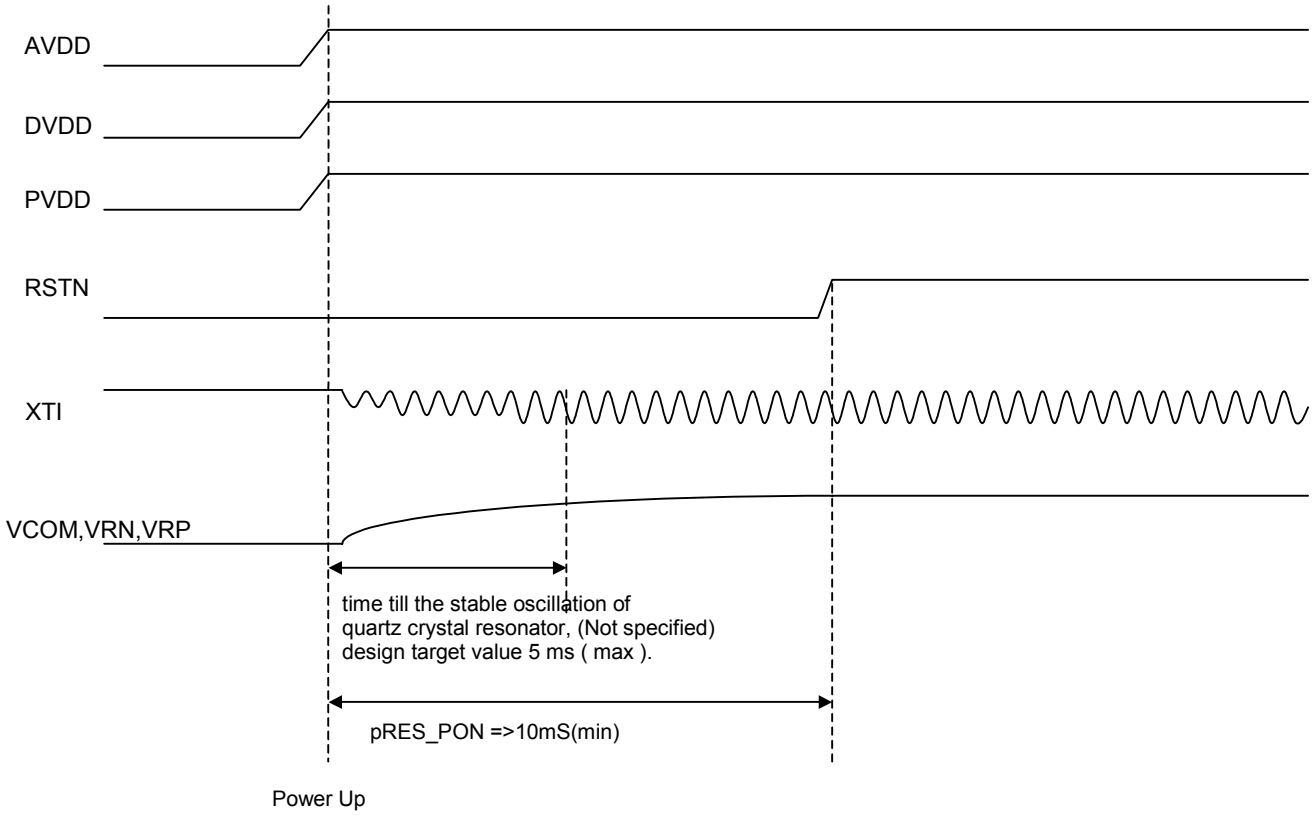
Power-on operation must be made with either simultaneous power-on of PVDD / AVDD / DVDD or PVDD first and then AVDD / DVDD



Parameter	Symbol	Min.	Typ.	Max	Unit	Parameter
RESETN pulse width	pRES_PON	10			msec	

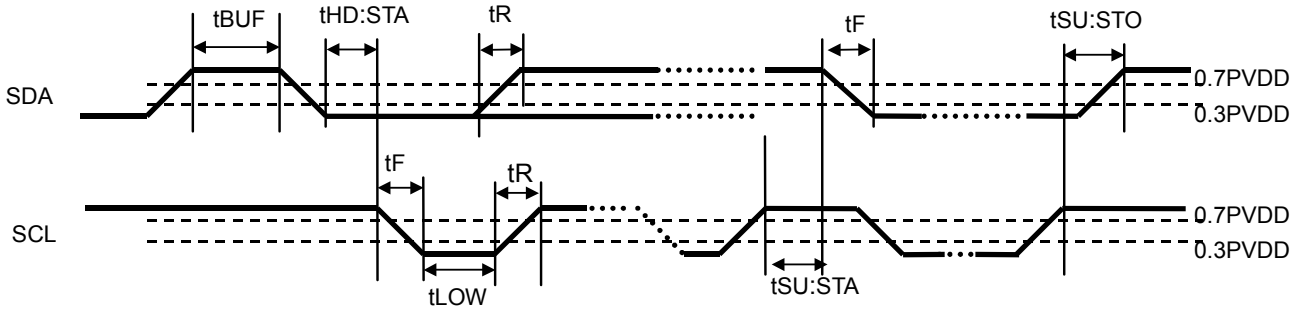
note) clock input is required for reset operation.

Power-On Sequence when crystal resonator is connected.



(7) I2C Bus Input / Output Timing(DVDD / PVDD 2.7 V ~ 3.3 V or PVDD 1.6 V ~ 2.0 V, Ta = -30 ~ + 85 °C)

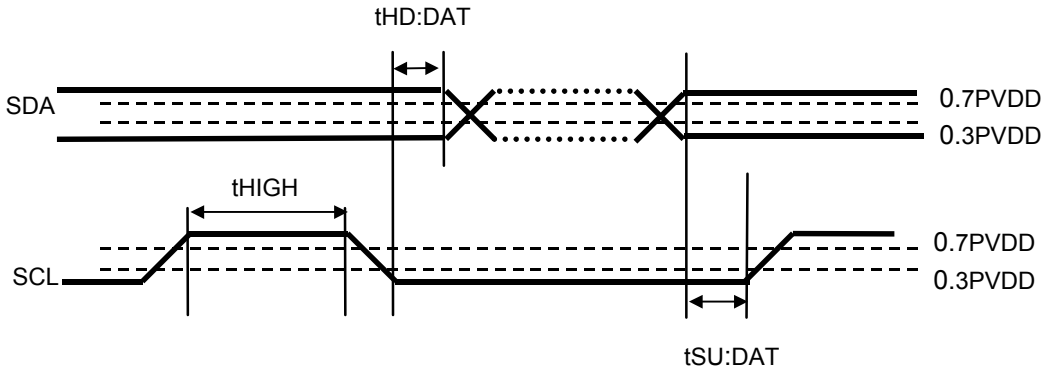
(7-1) Timing 1



Parameter	Symbol	Min.	Max.	Unit
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

The above I2C bus related timing is specified by the I2C Bus Specification, and it is not limited by the device performance. For details, please refer to the I2C Bus Specification.

(7-2) Timing 2



Parameter	Symbol	Min.	Max.	Unit
Data Setup Time	tSU:DAT	100 (note1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9 (note2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

note 1 : when to use I2C Bus Standard mode, tSU:DAT >- 250 ns must be met.

note 2 : when the AK8855 is used in such bus interface where tLOW is not extended (at minimum specification of tLOW), this condition must be met.

Functional Outline

(1) Clock

Feed a 24.5454 MHz clock. When a 27 MHz clock is required, it is generated by an internal PLL.
Internal operating clock rates are :

24.5454 MHz	at VGA / QVGA / rotated QVGA size / rotated CIF size outputs
27 MHz	at 601 Pixel mode, CIF / QCIF

Although clock is asynchronous with input signal, Vertical position is aligned since Digital Pixel Interpolator is integrated on-chip

(2) Analog Interface

The AK8855 accepts Composite Video signal.

(3) Input Signal

NTSC-M,PAL-B,-D, -G, -H, -I compatible Composite Video signals are accepted as input signal.

(4) Analog Input Signal Processing

Anti-aliasing filter is integrated on-chip.

PGA	: 0 dB ~ 12 dB (approximately 0.1 dB / step)
AD Converter	: operation at either 24.5454 MHz or 27.00 MHz

(5) Clamp Processing

Sync-Tip Clamping is processed in Analog part and Digital Pedestal Clamping in Digital Signal Processing part.

(6) Adaptive AGC Function

Based on the difference between the Sync-Tip level and Pedestal level, input signal value is corrected to a proper level.
A function to adjust gain by Video signal level is integrated for such a case where only the Video signal is larger.

(7) ACC Function

Based on the Color Burst level, input Color signal level is corrected to a proper level.

(8) Y / C Separation Function

Primary Y / C separation is done.

(9) Pixel Interpolator

The AK8855 has an on-chip Digital Pixel Interpolator to align output pixels' vertical position. Therefore no line-synchronized clock etc are required.

(10) Picture Quality Adjustment Function

Adjustments of Contrast, Brightness, Color Hue and Color Saturation levels are possible.

(11) Output Interface

Outputs are ITU-R BT.601 compatible signal levels (with limit ON / OFF).
Output interfaces are shown as follows :
- supporting Camera I / F
- ITU-R BT.656-like output format *
- Active Video region is indicated by HD / VD (FIELD) / DVALID

* with SAV / EAV, at 27 MHz output. There is a case where number of clock count from EAV to SAV may differ from Rec.656 format.

(12) Output Picture Size
- VGA (640 X 480) (interlaced output)
- QVGA (320 X 240)
- CIF (352 X 288)
- QCIF (176 X 144)
- 601 (NTSC : 720 X 480 / PAL : 720 X 576) (interlaced output)
- rotated QVGA (240 X 180)
- rotated CIF (288 X 216)

(13) Other Functions
- Black level signal (Y = 16, Cb / Cr = 128) is output in self-operating mode when no signal is input.
- No signal input detection function
- I2C Host interface
- Power-down function
- decoding function of Closed Caption, VBID (CGMS-A 525 line), WSS signal (625 line signal). CRCC which is added to CGMS-A is decoded by the AK8855.

Input Signal

Decodable Video signals by the AK8855 are,

- NTSC
- PAL-B, -D, -G, -H, -I.

Those input signal types are set by **Input Video Standard Register (R/W) [Sub Address 0x00]**.
Input signal is converted into digital code as follows.

Clamp Block ---- Anti-aliasing Filter ---- PGA Block ---- ADC Block

Then the digitized signal is signal-processed in digital block.
Setting of **Input Video Standard Register (R/W) [Sub Address 0x00]** is described here.
This register is the setting register to set input signal attribute. Bit allocation of the register is as follows.

Sub Address 0x00 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	AINSEL	VLF	VCEN	VSCF1	VSCF0
Default Value							
0	0	0	0	0	0	0	0

[VSCF1 : VSCF0]-bit
setting of input signal sub-carrier is made by [VSCF1 : VSCF0]-bit.

[VSCF1:VSCF0]-bit	Sub-carrier frequency [MHz]	Conditions
[00]	3.57954545	NTSC
[01]	3.57561188	
[10]	3.582054	
[11]	4.43361875	PAL-B,D,G,H,I

[VCEN]-bit
setting of input signal Color Encoding system is set by [VCEN]-bit.

[VCEN]-bit	Color Encoding system	Conditions
0	NTSC	
1	PAL	

[VLF]-bit
setting of number of lines per each Frame of input signal is made by [VLF]-bit.

[VLF]-bit	Number of lines	Conditions
0	525 lines	
1	625 lines	

[AINSEL]-bit
selection of input signal is made.

[AINSEL]-bit	Input signal	Conditions
0	AIN1 input is selected	
1	AIN2 input is selected	

PGA (Programmable Gain Amp)

PGA (Programmable Gain Amp) is integrated at the input stage of the AK8855.
PGA is adjustable from 0 dB to 12 dB, and its gain step is approximately 0.1 dB / step.
Signal input to the AK8855 is attenuated to 50 % level by a resistor-divider.
PGA setting is made by **PGA Control Register (R/W) [Sub Address 0x05].**

By writing "1" to **Control Register (R/W) [Sub Address 0x04]** AGC-bit, AGC function is enabled.
Since the set value by AGC is written at **PGA Control Register (R/W) [Sub Address 0x05]**, the AGC set value is known by reading this register (manual setting of PGA is invalid).
When AGC function is disabled, PGA gain setting by manual is possible.
Bit allocation of **PGA Control Register** is as follows.

[PGA Control Register]
Sub Address 0x05 **Default Value: 0x46**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA6	PGA5	PGA4	PGA3	PGA2	PGA1	PGA0
Default Value							
0	1	0	0	0	1	1	0

AGC

The AK8855 has an adaptive AGC function. When AGC is enabled, input signal is controlled to a optimized level by PGA.
When AGC is turned off, gain setting of PGA by manual is possible.
Enable / disable setting of AGC is done by **Control Register (R/W) [Sub Address 0x04].**
Sub Address 0x04 **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNTSEL	DTFIX	ODEV	FRMRT1	FRMRT0	COLKIL	ACC	AGC
Default Value							
0	0	0	0	0	0	0	0

[AGC]-bit
[AGC]-bit sets the mode of AGC

[AGC]-bit	Fumction	Condition
0	Disable	
1	Enable	

note) writing into PGA register is possible while AGC is enabled, but the written result is not valid to register. The written result becomes valid to register when AGC is disabled.

Clamp

Input signal is Analog Sync-Tip clamped.
The Sync-Tip clamped input signal is then clamped to Pedestal level after AD conversion.

Anti-Aliasing Filter

Analog Band Limit Filter is integrated before ADC input in the AK8855.
The Anti-Aliasing Filter has following characteristics.

+/-2.0dB (~5.5MHz)
27MHz -30dB (typ)

Clock

Sampling is done by a fixed clock in the AK8855. PLL to synchronize with Analog input signal is not built-in.
Clock rate differs depending on the selected output picture sizes and types of input signal.
Internal operating clock is either 24.5454 MHz input clock or 27 MHz which is generated from input clock by PLL.
Internal clock to be used is automatically selected by setting output picture size.

	operation clock	Size	Signal	Note
VGA	24.5454MHz	640 x 480	NTSC/PAL	Interlace output
QVGA	24.5454MHz	320 x 240	NTSC/PAL	Progressive output
CIF	27MHz	352 x 288	NTSC/PAL	Progressive output
QCIF	27MHz	176 x 144	NTSC/PAL	Progressive output
601	27MHz	720 x 480	NTSC	Interlace output
	27MHz	720 x 576	PAL	Interlace output
Rotated QVGA	24.5454MHz	240 x 180	NTSC/PAL	Progressive output
Rotated CIF	24.5454MHz	288 x 216	NTSC/PAL	Progressive output

note) In case of the rotated CIF size, both left-end and right-end 16 pixels are omitted and 288 X 216 picture size is output (90% area of the effective picture is output).
When decoding CIF (NTSC), output rate is 2X speed of input HD.

Output Picture Size

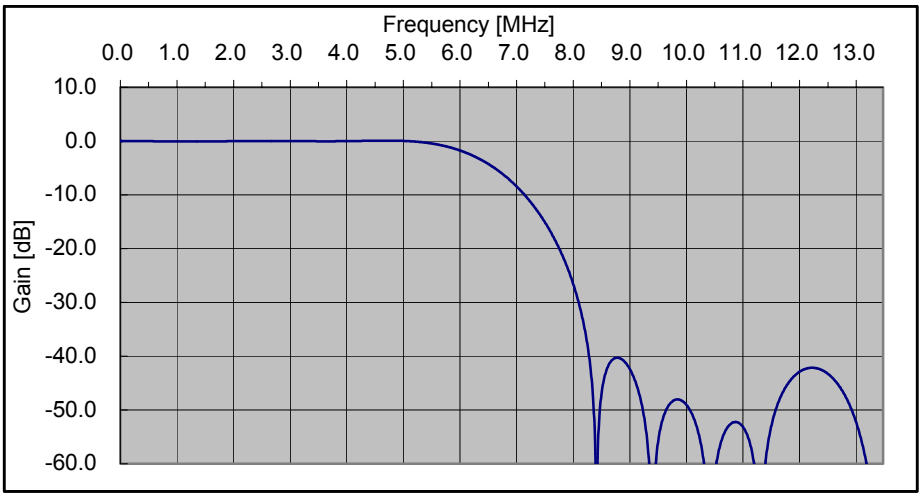
Setting of output picture size is done by [OFORM2 : OFORM0]-bit of **Output Control 1 Register (R/W) [Sub Address 0x01]**. Setting is as follows.

[OFORM2:OFORM0]-bit

[OFORM2:OFROM0]-bit	Function	Condition
000	QVGA	
001	VGA	
010	CIF	
011	QCIF	
100	Rotated QVGA	
101	Rotated CIF	
110	601	

Decimation Filter

Characteristic of Decimation Filter is shown as follows (shown below is a characteristic at 27 MHz sampling).



Sync-Separation, Sync-Detection

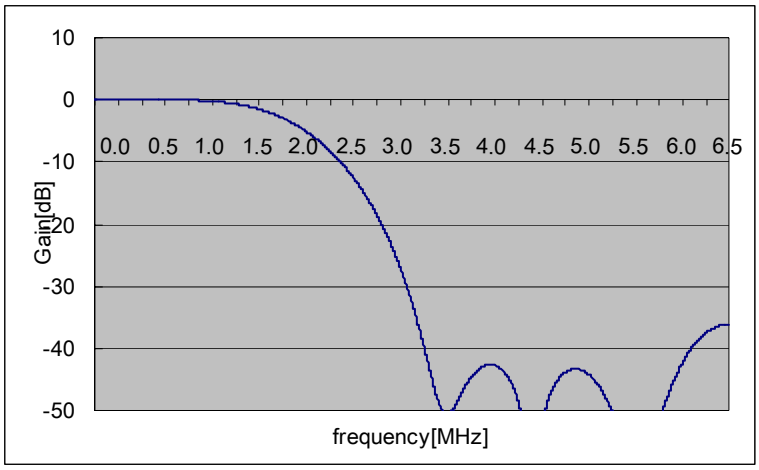
Sync-Detection and Separation are made from the digitized input signal.
The recognized Sync-signal is used as reference timing for decoding process.

Digital Pedestal Clamp

Converted input signal into digital code clamps the pedestal part.
Internal clamp levels differ depending on types of input signals (286mV Sync signal and 300 mV Sync signal), but output result operates such that pedestal position becomes at code 16 (8-bit Rec. 601 level) for either case.

YC Separation

YC separation is done in a primary YC separation mode in the AK8855.
Filter characteristic used for YC separation is as follows (shown below is a characteristic at 27 MHz sampling).



Auto Color Control (ACC)

This is a function to adjust Color Burst level of input signal to a proper level (NTSC : 286 [mV] / PAL : 300 [mV]).
Input Color signal level is decided by Color Burst signal. ACC gain is 20 dB maximum.

Sub Address 0x04 **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNTSEL	DTFIX	ODEV	FRMRT1	FRMRT0	COLKIL	ACC	AGC
Default Value							
0	0	0	0	0	0	0	0

[ACC]-bit
[ACC]-bit selects enable / disable of ACC and time constant.

[ACC]-bit	ACC Setting	Condition
0	Disable	
1	Enable	

ACC function operates independently from Color Saturation Adjust function (when ACC is enabled, Color Saturation adjustment is made on the signal which is adjusted to a proper level by ACC).

Color Killer

Chroma Signal Quality is decided by Color Burst level of input signal.
When the Chroma Signal level is lower than a threshold level, it is decided to be improper signal and input signal is all processed as luminance signal.
In this case, Cb / Cr data from the AK8855 is a fixed 0x80 in 601 level.
Color Killer functions when Color Burst level becomes lower than approximately -23 dB.

Bit allocation of **Control Register (R/W) [Sub Address 0x04]** is as follows.

Sub Address 0x04 **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNTSEL	DTFIX	ODEV	FRMRT1	FRMRT0	COLKIL	ACC	AGC
Default Value							
0	0	0	0	0	0	0	0

[COLKILL]-bit
[COLKILL]-bit selects enable / disable of Color Killer function.

COLKILL-bit	Color Killer Function	Condition
0	Enable	
1	Disable	

Frame Rate setting

This is to set the Frame Rate.
Frame Rate setting is done by [FRMRT1 : FRMRT0]-bits of **Control Register (R/W) [Sub Address 0x04]**.

[FRMRT1:FRMRT0]-bit	Frame Rate	Condition
00	30/25(525/625)	
01	15/12.25(525/625)	
10	7.5/6.25(525/625)	
11	Reserved	

Even / Odd Field selection

Even / Odd Field setting is done for QVGA / CIF / QCIF output modes.
Setting is done by [ODEV]-bit of **Control Register (R/W) [Sub Address 0x04]**.

ODEV-bit		Condition
0	ODD Field	
1	EVEN Field	

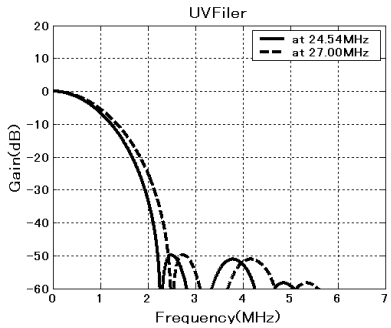
Power Saving Mode at Low Frame Rate

Power dissipation during no-output period is reduced when Frame Rate is dropped.
Setting is done by [DTFIX]-bit of **Control Register (R/W) [Sub Address 0x04]**.

DTFIX-bit	Power Saving mode	Condition
0	Disabled	
1	Enable	

UV Filter

UV Filter characteristic is as follows.



Picture Quality Adjust Process Function

Those Picture Quality Adjust processing such as Contrast adjust function, Brightness adjust function, Color Saturation adjust function and Color Hue adjust function are integrated in the AK8855.

(1) Contrast Adjust Function

Contrast Adjustment is processed by multiplying Luminance signal (Y), by the gain value which is set by **Contrast Control Register (R/W) [Sub Address 0x06]**.

CNTSEL-bit = 0
YOUT = CONT* (YIN – 128) + 125 ;

YOUT : Contrast arithmetic operation result
YIN : before Contrast arithmetic operation
CONT : Contrast coefficient (register set value)

It is also possible to define the equation as follows by register setting
CNTSEL-bit = 1
YOUT = CONT* (YIN – 128) + 16 ;

YOUT : Contrast arithmetic operation result
YIN : before Contrast arithmetic operation
CONT : Contrast coefficient (register set value)

Setting is made by [CNTSEL]-bit of **Control Register (R/W) [Sub Address 0x04]**.

Variable range of Contrast Gain coefficient is from 0 to 1.99 (1 / 128 step) and when the arithmetic operation result exceeds the above range, it is clipped to the upper-limit of [254], or the lower-limit of [1] (output result ranges from 16 to 235 when 601 Limit-bit is at [1]).

Bit allocation of **Contrast Control Register** is as follows.

Sub Address 0x06 **Default Value: 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Default Value							
1	0	0	0	0	0	0	0

Sub Address 0x04 **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNTSEL	DTFIX	ODEV	FRMRT1	FRMRT0	COLKIL	ACC	AGC
Default Value							
0	0	0	0	0	0	0	0

[CNTSEL]-bit

[CNTSEL]-bit sets the change-over point of Contrast adjustment.

[CNTSEL]-bit	Function	Condition
0	To be adjusted at Luminance 125 as a center point	
1	To be adjusted at Luminance 16 as a center point.	

(2) Brightness Adjust Function

Brightness Adjust function is processed by adding to the Luminance signal (Y), a value which is set by **Brightness Control Register (R/W) [Sub Address 0x07]**.

YOUT = YIN + BR

YOUT : Brightness arithmetic operation result
YIN : before Brightness arithmetic operation
BR : Brightness coefficient (register set value)

Variable range of Brightness adding coefficient is from – 127 to +127 and the value setting is made in 2's complement number.
When the arithmetic operation result exceeds the above range, it is clipped to the upper-limit of [254], or the lower-limit of [1] (output result ranges from 16 to 235 when 601 Limit-bit is at [1]).

Bit allocation of **Brightness Control Register** is as follows.

Sub Address 0x07 **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
Default Value							
0	0	0	0	0	0	0	0

(3) Color Saturation Adjust Function

Color Saturation adjustment is processed by multiplying the Color Signal (C), by a value which is set by **Saturation Control Register (R/W) [Sub Address 0x08]**.
Saturation coefficient is processed over C signal.
A multiplied result by Saturation coefficient is U / V de-modulated.
Variable range of Saturation multiplying coefficient is from 0 to 255 / 128 in 1 / 128 programmable step.
The default value of the register is un-adjusted value (0x80).

Bit allocation of **Saturation Control Register** is as follows.

Sub Address 0x08 **Default Value: 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
Default Value							
1	0	0	0	0	0	0	0

(4) Color Hue Adjust Function

The Color Hue can be rotated in the AK8855.
Rotation amount of Color Hue depends on a value which is set by **HUE Control Register (R/W) [Sub Address 0x09]**.
Variable Rotation range of the phase is +/- 45 degrees (in approximately 0.35 degree / step).
Default value of the register is un-adjusted value (0x00). Set value is made in 2's complement number.

Bit allocation of **Hue Control Register** is as follows.

Sub Address 0x09 **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
Default Value							
0	0	0	0	0	0	0	0

Input Video Decoding Period

This defines Decoding process period of input Video signal.
The period defined here is for the input Video source.
As for the decode data, a number of Lines differs, depending on the selected output mode.
Refer to a figure at next page which shows " Input Video Signal vs Output Data relation ".

Active Video Period is as follows.

525 Line system : Line 22 ~ Line 261 & Line 285 ~ Line 524
625 Line system : Line 23 ~ Line 310 & Line 336 ~ Line 623

Vertical Blanking Period is as follows .

525 Line system : Line 525 ~ Line 1 ~ Line 21 & Line 262 ~ Line 284
625 Line system : Line 624 ~ Line 625 – Line1 ~ Line 22 & Line 311 ~ Line 335

Default value of output during Vertical Blanking period is Black level (Y = 0x10, Cb / Cr = 0x80).

Closed Caption / Closed Caption Extended Data / VBID (CGMS) / WSS

Closed Caption data, Closed Caption Extended data, VBID (CGMS) and WSS signals which are super-imposed during VBI interval are decoded in the AK8855. Decoded data is written into register.
When Request bits [bit3 : bit 0] of **Request VBI Info Register (W) [Sub Address 0x0A]** are set, the AK8855 judges that a decode request of each data is made and it is put into data wait condition.
After data is detected and decoded, it informs to the Host, using [bit3 : bit 0] of **Macrovision Status Register** that decoding has been completed.
Decoded results are written into **Closed Caption 1 Register (R) [Sub Address 0x12]** / **Closed Caption 2 Register (R) [Sub Address 0x13]**, **Extended Data 1 Register (R) [Sub Address 0x14]** / **Extended Data 2 Register (R) [Sub Address 0x15]**, **VBID / WSS1 Register (R) [Sub Address 0x16]** / **VBID / WSS2 Register (R) [Sub Address 0x17]** respectively.
Each data is super-imposed on the respective Line as listed below.
CRCC code of VBID data (CGMS-A) is decoded and its result only is stored in register.

Signal	Line	Note
Closed Caption	NTSC : Line-21	525-Line
Closed Caption Extended	NTSC : Line-284	525-Line
VBID	NTSC : Line-20/283	525-Line
WSS	PAL : Line-23	625-Line

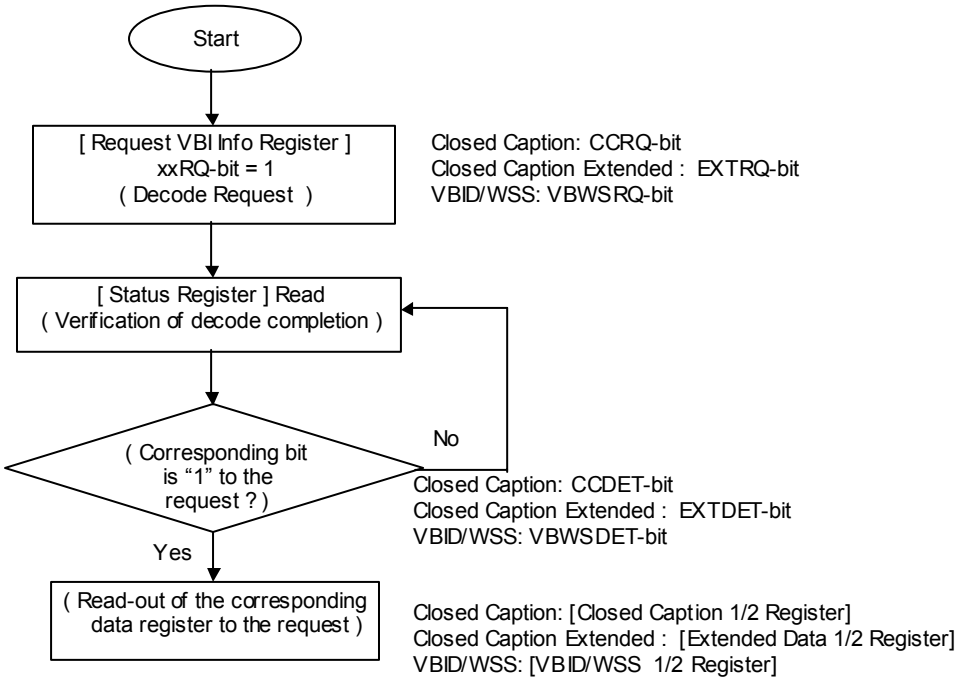
Configuration of **Request VBI INFO Register** is as follows.
Sub Address 0x0A **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	VBWSRQ	EXTRQ	CCRQ
Default Value							
0	0	0	0	0	0	0	0

Configuration of **Status Register** is as follows
Sub Address 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBWSSDET	EXTDET	CCDET	AGCSTS	CPLLLCK	PKWHITE	COLKILST	NSIG

Information Read-Out Flow during VBI interval is shown below.



When to read out Closed Caption data :

Write "1" to CCRQ-bit of Request VBI Info **Register (W) [Sub Address 0x0A]**.

When "1" is written to this bit, the AK8855 is put into a wait condition for Closed Caption Data decoding. Then when Data comes in, it is decoded and after the decoding, "1" is written back to CCDET-bit of **Status Register (R / W) [Sub Address 0x10]**.

CCDET-bit right after Reset, is "1" (it becomes "0" when "1" is written to CCRQ-bit).

Decoded result is written into **Closed Caption 1 Register (R) [Sub Address 0x12]** and **Closed Caption 2 Register (R) [Sub Address 0x13]** as shown next.

Data in **Closed Caption 1 Register** and **Closed Caption 2 Register** are retained till they are over-written with new data.

Configuration of **Closed Caption 1 Register** and **Closed Caption 2 Register** are as follow.

Closed Caption 1 Register (R) [Sub Address 0x12]

Sub Address 0x12

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Closed Caption 2 Register (R) [Sub Address 0x13]

Sub Address 0x13

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

When to read out Closed Caption Extended Data :

Write "1" to EXTRQ-bit of **Request VBI Info Register (W) [Sub Address 0x0A]**.

When "1" is written to this bit, the AK8855 is put into a wait condition for Extended Data decoding.

Then, when data comes in, it is decoded and after the decoding, "1" is written back to EXTDET-bit of **Status Register (R / W) [Sub Address 0x10]**.

EXTDET-bit right after the Reset, is "1" (it becomes "0" when "1" is written to EXTRQ-bit).

Decoded result is written into **Extended Data 1 Register (R) [Sub Address 0x14]** and **Extended Data 2 Register (R) [Sub Address ox15]** as shown next.

Data in **Extended Data 1 Register** and **Extended Data 2 Register** are retained till they are over-written with new data.

Configuration of **Extended Data 1 Register** and **Extended Data 2 Register** are as follow.

Extended Data 1 Register (R) [Sub Address 0x14]

Sub Address 0x14

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0

Extended Data 2 Register (R) [Sub Address 0x15]

Sub Address 0x15

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8

When to read out VBID Data :

Write “1” to VBWSRQ-bit of **Request VBI Info Register (W) [Sub Address 0x0A]**.
When “1” is written to this bit, the AK8855 is put into a wait condition for VBID data decoding.
Then when data comes in, it is decoded and after the decoding, “1” is written back to VBWSDET-bit of **Status Register (R / W) [Sub Address 0x10]**.
VBWSDET-bit right after reset, is “1” (it becomes “0” when “1” is written to VBWSRQ-bit).
Decoded data is 13 Bit-long and it is written into **VBID / WSS1 Register (R) [Sub Address 0x16]** and **VBID / WSS 2 Register (R) [Sub Address 0x17]**.
VBID data is valid only in 525 Line system. These registers are also commonly used for WSS Read-Out register.
CRCC code is decoded and its data only is stored in register.
Data in **VBID / WSS 1 Register and VBID / WSS 2 Register** are retained till they are over-written with new data.
Configuration of **VBID / WSS 1 Register** and **VBID / WSS 2 Register** are as follow.

VBID/WSS 1 Register (R) [Sub Address 0x16] Register to store VBID data
Sub Address 0x16

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6

VBID/WSS 2 Register (R) [Sub Address 0x17] Register to store VBID data
Sub Address 0x17

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14

When to read out WSS Data :

Write “1” to VBWSRQ-bit of **Request VBI Info Register (W) [Sub Address 0x0A]**.
When “1” is written to this bit, the AK8855 is put into a wait condition for VBWS data decoding.
Then when data comes in, it is decoded and after the decoding, “1” is written back to VBWS-bit of **Status Register (R / W) [Sub Address 0x10]**.
VBWS-bit right after reset, is “1” (it becomes “0” when “1” is written to VBWSRQ-bit).
WSS data is valid only in 625 Line system.
These registers are also commonly used for VBID Read-Out register.
Decoded results are written into **VBID / WSS 1 Register (R) [Sub Address 0x16]** and **VBID / WSS 2 Register (R) [Sub Address 0x17]** as shown next.
Data in VBID / WSS 1 Register and VBID / WSS 2 Register are retained till they are over-written with new data.

VBID/WSS 1 Register (R) [Sub Address 0x16] Register to store WSS data
Sub Address 0x16

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	G4-13	G4-12	G4-11	G3-10	G3-9	G3-8

VBID/WSS 2 Register (R) [Sub Address 0x17] Register to store WSS data
Sub Address 0x17

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0

Macrovision Decoding

When Macrovision Copy Protect signal is input, the AK8855 decodes the added Macrovision information and stores the result at **Macrovision Status Register (R/W) [Sub Address 0x11]**. Configuration of **Macrovision Status Register** is as follows.

Sub Address 0x11

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PSPDET	AGCPDET	BPPDET	SYNCRED	CSTYPE	CSDET	AGCDET

[AGCDET]-bit
When Macrovision AGC process is recognized, this bit becomes “1”.

[AGCDET]-bit	Status of Macrovision Detection	Condition
0	AGC Process in not detected	
1	AGC Process is detected	

[CSDET]-bit
When Macrovision Color Stripe Process is recognized, this bit becomes “1”.

[CSDET]-bit	Status of Macrovision Detection	Condition
0	Color Stripe Process is not detected	
1	Color Stripe Process is detected	

[CSTYPE]-bit
When CSDET-bit is “1”, Color Stripe Process type is indicated.

[CSTYPE]-bit	Status of Macrovision Detection	Condition
0	Color Stripe Type 2 is set	
1	Color Stripe Type 3 is set	

[SYNCRED]-bit
When SYNCRED-bit is “1”, it indicates that Sync Reduction has been detected.

[SYNCRED]-bit	Status of Macrovision Detection	Condition
0	-	
1	Sync Reduction is detected	

[BPPDET]-bit
When BPPDET-bit is “1”, it indicates that “ End of Field Back Porch Pulse “ has been detected.

[BPPDET]-bit	Status of Macrovision Detection	Condition
0	-	
1	End of Field Back Porch Pulse is detected	

[AGCPDET]-bit
When AGCPDET-bit is “1”, it indicates that AGC Pulse has been detected.

[AGCPDET]-bit	Status of Macrovision Detection	Condition
0	-	
1	AGC Pulse is detected	

[PSPDET]-bit
When PSPDET-bit is “1”, it indicates that Pseudo Sync Pulse has been detected.

[PSPDET]-bit	Status of Macrovision Detection	Condition
0	-	
1	Pseudo Sync Pulse is detected.	

Decode Data Output (Rec. 601 Limit)

The AK8855 outputs the decode data at the specified level (Y / Cb / Cb 4:2:2) by ITU-R BT.601.
Min. / Max. output data can be selected by [LIMIT601]-bit of **Output Control 1 Register (R/W) [Sub Address 0x01]**.
Bit allocation of **Output Control 1 Register** is as follows.

Sub Address 0x01 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VDPSUP	TRSVSEL	OIF1	OIF0	LIMIT601	OFORM2	OFORM1	OFORM0
Default Value							
0	0	0	0	0	0	0	0

[LIMIT601]-bit
Min. / Max. of Output Data is specified by [LIMIT601]-bit.
All internal, arithmetic operations are processed at Min. = 1, Max. = 254.
Clipping value of Output code differs by [LIMIT601] –bit setting.
Default value setting is “0”.

[LIMIT601]-bit	Output code Min.Max	Condition
0	Y : 1 ~ 254 Cb/Cr : 1 ~ 254	(Default value)
1	Y : 16 ~ 235 Cb/Cr : 16 ~ 240	

Output Interface

The AK8855 supports 3 types of Interfaces.

(1) Camera Interface (QVGA / CIF / QCIF)
(2) Interface by HD / VD / DVALID (VGA / QVGA / CIF / QCIF)
(3) 656 Interface (601 specification compatible size (720 X 480))

Timing diagrams of each output mode are shown in each output mode description section.
The AK8855 outputs data (D [7:0]) and output timing signals (HD / HV, VD / VAF, DVALID , FIELD) in accordance with the specified timing diagram only when either of the following conditions is met :

(a) when the AK8855 operation is in sync with input signal,
(b) when the AK8855 cannot establish synchronization with input signal and it is decided that no signal is input (Black signal output at default condition).

During transition from condition (a) to condition (b) or from condition (b) to condition (a), specified data (D [7:0]) and output timing signals (HD / HV, VD / VAF, DVALID, FIELD) may differ from the one shown in the specified timing diagram.

(1) Camera Interface
There are 2 types of data interface – " (1-1) HV & VAF Interface Mode " and " (1-2) SAV / EAV Interface Mode ".

In this mode, since shift of synchronization with the input signal is adjusted at the head part of Line, interval between Lines may fluctuate in some degree.
When an exceptional input signal is decoded, there may be cases where lack of # of Lines and lack of # of Pixels per Line occur, regardless of operation mode.
At the default value, end of Frame is made at the rising edge of VAF signal, and end of Line is made by HV signal.
Polarity of VAF / HV / DVALID / CLKO is programmable by **Output Control 2 Register (R/W) [Sub Address 0x02]**.
Following timing diagrams show operation examples at HDP = 0, VDP = 0, DVALDP = 0, CLKINV = 1 settings.

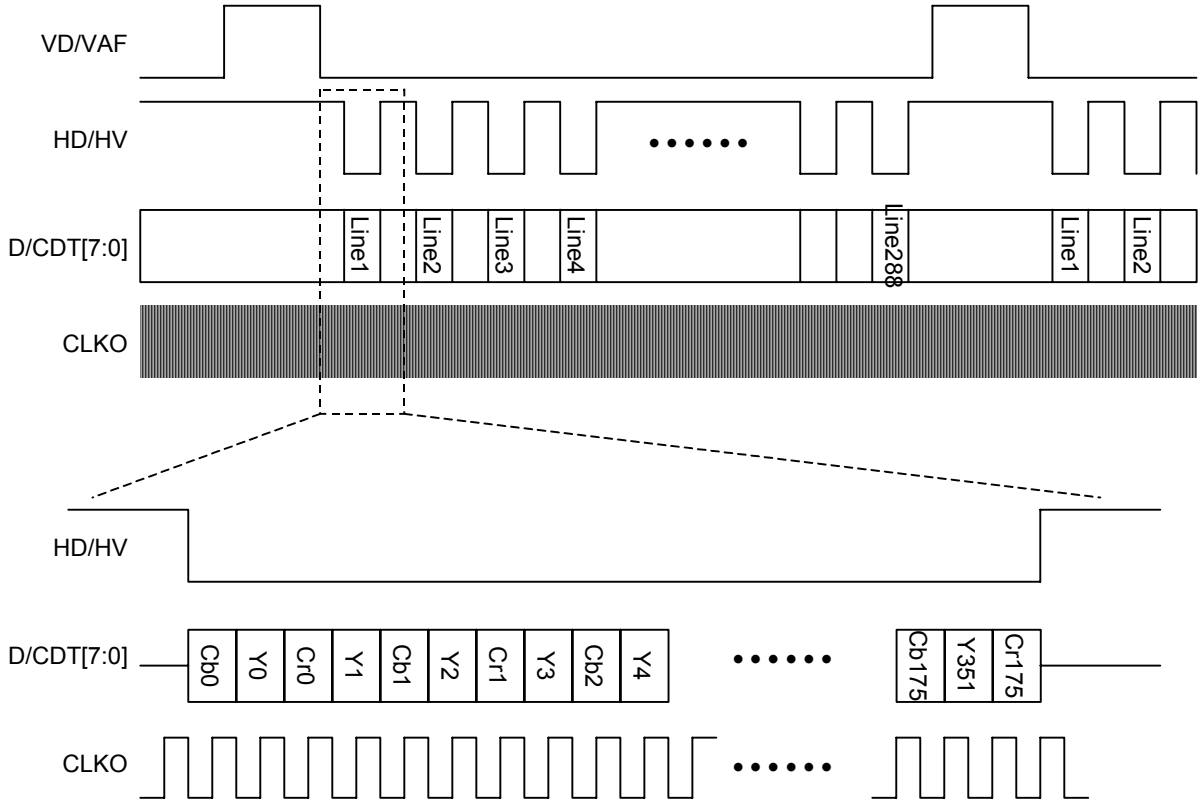
Since output is Progressive Output in Camera Interface mode, picture sizes to be handled in this mode are QVGA / CIF / QCIF / rotated QVGA / rotated CIF.
Definition of SAV / EAV at section (1-2) SAV / EAV Interface Mode is as follows.

	SAV	EAV
Active	0x80	0x9D
VBlank	0xAB	0xB6

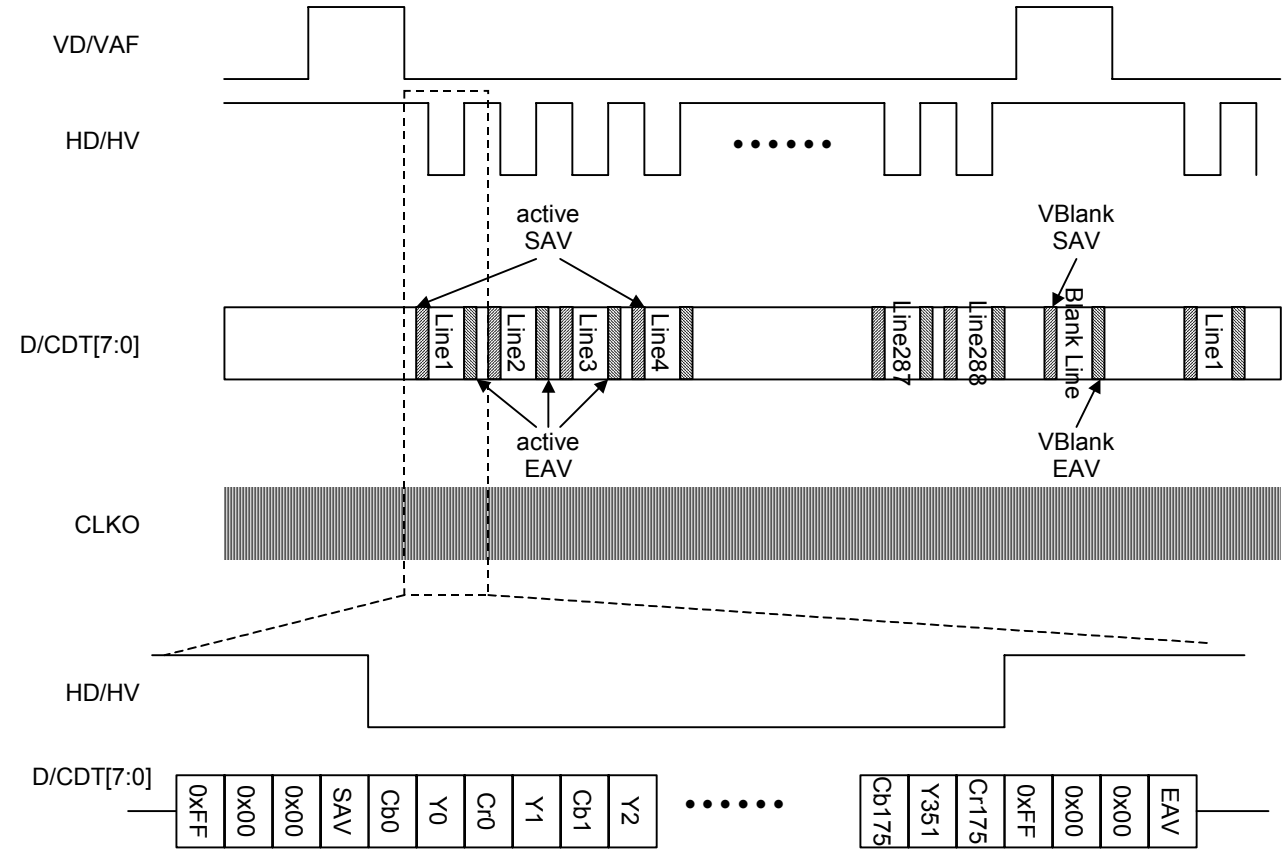
In SAV / EAV Output mode, HV / VAF signal is not output at default value. It is possible to output by setting register.

(1-1) Interface by HV / VAF

Following timing diagram shows CIF size output case as an example.

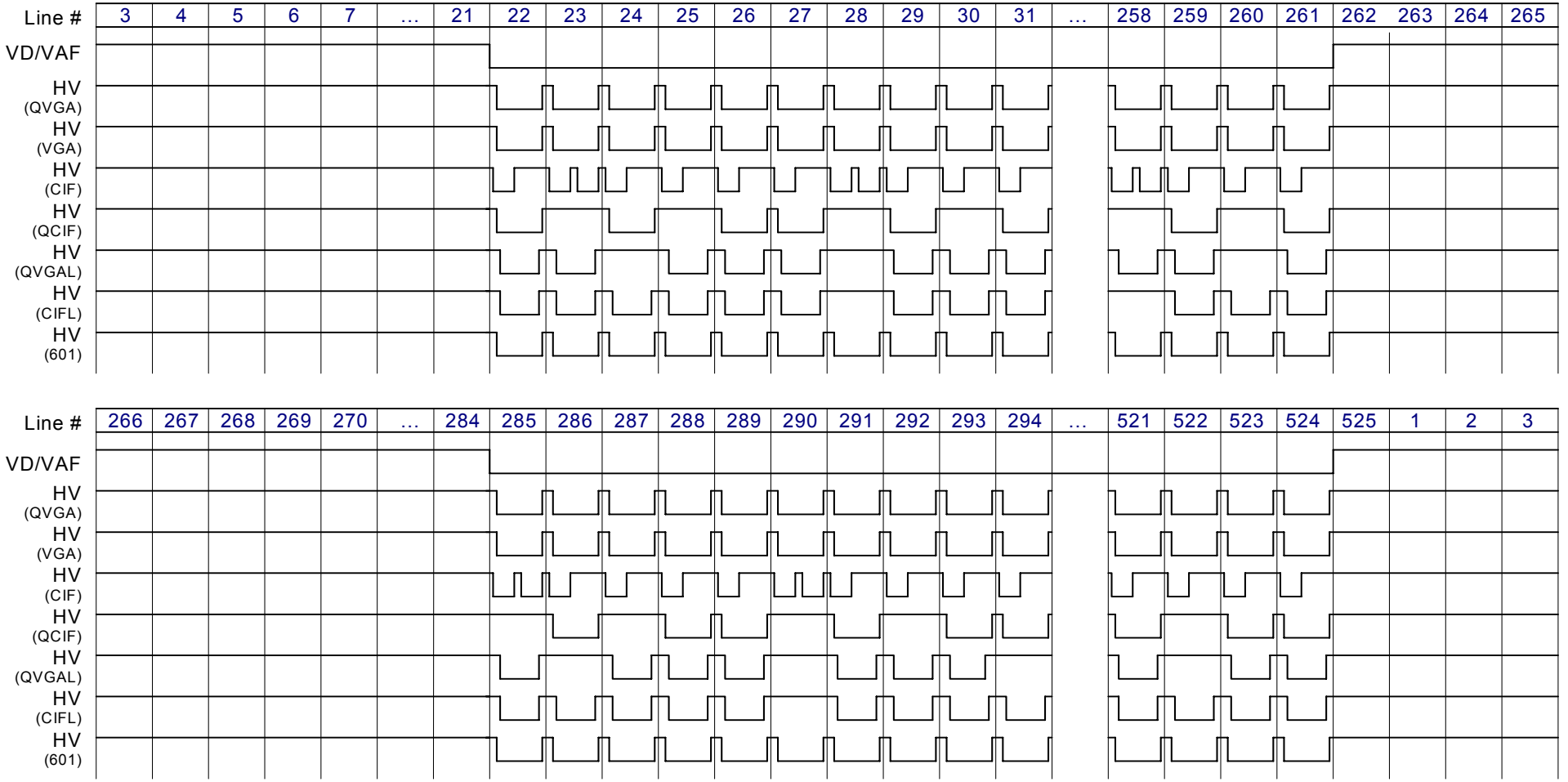


(1-2) Interface by SAV / EAV (CIF size output example)



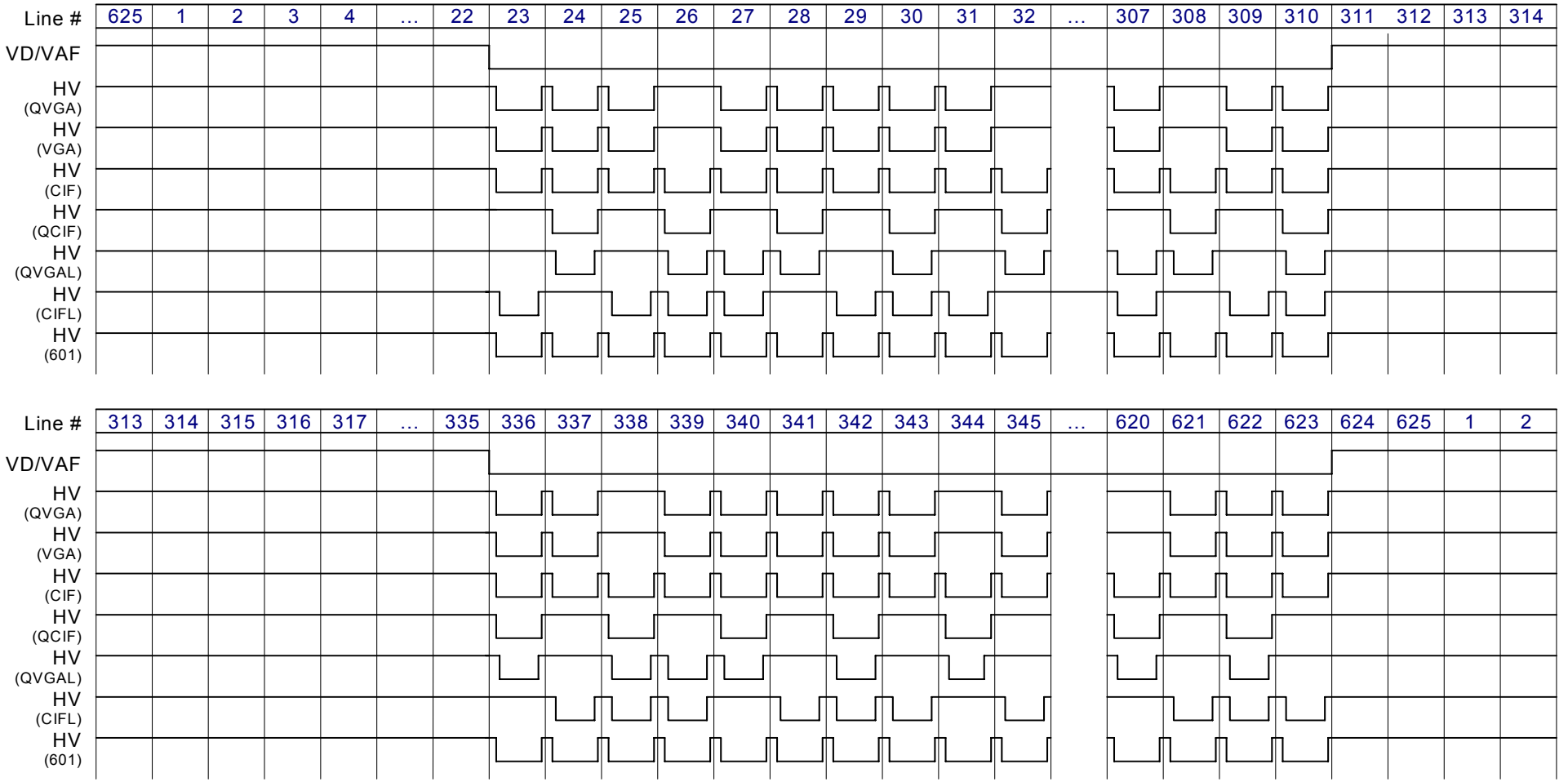
Output Timings of Camera I/F mode are shown as follows. (The polarity of HV/VAF/DVALID can be changed by register setting.)

NTSC Register: VLF = 1'b0, OIF[1:0] = 2'b10



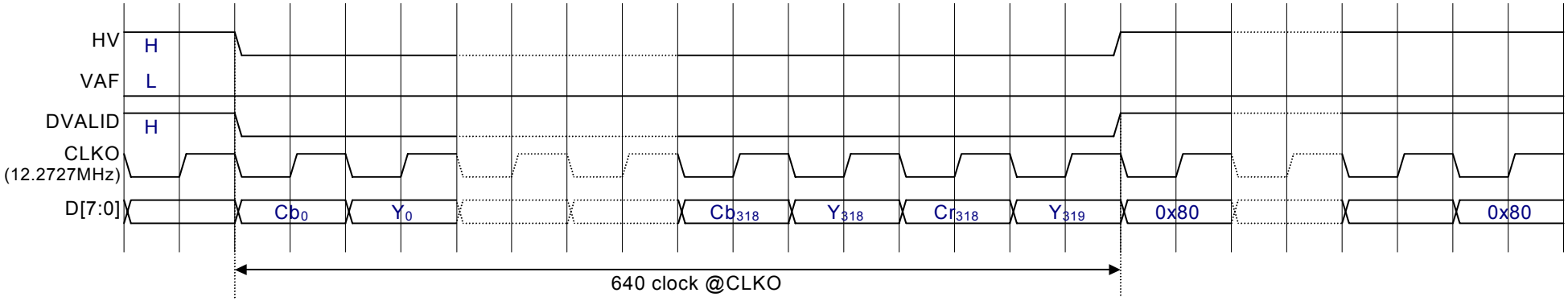
Note: In case of the output mode except VGA, 601, DVALID signal becomes active(Low) either ODD or EVEN timing. The timing chart is shown the both case for the sake of convenience.
QVGAL: Rotated QVGA, CIFL: Rotated CIF

PAL Register Set : VLF = 1'b1, OIF[1:0] = 2'b10

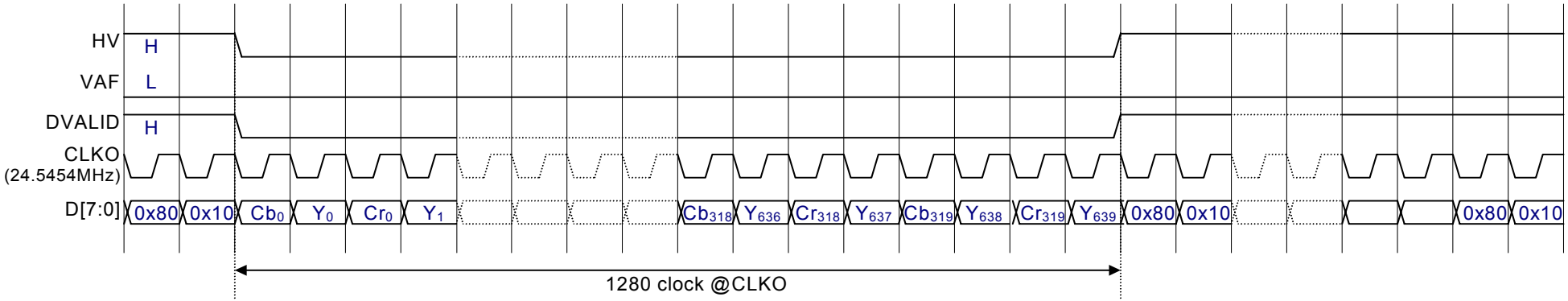


Note: In case of the output mode except VGA, 601, DVALID signal becomes active(Low) either ODD or EVEN timing. The timing chart is shown the both case for the sake of convenience.
QVGAL: Rotated QVGA, CIFL: Rotated CIF

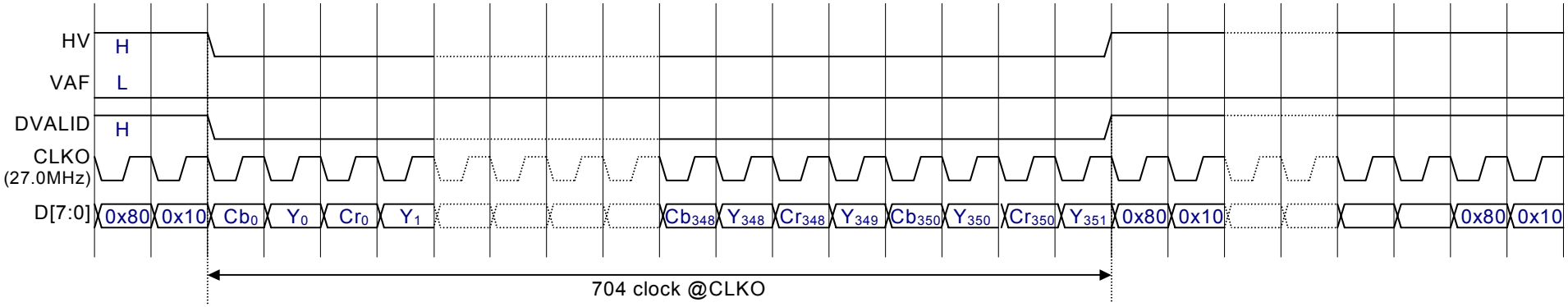
Timing Chart (Camera I/F) QVGA (NTSC) Register Set : VLF = 1'b0, OFORM[2:0] = 3'b000, OIF[1:0] = 2'b00



Timing Chart (Camera I/F) VGA (NTSC) Register Set : VLF = 1'b0, OFORM[2:0] = 3'b001, OIF[1:0] = 2'b00

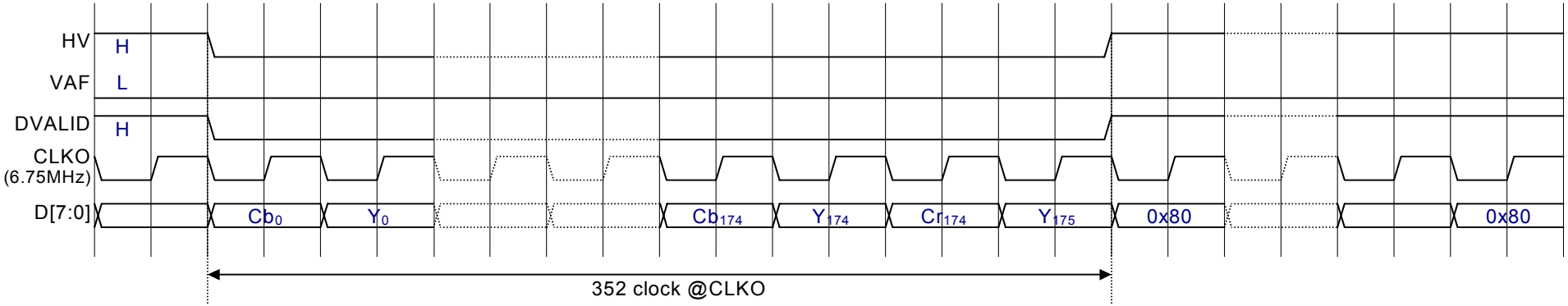


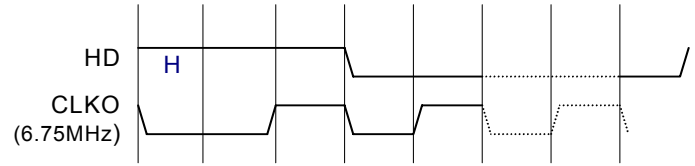
Timing Chart (Camera I/F) CIF (NTSC) Register Set : VLF = 1'b0, OFORM[2:0] = 3'b010, OIF[1:0] = 2'b00



In case of NTSC, CIF output mode, 2 Lines are output while the 1 line input. HD/VD signal are also output doubled rate.

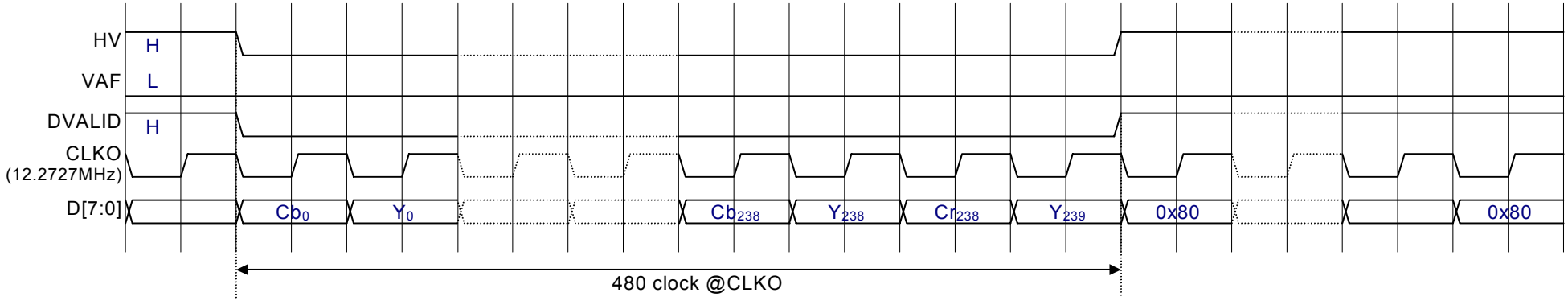
Timing Chart (Camera I/F) QCIF (NTSC) Register Set : VLF = 1'b0, OFORM[2:0] = 3'b011, OIF[1:0] = 2'b00



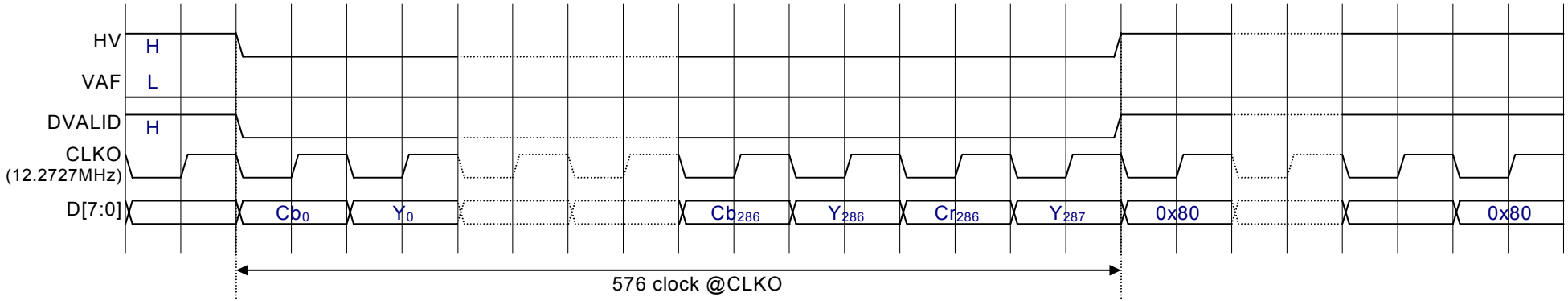


In case of QCIF, there is a possibility that the Low period of CLKO signal just before the HV falling edge becomes 1.5 longer than usual case as left chart.
Even in this case, falling edge of HV and falling edge of CLKO is same timing.

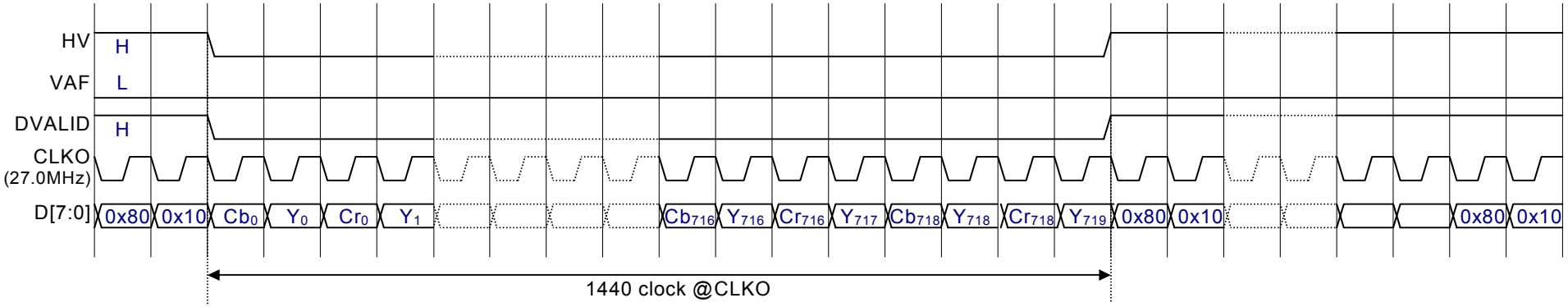
Timing Chart (Camera I/F) Rotated QVGA (NTSC) Register Set: VLF = 1'b0, OFORM[2:0] = 3'b100, OIF[1:0] = 2'b00



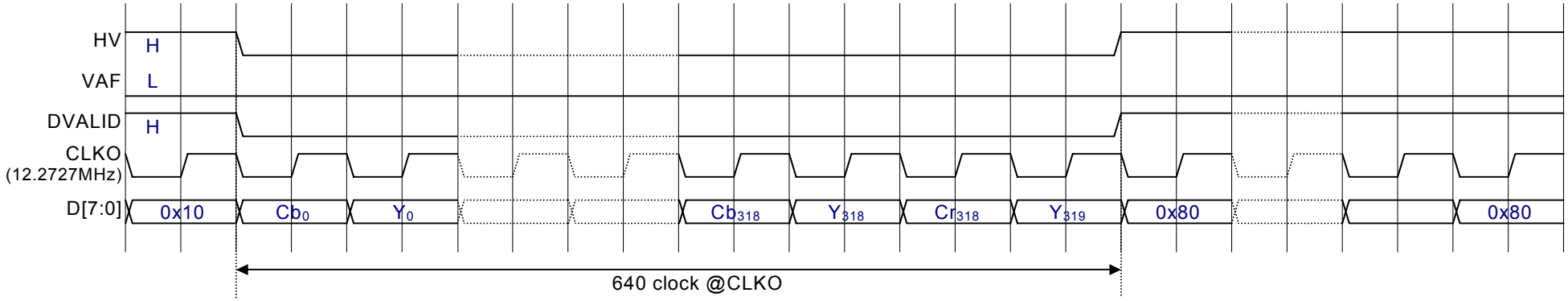
Timing Chart (Camera I/F) Rotated CIF (NTSC) Register Set: VLF = 1'b0, OFORM[2:0] = 3'b101, OIF[1:0] = 2'b00



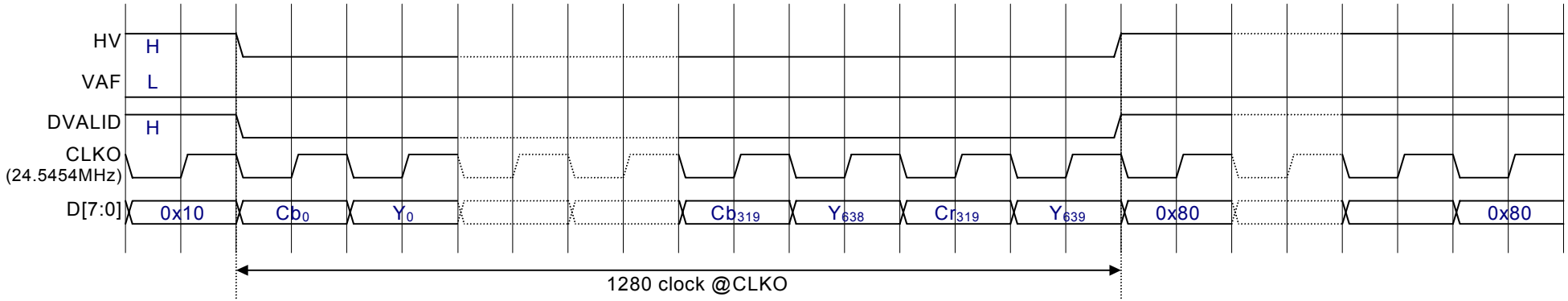
Timing Chart (Camera I/F) 601Output (NTSC) Register Set: VLF = 1'b0, OFORM[2:0] = 3'b110, OIF[1:0] = 2'b00



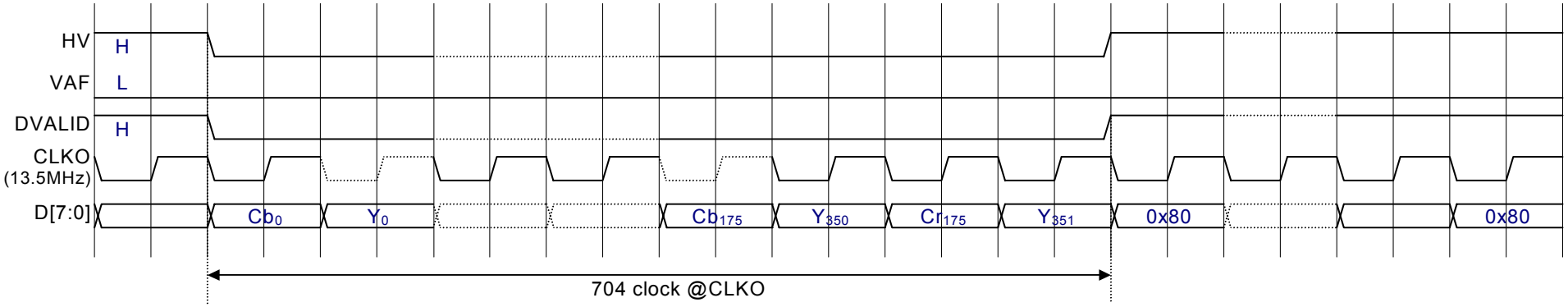
Timing Chart (Camera I/F) QVGA (PAL) Register Set: VLF = 1'b1, OFORM[2:0] = 3'b000, OIF[1:0] = 2'b00



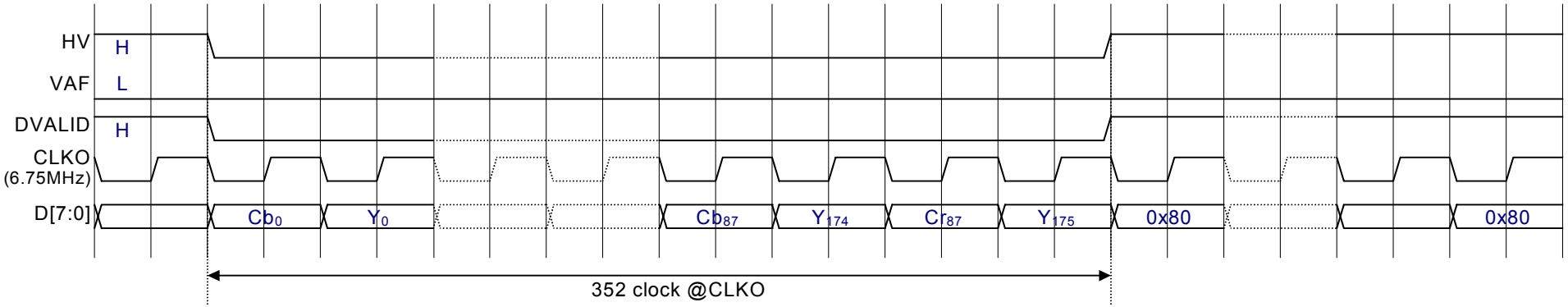
Timing Chart (Camera I/F) VGA (PAL) Register Set: VLF = 1'b1, OFORM[2:0] = 3'b001, OIF[1:0] = 2'b00

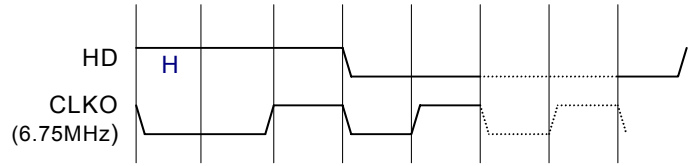


Timing Chart (Camera I/F) CIF (PAL) Register Set : VLF = 1'b1, OFORM[2:0] = 3'b010, OIF[1:0] = 2'b00



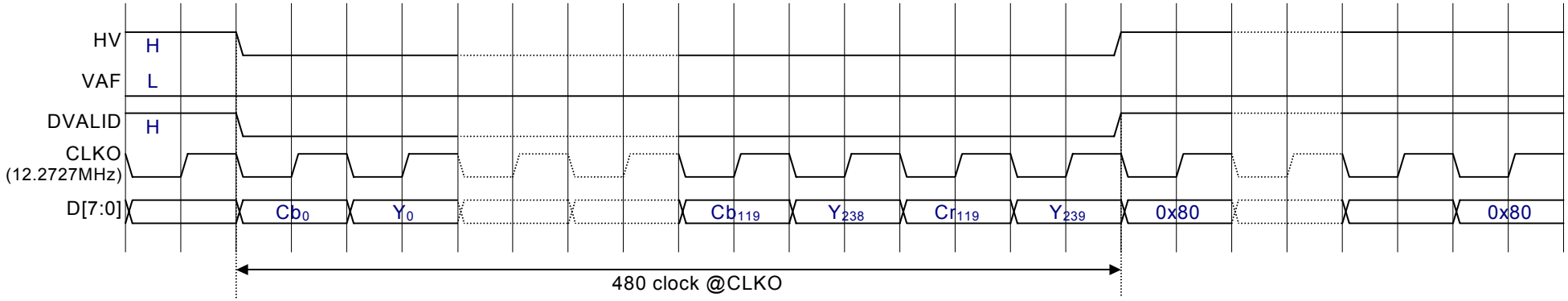
Timing Chart (Camera I/F) QCIF (PAL) Register Set : VLF = 1'b1, OFORM[2:0] = 3'b011, OIF[1:0] = 2'b00



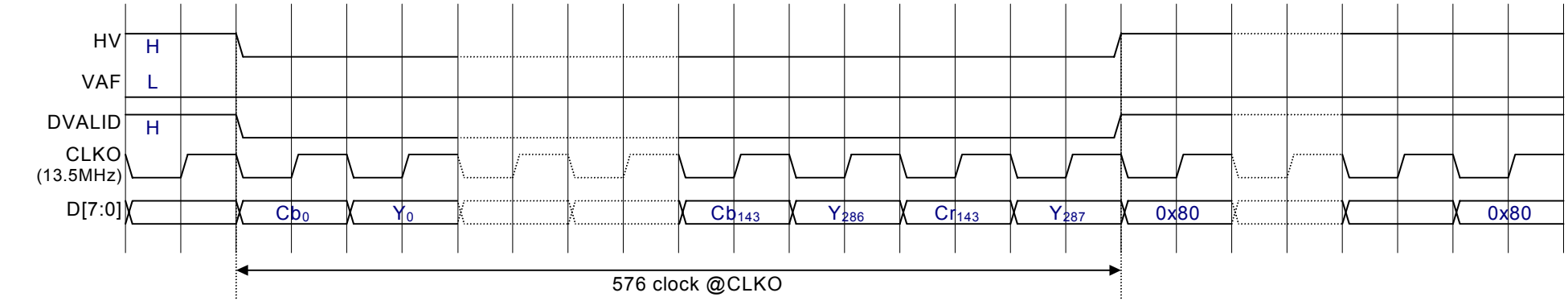


In case of QCIF, there is a possibility that the Low period of CLKO signal just before the HV falling edge becomes 1.5 longer than usual case as left chart.
Even in this case, falling edge of HV and falling edge of CLKO is same timing.

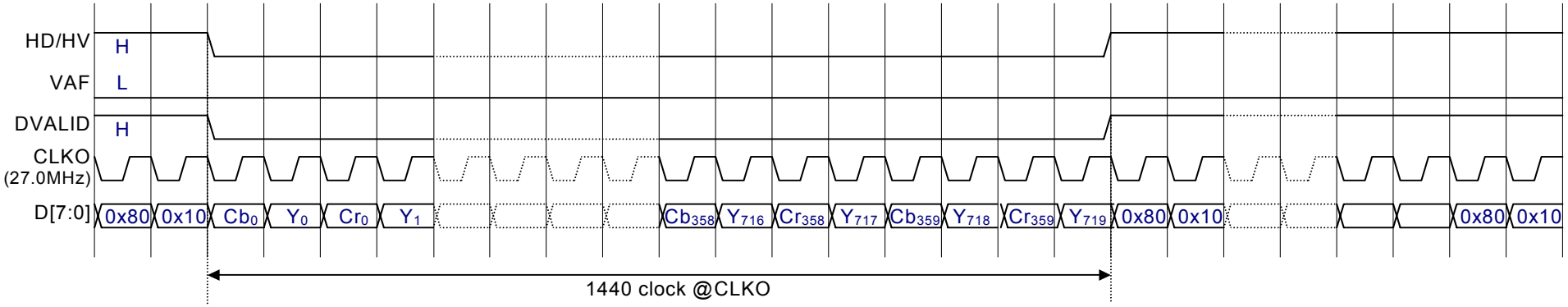
Timing Chart (Camera I/F) Rotated QVGA (PAL) Register Set: VLF = 1'b1, OFORM[2:0] = 3'b100, OIF[1:0] = 2'b00



Timing Chart (Camera I/F) Rotated CIF (PAL) Register Set: VLF = 1'b1, OFORM[2:0] = 3'b101, OIF[1:0] = 2'b00



Timing Chart (Camera I/F) 601Output (PAL) Register Set : VLF = 1'b1, OFORM[2:0] = 3'b110, OIF[1:0] = 2'b00



(2) Interface by HD / VD / DVALID

Synchronization is made by HD / VD.

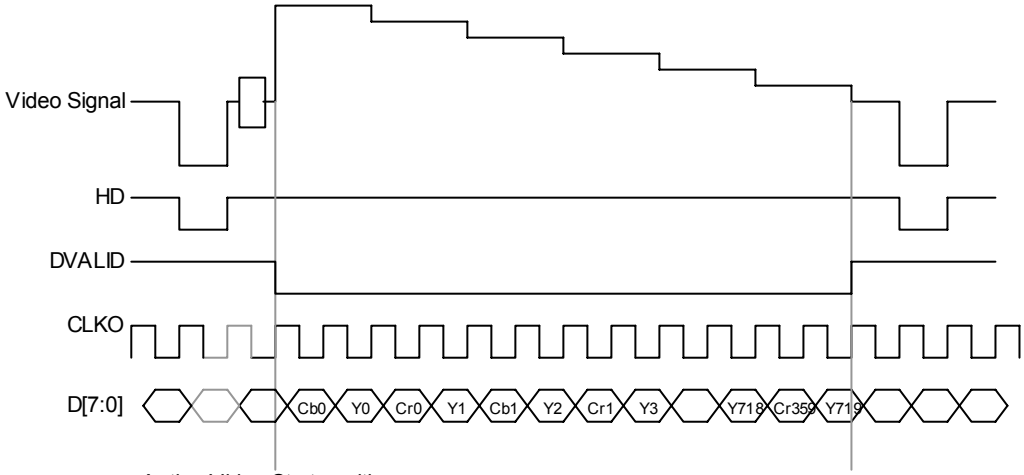
DVALID signal which becomes active during active Video interval, is used.

Since Even / Odd Field recognition is possible by HD / VD signal, interlace information is known.

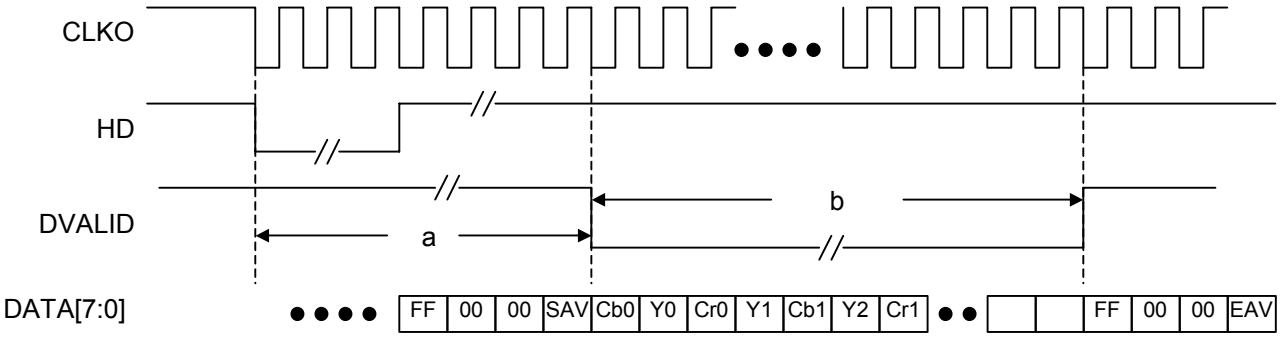
In the AK8855, data is output by DVALID signal which becomes active during active Video region.

Relation between DVALID signal and data is shown in the following diagram (example shown is at 27 MHz sampling).

DVALID signal which indicates active video interval, is output at the following timing shown below (601 output case).



Timing Diagram is shown below.



(data FF0000SAV & FF0000EAV are at Rec.656 mode. For other than Rec.656 mode, they are replaced with 10H80H10H80H data)

Mode	[OFORM2:OFROM0]	525-Line (VLF-bit = 0) Number of CLKO count			625-Line (VLF-bit = 1) Number of CLKO count		
		a	b	CLKO Rate	a	b	CLKO Rate
QVGA	000	118	640	12.2727MHz	127	640	12.2727MHz
VGA	001	236	1280	24.5454MHz	254	1280	24.5454MHz
CIF	010	130	704	27.0MHz	140	704	13.5MHz
QCIF	011	65	352	6.75MHz	70	352	6.75MHz
Rotated QVGA	100	198	480	12.2727MHz	207	480	12.2727MHz
Rotated CIF	101	150	576	12.2727MHz	159	576	12.2727MHz
601	110	244	1440	27MHz	264	1440	27.0MHz

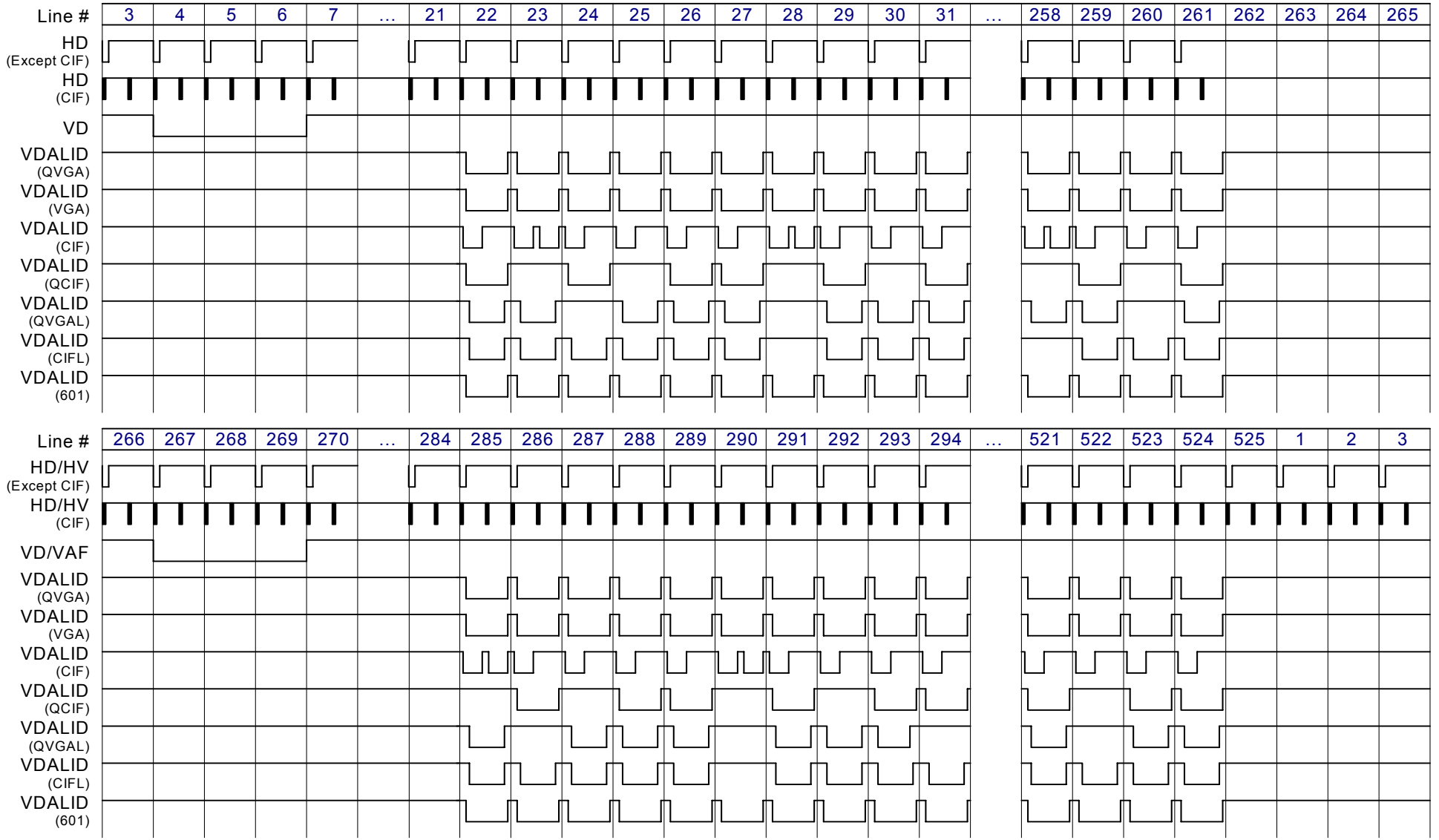
* note : output data rate of CIF size mode in 525 Line system (NTSC) is doubled.

Polarity of CLKO / HD / VD / DVALID is programmable by setting **Output Control 2 Register (R/W) [Sub Address 0x02]**.

Timing diagrams shown at next page and thereafter are for operation at HDP = 0, VDP = 0, DVALDP = 0, CLKINV = 1 settings.

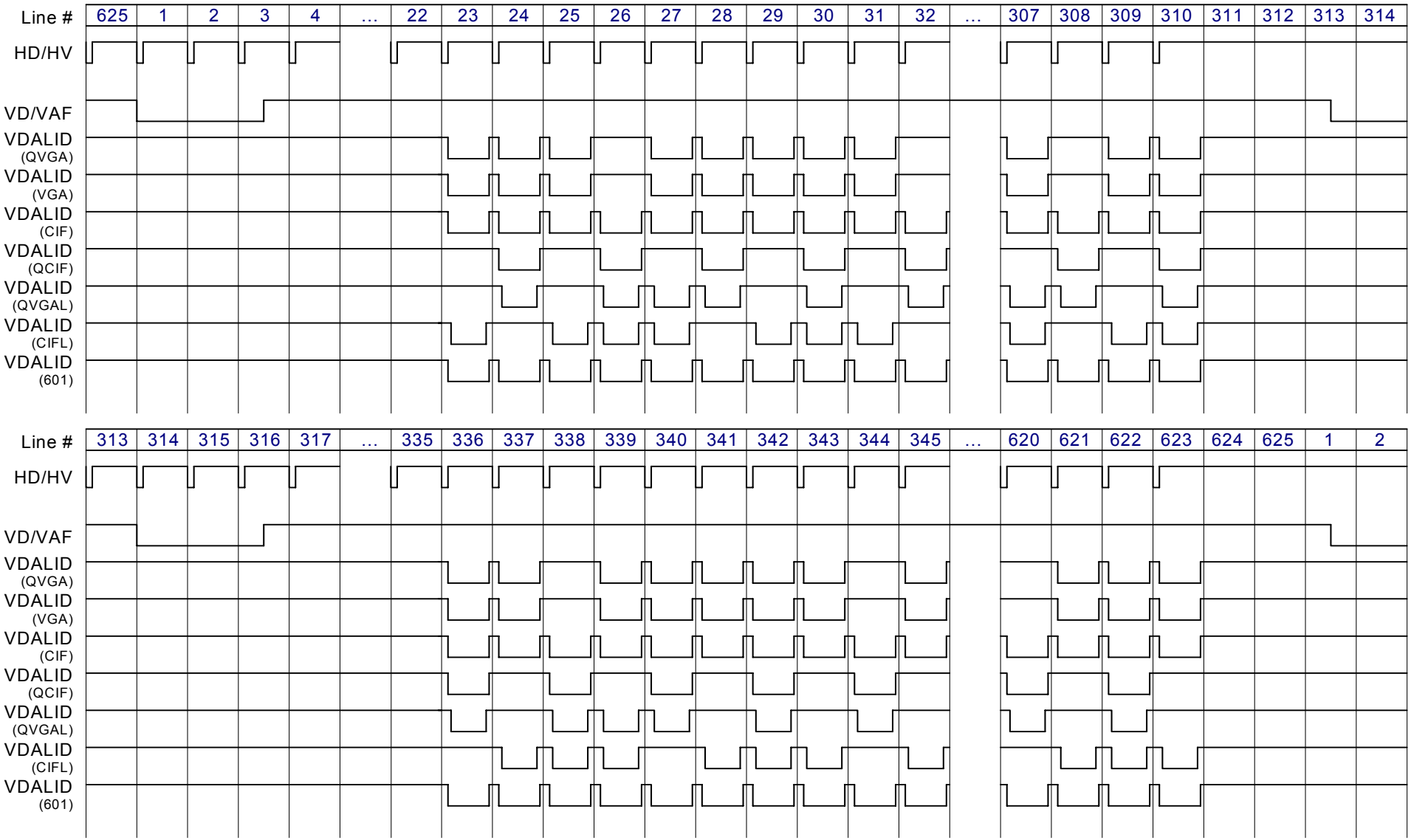
The relationship of HD/VD/DVALID are shown as follows. (The polarity of HD/VD/DVALID can be changed with register setting)

NTSC Register Set: VLF = 1'b0, OIF[1:0] = 2'b10



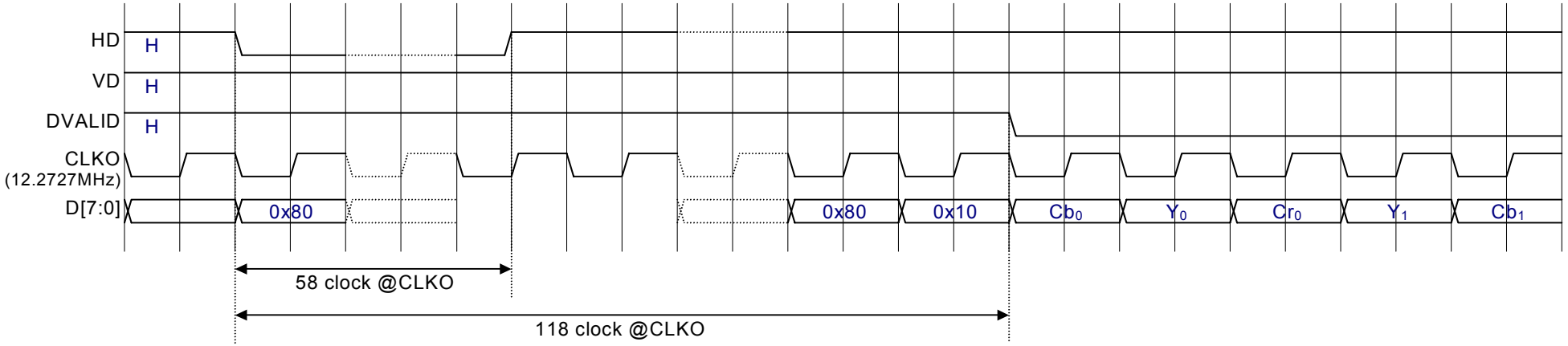
Note: In case of the output mode except VGA, 601, DVALID signal becomes active(Low) either ODD or EVEN timing. The timing chart is shown the both case for the sake of convenience. QVGAL: Rotated QVGA, CIFL: Rotated CIF

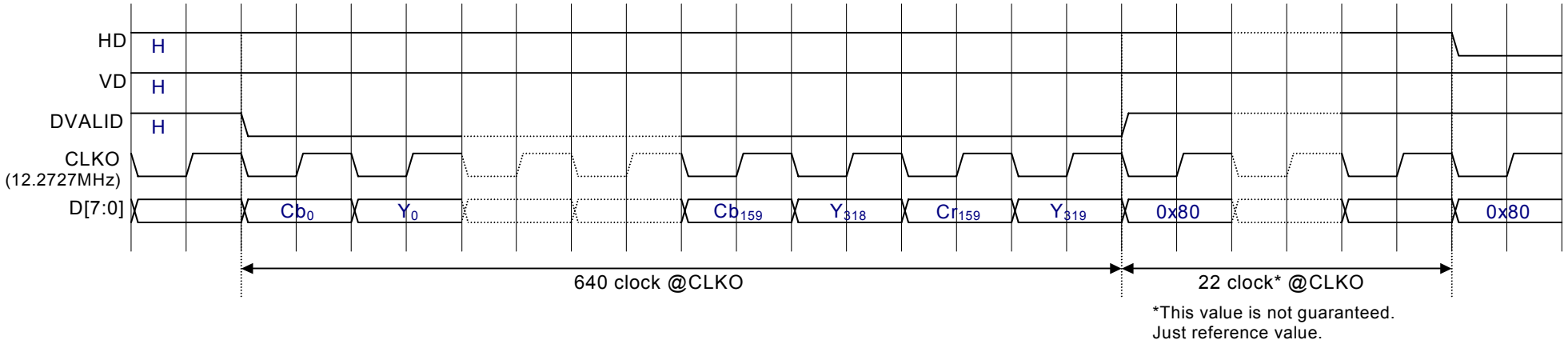
PAL Register Set: VLF = 1'b1, OIF[1:0] = 2'b10



Note: In case of the output mode except VGA, 601, DVALID signal becomes active(Low) either ODD or EVEN timing. The timing chart is shown the both case for the sake of convenience.
QVGAL: Rotated QVGA, CIFL: Rotated CIF

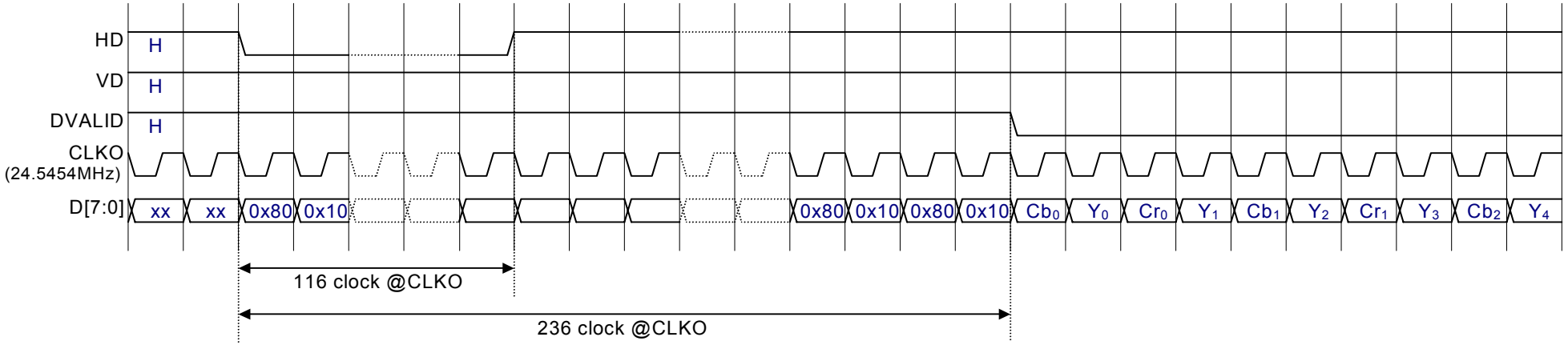
Timing Chart (HD/VD/DVALID mode) QVGA (NTSC) Register Set: VLF = 1'b0, OFORM[2:0] = 3'b000, OIF[1:0] = 2'b10

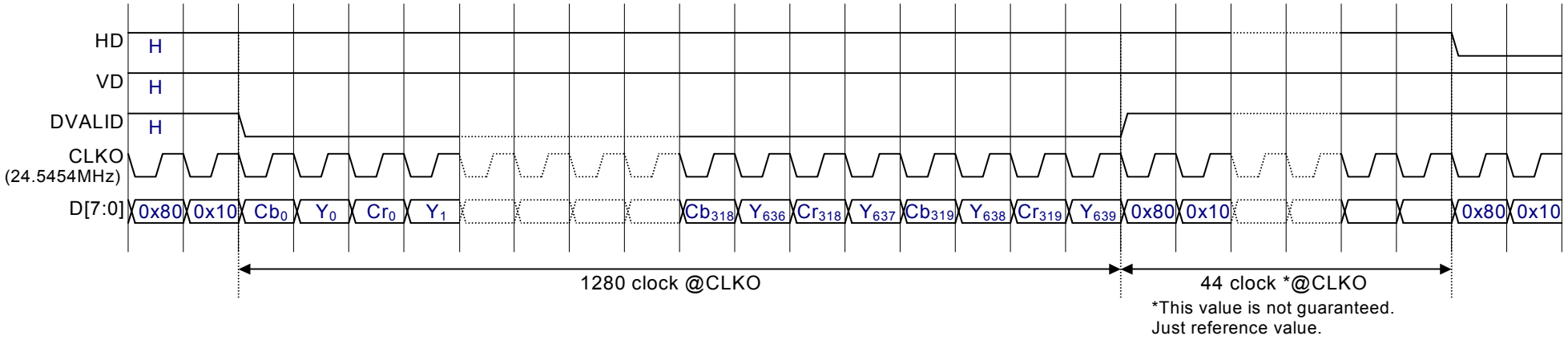




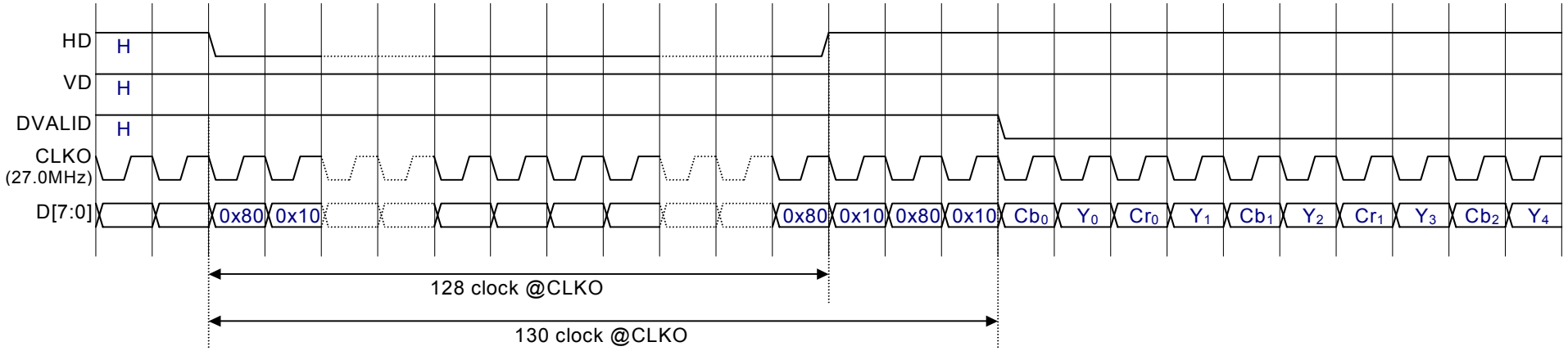
*This value is not guaranteed.
Just reference value.

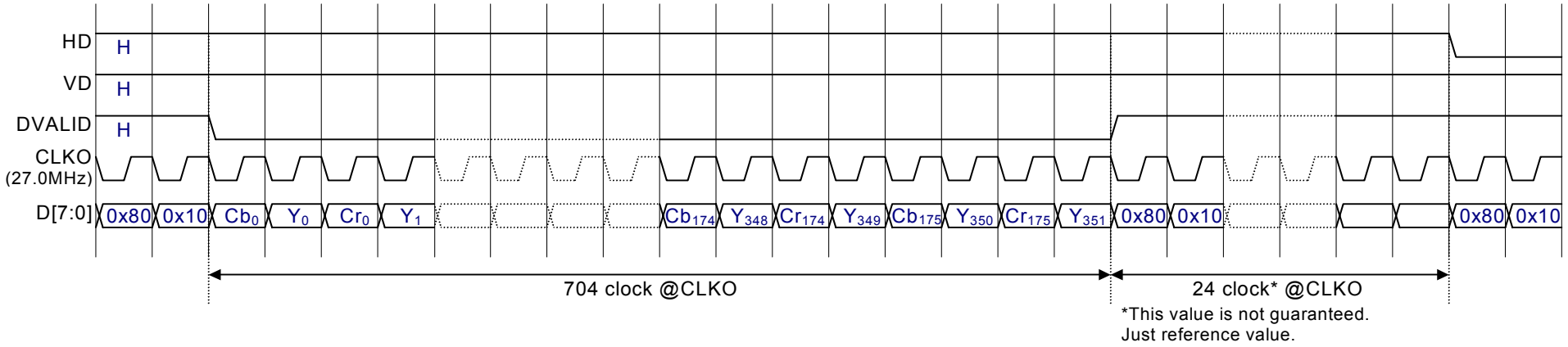
Timing Chart (HD/VD/DVALID mode) VGA (NTSC) Register set: VLF = 1'b0, OFORM[2:0] = 3'b001, OIF[1:0] = 2'b10





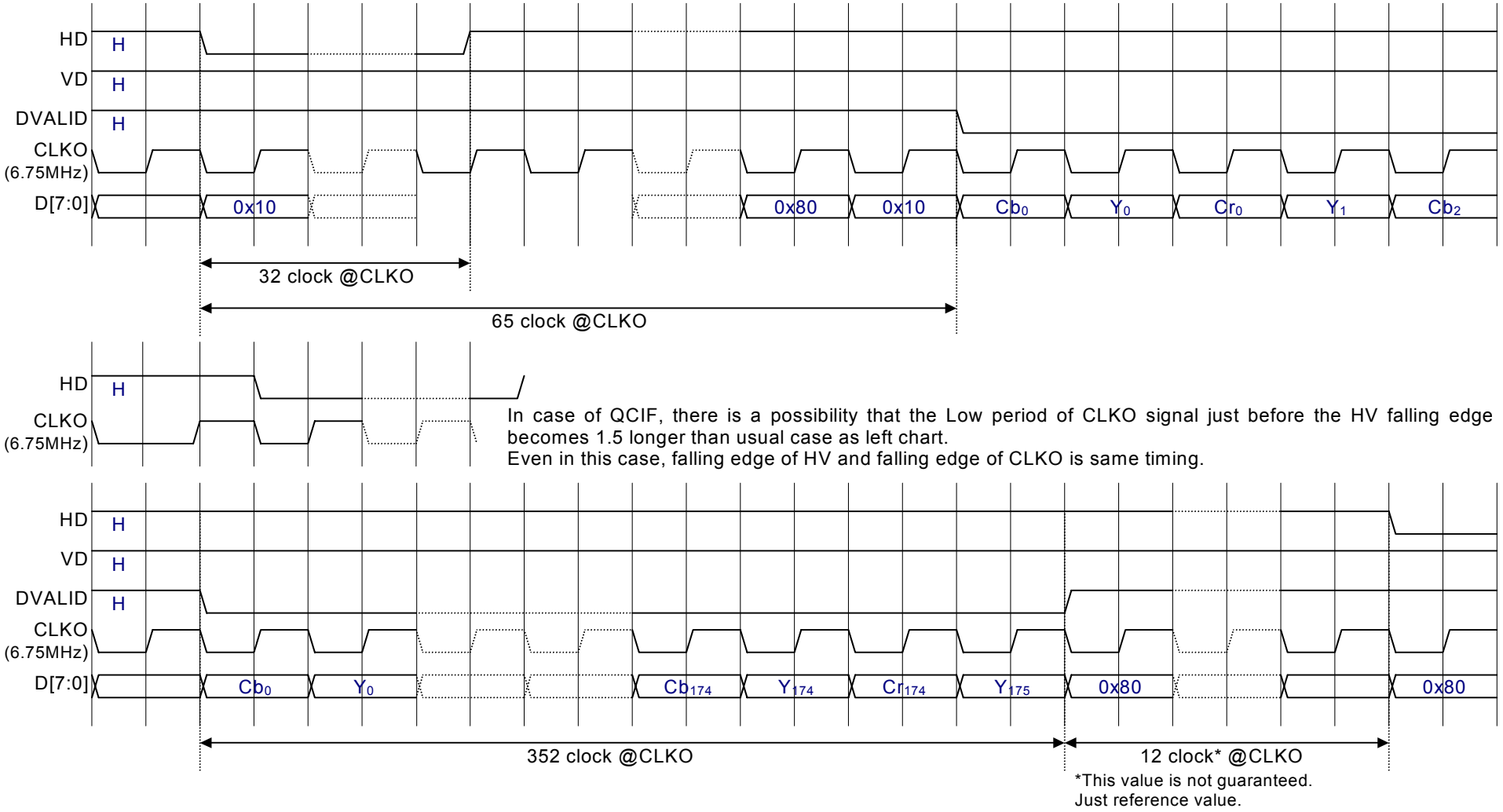
Timing Chart (HD/VD/DVALID mode) CIF(NTSC) Register Set: VLF = 1'b0, OFORM[2:0] = 3'b010, OIF[1:0] = 2'b10





In case of NTSC and CIF output mode, 2 Lines are output while the 1 line input. HD/VD signal are also output doubled rate.

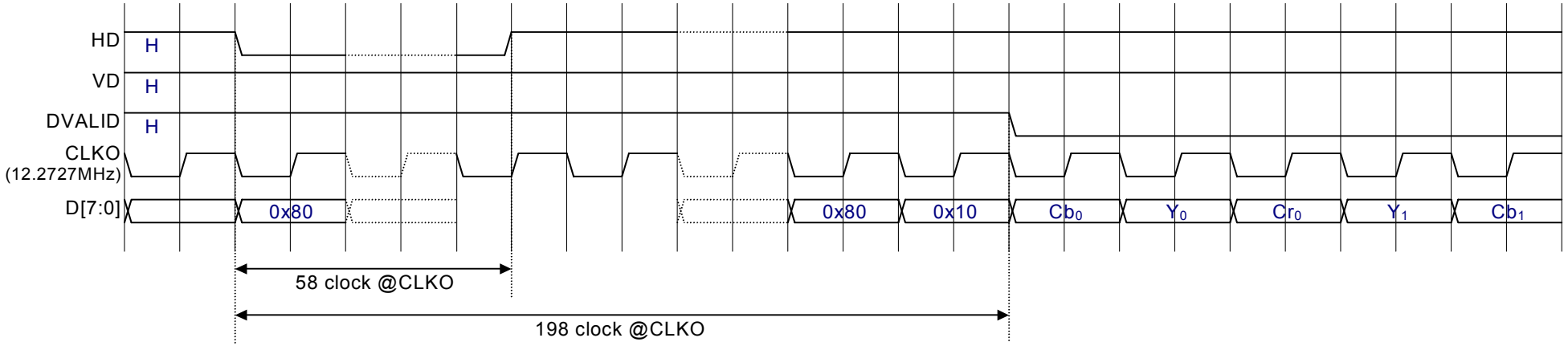
Timing Chart (HD/VD/DVALID mode) QCIF (NTSC) Register Set: VLF = 1'b0, OFORM[2:0] = 3'b011, OIF[1:0] = 2'b10

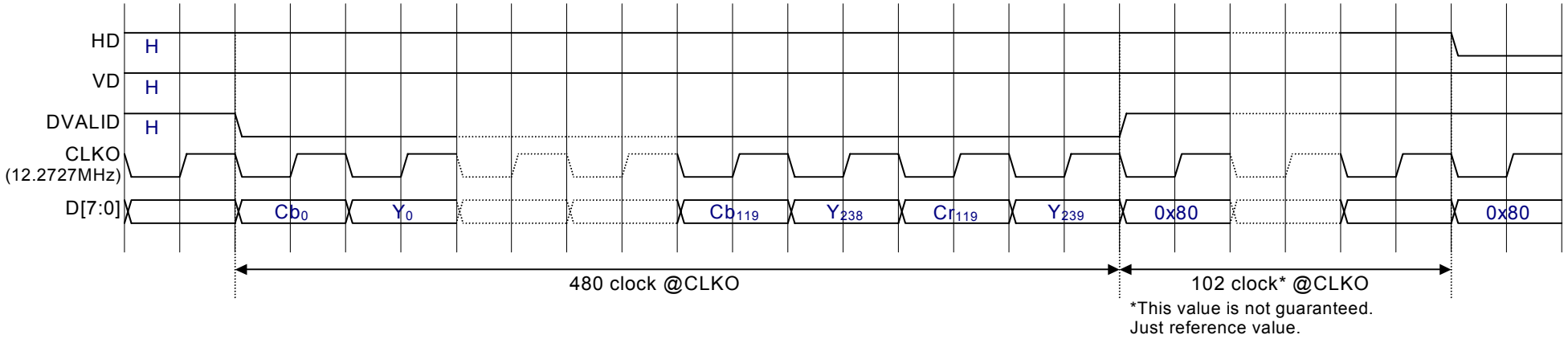


In case of QCIF, there is a possibility that the Low period of CLKO signal just before the HV falling edge becomes 1.5 longer than usual case as left chart.
Even in this case, falling edge of HV and falling edge of CLKO is same timing.

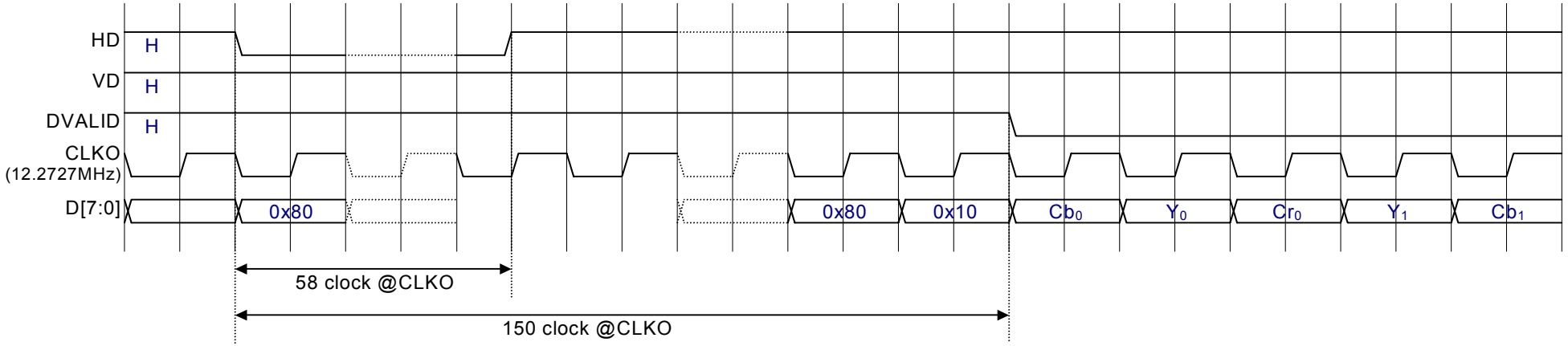
*This value is not guaranteed.
Just reference value.

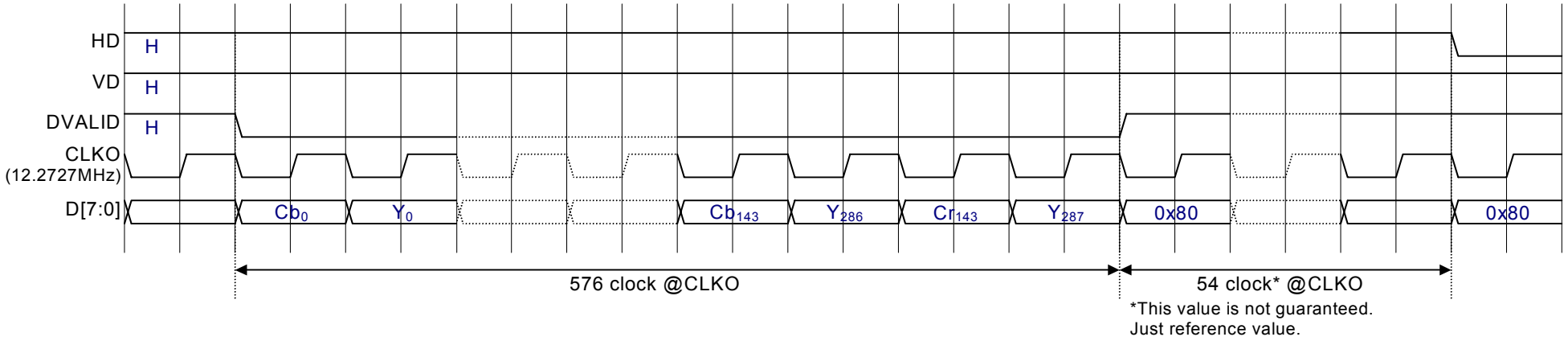
Timing Chart (HD/VD/DVALID mode) Rotated QVGA (NTSC) Register Set: VLF = 1'b0, OFORM[2:0] = 3'b100, OIF[1:0] = 2'b10



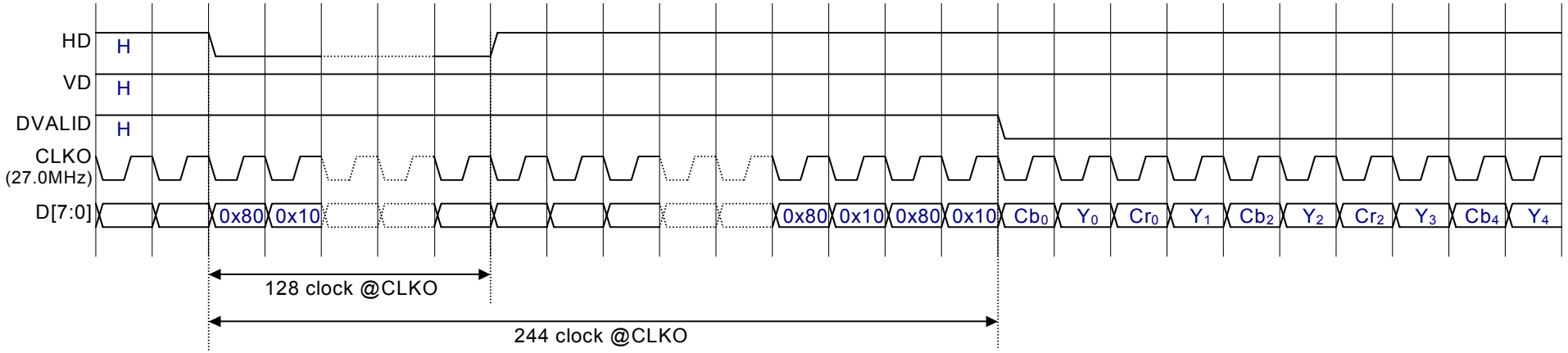


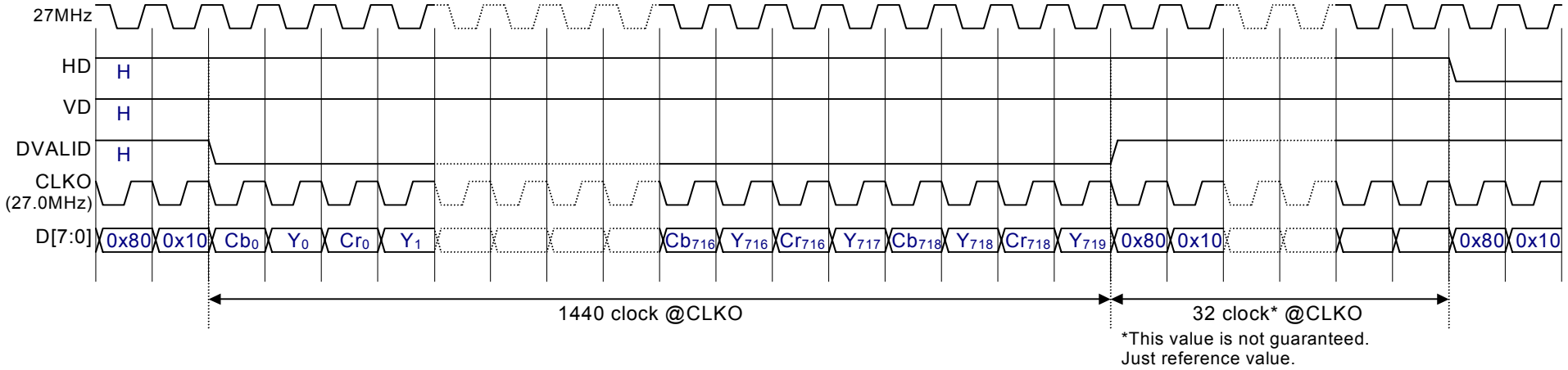
Timing Chart (HD/VD/DVALID mode) Rotated CIF(NTSC) Register Set: VLF = 1'b0, OFORM[2:0] = 3'b101, OIF[1:0] = 2'b10



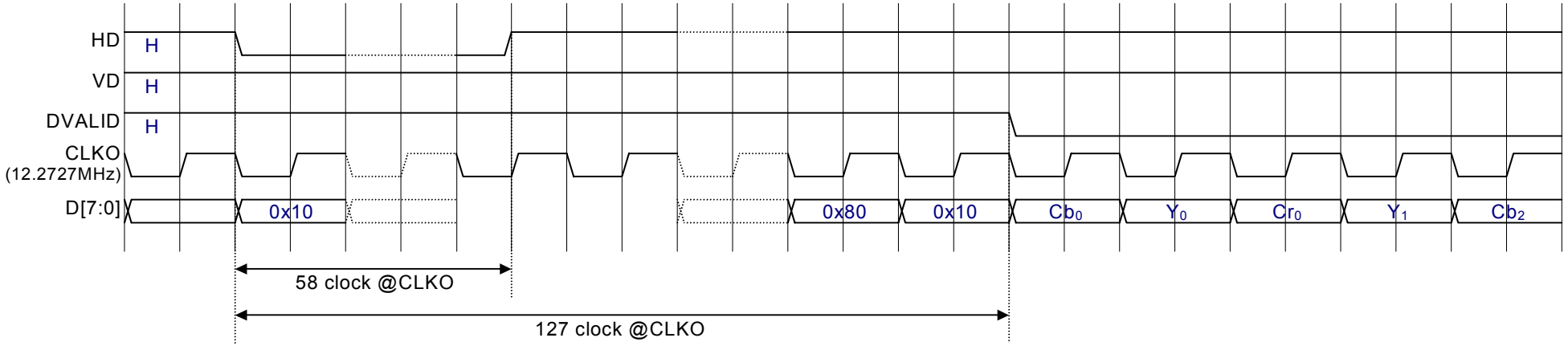


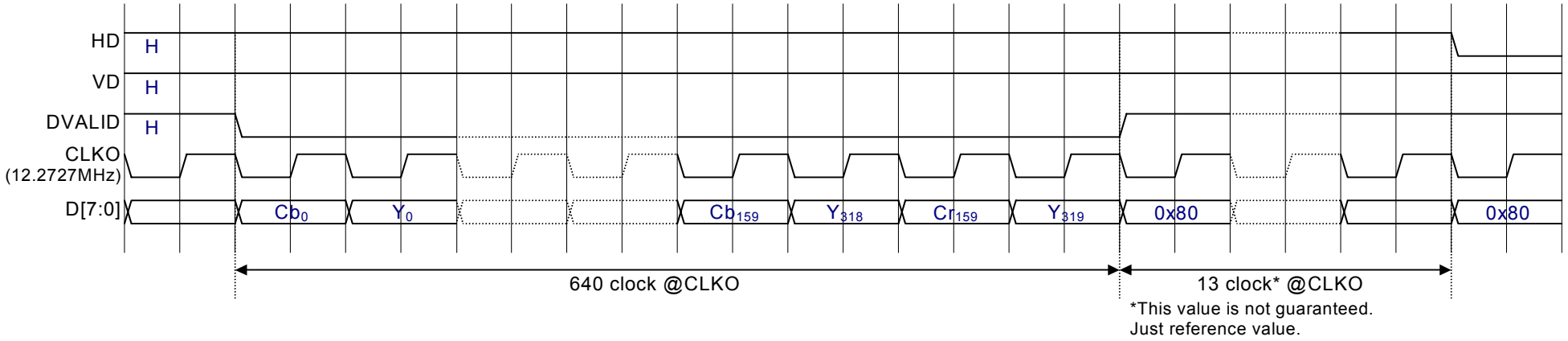
Timing Chart (HD/VD/DVALID mode) 601output (NTSC) Register Set: VLF = 1'b0, OFORM[2:0] = 3'b110, OIF[1:0] = 2'b10



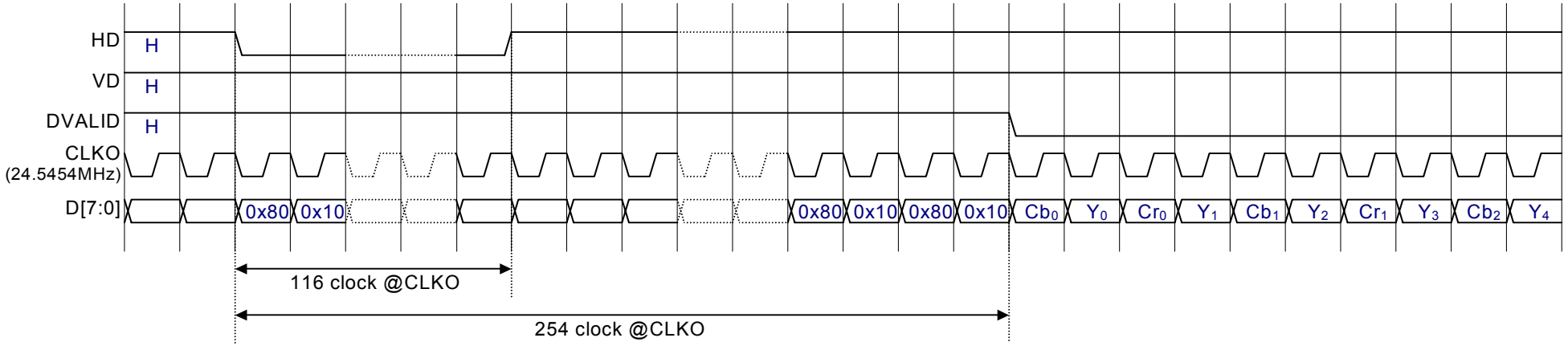


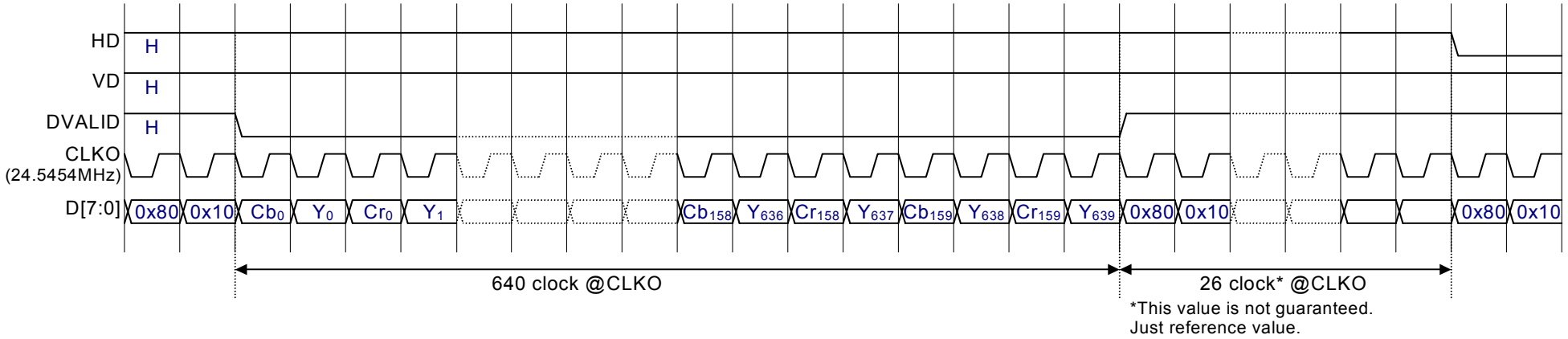
Timing Chart (HD/VD/DVALID mode) QVGA (PAL) Register Set: VLF = 1'b1, OFORM[2:0] = 3'b000, OIF[1:0] = 2'b10



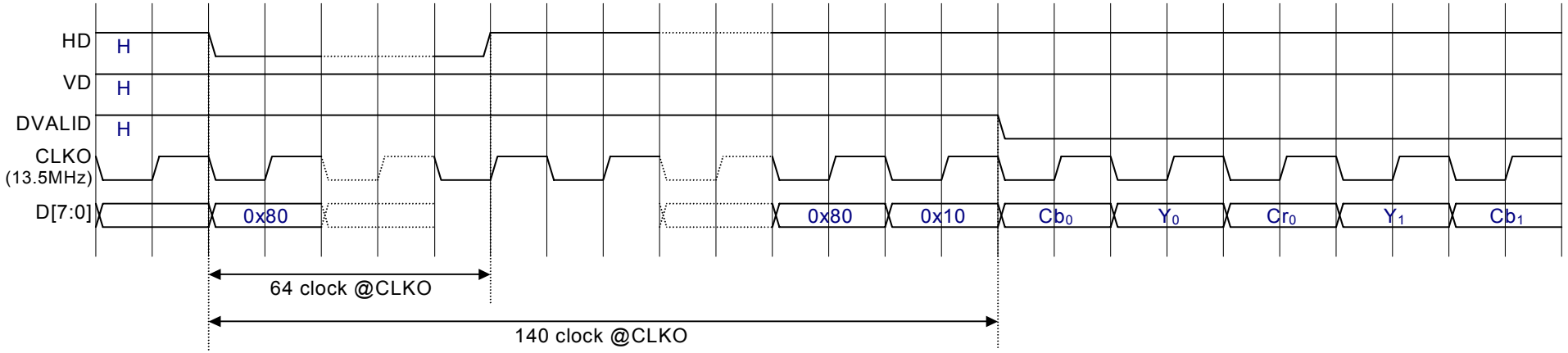


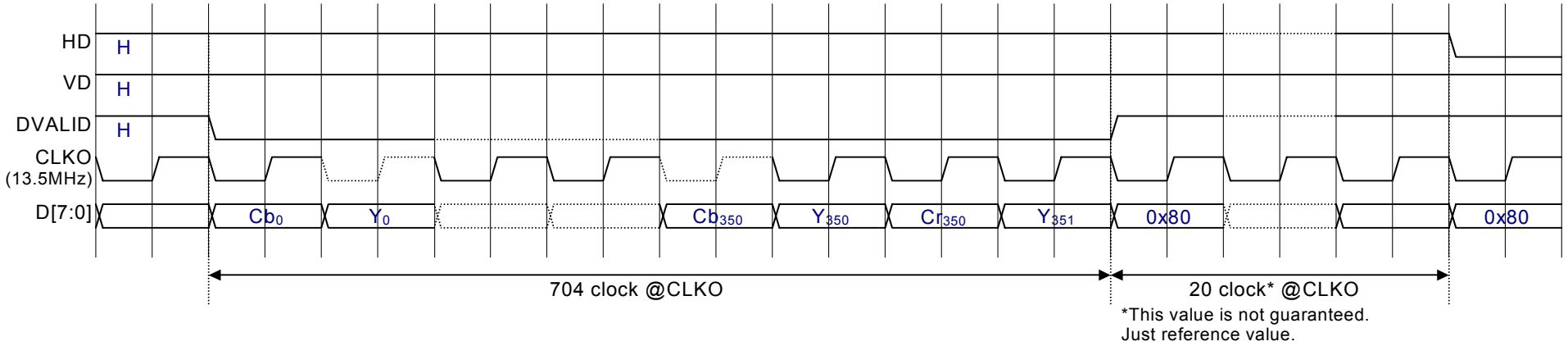
Timing Chart VGA (PAL) Register Set : VLF = 1'b1, OFORM[2:0] = 3'b001, OIF[1:0] = 2'b10



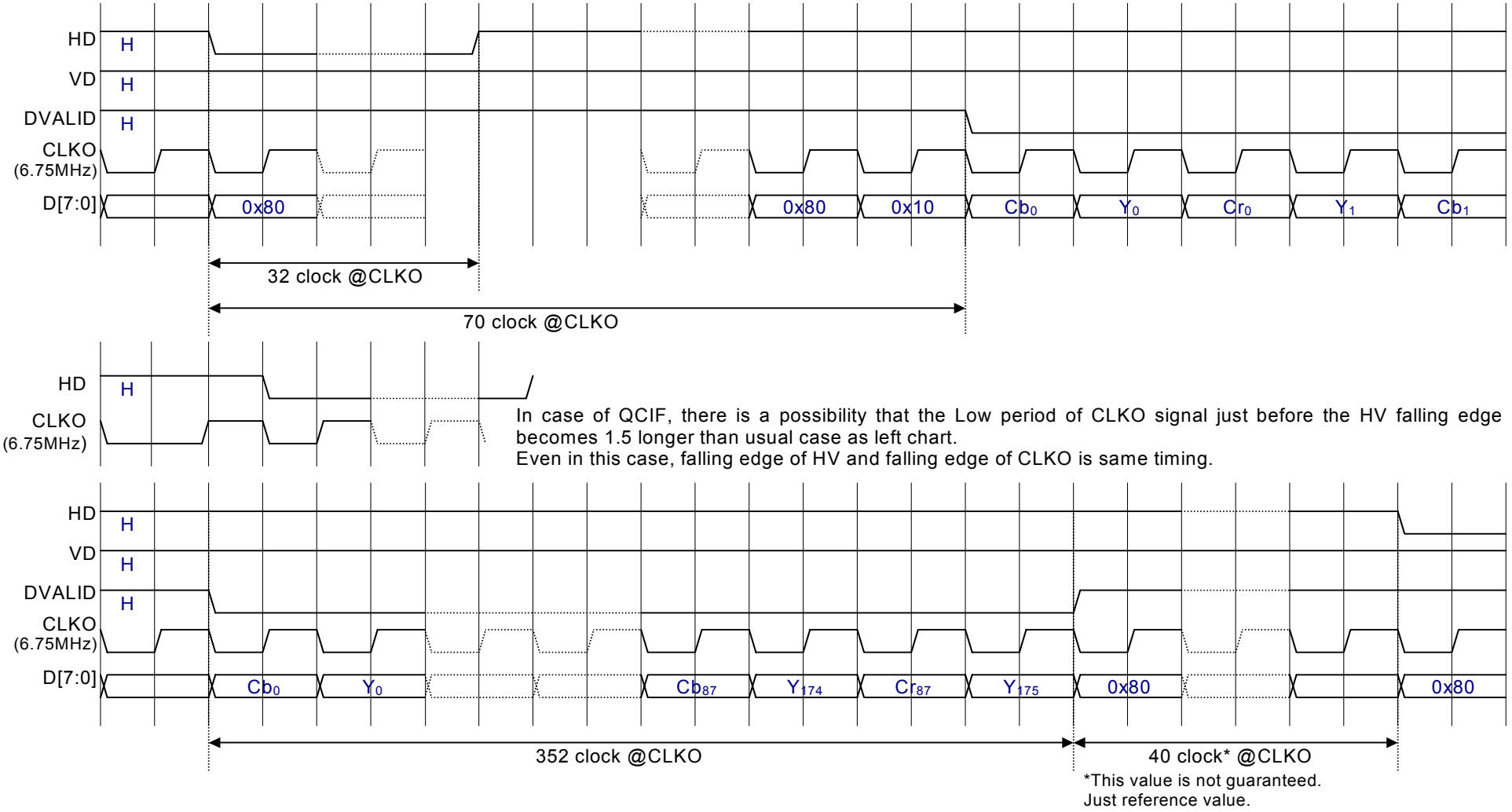


Timing Chart CIF (PAL) Register Set: VLF = 1'b1, OFORM[2:0] = 3'b010, OIF[1:0] = 2'b10

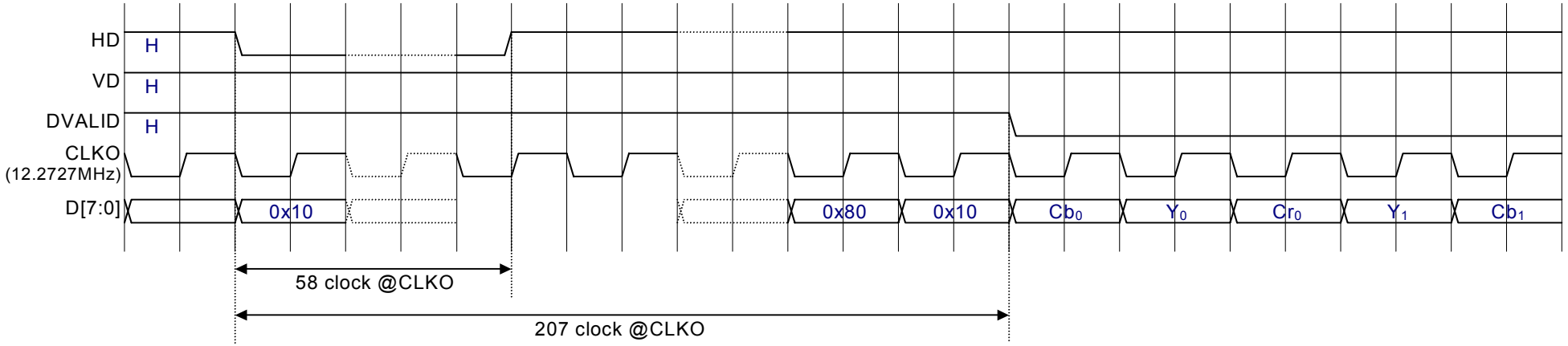


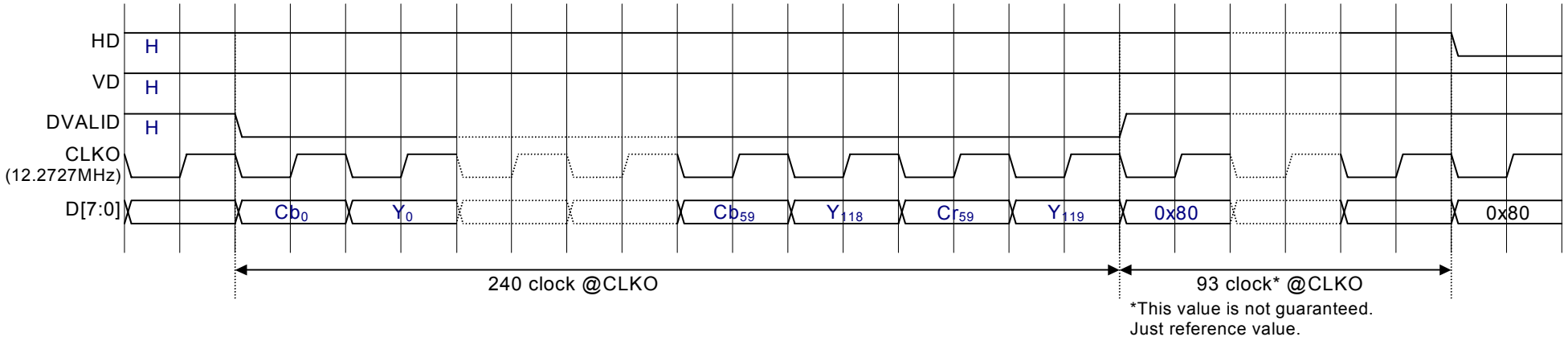


Timing Chart QCIF (PAL) Register Set : VLF = 1'b1, OFORM[2:0] = 3'b011, OIF[1:0] = 2'b10

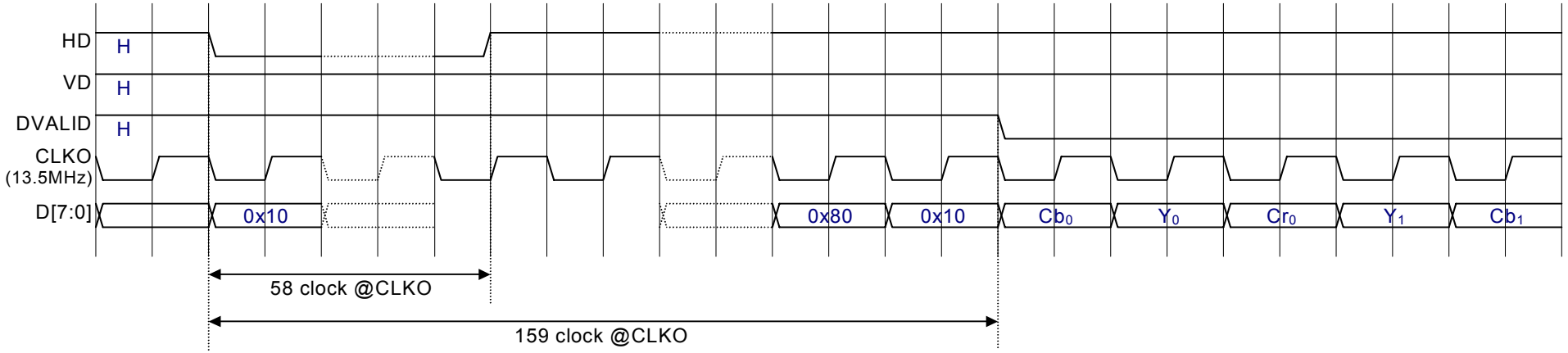


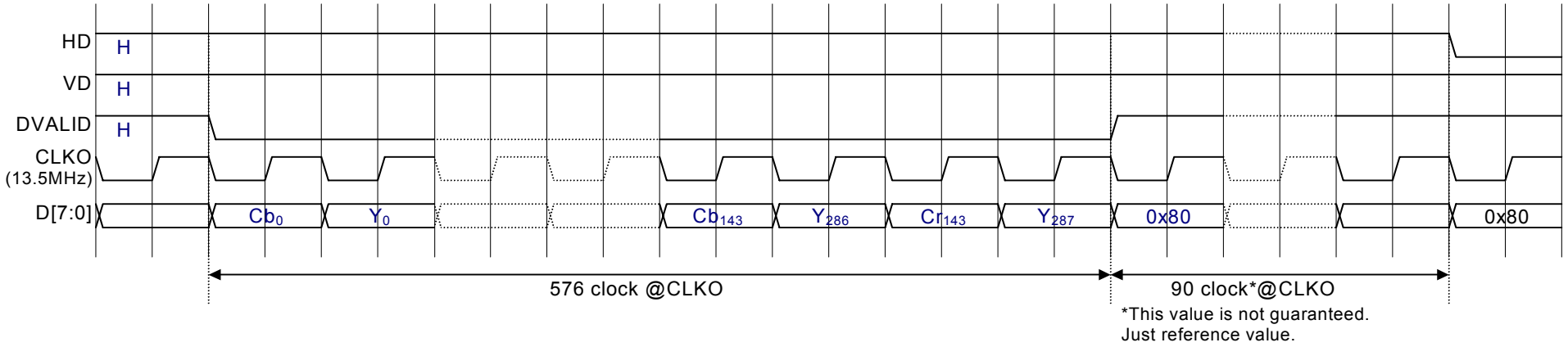
Timing Chart Rotated QVGA (PAL) Register Set : VLF = 1'b1, OFORM[2:0] = 3'b100, OIF[1:0] = 2'b10



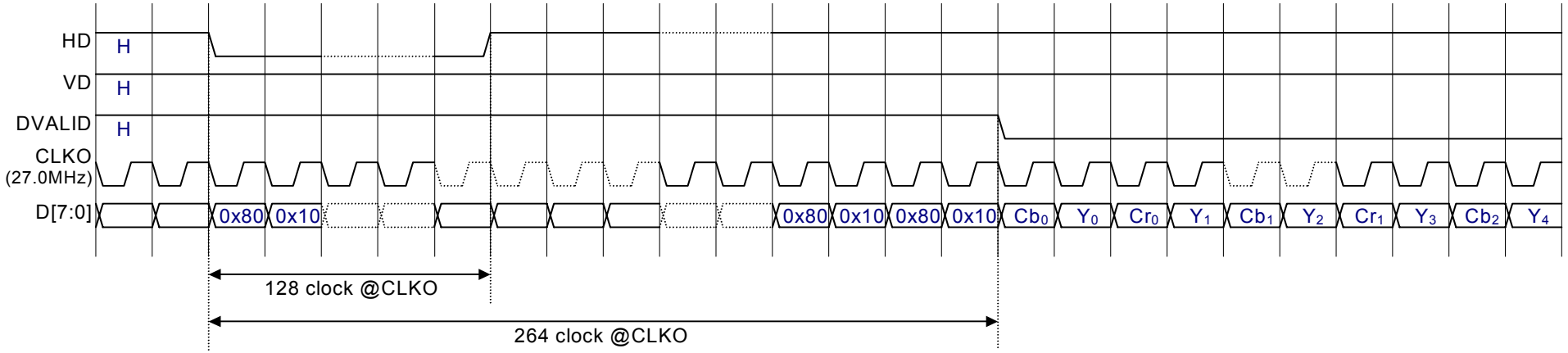


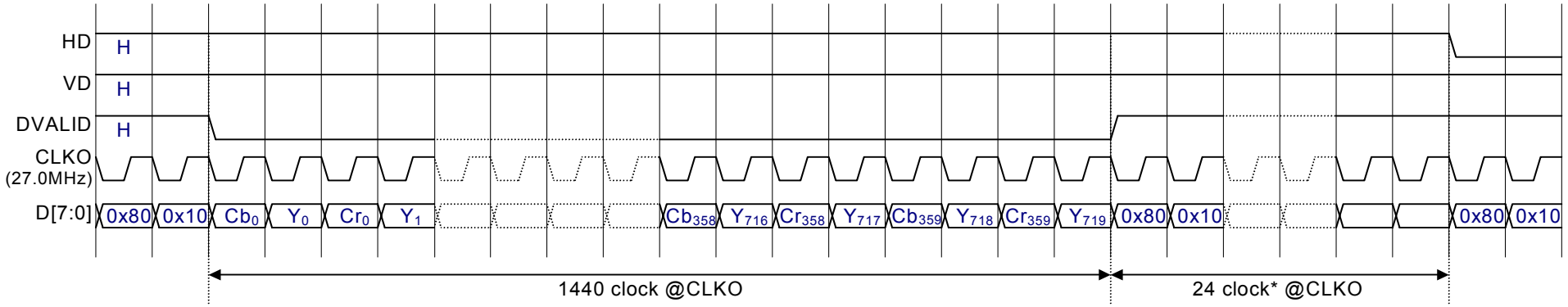
Timing Chart Rotated CIF (PAL) Register Set : VLF = 1'b1, OFORM[2:0] = 3'b101, OIF[1:0] = 2'b10





Timing Chart 601output (PAL) Register Set: VLF = 1'b1, OFORM[2:0] = 3'b110, OIF[1:0] = 2'b10





*This value is not guaranteed.
Just reference value.

(3) 656 Interface

Since synchronization with input by PLL is not made in 656 Interface mode, those specifications as [858 samples / Line, 525 Lines / Frame] and [864 samples / Line, 625 Lines / Frame] are not strictly satisfied which are specified by ITU-R BT.656.

Picture data is defined based on HSYNC, and SAV is specified.

In 656 Interface mode, HD / VD / DVALID signals are fixed to low.

HD / VD signals can be output by register setting.

Note)Relation between above mentioned various interface modes and their output format-related registers is summarized below.

Related registers are [OFORM1 : OFORM0]-bits and [OIF2 : OIF0]-bits of **Output Control 1 Register (R/W) [Sub Address 0x01]**.

[OIF1:OIF0]-bit	I/F mode	[OFORM2:OFORM0]-bit	
		110(601output mode)	Except 110 set
00	Camera I/F mode	O	O
01	Camera I/F mode (with SAV/EAV)	Not permited	O
10	HD/VD/DVALID I/F	O	O
11	Rec.656	O	Not permited

When items which are impossible to be set are selected, SAV / EAV codes are not guaranteed.

By setting [TRSVSEL]-bit of **Output Control 1 Register (R/W) [Sub Address 0x01]**, it is possible to change V-bit shift point of the 656 specified Video Timing Reference code (SAV / EAV), separately from the above
values.

By properly setting [TRSVSEL]-bit, it is possible to make the shift point of V-bit compatible with ITU-R BT.656-3
or ITU-R BT.656-4 & SMPTE125M.

Bit allocation of **Output Control 1 Register** is as follows.

Sub Address 0x01 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VDPSUP	TRSVSEL	OIF1	OIF0	LIMIT601	OFORM2	OFORM1	OFORM0
Default Value							
0	0	0	0	0	0	0	0

[TRSVSEL]-bit

TRSVSEL-bit is a control bit to specify V-bit handling within Rec 656 EAV / SAV code.

< V-bit value in Rec. 656 TRS signal and Line relation >

V-bit	NTSC(525Lines)		PAL(625Lines)	
	TRSVSEL=0 Based on ITU-R Bt.656-3	TRSVSEL=1 Based on ITU-R Bt.656-4 and SMPTE125M	TRSVSEL=0	TRSVSEL=1
V-bit = 0	Line10 ~ Line263 Line273 ~ Line525	Line20 ~ Line263 Line283 ~ Line525	Line23 ~ Line310 Line336 ~ Line623	
V-bit = 1	Line1 ~ Line9 Line264 ~ Line272	Line1 ~ Line19 Line264 ~ Line282	Line1 ~ Line22 Line311 ~ Line335 Line624 ~ Line625	

(4) About Field Signal Output

The AK8855 has a Field signal output pin.

Pin output and Field relation is shown as follows.

FIELD Signal State	field information
Low	Odd
High	Even

Value of Field signal is determined during DVALID active.

Field signal does not directly reflect input field , but it is a field signal which is forced to toggle at each VSYNC signal. Therefore, even when Odd Field only or Even Field only signal is input, Field signal also toggles.

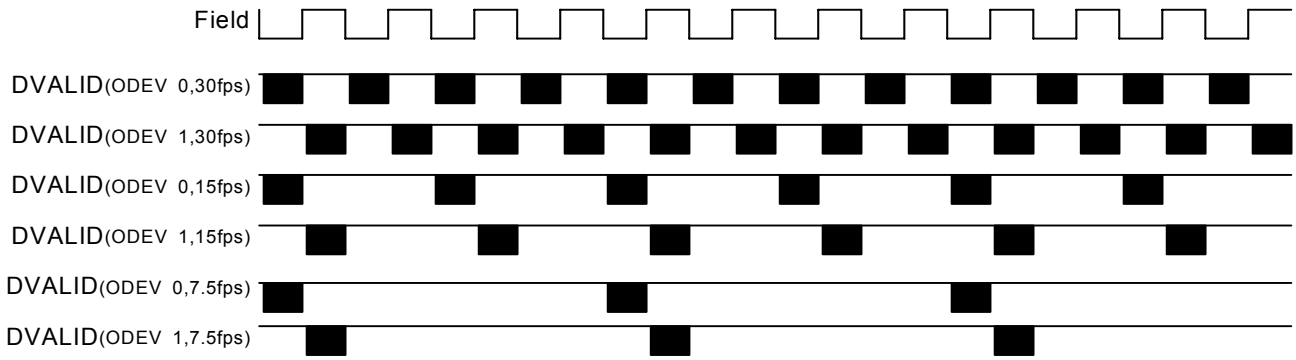
Variable Frame Rate Function

The AK8855 can vary output Frame rate.
Frame rate can be selected by [FRMRT 1 : FRMRT 0]-bits of **Control Register (R/W) [Sub Address 0x04]** as follows.

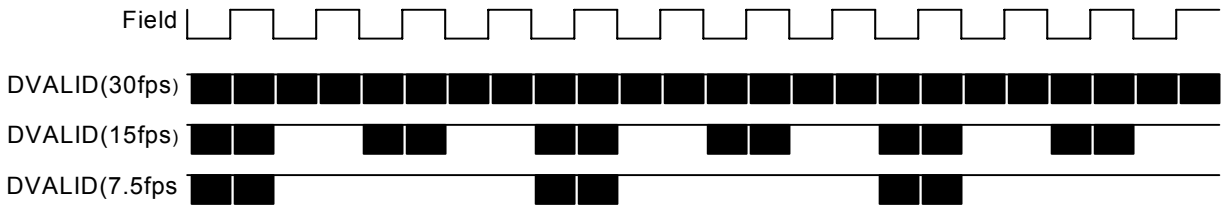
NTSC : 30 / 15 / 7.5 [fps]
PAL : 25 / 12.5 / 6.25 [fps]

Output Timing is shown as follows. ■ indicates " active ".

QVGA, CIF, QCIF, Rotated QVGA, Rotated CIF



VGA,601



Note 1 : Above diagrams are common for each of OFORM and OIF modes.
Note 2 : when OIF[1:0] = 2'b 10 is set, VD / VAF are not output but it is output even during such Field (Frame) where HD / HV, DVALID are not output.
Note 3 : in VGA, 601 mode, ODEV setting does not affect output.
Note 4 : when Vertical Sync is disturbed during switching signals etc., above timing may not temporarily be satisfied.

Digital Pixel Interpolator

This function is equipped to align pixel position in vertical direction.

Notification Function of Internal Conditions

The AK8855 has **Status Register (R/W) [Sub Address 0x10]** to notify externally the AK8855 internal condition.
Bit allocation of **Status Register** is as follows.

Sub Address 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBWSSDET	EXTDET	CCDET	AGCSTS	CPLLLCK	PKWHITE	COLKILST	NSIG

(1) No Signal Decision
The AK8855 makes a decision of no signal input condition. When it is decided to be no input signal, data output becomes Black level output (Y = 0x10, Cr / Cb = 0x80).
Its result is notified to outside by output pin NSIG and [NSIG]-bit of **Status Register**.
Output Logical State is as follows.

Signal condition	[NOSIG]-bit	NSIG pin
With signal input	0	0
No signal input	1	1

(2) COLKILST
This is to indicate that Color Killer Function has been activated as Color signal level is very small.

[COLKIL]-bit	Input level	Condition
0	Normal signal	
1	Color Killer is enabled	

(3) Input Level Overflow Notification Function
This function is activated when the decoded result of Luminance signal exceeds 255.
[PKWHITE]-bit
"1" is set to this bit when an overflow of Luminance signal is detected.
When [PKWHITE]-bit becomes "1", an overflow occurred at Luminance signal processing path.

[PKWHITE]- bit	Input level	Condition
0	Input signal overflow occurred	
1	No input overflow occurred	

(4) Color PLL Status
This is to indicate PLL Lock condition with input Color Burst signal.
[CPLLLCK]-bit

[CPLLLCK]-bit	Input level	Condition
0	It is locked with input Color Burst signal	
1	It is not locked with input Color Burst signal	

(5) AGC Status
This is to indicate status of adaptive AGC
[AGCSTS]-bit

[AGCSTS]-bit	Input level	Condition
0	Operation in Sync AGC	
1	Operation in Peak AGC	

At No Input Signal Condition

Two output modes can be selected when no Video signal is input to the AK8855.
Default value is Black code output. Setting is made by NSIGMD-bit of **Output Control 2 Register (R/W) [Sub Address 0x02]**.
Detection of no signal condition is notified by a hardware pin and **Status Register (R / W) [Sub Address 0x10]**.

[NSIGMD]-bit
This is a control bit to set output signal processing when no signal is input.

[NSIGMD]-bit	Output signal when no signal is input	Condition
0	Black code output	Y = 0x10 Cb/Cr = 0x80
1	Input signal is directly output as is.	So-called " Sand-Storm " mode output.

Power-Down Mode

The AK8855 has a power-saving wait mode function.
PDN pin is used to put the AK8855 into power-saving mode, including digital block. By setting this pin to low, all blocks in Analog and Digital parts are put into power-saving mode.
Recover from the power-saving mode by PDN pin , a Reset sequence must be executed.

When to turn down power supplies except for PVDD, a power-down sequence must be followed, using PDN pin and then turn-down AVDD /DVDD after power-down condition is established.
It is recommended to fix the digital output pins to PVDD power supply or to set OE pin = high (high output).

Output Pin Condition

Output pins of the AK8855 are controlled by OE (Output Enable) pin and RSTN pin conditions.
Output pin conditions are :

	After Power up	RSTN = Low	After Reset sequence	
			PDN = Low	PDN = High
OE = High	unknown	Hi-z	High	Data output
OE = Low	Hi-z	Hi-z	Hi-z	Hi-z

Note) there is a possibility that leak current may flow at OE = Low (Hi-Z condition).
It is recommended that output pins are set to same PVDD potential or OE pin is set to High in Power-Down mode setting.
Pins to be controlled by OE pin are, CLKO, D [7 : 0], FIELD, HD / HV, VD / VAF, NSIG and DVALID pins.

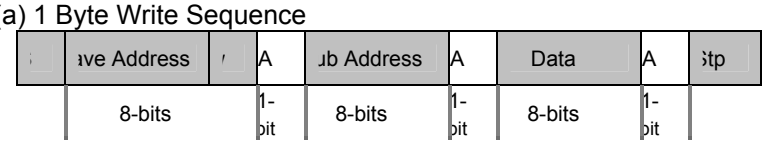
Device Control Interface

The AK8855 is controlled via I2C Bus Control Interface.

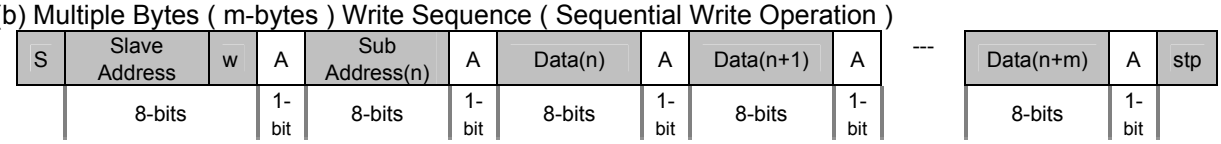
[I2C SLAVE Address]
I2C Slave Address is 0x88

[I2C Control Sequence]
(1) Write Sequence
When the Slave Address of the AK8855 Write mode is received at the first byte, Sub Address at the second byte
and Data at the third and succeeding bytes are received.
There are 2 operations in Write Sequence - a sequence to write at every single byte, and a sequential write operation to write multiple bytes successively.

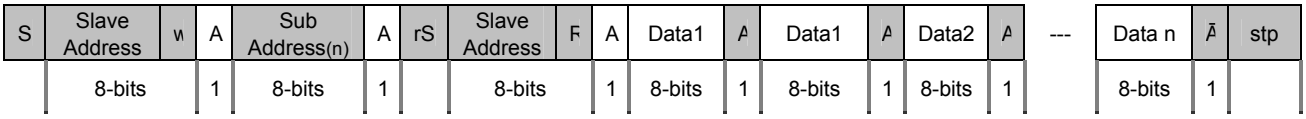
(a) 1 Byte Write Sequence



(b) Multiple Bytes (m-bytes) Write Sequence (Sequential Write Operation)



(2) Read Sequence
When the Slave Address of the AK8855 Read mode is received, Data at the second and succeeding bytes are transmitted.



Note) At Sequential Read Operation, the first byte Read-out Data is repeatedly output (this does not happen in a normal, single byte Read operation).

Abbreviated terms listed above mean :

S, rS : Start Condition
A : Acknowledge (SDA Low)
A- : Not Acknowledge (SDA High)
stp : Stop Condition
R/W 1 : Read 0 : Write
: to be controlled by the Master Device. Micro-computer interface is output normally .
: to be controlled by the Slave Device. To be output by the AK8855.

Register Definition

Sub Address	Register	Defa-ult	R/W	Function
0x00	Input Video standard Register	0x00	R/W	To set the Input signal Standard
0x01	Output Control 1 Register	0x00	R/W	To set output picture sizes etc
0x02	Output Control 2 Register	0x00	R/W	To set output characteristics of output pins
0x04	Control Register	0x00	R/W	Various control registers.
0x05	PGA Control Register	0x46	R/W	PGA Control Register
0x06	Contrast Control Register	0x80	R/W	Contrast Control Register
0x07	Brightness Control Register	0x00	R/W	Brightness Control Register
0x08	Saturation Control Register	0x80	R/W	Saturation Control Register
0x09	HUE Control Register	0x00	R/W	HUE Control Register
0x0A	Request VBI Info Register	0x00	W	Request VBI Info Register
0x10	Status Register		R	Status Register
0x11	Macrovision Status Register		R	Macrovision Status Register
0x12	Closed Caption 1 Register		R	Closed Caption Data 1 register
0x13	Closed Caption 2 Register		R	Closed Caption Data 2 register.
0x14	Extended Data 1 Register		R	Closed Caption Extended Data 1 register.
0x15	Extended Data 2 Register		R	Closed Caption Extended Data 2 register.
0x16	VBID/WSS 1 Register		R	VBID (CGMS-A) / WSS1 Data register
0x17	VBID/WSS 2 Register		R	VBID (CGMS-A) / WSS 2 Data register
0x18	Device & Revision ID Register	0x37	R	Device & Revision ID Register

Input Video Standard Register (R/W) [Sub Address 0x00]

Register to set input signal

Sub Address 0x00 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	AINSEL	VLF	VCEN	VSCF1	VSCF0
Default Value							
0	0	0	0	0	0	0	0

Input Video Standard Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	VSCF0 ~ VSCF1	Sub carrier Frequency	R/W	to set Sub-carrier frequency of input video signal VSCF1 - VSCF0 [MHz] 00 : 3.57954545 01 : 3.57561188 10 : 3.5820558 11 : 4.43361875
bit 2	VCEN	Video Color Encode	R/W	to set Color Encoding System of input video signal. 0: NTSC 1: PAL
bit 3	VLF	Video Line Frequency	R/W	to set Line Frequency of input video signal. 0 : 525 Lines 1 : 625 Lines
bit 4	AINSEL	AIN Select bit	R/W	to select AIN Input Select switch. 0: to decode AIN 1 1: to decode AIN 2
bit 5 ~ bit 7	Reserved	Reserved	R/W	Reserved

Output Control 1 Register (R/W) [Sub Address 0x01]

Register to set the output data format.

Sub Address 0x01 **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VDPSUP	TRSVSEL	OIF1	OIF0	LIMIT601	OFORM2	OFORM1	OFORM0
Default Value							
0	0	0	0	0	0	0	0

Output Control 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	OFORM1 ~ OFORM2	Output Format Set bit	R/W	to set output picture sizes. 000: QVGA 001: VGA (interlaced output) 010: CIF 011: QCIF 100: rotated QVGA (240 X 180) 101: rotated CIF (288 X 216) 110: 601 output 111: Reserved
bit 3	LIMIT601	601 Output Limit	R/W	to set Min. / Max. of output data. 0 : 1 - 254 (Y / Cb / Cr) 1 : 16 - 235 (Y) / 16 - 240 (Cb / Cr) when “1” is set at LIMIT601 register, data smaller than 16 is clipped to 16 and data larger than 235 / 240 (Y / Cb, Cr) is clipped to 240.
bit 4 ~ bit 5	OIF0 ~ OIF1	Output interface set bit	R/W	to set output interface mode. 00: Camera Interface mode (without SAV / EAV) 01: Camera Interface mode (with SAV / EAV) 10: HD / VD mode 11: 656 Interface mode In setting modes of 01 / 11, HD / VD output is fixed to low.
bit 6	TRSVSEL	Time Reference Signal V Select bit	R/W	to switch shift line of V-bit of EAV / ASAV which is included in TRS. This register is valid when OFORM [2:0] = 110. **NTSC system (at 525 Line input)** TRSVSEL=0 : V = 1 when Line 1 ~ Line 9 / Line 264 ~ Line 272 V = 0 when Line 10 ~ Line 263 / Line 272 ~ Line 525 TRSVSEL=1: V = 1 when Line 1 ~ Line 19 / Line 264 ~ Line 282 V = 0 when Line 20 ~ Line 263 / Line 283 ~ Line 525 **PAL system (at 625 Line input)** Regardless of set value of TRSVSEL-bit, V = 1 when Line 1 ~ Line 22 / Line 311 ~ Line 355 / Line 624 ~ Line 625 V = 0 when Line 23 ~ Line 310 / Line 336 ~ Line 623
bit 7	VDPSUP	VD Pulse SUPress	R/W	When Frame Rate Variable Function is activated in HD / VD mode and 656 I / F mode, 0 : VD / VAF pulse is not output at the Frames which are not active. 1 : VD / VAF pulse is output even at the Frames which are not active.

Output Control 2 Register (R/W) [Sub Address 0x02]

Register to set polarity of output pin and to set output condition when no input signal is fed.

Sub Address 0x02 **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OF_OFF	NSIGMD	DVALACT	HVACT	CLKINV	DVALIDP	VDP	HDP
Default Value							
0	0	0	0	0	0	0	0

Output Control 2 Register Definition

BIT	Register Name		R/W	Definition
bit 0	HDP	HD pin Polarity set bit	R/W	to set polarity of HD signal. 0: Active Low 1: Active High
bit 1	VDP	VD pin Polarity set bit	R/W	to set polarity of VD signal. 0: Active Low 1: Active High
bit 2	DVALDP	DVALID pin Polarity set bit	R/W	to set polarity of DVALID signal. 0: Active Low 1: Active High
bit 3	CLKINV	CLK invert set bit	R/W	to set polarity of CLKO. 0: normal output (data should be taken at the rising edge) 1: phase relation between data and clock is inverted (data should be taken at the falling edge).
bit 4	HVACT	HD/VD action bit	R/W	to output HD & VD in EAV / SAV Interface mode. no output (fixed to low) 1 : to output
bit 5	DVALACT	DVALID action bit	R/W	to output DVALID signal in EAV / SAV Interface mode. 0: no output (fixed to low) 1: to output
bit 6	NSIGMD	No SiGnal Output MoDe	R/W	to decide output condition when no signal input condition is detected. 0 : to output Black level 1 : to output input condition directly as is (“ Sand-Storm “ condition).
bit 7	OF_OFF	OutputFilter_OFF bit	R/W	to turn off the vertical interpolator filter in the rotated QVGA output operation. 0 : with vertical interpolator filter 1 : without vertical interpolator filter

Reserved Register (R/W) [Sub Address 0x03]

Sub Address 0x03 **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default Value							
0	0	0	0	0	0	0	0

Reserved Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	Reserved	Reserved Register	R/W	Reserved

Control Register (R/W) [Sub Address 0x04]

Control Register

Sub Address 0x04 **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNTSEL	DTFIX	ODEV	FRMRT1	FRMRT0	COLKIL	ACC	AGC
Default Value							
0	0	0	0	0	0	0	0

Control Register Definition

BIT	Register Name		R/W	Definition
bit 0	AGC	AGC set bit	R/W	0 : AGC disabled (PGA manual setting is possible) 1 : AGC enabled
bit 1	ACC	ACC set bit	R/W	0 : ACC Disable 1 : ACC Enable
bit 2	COLKIL	Color Killer Set bit	R/W	0 : Color Killer enabled 1 : Color Killer disabled
bit 3 ~ bit 4	FRMRT0 ~ FRMRT1	Frame Rate Set bit	R/W	to set Frame Rate [Frame / sec] FRMRT 1:0 (525 / 625) 00: 30/25 01: 15/12.5 10: 7.5/6.25 11: Reserved
bit 5	ODEV	ODD Even Select bit	R/W	to set decode field when QVGA / CIF / QCIF decodings are made. 0 : to decode Odd Field 1 : to decode Even Field
bit 6	DTFIX	DaTa Fix control bit	R/W	to fix data in the data path while data is not output. 0 : OFF 1 : ON (data in the Data path is fixed)
bit 7	CNTSEL	Contrast mode select bit	R/W	to set the start point of Contrast adjustment 00 : Contrast varies, starting at Luminance level of 128 (gray) as a center value. 1 : Contrast varies, starting at Luminance level of 16 (black) as a center value.

PGA Control Register (R/W) [Sub Address 0x05]

Register to set gain of PGA.
When AGC function is enabled, gain value set by AGC is set to this register.

Sub Address 0x05 **Default Value: 0x46**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA6	PGA5	PGA4	PGA3	PGA2	PGA1	PGA0
Default Value							
0	1	0	0	0	1	1	0

PGA Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 6	PGA0 ~ PGA6	PGA Gain Set	R/W	to set gain of PGA. PGA can be adjusted in approximately 0.1 dB / step.
bit 7	Reserved	Reserved	R/W	Reserved

Note) when to read this register while AGC is enabled, the PGA value which is set by AGC is returned.
It is possible to write value by user (user-set-value) while AGC is enabled, but its value is not written to PGA.
A returned value made by register read operation also becomes above mentioned AGC set-value.
When AGC is disabled, user-set-value is valid, and its value (user-set-value) is returned by Register Read operation.

Contrast Control Register (R/W) [Sub Address 0x06]

Register to make Contrast Adjustment. Default value 0x80 corresponds to un-adjusted value.

Sub Address 0x06 **Default Value: 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Default Value							
1	0	0	0	0	0	0	0

Contrast Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	CONT0 ~ CONT7	Contrast Control	R/W	to make Contrast Adjustment. Setting can be made in 1 / 256 step and setting range is from 0 to 255 / 128. Default value is 0x80.

Brightness Control Register (R/W) [Sub Address 0x07]

Register to make Brightness Adjustment. Default value 0x00 corresponds to un-adjusted value.

Sub Address 0x07 **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
Default Value							
0	0	0	0	0	0	0	0

Brightness Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	BR0 ~ BR7	Brightness Control	R/W	to make Brightness Adjustment. Setting is made in 2's complement number.

Saturation Control Register (R/W) [Sub Address 0x08]

Register to make Color Saturation Adjustment. Default value corresponds to un-adjusted value.

Sub Address 0x08 **Default Value: 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
Default Value							
1	0	0	0	0	0	0	0

Saturation Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	SAT0 ~ SAT7	Saturation Control	R/W	to make Saturation Adjustment. Setting value can be made in 1 / 256 step and setting range is from 0 to 255 / 128. SAT7:SAT0 0 : 0 x (no color exists) 0xff : 255 / 128 x

HUE Control Register (R/W) [Sub Address 0x09]

Register to make Hue Adjustment. Default value 0x00 corresponds to un-adjusted value.

Sub Address 0x09 **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
Default Value							
0	0	0	0	0	0	0	0

HUE Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	HUE0 ~ HUE7	HUE Control	R/W	to make Hue adjustment. Setting should be made in 2's complement number. Default value is 0x00. Setting is made in 1 / 256 step (approximately 0.35 degree step), which ranges +/- 45 degrees.

Request VBI Info Register (W) [Sub Address 0x0A]

Register to request decoding of VBLANK information such as Closed Caption Data / Extended Data / VBID (CGMS) / WSS Data etc.

When “1” is written to the decode request bit of each VBLANK information, the AK8855 is put into Data Decode Ready state and waits for Data.
After decoding is completed, “1” is written to CCDET-bit / EXTDET-bit / VBWSSDET-bit which correspond to a **Status Register (R / W) [Sub Address 0x10]** Request, and decoded data are written to
Closed Caption Data 1 / 2 Registers, Extended Data 1 / 2 Registers and VBID / WSS Data 1/ 2 Registers respectively.

Sub Address 0x0A **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	VBWSRQ	EXTRQ	CCRQ
Default Value							
0	0	0	0	0	0	0	0

Request VBI Info Register Definition

BIT	Register Name		R/ W	Definition
bit 0	CCRQ	Closed Caption Data Decode Request	W	to request decoding of Closed Caption Data 0 : - 1 : decode request
bit 1	EXTRQ	Extended Data Decode Request	W	to request decoding of Extended Data 0 : - 1 : decode request
bit 2	VBWSRQ	VBID Data Decode Request	W	to request decoding of VBID / WSS Data 0 : - 1 : decode request
bit 3 ~ bit 7	Reserved	Reserved	W	Reserved

Note)
when “1” is written to RQ-bit, CCDET-bit / EXTDET-bit / VBWSSDET-bit are cleared to “0” which correspond to a Status Register Request.

Status Register (R/W) [Sub Address 0x10]

Register to indicate internal conditions of the AK8855.

Sub Address 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBWSSDET	EXTDET	CCDET	AGCSTS	CPLLLCK	PKWHITE	COLKILST	NSIG

Status Register Definition

BIT	Register Name		R/W	Definition
bit 0	NOSIG	No Signal	R	to judge existence / non-existence of input signal. 0 : signal is being input 1 : no signal input condition
bit 1	COLKILST	Color killer	R	to judge if Color Killer is active or not. 0 : Color Killer is in-active 1 : Color Killer process is active
bit 2	PKWHITE	Peak White Detection	R	to detect if AD-converted input signal is over-flowing or not. 0 : normal 1 : input level is over-flowing
bit 3	CPLLLCK	Color PLL Locked Flag	R	to show Lock condition of Color PLL 0 : PLL is locked 1 : PLL is not locked
bit 4	AGCSTS	AGC Status bit	R	0 : Sync AGC operation 1 : Peak AGC operation
bit 5	CCDET	Closed Caption Detect	R	to show that decoded data exist at Closed Caption Data 1 / 2 registers. 0 : no Closed Caption Data exists 1 : decoded Closed Caption Data exists
bit 6	EXTDET	Extended Data Detect	R	to show that decoded data exist at Extended Data 1 / 2 Registers 0 : no Extended Data exists 1 : decoded Extended Data exists
bit 7	VBWSDET	VBID / WSS Data Detect	R	to show that decoded data exist at VBID / WSS Data 1 / 2 Registers. 0 : no VBID / WSS data exists 1 : decoded VBID / WSS data exists

Macrovision Status Register (R/W) [Sub Address 0x11]

Register to indicate the Macrovision Detect Result.

Sub Address 0x11

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PSPDET	AGCPDET	BPPDET	SYNCRED	CSTYPE	CSDET	AGCDET

Macrovision Status Register Definition

BIT	Register Name		R/W	Definition
bit 0	AGCDET	AGC Process Detect	R	to show that Macrovision AGC Process is included on input signal. 0 : no Macrovision AGC Process is detected 1 : Macrovision AGC Process is detected
bit 1	CSDET	Color Stripe Detect	R	to show that Macrovision Color Stripe Process is included on input signal. 0 : no Color Stripe process 1 : Color Stripe process is detected
bit 2	CSTYPE	Color Stripe Type	R	to show types of Color Stripe which is included on input signal 0 : Color Stripe Type 2 1 : Color Stripe Type 3
bit 3	SYNCRED	Sync Reduction bit	R	to show that Sync Reduction is detected 0 : - 1 : Sync Reduction is detected
bit 4	BPPDET	Back Porch Pulse Detect bit	R	to show that end of Field Back Porch Pulse is detected 0 : - 1 : end of Field Back Porch Pulse is detected
bit 5	AGCPDET	AGC Pulse Detect bit	R	to show that AGC Pulse is detected. 0 : - 1 : AGC Pulse is detected
bit 6	PSPDET	Pseudo Sync Pulse Detect bit	R	to show that Pseudo Sync Pulse is detected. 0 : - 1 : Pseudo Sync Pulse is detected
bit 7	Reserved	Reserved bit	R	Reserved

Closed Caption 1 Register (R) [Sub Address 0x12]

Register to store Closed Caption Data.

Sub Address 0x12

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Closed Caption 2 Register (R) [Sub Address 0x13]

Register to store Closed Caption Data.

Sub Address 0x13

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

Extended Data 1 Register (R) [Sub Address 0x14]

Register to store Closed Caption Extended Data.

Sub Address 0x14

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0

Extended Data 2 Register (R) [Sub Address 0x15]

Register to store Closed Caption Extended Data.

Sub Address 0x15

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8

VBID/WSS 1 Register (R) [Sub Address 0x16]

Register to store VBID data and to store WSS data.

Sub Address 0x16

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6
Reserved	Reserved	G4-13	G4-12	G4-11	G3-10	G3-9	G3-8

VBID/WSS 2 Register (R) [Sub Address 0x17]

Register to store VBID data and to store WSS data.

Sub Address 0x17

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0

Device & Revision ID Register (R) [Sub Address 0x18]

Register to show Device ID & Revision of the AK8855.
Device ID of the AK8855 is 55 in decimal.
Initial Version of the Revision ID is 0x00.
Revision number is modified only when a control software needs to be modified.

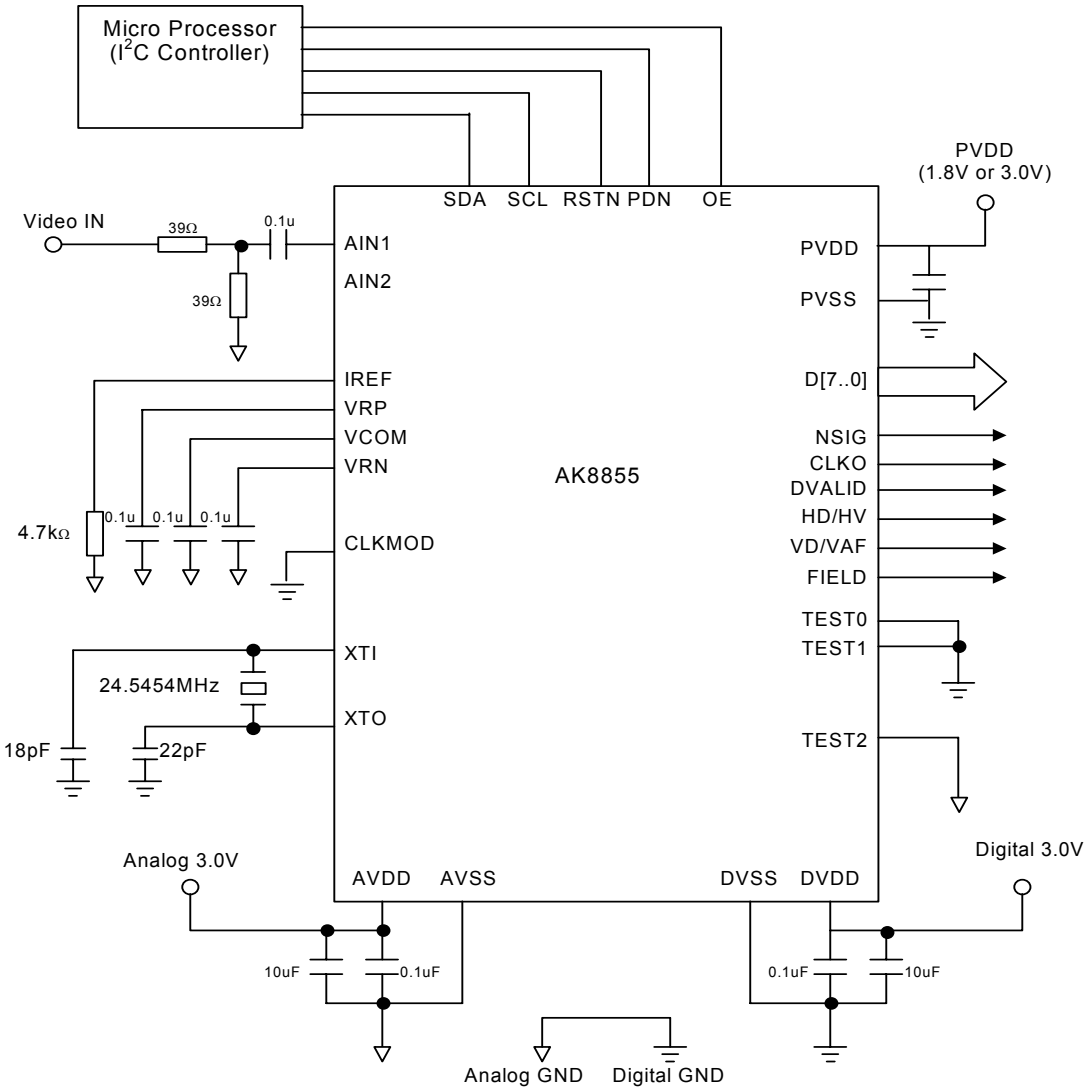
Sub Address 0x18 **Default Value 0x37**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REV1	REV0	DID5	DID4	DID3	DID2	DID1	DID0
0	0	1	1	0	1	1	1

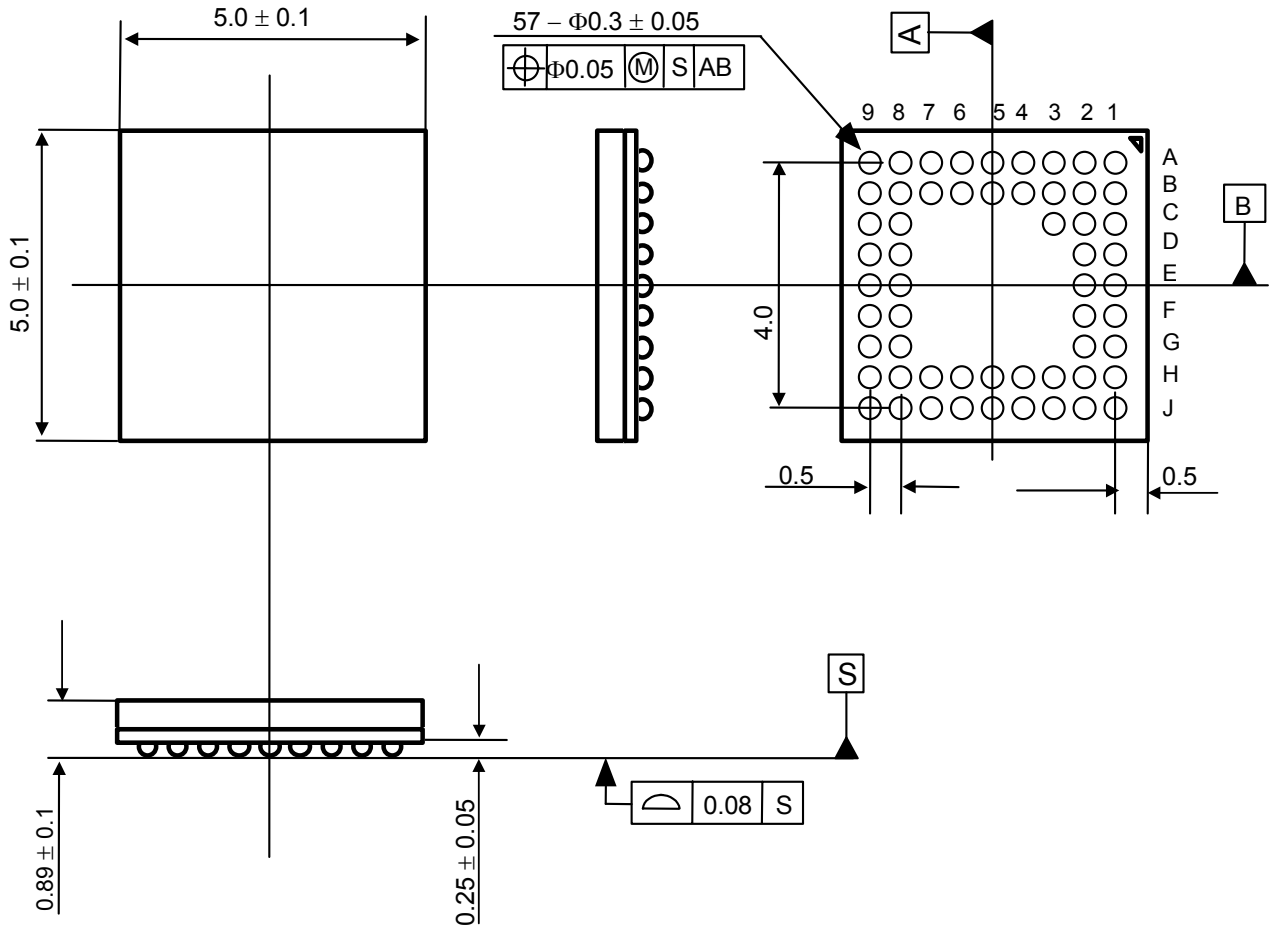
Revision Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 3	DID0 ~ DID5	Revision bit	R	to show Device ID Device ID is 55 (decimal) (0x37h).
bit 4 ~ bit 7	REV0 ~ REV1	Device ID	R	to show Revision information REV1 – REV0 Initial version is 0x00

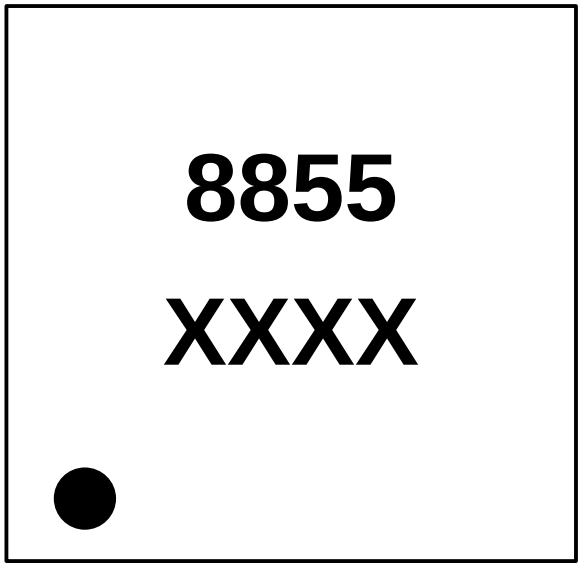
System Connection Example



Package Drawing



Package Marking Drawing



a. Package type : BGA
b. Number of pins : 57 pins (including an index pin)
c. Product number : 8855
d. Control Code : xxxxx (5 digit number)

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