ISL6266, ISL6266A

Two-phase Core Controllers (Montevina, IMVP-6+)

FN6398
Rev 4.00
August 25, 2015

The ISL6266 and ISL6266A are two-phase buck converter regulators implementing Intel® IMVP-6 protocol with embedded gate drivers. Both converters use interleaved channels to double the output voltage ripple frequency and thereby reduce output voltage ripple amplitude with fewer components, lower component cost, reduced power dissipation, and smaller real estate area.

The ISL6266A utilizes the patented R^3 Technology™, Intersil's Robust Ripple Regulator modulator. Compared with traditional multiphase buck regulators, the R^3 Technology™ has the fastest transient response. This is due to the R^3 modulator commanding variable switching frequency during load transient events.

Intel Mobile Voltage Positioning (IMVP) is a smart voltage regulation technology, which effectively reduces power dissipation in Intel Pentium processors. To boost battery life, the ISL6266A supports DPRSLRVR (deeper sleep), DPRSTP# and PSI# functions, which maximizes efficiency by enabling different modes of operation. In active mode (heavy load), the regulator commands the two phase continuous conduction mode (CCM) operation. When PSI# is asserted in active mode (medium load), the ISL6266A operates in one-phase CCM. When the CPU enters deeper sleep mode, the ISL6266A enables diode emulation to maximize efficiency.

For better system power management, the ISL6266A provides a CPU power monitor output. The analog output at the power monitor pin can be fed into an A/D converter to report instantaneous or average CPU power.

A 7-bit digital-to-analog converter (DAC) allows dynamic adjustment of the core output voltage from 0.300V to 1.500V. Over-temperature, the ISL6266A achieves a 0.5% system accuracy of core output voltage.

A unity-gain differential amplifier is provided for remote CPU die sensing. This allows the voltage on the CPU die to be accurately measured and regulated per Intel IMVP-6+ specifications. Current sensing can be realized using either lossless inductor DCR sensing or discrete resistor sensing. A single NTC thermistor network thermally compensates the gain and the time constant of the DCR variations.

The ISL6266 also includes all the functions for IMVP-6+ core power delivery. In addition, it has been optimized for use with coupled-inductor solutions. More information on the differences between ISL6266 and ISL6266A can be found in the "Electrical Specifications" on page 3 and the "ISL6266 Features" on page 21.

Features

- Precision Two/One-phase CORE Voltage Regulator
  - 0.5% System Accuracy Over-Temperature
  - Enhanced Load Line Accuracy
- Internal Gate Driver with 2A Driving Capability
- Dynamic Phase Adding/Dropping
- Microprocessor Voltage Identification Input
  - 7-Bit VID Input
  - 0.300V to 1.500V in 12.5mV Steps
  - Support VID Change On-the-Fly
- Multiple Current Sensing Schemes Supported
  - Lossless Inductor DCR Current Sensing
  - Precision Resistive Current Sensing
- CPU Power Monitor
- Thermal Monitor
- User Programmable Switching Frequency
- Differential Remote CPU Die Voltage Sensing
- Static and Dynamic Current Sharing
- Support All Ceramic Output with Coupled Inductor (ISL6266)
- Overvoltage, Undervoltage and Overcurrent Protection
- Pb-Free (RoHS Compliant)

Ordering Information

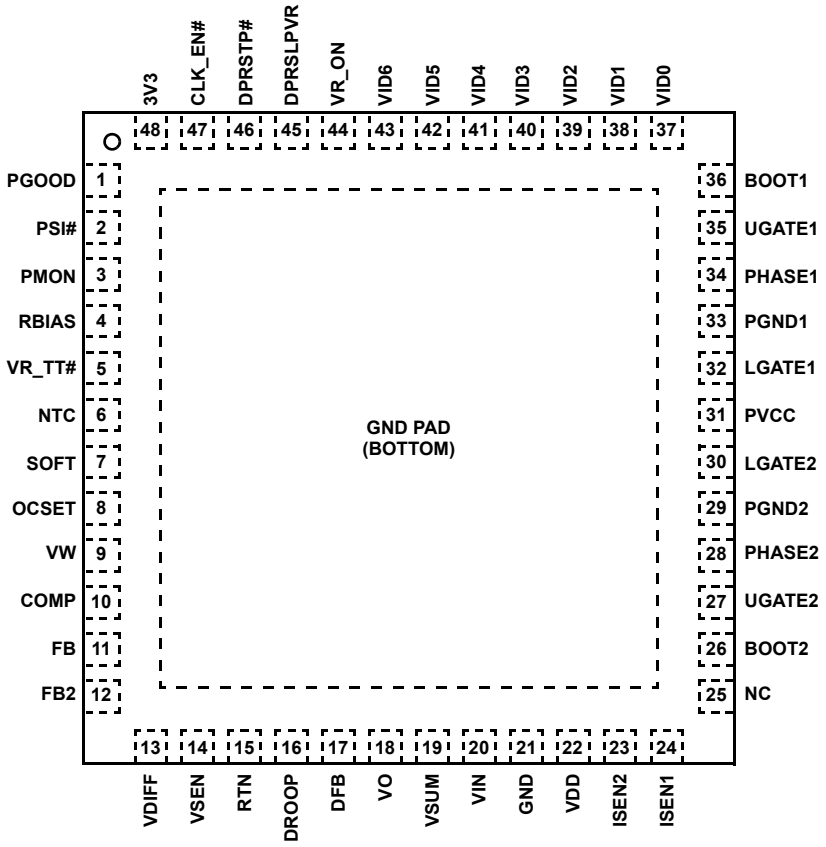
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6266HRZ **(No longer available or supported)**	ISL6266 HRZ	-10 to +100	48 Ld 7x7 QFN	L48.7x7
ISL6266HRZ-T* **(No longer available or supported)**	ISL6266 HRZ	-10 to +100	48 Ld 7x7 QFN	L48.7x7
ISL6266AIRZ	ISL6266A IRZ	-40 to +100	48 Ld 7x7 QFN	L48.7x7
ISL6266AIRZ-T*	ISL6266A IRZ	-40 to +100	48 Ld 7x7 QFN	L48.7x7

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL6266, ISL6266A
(48 LD 7x7 QFN)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . -0.3V to +7V
Battery Voltage (V_{IN}) . . . . . +28V
Boot Voltage (BOOT) . . . . . -0.3V to +33V
Boot to Phase Voltage (BOOT to PHASE) . . . . . -0.3V to +7V (DC)
. . . . . -0.3V to +9V (<10ns)
Phase Voltage (PHASE) . . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . PHASE -0.3V (DC) to BOOT
. . . . . PHASE-5V (<20ns Pulse Width, 10µJ) to BOOT
LGATE Voltage (LGATE) . . . . . -0.3V (DC) to (VDD + 0.3V)
. . . . . -2.5V (<20ns Pulse Width, 5µJ) to (VDD + 0.3V)
All Other Pins . . . . . -0.3V to (VDD + 0.3V)
Open Drain Outputs, PGOOD, VR_TT# . . . . . -0.3V to +7V

Thermal Information

Thermal Resistance (Typical)	θ_{JA}°C/W	θ_{JC}°C/W
QFN Package (Notes 1, 2)	29	4.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage, V_{DD} . . . . . +5V ±5%
Battery Voltage, V_{IN} . . . . . +5V to 25V
Ambient Temperature . . . . . -40°C to +100°C
Junction Temperature . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{DD} = 5V, T_A = -40°C to +100°C, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	VR_ON = 3.3V		5.1	5.7	mA
		VR_ON = 0V			1	µA
+3.3V Supply Current	I_{3V3}	No load on CLK_EN#			1	µA
Battery Supply Current at VIN pin	I_{VIN}	VR_ON = 0V, V_{IN} = 25V			1	µA
POR (Power-On Reset) Threshold	POR_r	V_{DD} Rising		4.35	4.5	V
	POR_f	V_{DD} Falling	4.0	4.15		V
SYSTEM AND REFERENCES						
System Accuracy (ISL6266AHRZ)	%Error (V_{CC_CORE})	No load, closed loop, active mode, T_A = 0°C to +100°C, VID = 0.75V to 1.5V	-0.5		0.5	%
		VID = 0.5V to 0.7375V	-8		8	mV
		VID = 0.3V to 0.4875V	-15		15	mV
System Accuracy (ISL6266AIRZ)	%Error (V_{cc_core})	No load, closed loop, active mode, VID = 0.75V to 1.5V	-0.8		0.8	%
		VID = 0.5V to 0.7375V	-10		10	mV
		VID = 0.3V to 0.4875V	-18		18	mV
RBIAS Voltage	R_{RBIAS}	R_{RBIAS} = 147kΩ	1.45	1.47	1.49	V
Boot Voltage	V_{BOOT}		1.188	1.2	1.212	V
Output Voltage Range	V_{CC_CORE} (max)	VID = [0000000]		1.5		V
	V_{CC_CORE} (min)	VID = [1100000]		0.3		V
VID Off State		VID = [1111111]		0		V

Electrical Specifications V_{DD} = 5V, T_A = -40°C to +100°C, unless otherwise specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
CHANNEL FREQUENCY						
Nominal Channel Frequency	f_{SW}	ISL6266, 2 channel operation	410	440	470	kHz
		ISL6266A, 2 channel operation	280	300	320	kHz
Adjustment Range			100		600	kHz
AMPLIFIERS						
Droop Amplifier Offset			-0.25		0.25	mV
Error Amp DC Gain	A_{V0}	(Note 3)		90		dB
Error Amp Gain-Bandwidth Product	GBW	C_L = 20pF (Note 3)		18		MHz
Error Amp Slew Rate	SR	C_L = 20pF (Note 3)		5		V/µs
FB Input Current	$I_{IN(FB)}$			10	150	nA
ISEN						
Imbalance Voltage					2	mV
Input Bias Current				20		nA
SOFT-START CURRENT						
Soft-Start Current	I_{SS}		-47	-42	-37	µA
Soft Geyserville Current	I_{GV}	|SOFT - REF| > 100mV	±180	±205	±230	µA
Soft Deeper Sleep Entry Current	I_{C4}	DPRSLPVR = 3.3V	-47	-42	-37	µA
Soft Deeper Sleep Exit Current	I_{C4EA}	DPRSLPVR = 3.3V	37	42	47	µA
Soft Deeper Sleep Exit Current	I_{C4EB}	DPRSLPVR = 0V	180	205	230	µA
GATE DRIVER DRIVING CAPABILITY						
UGATE Source Resistance	$R_{SRC(UGATE)}$	500mA Source Current (Note 3)		1	1.5	Ω
UGATE Source Current	$I_{SRC(UGATE)}$	V_{UGATE_PHASE} = 2.5V (Note 3)		2		A
UGATE Sink Resistance	$R_{SNK(UGATE)}$	500mA Sink Current (Note 3)		1	1.5	Ω
UGATE Sink Current	$I_{SNK(UGATE)}$	V_{UGATE_PHASE} = 2.5V (Note 3)		2		A
LGATE Source Resistance	$R_{SRC(LGATE)}$	500mA Source Current (Note 3)		1	1.5	Ω
LGATE Source Current	$I_{SRC(LGATE)}$	V_{LGATE} = 2.5V (Note 3)		2		A
LGATE Sink Resistance	$R_{SNK(LGATE)}$	500mA Sink Current (Note 3)		0.5	0.9	Ω
LGATE Sink Current	$I_{SNK(LGATE)}$	V_{LGATE} = 2.5V (Note 3)		4		A
UGATE to PHASE Resistance	$R_{p(UGATE)}$			1		kΩ
GATE DRIVER SWITCHING TIMING (refer to “ISL6266, ISL6266A Gate Driver Timing Diagram” on page 6)						
UGATE Rise Time	t_{RU}	PV_{CC} = 5V, 3nF Load (Note 3)		8.0		ns
LGATE Rise Time	t_{RL}	PV_{CC} = 5V, 3nF Load (Note 3)		8.0		ns
UGATE Fall Time	t_{FU}	PV_{CC} = 5V, 3nF Load (Note 3)		8.0		ns
LGATE Fall Time	t_{FL}	PV_{CC} = 5V, 3nF Load		4.0		ns
UGATE Turn-on Propagation Delay	t_{PDHU} ISL6266AHRZ	T_A = -10°C to +100°C PV_{CC} = 5V, Outputs Unloaded	20	30	44	ns
	t_{PDHU} ISL6266AIRZ	PV_{CC} = 5V, Outputs Unloaded	18	30	44	ns

Electrical Specifications V_{DD} = 5V, T_A = -40°C to +100°C, unless otherwise specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
LGATE Turn-on Propagation Delay	t_{PDHL} ISL6266AHRZ	T_A = -10°C to +100°C PV_{CC} = 5V, Outputs Unloaded	7	15	30	ns
	t_{PDHL} ISL6266AIRZ	PV_{CC} = 5V, Outputs Unloaded	5	15	30	ns
BOOTSTRAP DIODE						
Forward Voltage		V_{DDP} = 5V, Forward Bias Current = 2mA	0.43	0.58	0.72	V
Leakage		V_R = 16V			1	µA
POWER GOOD and PROTECTION MONITOR						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA		0.26	0.4	V
PGOOD Leakage Current	I_{OH}	P_{GOOD} = 3.3V	-1		1	µA
PGOOD Delay	t_{pgd}	CLK_EN# Low to PGOOD High	6.3	7.6	8.9	ms
Overvoltage Threshold	O_{VH}	V_O rising above setpoint >1ms	155	195	235	mV
Severe Overvoltage Threshold	O_{VHS}	V_O rising above setpoint >0.5µs	1.675	1.7	1.725	V
OCSET Reference Current		$I(R_{BIAS})$ = 10µA	9.8	10	10.2	µA
OC Threshold Offset		DROOP rising above OCSET >120µs	-3.5		3.5	mV
Current Imbalance Threshold		Difference between ISEN1 and ISEN2 >1ms		9		mV
Undervoltage Threshold (VDIFF-SOFT)	UV_f	V_O falling below setpoint for >1ms	-360	-300	-240	mV
LOGIC INPUTS						
VR_ON, DPRSLPVR Input Low	$V_{IL(3.3V)}$				1	V
VR_ON, DPRSLPVR Input High	$V_{IH(3.3V)}$		2.3			V
Leakage Current of VR_ON	$I_{IL(3.3V)}$	Logic input is low	-1	0		µA
	$I_{IH(3.3V)}$	Logic input is high at 3.3V		0	1	µA
Leakage Current of DPRSLPVR	$I_{IL_DPRSLP(3.3V)}$	DPRSLPVR input is low	-1	0		µA
	$I_{IH_DPRSLP(3.3V)}$	DPRSLPVR input is high at 3.3V		0.45	1	µA
DAC(VID0-VID6), PSI# and DPRSTP# Input Low	$V_{IL(1V)}$				0.3	V
DAC(VID0-VID6), PSI# and DPRSTP# Input High	$V_{IH(1V)}$		0.7			V
Leakage Current of DAC (VID0-VID6), PSI# and DPRSTP#	$I_{IL(1V)}$	Logic input is low	-1	0		µA
	$I_{IH(1V)}$	Logic input is high at 1V		0.45	1	µA
THERMAL MONITOR						
NTC Source Current		NTC = 1.3V	53	60	67	µA
Over-Temperature Threshold		V(NTC) falling	1.18	1.2	1.22	V
VR_TT# Low Output Resistance	R_{TT}	I = 20mA		6.5	9	Ω
POWER MONITOR						
PMON Output Voltage Range	V_{pmon}	VSEN = 1.2V, Droop - V_O = 80mV	1.638	1.680	1.722	V
		VSEN = 1V, Droop - V_O = 20mV	0.308	0.350	0.392	V
PMON Maximum Voltage	$V_{pmonmax}$		2.8	3.0		V

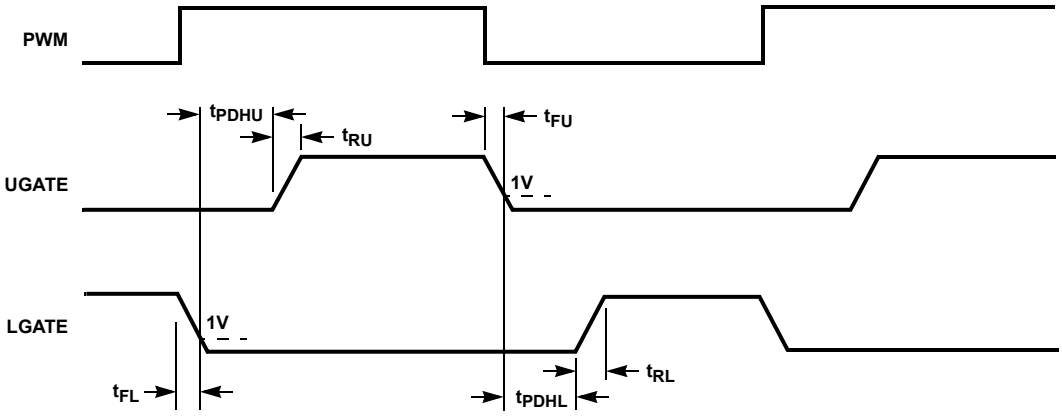
Electrical Specifications V_{DD} = 5V, T_A = -40°C to +100°C, unless otherwise specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
PMON Sourcing Current	I_{sc_pmon}	VSEN = 1V, Droop - V_O = 50mV	2			mA
PMON Sinking Current	I_{sk_pmon}	VSEN = 1V, Droop - V_O = 50mV	2			mA
Maximum Current Sinking Capability		Refer to Figure 29	PMON/ 250Ω	PMON/ 180Ω	PMON/ 100Ω	A
PMON Impedance		When PMON is within its sourcing/sinking current range (Note 3)		7		Ω
CLK_EN# OUTPUT LEVELS						
CLK_EN# High Output Voltage	V_{OH}	3V3 = 3.3V, I = -4mA	2.9	3.1		V
CLK_EN# Low Output Voltage	V_{OL}	$I_{CLK_}$EN# = 4mA		0.26	0.4	V

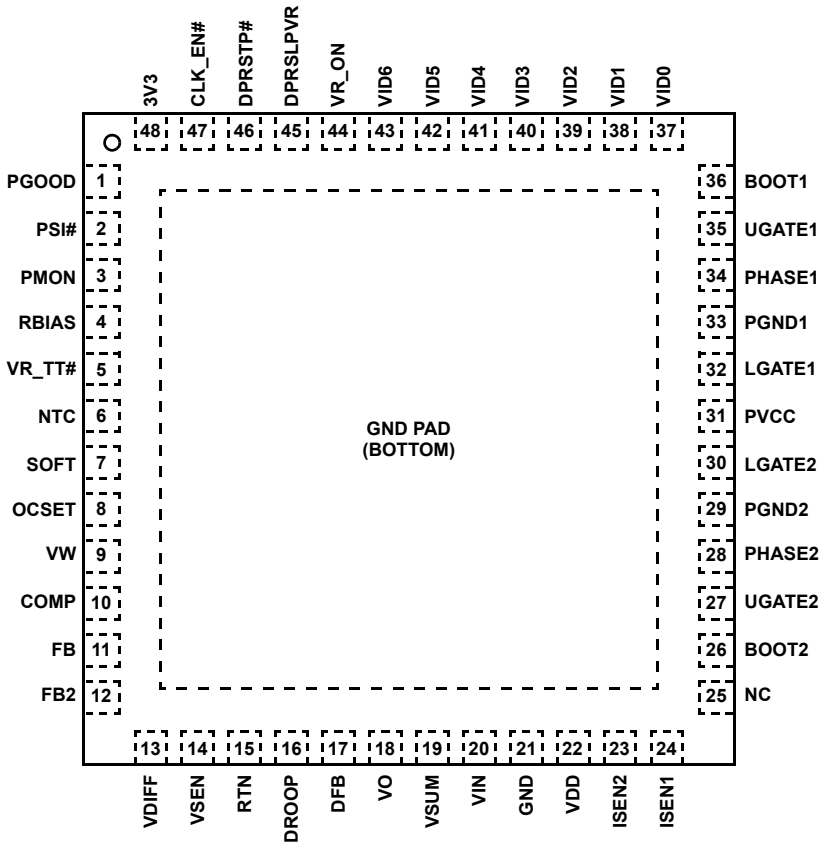
NOTES:

3. Limits established by characterization and are not production tested.
4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

ISL6266, ISL6266A Gate Driver Timing Diagram



Functional Pin Description



PGOOD - Power good open-drain output. Connect externally with 680Ω to VCCP or 1.9kΩ to 3.3V.

PSI# - Current indicator input. When asserted low, indicates a reduced load-current condition and initiates single-phase operation.

PMON - Analog output. PMON is proportional to the product of Vsen and droop voltage.

RBIAS - 147kΩ resistor to VSS sets internal current reference.

VR_TT# - Thermal overload output indicator with open-drain output. Over-temperature pull-down resistance is 10Ω.

NTC - Thermistor input to VRTT# circuit and a 60µA current source is connected internally to this pin.

SOFT - A capacitor from this pin to GND sets the maximum slew rate of the output voltage. SOFT is the non-inverting input of the error amplifier.

OCSET - Overcurrent set input. A resistor from this pin to VO sets DROOP voltage limit for OC trip. A 10µA current source is connected internally to this pin.

VW - A resistor from this pin to COMP programs the switching frequency (for example, 6.45kΩ ≅ 400kHz).

COMP - This pin is the output of the error amplifier.

FB - This pin is the inverting input of error amplifier.

FB2 - There is a switch between FB2 pin and the FB pin. The switch is closed in single-phase operation and is opened in two phase operation. The components connecting to FB2 are to adjust the compensation in single phase operation to achieve optimum performance.

VDIFF - This pin is the output of the differential amplifier.

VSEN - Remote core voltage sense input.

RTN - Remote core voltage sense return.

DROOP - Output of the droop amplifier. The voltage level on this pin is the sum of V_O and the droop voltage.

DFB - Inverting input to droop amplifier.

VO - An input to the IC that reports the local output voltage.

VSUM - This pin is connected to the summation junction of channel current sensing.

VIN - Battery supply voltage. It is used for input voltage feed forward to improve input line transient performance.

VSS - Signal ground. Connect to local controller ground.

VDD - 5V control power supply.

ISEN2 - Individual current sharing sensing for Channel 2.

ISEN1 - Individual current sharing sensing for Channel 1.

N/C - Not connected. Grounding this pin to signal ground in the practical layout.

BOOT2 - This pin is the upper gate driver supply voltage for Phase 2. An internal boot strap diode is connected to the PVCC pin.

UGATE2 - Upper MOSFET gate signal for Phase 2.

PHASE2 - The phase node of Phase 2. Connect this pin to the source of the Channel 2 upper MOSFET.

PGND2 - The return path of the lower gate driver for Phase 2.

LGATE2 - Lower-side MOSFET gate signal for Phase 2.

PVCC - 5V power supply for gate drivers.

LGATE1 - Lower-side MOSFET gate signal for Phase 1.

PGND1 - The return path of the lower gate driver for Phase 1.

PHASE1 - The phase node of phase 1. Connect this pin to the source of the Channel 1 upper MOSFET.

UGATE1 - Upper MOSFET gate signal for Phase 1.

BOOT1 - This pin is the upper-gate-driver supply voltage for Phase 1. An internal boot strap diode is connected to the PVCC pin.

VID0, VID1, VID2, VID3, VID4, VID5, VID6 - VID input with VID0 is the least significant bit (LSB) and VID6 is the most significant bit (MSB).

VR_ON - Digital enable input. A logic high signal on this pin enables the regulator.

DPRSLPVR - Deeper sleep enable signal. A logic high signal on this pin indicates the micro-processor is in deeper-sleep mode and also indicates a slow C4 entry or exit rate with 41µA discharging or charging the SOFT capacitor.

DPRSTP# - Deeper sleep slow wake up signal. A logic low signal on this pin indicates the micro-processor is in deeper-sleep mode.

CLK_EN# - Digital output for system clock. Goes active 10µs after V_{CORE} is within 10% of Boot voltage.

3V3 - 3.3V supply voltage for CLK_EN#.

Functional Block Diagram

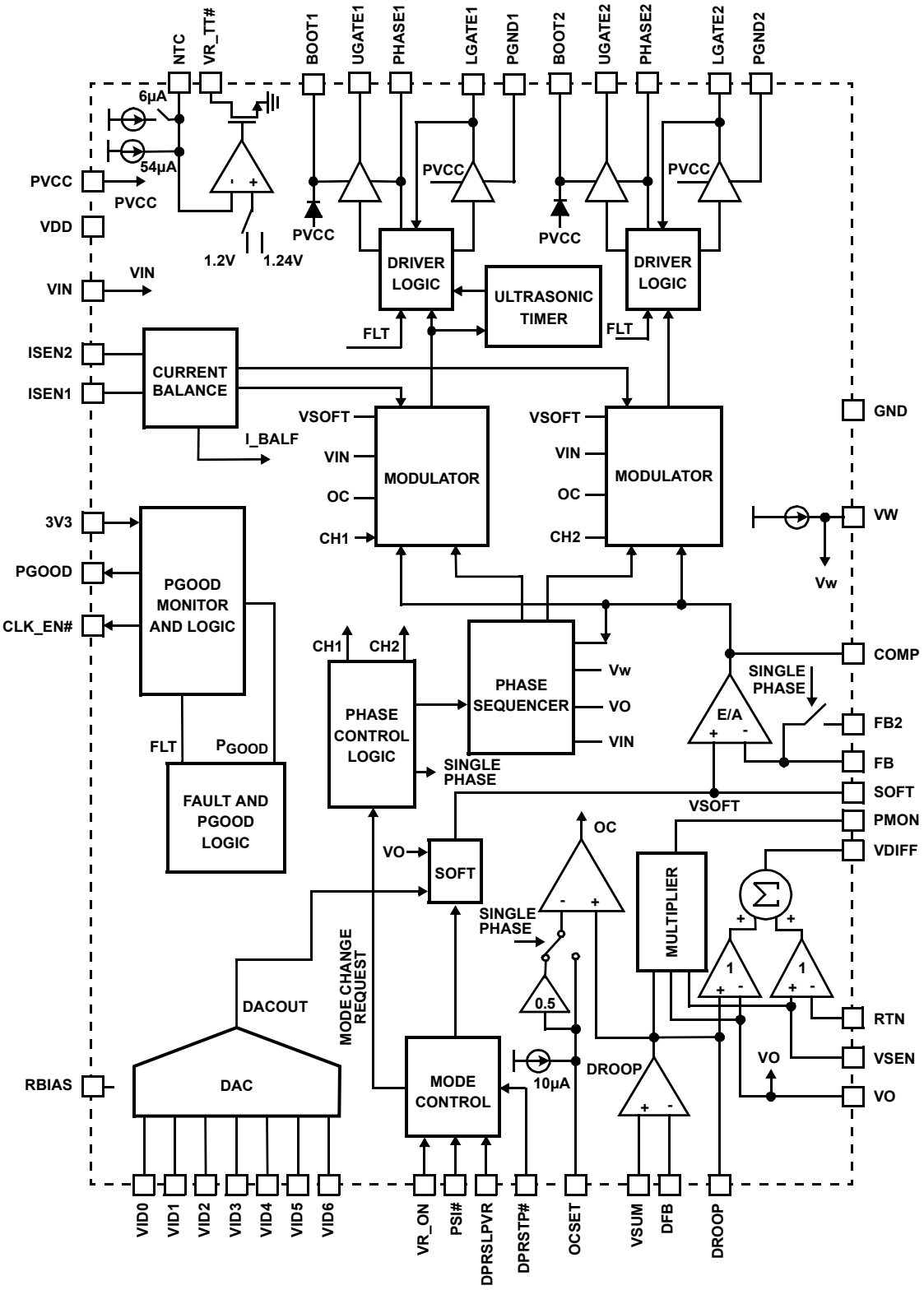


FIGURE 1. SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF ISL6266, ISL6266A

Typical Performance Curves

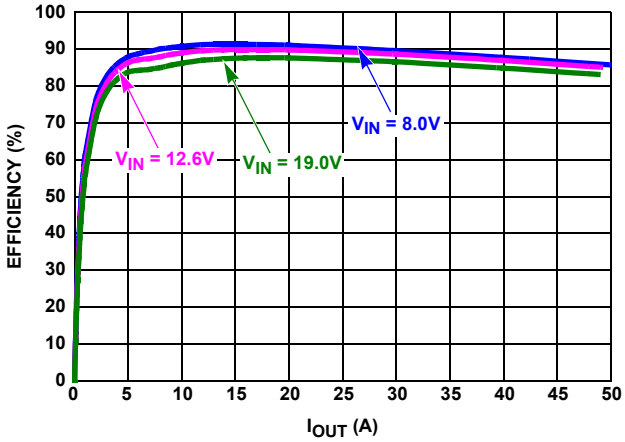


FIGURE 2. ACTIVE MODE EFFICIENCY, 2-PHASE, CCM, PSI# = HIGH, VID = 1.15V

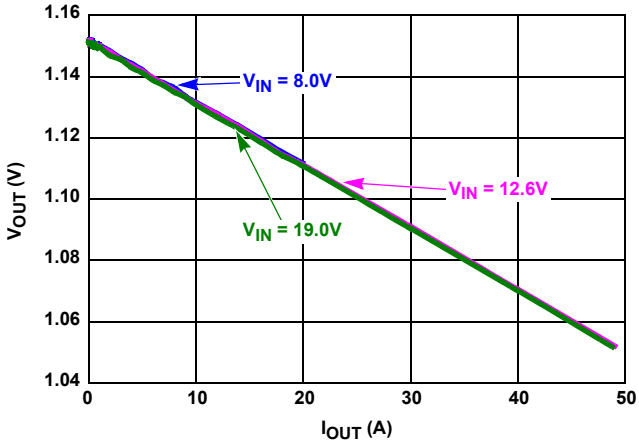


FIGURE 3. ACTIVE MODE LOAD LINE, 2-PHASE, CCM, PSI# = HIGH, VID = 1.15V

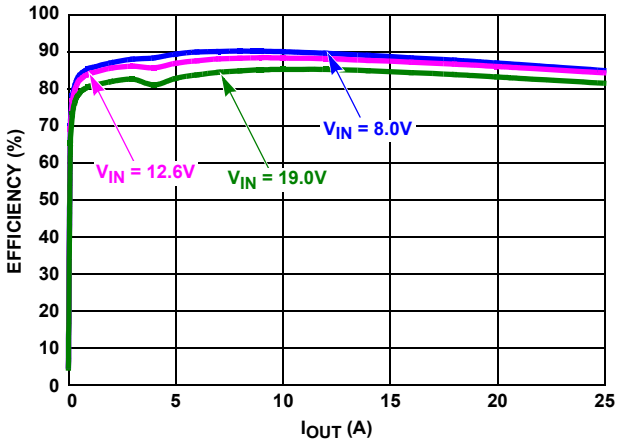


FIGURE 4. ACTIVE MODE EFFICIENCY, 1-PHASE, CCM, PSI# = LOW, VID = 1.00V (ISL6266 ONLY)

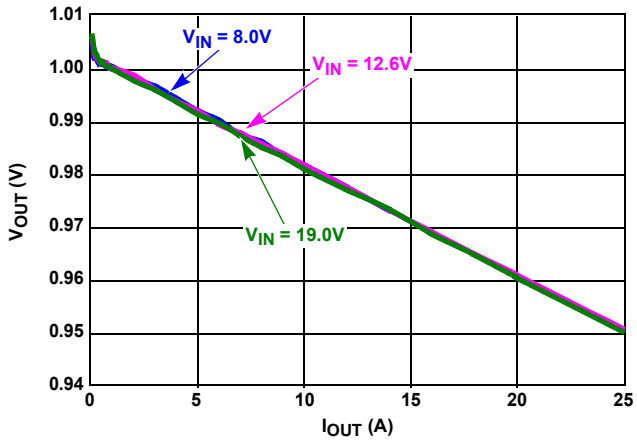


FIGURE 5. ACTIVE MODE LOAD LINE, 1-PHASE, CCM, PSI# = LOW, VID = 1.00V (ISL6266 ONLY)

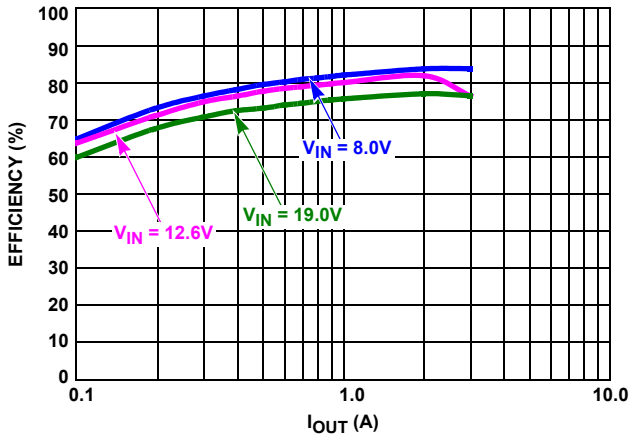


FIGURE 6. DEEPER SLEEP MODE EFFICIENCY

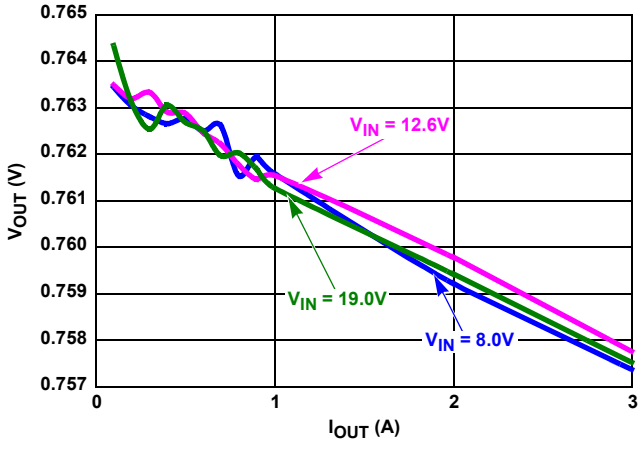


FIGURE 7. DEEPER SLEEP MODE LOAD LINE

Typical Performance Curves (Continued)

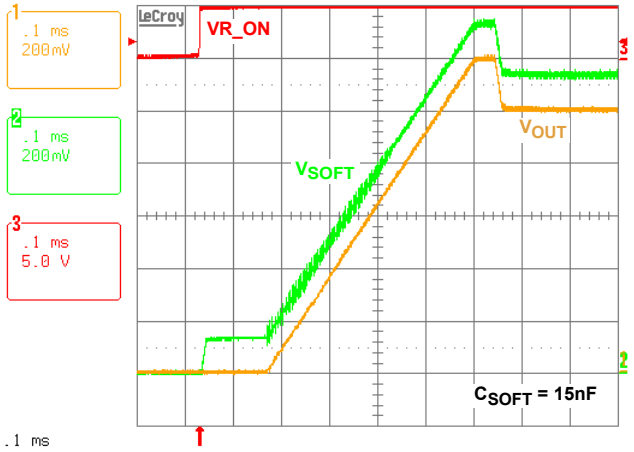


FIGURE 8. SOFT-START WAVEFORM SHOWING SLEW RATE OF 2.5mV/µs AT VID = 1V, I_{LOAD} = 0A

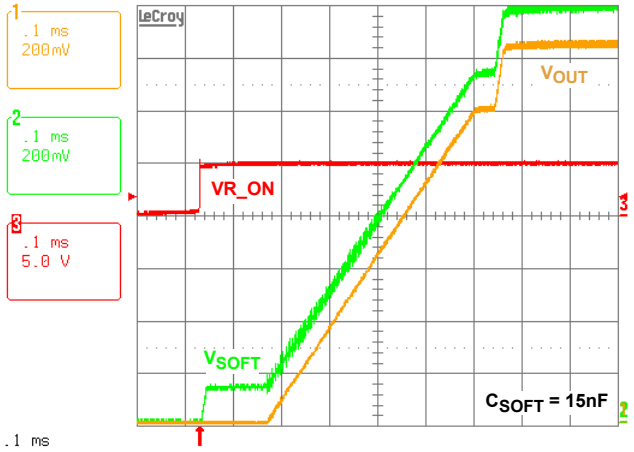


FIGURE 9. SOFT-START WAVEFORM SHOWING SLEW RATE OF 2.5mV/µs AT VID = 1.4375V, I_{LOAD} = 0A

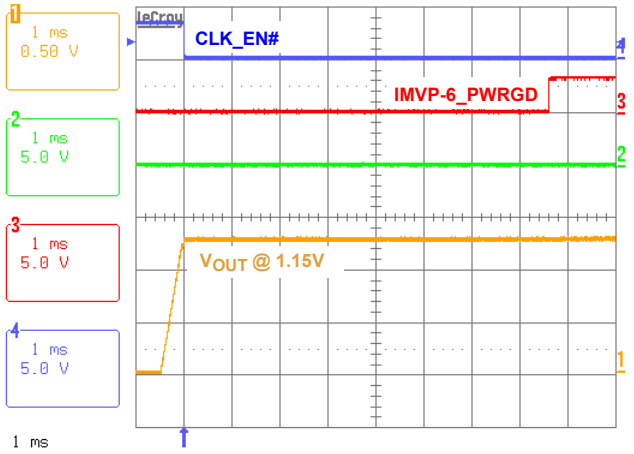


FIGURE 10. SOFT-START WAVEFORM SHOWING CLK_EN# AND IMVP-6 PGOOD

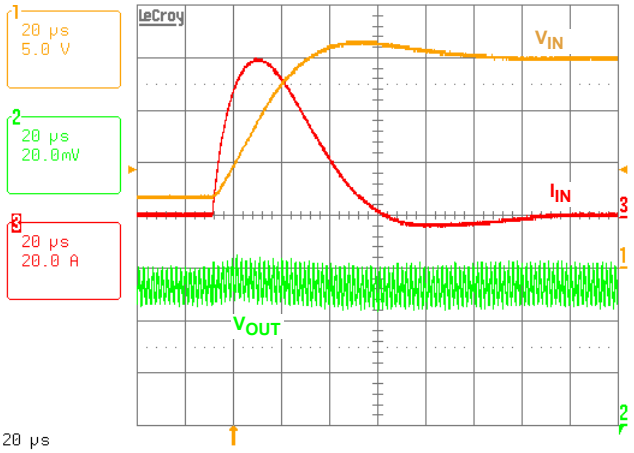


FIGURE 11. 8V TO 20V INPUT LINE TRANSIENT RESPONSE, C_{IN} = 240µF

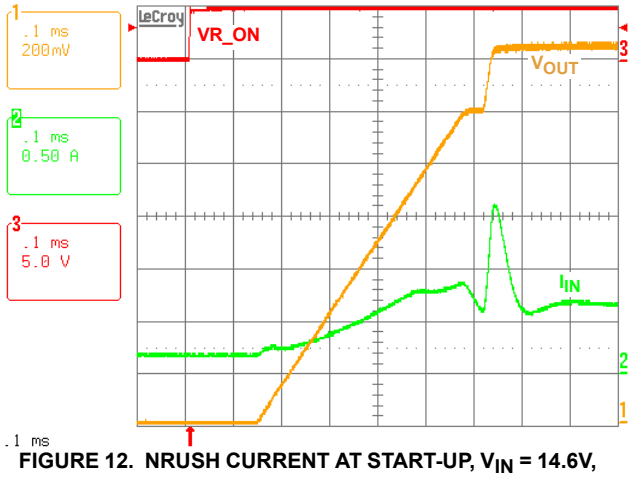


FIGURE 12. NRUSH CURRENT AT START-UP, V_{IN} = 14.6V, VID = 1.4375V, I_{LOAD} = 5A

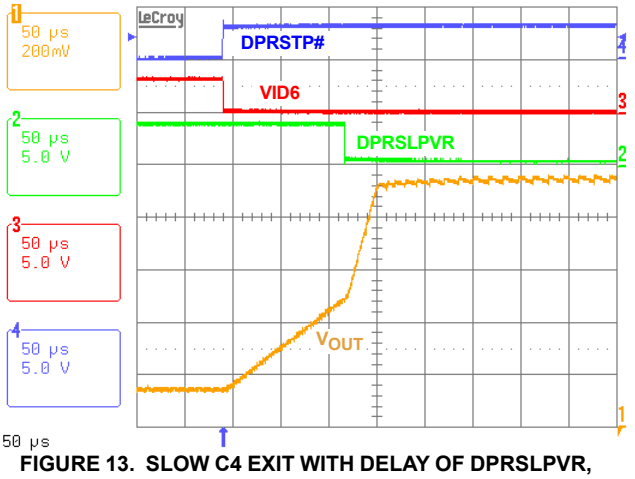


FIGURE 13. SLOW C4 EXIT WITH DELAY OF DPRSLPVR, FROM VID1000000 (0.7V) TO 0110000 (0.9V)

Typical Performance Curves (Continued)

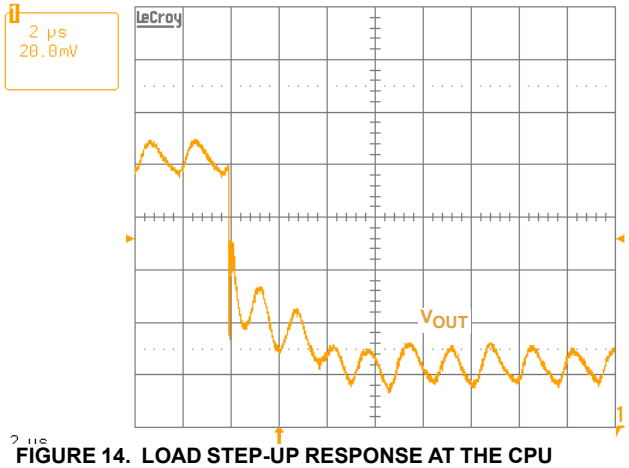


FIGURE 14. LOAD STEP-UP RESPONSE AT THE CPU SOCKET MPGA479, 35A LOAD STEP @ 1000A/µs, 2-PHASE CCM

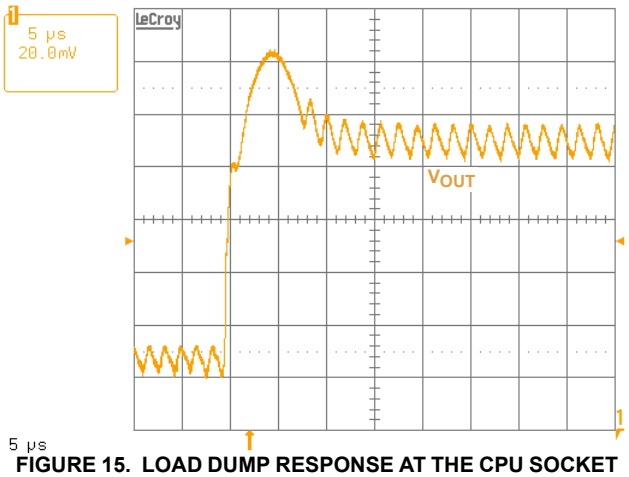


FIGURE 15. LOAD DUMP RESPONSE AT THE CPU SOCKET MPGA479, 35A LOAD STEP @ 1000A/µs, 2-PHASE CCM

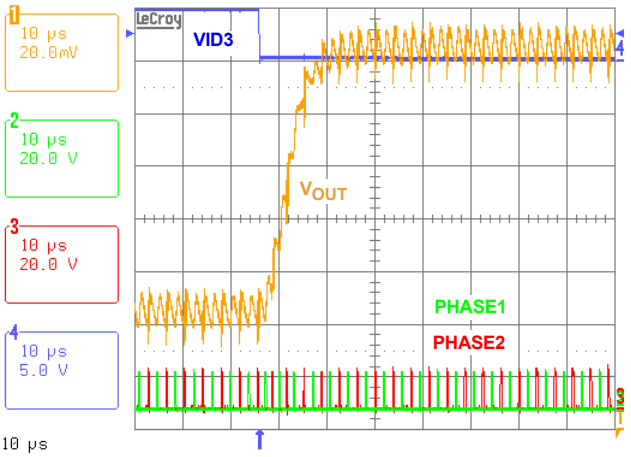


FIGURE 16. VID3 CHANGE OF 010X000 FROM 1V TO 1.1V WITH DPRSLPVR = 0, DPRSTP# = 1, PSI# = 1

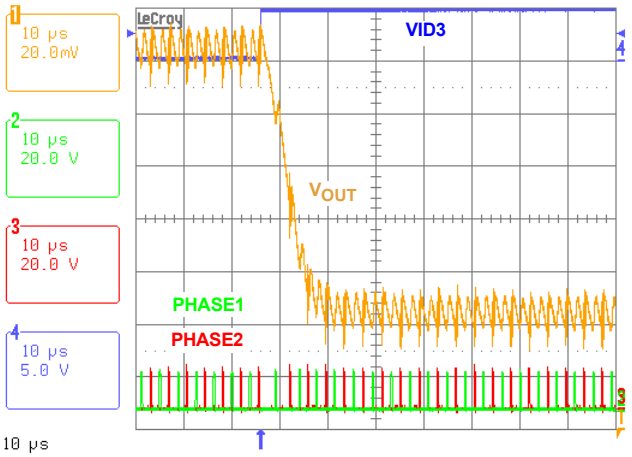


FIGURE 17. VID3 CHANGE OF 010X000 FROM 1.1V TO 1V WITH DPRSLPVR = 0, DPRSTP# = 1, PSI# = 1

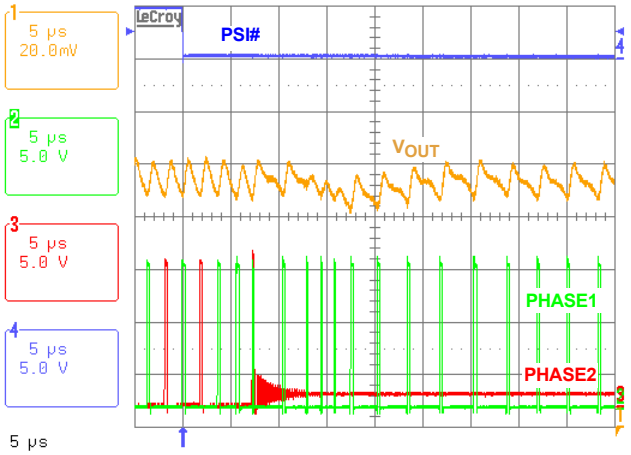


FIGURE 18. 2-CCM TO 1-CCM UPON PSI# ASSERTION WITH DPRSLPVR = 0, DPRSTP# = 1

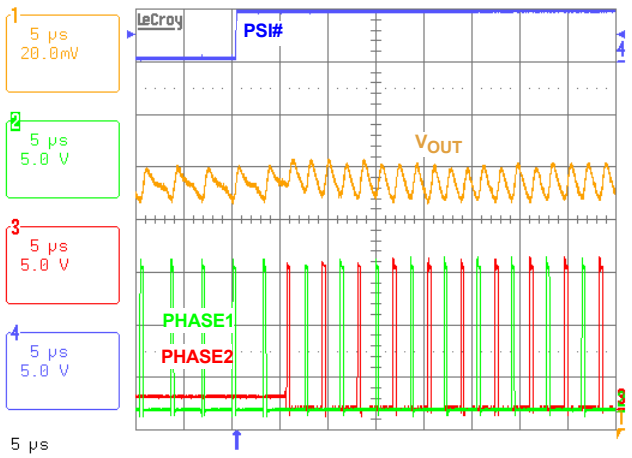


FIGURE 19. 1-CCM TO 2-CCM UPON PSI# DEASSERTION WITH DPRSLPVR = 0, DPRSTP# = 1

Typical Performance Curves (Continued)

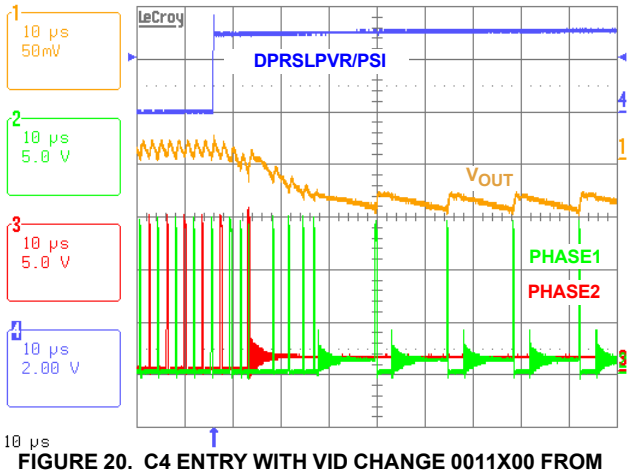


FIGURE 20. C4 ENTRY WITH VID CHANGE 0011X00 FROM 1.2V TO 1.15V, I_{LOAD} = 2A, TRANSITION OF 2-CCM TO 1-DCM, PSI# TOGGLE FROM 1 TO 0 WITH DPRSLPVR FROM 0 TO 1

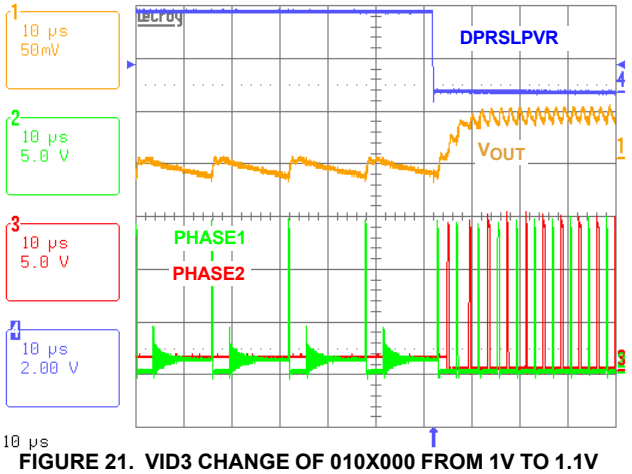


FIGURE 21. VID3 CHANGE OF 010X000 FROM 1V TO 1.1V WITH DPRSLPVR = 0, DPRSTP# = 1, PSI# = 1

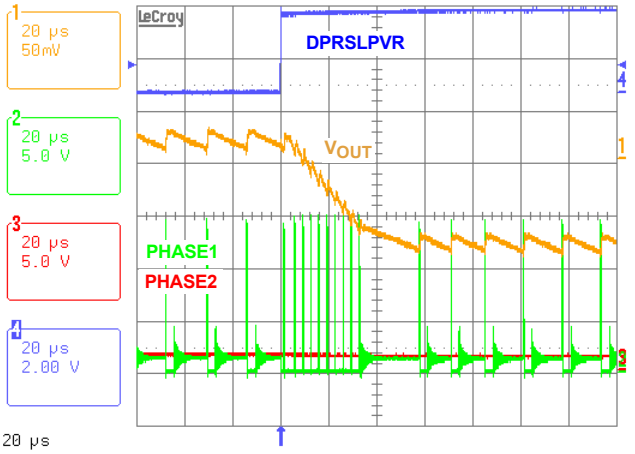


FIGURE 22. C4 ENTRY WITH VID CHANGE OF 011X011 FROM 0.8625V TO 0.7625V, I_{LOAD} = 3A, 1-CCM TO 1-DCM

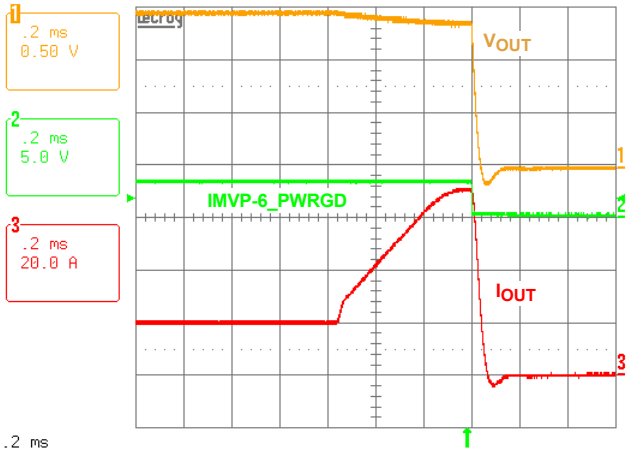


FIGURE 23. OVERCURRENT PROTECTION

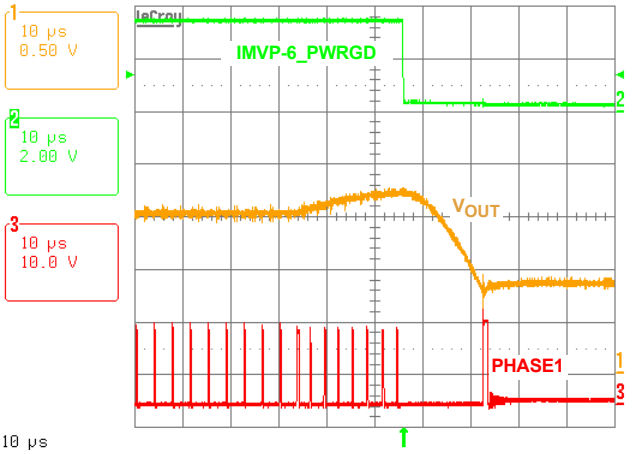


FIGURE 24. 1.7V OVERVOLTAGE PROTECTION SHOWS OUTPUT VOLTAGE PULLED TO 0.9V AND PWM TRI-STATE

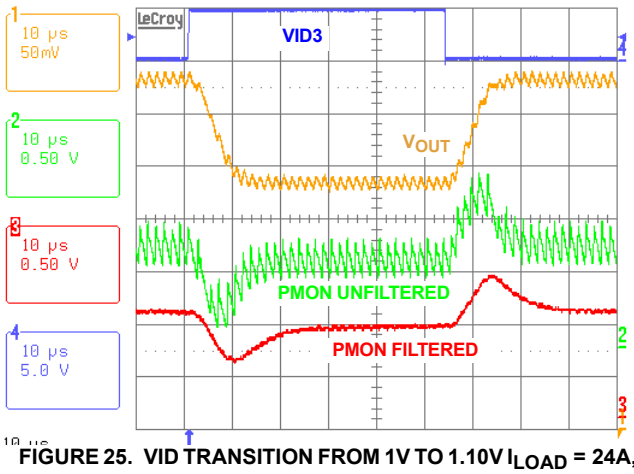


FIGURE 25. VID TRANSITION FROM 1V TO 1.10V I_{LOAD} = 24A, EXTERNAL FILTER 40kΩ AND 100pF AT PMON

Typical Performance Curves (Continued)

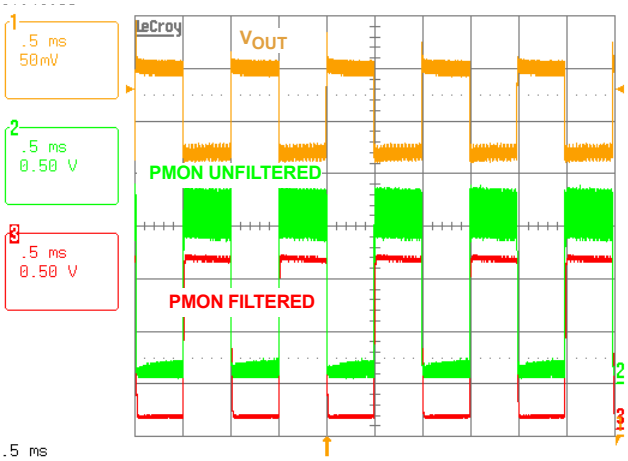


FIGURE 26. VID = 1.15V, LOAD TRANSIENT OF 0A TO 36A WITH INTEL VTT TOOL, 1kHz RATE, 50% DUTY CYCLE, TR = 35

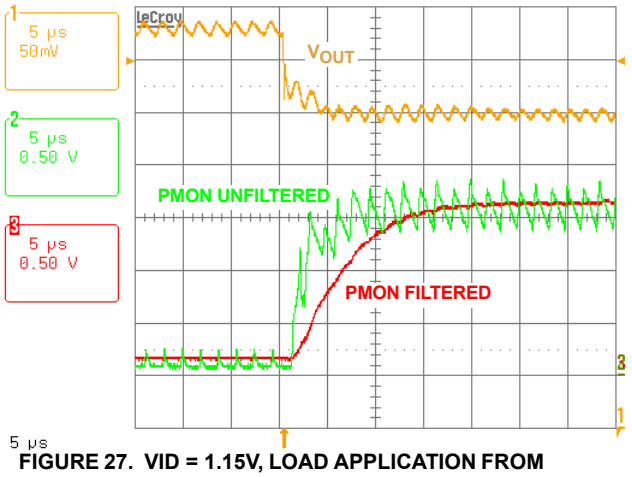


FIGURE 27. VID = 1.15V, LOAD APPLICATION FROM 0A TO 36A WITH INTEL VTT TOOL, 1kHz RATE, 50% DUTY CYCLE, TR = 35

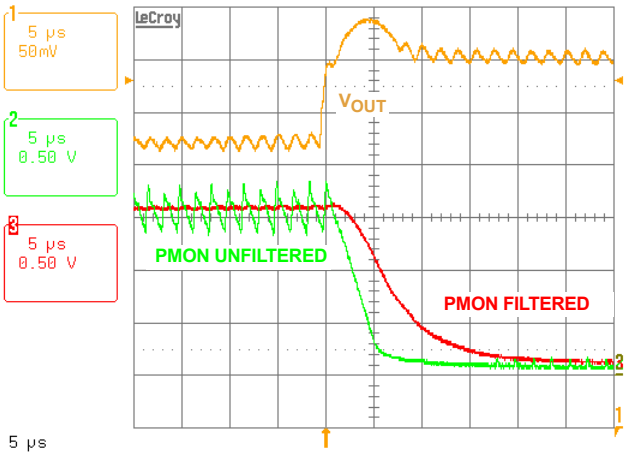


FIGURE 28. VID = 1.15V, LOAD RELEASE FROM 36A TO 0A WITH INTEL VTT TOOL, 1kHz RATE, 50% DUTY CYCLE, TR = 35

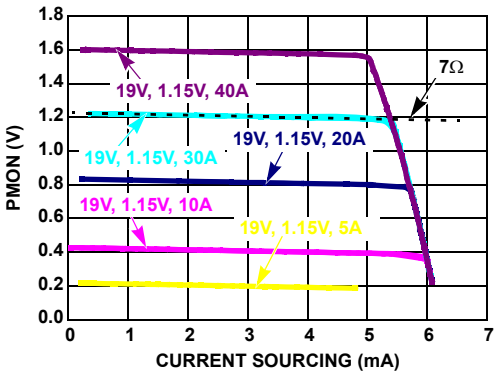


FIGURE 29. POWER MONITOR CURRENT SOURCING CAPABILITY

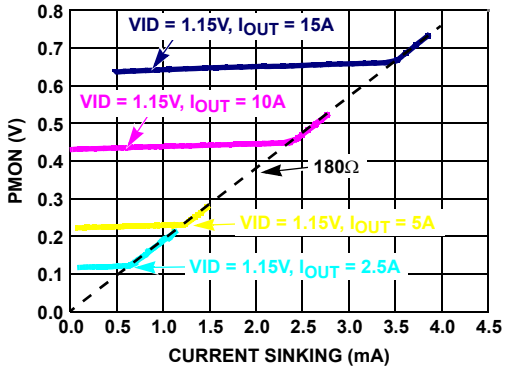


FIGURE 30. POWER MONITOR CURRENT SINKING CAPABILITY

Simplified Coupled Inductor Application Circuit for DCR Current Sensing

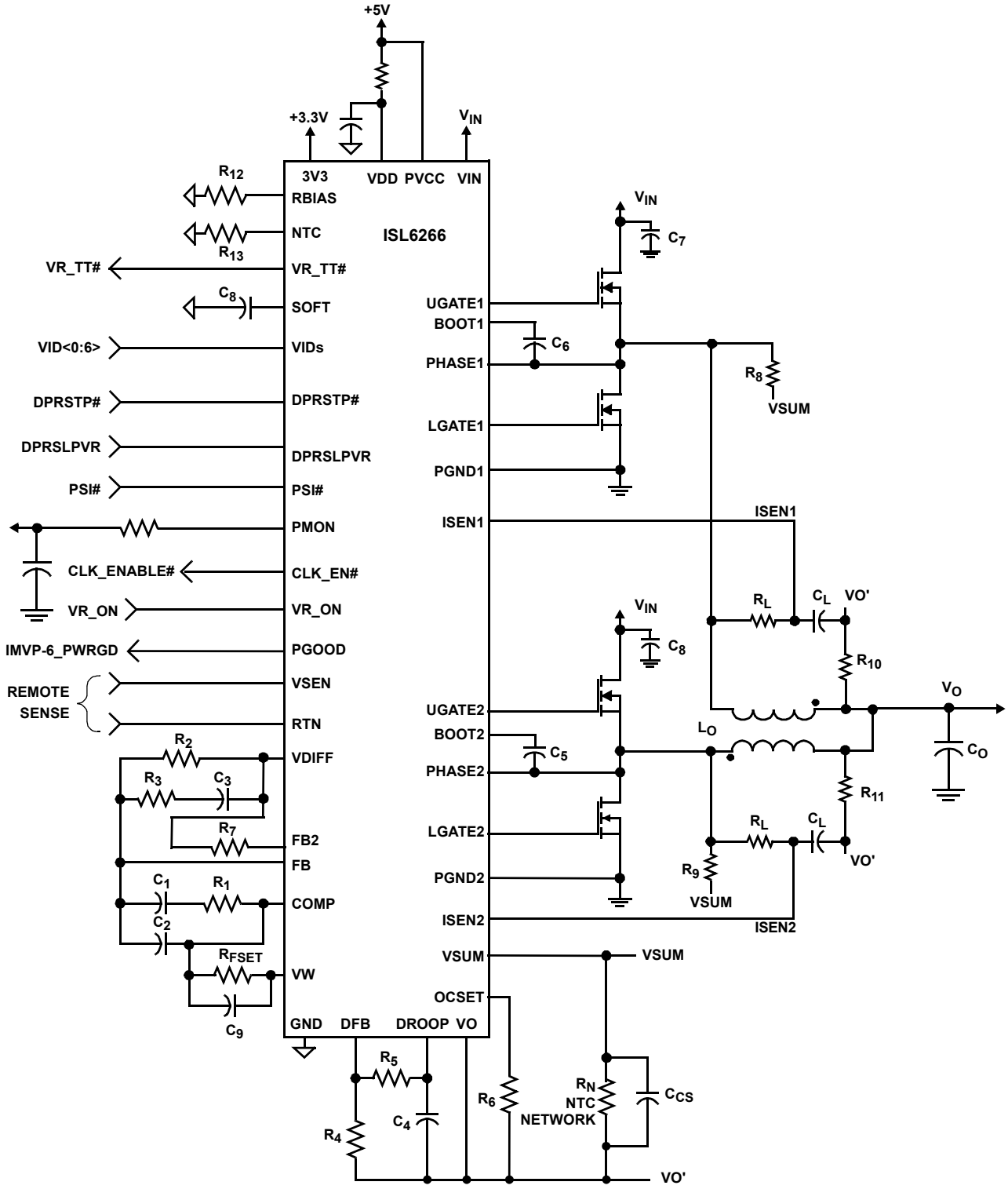


FIGURE 31. ISL6266 BASED TWO-PHASE COUPLED INDUCTOR DESIGN WITH DCR SENSING

Simplified Application Circuit for DCR Current Sensing

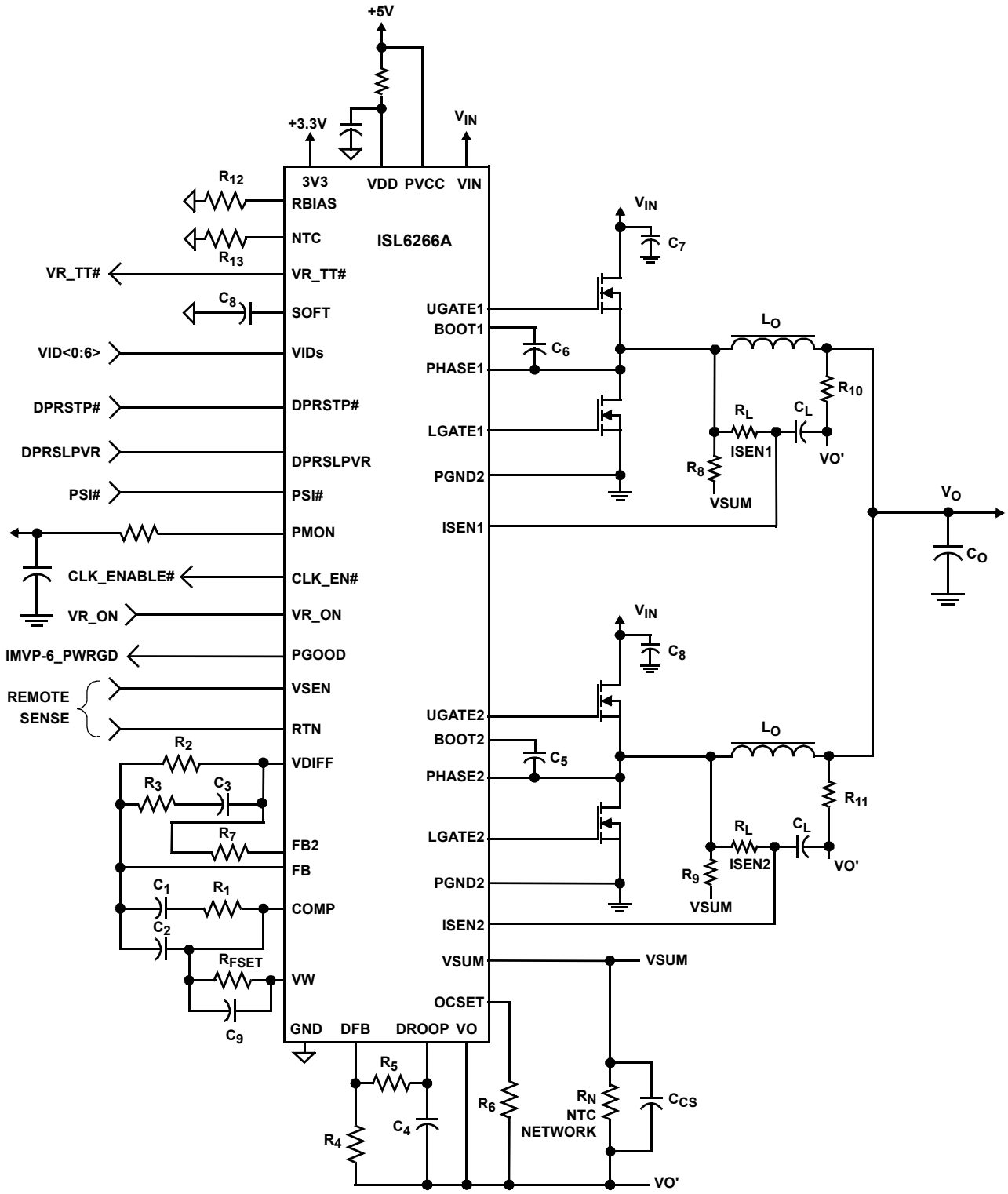


FIGURE 32. ISL6266A BASED TWO-PHASE BUCK CONVERTER WITH INDUCTOR DCR CURRENT SENSING

Simplified Application Circuit for Resistive Current Sensing

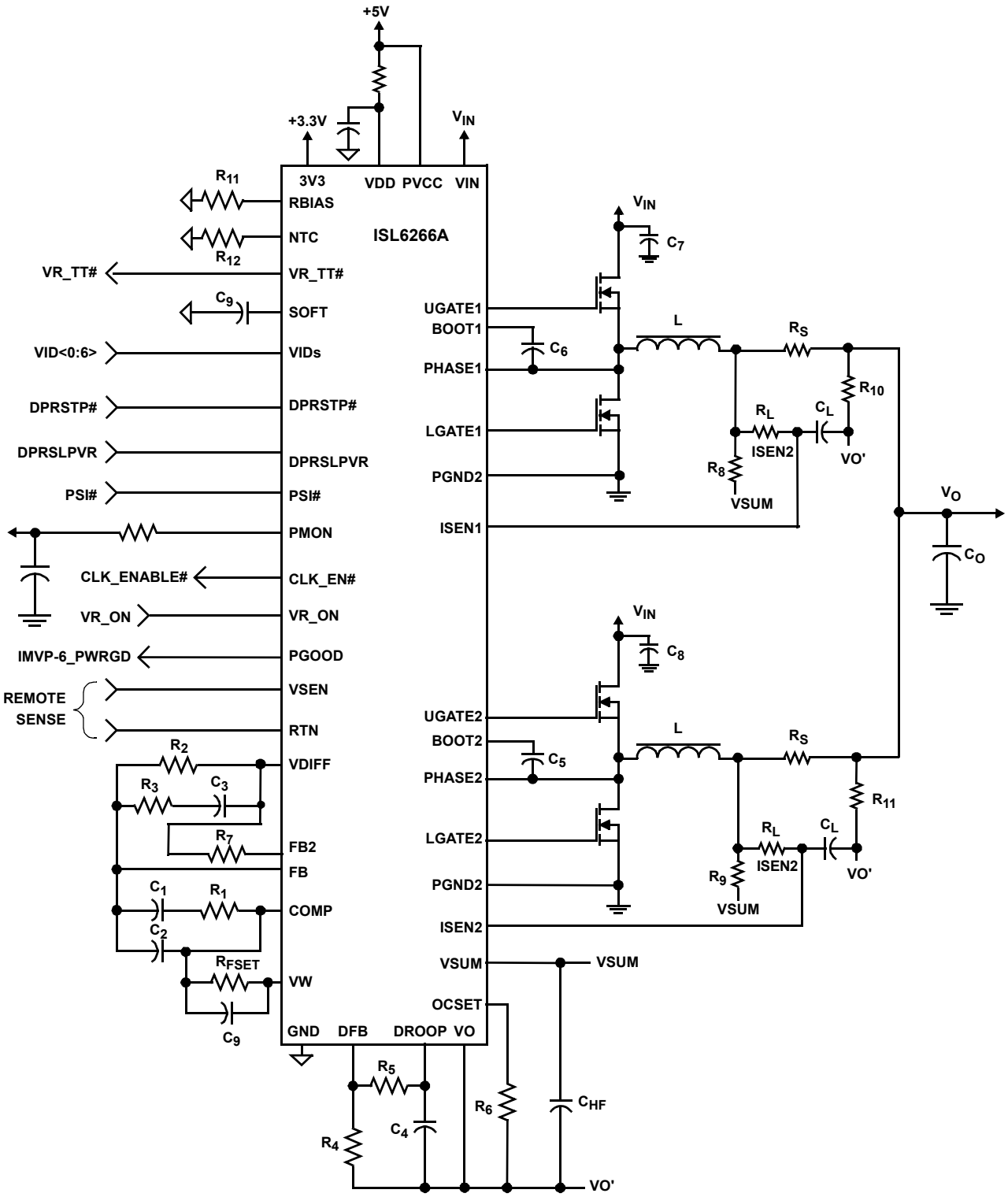


FIGURE 33. ISL6266A BASED TWO-PHASE BUCK CONVERTER WITH RESISTIVE CURRENT SENSING

Theory of Operation

The ISL6266A is a two-phase regulator implementing Intel® IMVP-6 protocol and includes embedded gate drivers for reduced system cost and board area. The regulator provides optimum steady-state and transient performance for microprocessor core applications up to 50A. System efficiency is enhanced by idling one phase at low-current and implementing automatic DCM-mode operation.

The heart of the ISL6266A is R^3 Technology™, Intersil's Robust Ripple Regulator modulator. The R^3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. The ISL6266A modulator internally synthesizes an analog of the inductor ripple current and uses hysteretic comparators on those signals to establish PWM pulse widths. Operating on these large-amplitude, noise-free synthesized signals allows the ISL6266A to achieve lower output ripple and lower phase jitter than either conventional hysteretic or fixed frequency PWM controllers. Unlike conventional hysteretic converters, the ISL6266A has an error amplifier that allows the controller to maintain a 0.5% voltage regulation accuracy throughout the VID range from 0.75V to 1.5V.

The hysteresis window voltage is relative to the error amplifier output such that load current transients results in increased switching frequency, which gives the R^3 regulator a faster response than conventional fixed frequency PWM controllers. Transient load current is inherently shared between active phases due to the use of a common hysteretic window voltage. Individual average phase voltages are monitored and controlled to equally share the static current among the active phases.

Start-Up Timing

With the controller's VDD voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the 3.3V logic HIGH threshold. Approximately 100µs later, SOFT and VOUT begin ramping to the boot voltage of 1.2V. At start-up, the regulator always operates in a 2-phase CCM mode regardless of control signal assertion levels. During this interval, the SOFT capacitor is charged by 41µA current source. If the SOFT capacitor is selected to be 20nF, the SOFT ramp will be at 2mV/µs for a soft-start time of 600µs. Once VOUT is within 10% of the boot voltage for 13 PWM cycles (43µs for frequency = 300kHz), then CLK_EN# is pulled LOW and the SOFT capacitor is charged/discharged by approximately 200µA. Therefore, VOUT slews at 10mV/µs to the voltage set by the VID pins. Approximately 7ms later, PGOOD is asserted HIGH. Typical start-up timing is shown in Figure 34.

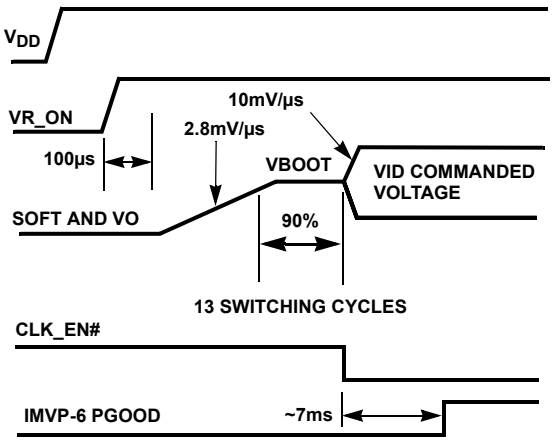


FIGURE 34. SOFT-START WAVEFORMS USING A 15nF SOFT CAPACITOR

Static Operation

After the start sequence, the output voltage will be regulated to the value set by the VID inputs shown in Table 1. The entire VID table is presented in the intel IMVP-6 specification. The ISL6266A will control the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.5V.

TABLE 1. TRUNCATED VID TABLE FOR INTEL IMVP-6+ SPECIFICATION

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOUT (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	1	0	1	1.4375
0	0	1	0	0	0	1	1.2875
0	0	1	1	1	0	0	1.15
0	1	1	0	1	0	1	0.8375
0	1	1	1	0	1	1	0.7625
1	1	0	0	0	0	0	0.3000
1	1	1	1	1	1	1	0.0000

A fully-differential amplifier implements core voltage sensing for precise voltage control at the microprocessor die. The inputs to the amplifier are the VSEN and RTN pins.

As the load current increases from zero, the output voltage will droop from the VID table value by an amount proportional to current to achieve the IMVP-6+ load line. The ISL6266A provides options for current to be measured using either resistors in series with the channel inductors as shown in the application circuit of Figure 33, or using the intrinsic series resistance of the inductors as shown in the application circuit of Figure 32. In both cases, signals representing the inductor currents are summed at VSUM, which is the non-inverting input to the DROOP amplifier shown in the block diagram of Figure 1. The voltage at the DROOP pin minus the output voltage, VO´, is a high-bandwidth analog of the total inductor

current. This voltage is used as an input to a differential amplifier to achieve the IMVP-6+ load line, and also as the input to the overcurrent protection circuit.

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding thus maintaining the load-line accuracy.

In addition to monitoring the total current (used for DROOP and overcurrent protection), the individual channel average currents are also monitored and used for balancing the load between channels. The IBAL circuit will adjust the channel pulse-widths up or down relative to the other channel to cause the voltages presented at the ISEN pins to be equal.

The ISL6266A controller can be configured for two-channel operation, with the channels operating 180° apart. The channel PWM frequency is determined by the value of R_{FSET} connected to pin VW as shown in Figures 32 and 33. Input and output ripple frequencies will be the channel PWM frequency multiplied by the number of active channels.

High Efficiency Operation Mode

The ISL6266A has several operating modes to optimize efficiency. The controller's operational modes are designed to work in conjunction with the Intel IMVP-6+ control signals to maintain the optimal system configuration for all IMVP-6+ conditions. These operating modes are established by the IMVP-6+ control signal inputs PSI#, DPRSLPVR, and DPRSTP# as shown in Table 2. At high current levels, the system will operate with both phases fully active, responding rapidly to transients and delivering maximum power to the load. At reduced load-current levels, one of the phases may be idled. This configuration will minimize switching losses, while still maintaining transient response capability. At the lowest current levels, the controller automatically configures the system to operate in single-phase automatic-DCM mode, thus achieving the highest possible efficiency. In this mode of operation, the lower MOSFET will be configured to automatically detect and prevent discharge current flowing from the output capacitor through the inductors, and the switching frequency will be proportionately reduced, thus greatly reducing both conduction and switching losses.

Smooth mode transitions are facilitated by the R^3 Technology™, which correctly maintains the internally synthesized ripple currents throughout mode transitions. The controller is thus able to deliver the appropriate current to the load throughout mode transitions. The controller contains embedded mode-transition algorithms that maintain voltage-regulation for all control signal input sequences and durations.

While the ISL6266A will respond according to the logic states shown in Table 2, it can deviate from the commanded state during sleep state exit. If the core voltage is directed by the CPU to make a VID change that causes excessive output capacitor inrush current when going from 1-phase DCM to 1-phase CCM, the controller will automatically add Phase 2 until the VID transition is complete. This is beneficial for designs that have very large C_{OUT} values.

The controller contains internal counters that prevent spurious control signal glitches from resulting in unwanted mode transitions. Control signals of less than two switching periods do not result in phase-idling.

TABLE 2. CONTROL SIGNAL TRUTH TABLES FOR OPERATION MODES OF ISL6266 AND ISL6266A

DPRSLPVR	DPRSTP#	PSI#	ISL6266	ISL6266A	VID SLEW RATE	CPU MODE
0	0	0	1-phase CCM	1-phase diode emulation	fast	awake
0	0	1	2-phase CCM	2-phase CCM	fast	awake
0	1	0	1-phase CCM	1-phase diode emulation	fast	awake
0	1	1	2-phase CCM	2-phase CCM	fast	awake
1	0	0	1-phase diode emulation	1-phase diode emulation	slow (Note 5)	sleep
1	0	1	1-phase diode emulation	1-phase diode emulation	slow (Note 5)	sleep
1	1	0	1-phase CCM	1-phase diode emulation	slow	awake
1	1	1	2-phase CCM	2-phase CCM	slow	awake

NOTE:

5. The negative VID slew rate when DPRSTP# = 0 and DPRSLPVR = 1 is limited to no faster than the slow slew rate. However, slower slew rates can be seen. To conserve power, the ISL6266A will tri-state UGATE and LGATE and let the load gradually pull the core voltage back into regulation.

While transitioning to single-phase operation, the controller smoothly transitions current from the idling-phase to the active-phase, and detects the idling-phase zero-current condition. During transitions into automatic-DCM or forced-CCM mode, the timing is carefully adjusted to eliminate output voltage excursions. When a phase is added, the current balance between phases is quickly restored.

When commanded into 1-phase CCM operation according to Table 2, both MOSFETs of Phase 2 will be off. The controller will thus eliminate switching losses associated with the unneeded channel.

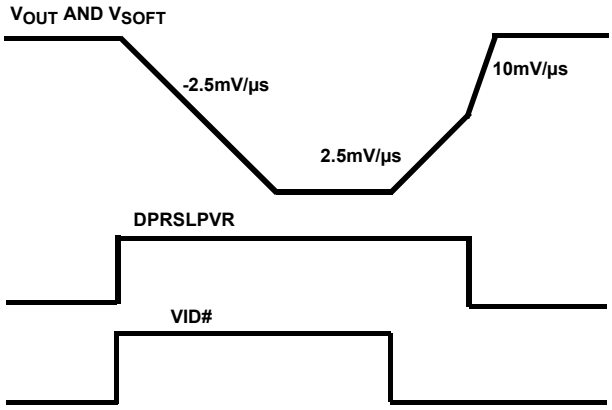


FIGURE 35. DEEPER SLEEP TRANSITION SHOWING DPRSLPVR'S EFFECT ON EXIT SLEW RATE

When commanded to single-phase DCM mode, both MOSFETs associated with Phase 2 are off, and the ISL6266A turns off the lower MOSFET of Channel 1 whenever the Channel 1 current decays to zero. As load is further reduced, the Phase 1 channel switching frequency decreases to maintain high efficiency. The operation of the inactive for 1-phase DCM and 1-phase CCM described previously refers to the ISL6266A only. See “ISL6266 Features” on page 21 for information on the ISL6266.

The ISL6266A can be configured to operate as a single phase regulator using the same layout as a two phase design to accommodate lower power CPUs. To accomplish this, the designer must connect ISEN1 and ISEN2 to VCC_PRM (reference AN1376 for signal names). Channel 2 components can be removed as well as current balance circuitry. The ISL6266A will power-up and regulate in DCM or CCM based on the state of PSI#, as outlined in Table 2. The OCP threshold will also change based on the state of PSI#, as outlined in “Protection” on page 20.

Dynamic Operation

Figure 35 shows that the ISL6266A responds to changes in VID command voltage by slewing to new voltages with a dV/dt set by the SOFT capacitor and by the state of DPRSLPVR. With C_{SOFT} = 15nF and DPRSLPVR HIGH, the output voltage will move at ±2.8mV/µs for large changes in voltage. For DPRSLPVR LOW, the large signal dV/dt will be ±10mV/µs. As the output voltage approaches the VID command value, the dV/dt moderates to prevent overshoot.

Keeping DPRSLPVR HIGH for voltage transitions into and out of Deeper Sleep will result in low dV/dt output voltage changes with resulting minimized audio noise. For fastest recovery from Deeper Sleep to Active mode, holding DPRSLPVR LOW results in maximum dV/dt. Therefore, the ISL6266A is IMVP-6+ compliant for DPRSTP# and DPRSLPVR logic.

Intersil's R^3 Technology™ has intrinsic voltage feedforward. As a result, high-speed input voltage steps do not result in significant output voltage perturbations. In response to load current step increases, the ISL6266A will transiently raise the switching frequency so that response time is decreased and current is shared by two channels.

Protection

The ISL6266A provides overcurrent, overvoltage, undervoltage protection and over-temperature protection, as shown in Table 3.

TABLE 3. FAULT-PROTECTION SUMMARY OF ISL6266, ISL6266A

	FAULT DURATION PRIOR TO PROTECTION	PROTECTION ACTIONS	FAULT RESET
Overcurrent fault	120µs	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Way-Overcurrent fault	<2µs	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Overvoltage fault (1.7V)	Immediately	Low-side MOSFET on until V_{CORE} <0.85V, then PWM three-state, PGOOD latched low (0V to 1.7V always)	VDD toggle
Overvoltage fault (+200mV)	1ms	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Undervoltage fault (-300mV)	1ms	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Current imbalance fault (7.5mV)	1ms	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Over-temperature fault (NTC <1.18V)	Immediately	VR_TT# goes low	N/A

Overcurrent protection is tied to the voltage droop, which is determined by the resistors selected as described in "Component Selection and Application" on page 22. After the load-line is set, the OCSET resistor can be selected to detect overcurrent at any level of droop voltage. An overcurrent fault will occur when the load current exceeds the overcurrent setpoint voltage while the regulator is in a 2-phase mode. While the regulator is in a 1-phase mode of operation, the overcurrent setpoint is automatically reduced to 50% of two-phase overcurrent level, and the fast-trip way-overcurrent set point is reduced to 66%. For overcurrents less than 2.5 times the OCSET level, the over-load condition must exist for 120µs in order to trip the OC fault latch. This is shown in Figure 25.

For over-loads exceeding 2.5 times the set level, the PWM outputs will immediately shut off and PGOOD goes low to maximize protection due to hard shorts.

In addition, excessive phase imbalance (for example, due to gate driver failure) will be detected in two-phase operation and the controller will be shut-down 1ms after detection of the excessive phase current imbalance. The phase imbalance is detected by the voltage on the ISEN pins if the difference is greater than 9mV.

Undervoltage protection is independent of the overcurrent limit. If the output voltage is less than the VID set value by 300mV or more, a fault will latch after 1ms in that condition, turning the PWM outputs off and pulling PGOOD to ground. Note that most practical core regulators will have the overcurrent set to trip before the -300mV undervoltage limit.

There are two levels of overvoltage protection and response.

1. For output voltage exceeding the set value by +200mV for 1ms, a fault is declared. All of the above faults have the same action taken: PGOOD is latched low and the upper and lower power MOSFETs are turned off so that inductor current will decay through the MOSFET(s) body diode(s). This condition can be reset by bringing VR_ON low or by bringing VDD below 4V. When these inputs are returned to their high operating levels, a soft-start will occur.
2. The second level of overvoltage protection behaves differently (see Figure 26). If the output exceeds 1.7V, an OV fault is immediately declared, PGOOD is latched low and the low-side MOSFETs are turned on. The low-side MOSFETs will remain on until the output voltage is pulled down below about 0.85V, at which time all MOSFETs are turned off. If the output again rises above 1.7V, the protection process is repeated. This offers the maximum amount of protection against a shorted high-side MOSFET while preventing output ringing below ground. The 1.7V OV is not reset with VR_ON, but requires that VDD be lowered to reset. The 1.7V OV detector is active at all times that the controller is enabled including after one of the other faults occurs so that the processor is protected against high-side MOSFET leakage while the MOSFETs are commanded off.

The ISL6266A has a thermal throttling feature. If the voltage on the NTC pin goes below the 1.2V over-temperature threshold, the VR_TT# pin is pulled low indicating the need for thermal throttling to the system oversight processor. No other action is taken within the ISL6266A in response to NTC pin voltage.

Power Monitor

The power monitor signal is an analog output. Its magnitude is proportional to the product of $V_{CCSENSE}$ and the voltage difference between V_{droop} and V_O, which is the programmed voltage droop value, equal to load current multiplied by the load line impedance (for example 2.1mΩ). The output voltage of the PMON pin in two-phase design is given by Equation 1:

$$V_{PMON} = V_{CCSENSE} \bullet (V_{DROOP} - V_O) \bullet 17.5 \quad \text{(EQ. 1)}$$

Equation 1 can be expressed in terms of load current as seen in Equation 2:

$$V_{PMON} = (V_{CCSENSE} \bullet I_{CORE}) \bullet 2.1m\Omega \bullet 17.5 \quad \text{(EQ. 2)}$$

The power consumed by the CPU can be calculated by Equation 3:

$$P_{CPU} = V_{PMON} / (17.5 \bullet 0.0021) \bullet (WATT) \quad \text{(EQ. 3)}$$

where 0.0021 is the typical load line slope. The power monitor load regulation is approximately 7Ω. Within its sourcing/sinking current capability range, when the power monitor loading changes to 1mA, the output of the power monitor will change to 7mV. The 7Ω impedance is associated with the layout and package resistance of PMON inside the IC. In practical applications, compared to the load resistance on the PMON pin, 7Ω output impedance contributes no significant error.

ISL6266 Features

The ISL6266 incorporates all the features previously listed for the ISL6266A. However, the sleep state logic is slightly altered (see Table 2). In addition to those differences, the ISL6266 has been optimized to work with coupled-inductor solutions. Due to mutual magnetic fields between the individual phase windings of the coupled-inductor, the effective per-phase inductance equals the leakage inductance of the transformer. This can be very low (e.g. 90nH), which allows for faster channel current slew rates and, consequently, an all-ceramic output capacitor bank can be utilized. Additionally, the current ripple is lower than would be produced with two discrete inductors of equivalent value to the coupled-inductor leakage. This improves coupled-inductor efficiency over discrete inductor solutions for the same transient response.

In single phase operation, the active channel inductor will continue to build a mutual field in the inactive channel inductor. This field must be dissipated every cycle to maintain inductor volt-second balance. The ISL6266 continues to turn on the lower MOSFET for the inactive channel to deplete the induced field with minimum power loss.

Component Selection and Application

Soft-Start and Mode Change Slew Rates

The ISL6266A uses two slew rates for various modes of operation. The first is a slow slew rate used to reduce in-rush current during start-up. It is also used to reduce audible noise when entering or exiting Deeper Sleep Mode. A faster slew rate is used to exit out of Deeper Sleep and to enhance system performance by achieving active mode regulation more quickly. Note that the SOFT capacitor current is bidirectional. The current is flowing into the SOFT capacitor when the output voltage is commanded to rise and out of the SOFT capacitor when the output voltage is commanded to fall.

Figure 36 illustrates how the two slew rates are determined by commanding one of two current sources into or out of the SOFT pin. The capacitor from the SOFT pin to ground holds the voltage commanded by the two current sources. The voltage is fed into the non-inverting input of the error amplifier and sets the regulated system voltage. Depending on the state of the system (Start-Up or Active mode) and the state of the DPRSLPVR pin, one of the two currents shown in Figure 36 will be used to charge or discharge this capacitor, thereby controlling the slew rate of the newly commanded voltage. These currents can be found under “SOFT-START CURRENT” on page 4 of the “Electrical Specifications” table.

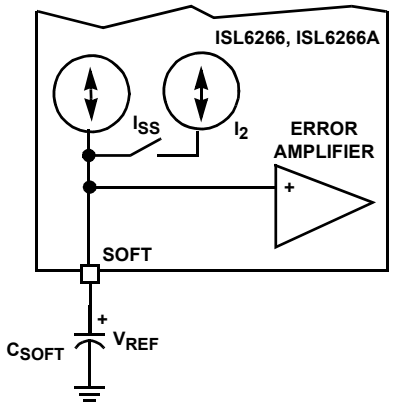


FIGURE 36. SOFT PIN CURRENT SOURCES FOR FAST AND SLOW SLEW RATES

The first current, labeled I_{SS}, is given in the “Electrical Specifications” table on page 4 as 42µA. This current is used during soft-start. The second current (I_2) sums with I_{SS} to get the larger of the two currents, labeled I_{GV} in the “Electrical Specifications” table on page 4. This total current is typically 205µA with a minimum of 180µA.

The IMVP-6+ specification dictates the critical timing associated with regulating the output voltage. The symbol, SLEWRATE, as given in the IMVP-6+ specification will determine the choice of the SOFT capacitor (C_{SOFT}) by Equation 4.

$$C_{SOFT} = \frac{I_{GV}}{SLEWRATE} \quad \text{(EQ. 4)}$$

Using a SLEWRATE of 10mV/µs and the typical I_{GV} value given in the “Electrical Specifications” table on page 4 of 205µA, C_{SOFT} is as shown in Equation 5.

$$C_{SOFT} = 205\mu A/(10mV/1\mu s) \quad \text{(EQ. 5)}$$

A choice of 0.015µF would guarantee a SLEWRATE of 10mV/µs is met for the minimum I_{GV} value given in the “Electrical Specifications” table on page 4. This choice of C_{SOFT} will then control the start-up slewrate as well. One should expect the output voltage to slew to the boot value of 1.2V at a rate given by Equation 6.

$$\frac{dV}{dt} = \frac{I_{SS}}{C_{SOFT}} = \frac{41\mu A}{0.015\mu F} = 2.8mV/\mu s \quad \text{(EQ. 6)}$$

Selecting RBIAS

To properly bias the ISL6266A, a reference current is established by placing a 147kΩ, 1% tolerance resistor from the RBIAS pin to ground. This will provide a highly accurate 10µA current source from which the OCSET reference current can be derived.

Care should be taken in layout that the resistor is placed very close to the RBIAS pin and that a good quality signal ground is connected to the opposite side of the RBIAS resistor. Do not connect any other components to this pin as this would negatively impact performance. Capacitance on this pin would create instabilities and should be avoided.

Start-Up Operation - CLK_EN# and PGOOD

The ISL6266A provides a 3.3V logic output pin for CLK_EN#. The 3V3 pin allows for a system 3.3V source to be connected to separated circuitry inside the ISL6266A, solely devoted to the CLK_EN# function. The output is a 3.3V CMOS signal with 4mA sourcing and sinking capability. This implementation removes the need for an external pull-up resistor on this pin, thereby removing a leakage path from the 3.3V supply to ground when the logic state is low. The lack of superfluous current leakage paths serves to prolong battery life. For noise immunity, the 3.3V supply should be decoupled to digital ground rather than to analog ground.

As mentioned in “Theory of Operation” on page 18, CLK_EN# is logic level high at start-up until approximately 43µs after the V_{CC_CORE} is in regulation at the Boot level. Afterwards, CLK_EN# transitions low, triggering an internal timer for the IMVP6_PWRGD signal. When the timer reaches 6.8ms, IMVP-6_PWRGD will toggle high.

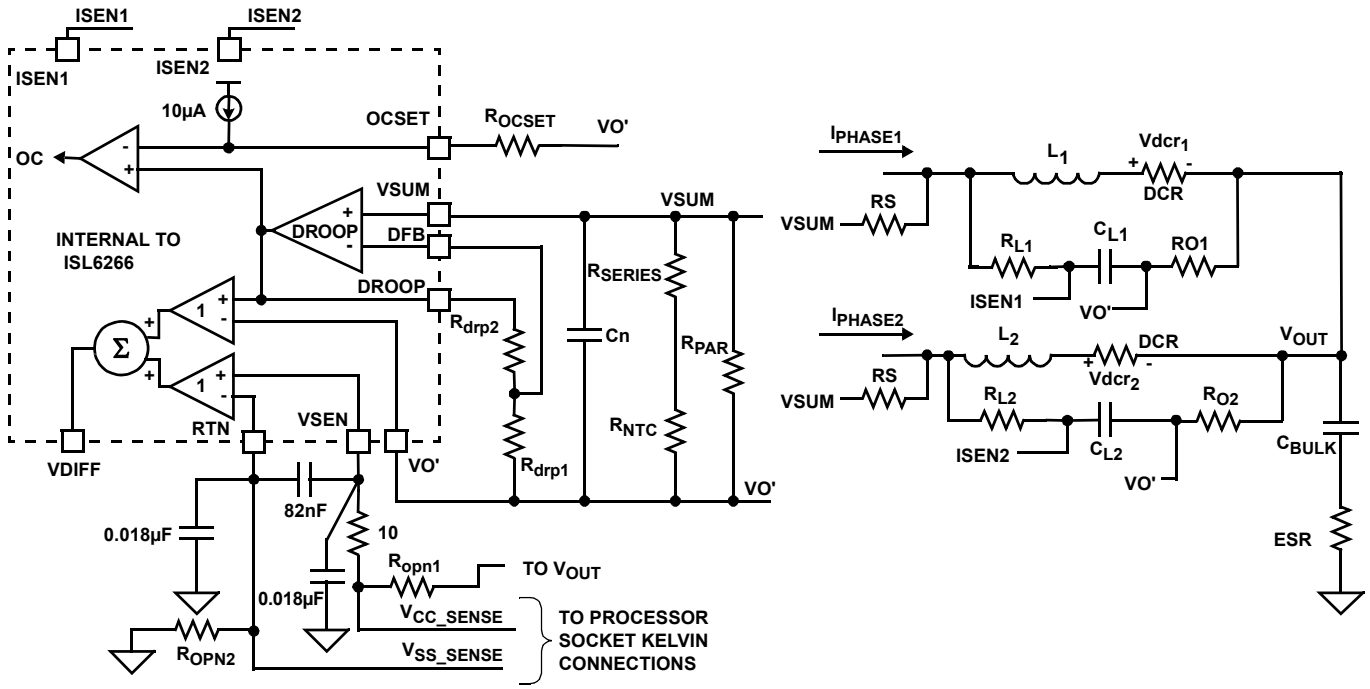


FIGURE 37. SIMPLIFIED SCHEMATIC FOR DROOP AND DIE SENSING WITH INDUCTOR DCR CURRENT SENSING

Static Mode of Operation - Processor Die Sensing

Die sensing is the ability of the controller to regulate the core output voltage at a remotely sensed point. This allows the voltage regulator to compensate for various resistive drops in the power path and ensure that the voltage seen at the CPU die is the correct level independent of load current.

The VSEN and RTN pins of the ISL6266A are connected to Kelvin sense leads at the die of the processor through the processor socket. These signal names are V_{CC_SENSE} and V_{SS_SENSE} respectively. This allows the voltage regulator to tightly control the processor voltage at the die, independent of layout inconsistencies and voltage drops. This Kelvin sense technique provides for extremely tight load line regulation.

These traces should be treated as noise sensitive traces. For optimum load line regulation performance, the traces connecting these two pins to the Kelvin sense leads of the processor must be laid out away from rapidly rising/falling voltage nodes (switching nodes) and other noisy traces. To achieve optimum performance, place common mode and differential mode RC filters to analog ground on VSEN and RTN as shown in Figure 37. The filter resistors should be 10Ω so that they do not interact with the 50kΩ input resistance of the differential amplifier. The filter resistor may be inserted between V_{CC_SENSE} and the VSEN pin. Another option is to place to the filter resistor between Vcc_sense and VSEN pin and between V_{SS_SENSE} and RTN pin. The need for RC filters really depends on the actual board layout and noise environment.

Intersil recommends the use of the R_{OPN1} and R_{OPN2} connected to V_{OUT} and ground as shown in Figure 37. These resistors provide voltage feedback in the event that the system is powered up without a processor installed. These resistors typically range from 20Ω to 100Ω.

Setting the Switching Frequency - FSET

The R^3 modulator scheme is not a fixed frequency PWM architecture. The switching frequency can increase during the application of a load to improve transient performance.

It also varies slightly due to changes in input and output voltage and output current, but this variation is normally less than 10% in continuous conduction mode.

See Figure 32. The resistor connected between the VW and COMP pins of the ISL6266A adjusts the switching window, and therefore adjusts the switching frequency. The R_{FSET} resistor that sets up the switching frequency of the converter operating in CCM can be determined using Equation 7, where R_{FSET} is in kΩ and the switching frequency is in kHz.

$$R_{FSET(k\Omega)} = \left(\frac{F_{SW(kHz)}}{2232}\right)^{-1.1202} \quad \text{(EQ. 7)}$$

Equation 7 is only a rough estimate of actual frequency. It should be used to choose an R_{FSET} value in the vicinity of the desired switching frequency. Empirical fine tuning may be necessary to achieve the actual frequency target. In addition, droop amplifier gain may slightly affect the switching frequency. Equation 7 is derived using the droop gain seen on the ISL6266AEVAL1Z REV A evaluation board.

For 300kHz operation, R_{FSET} is suggested to be 9.53kΩ. In discontinuous conduction mode (DCM), the ISL6266A runs in period stretching mode. The switching frequency is dependent on the load current level. In general, lighter loads will produce lower switching frequencies. Therefore, switching loss is greatly reduced for light load operation, which conserves battery power in portable applications.

Voltage Regulator Thermal Throttling

Intel® IMVP-6+ technology supports thermal throttling of the processor to prevent catastrophic thermal damage to the voltage regulator. The ISL6266A features a thermal monitor that senses the voltage change across an externally placed negative temperature coefficient (NTC) thermistor.

Proper selection and placement of the NTC thermistor allows for detection of a designated temperature rise by the system.

Figure 38 shows the thermal throttling feature with hysteresis. At low temperature, SW1 is on and SW2 connects to the 1.2V side. The total current going into NTC pin is 60µA. The voltage on the NTC pin is higher than the threshold voltage of 1.2V and the comparator output is low. VR_TT# is pulled high by the external resistor.

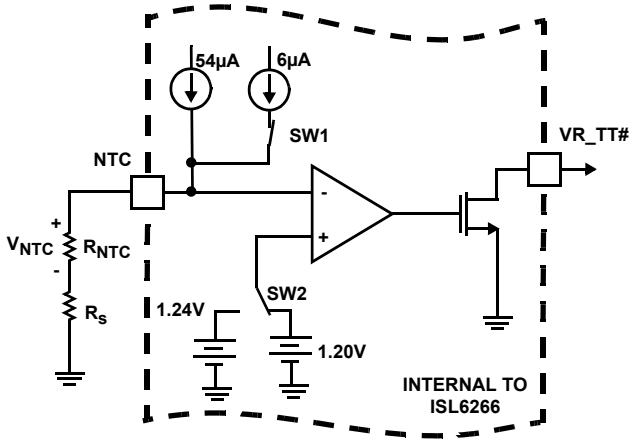


FIGURE 38. CIRCUITRY ASSOCIATED WITH THE THERMAL THROTTLING FEATURE IN ISL6266

When the temperature increases, the NTC resistor value decreases, thus reducing the voltage on the NTC pin. When the voltage decreases to a level lower than 1.2V, the comparator output changes polarity and turns SW1 off and connects SW2 to 1.24V. This pulls VR_TT# low and sends the signal to start thermal throttle. There is a 6µA current reduction on the NTC pin and 20mV voltage increase on the threshold voltage of the comparator in this state. The VR_TT# signal will be used to change the CPU operation and decrease the power consumption. Temperature will decrease over time and the NTC thermistor voltage will go up. When the NTC pin voltage achieves 1.24V, the comparator output will resume its original state. This temperature hysteresis feature of VR_TT# is illustrated in Figure 39. T_1 represents the higher temperature point at which the VR_TT# goes from low to high due to the system temperature rise. T_2 represents the lower temperature point at which the VR_TT# goes high from low because the system temperature decreases to acceptable levels.

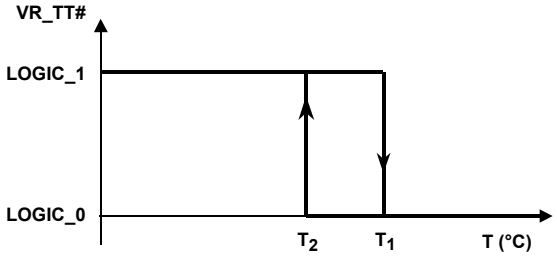


FIGURE 39. TEMPERATURE HYSTERESIS OF VR_TT#

Usually, the NTC thermistor's resistance can be approximated by Equation 8.

$$R_{NTC}(T) = R_{NTCTo} \bullet e^{b \bullet \left(\frac{1}{T+273} - \frac{1}{To+273}\right)} \quad \text{(EQ. 8)}$$

T is the temperature of the NTC thermistor and b is a parameter constant depending on the thermistor material. T_o is the reference temperature in which the approximation is derived. The most common temperature for T_o is +25°C. For example, there are commercial NTC thermistor products with b = 2750kΩ, b = 2600kΩ, b = 4500kΩ or b = 4250kΩ.

From the operation principle of the VR_TT# circuit explained, the NTC resistor satisfies Equations 9 through 13:

$$R_{NTC}(T_1) + R_S = \frac{1.2V}{60\mu A} = 20k\Omega \quad \text{(EQ. 9)}$$

$$R_{NTC}(T_2) + R_S = \frac{1.24V}{54\mu A} = 22.96k\Omega \quad \text{(EQ. 10)}$$

From Equation 9 and Equation 10, Equation 11 can be derived:

$$R_{NTC}(T_2) - R_{NTC}(T_1) = 2.96k\Omega \quad \text{(EQ. 11)}$$

Using Equation 8 into Equation 11, the required nominal NTC resistor value can be obtained by Equation 12:

$$R_{NTCTo} = \frac{2.96k\Omega \bullet e^{b \bullet \left(\frac{1}{T_o+273}\right)}}{e^{b \bullet \left(\frac{1}{T_2+273}\right)} - e^{b \bullet \left(\frac{1}{T_1+273}\right)}} \quad \text{(EQ. 12)}$$

For those cases where the constant b is not accurate enough to approximate the resistor value, the manufacturer provides the resistor ratio information at different temperatures. The nominal NTC resistor value may be expressed in another way shown in Equation 13.

$$R_{NTCTo} = \frac{2.96k\Omega}{\frac{\Lambda}{R_{NTC(T_2)}} - \frac{\Lambda}{R_{NTC(T_1)}}} \quad \text{(EQ. 13)}$$

where $\overset{\Lambda}{R}_{NTC(T)}$ is the normalized NTC resistance to its nominal value. Most data sheets of the NTC thermistor give the normalized resistor value based on its value at +25°C.

Once the NTC thermistor resistor is determined, the series resistor can be derived by Equation 14:

$$R_S = \frac{1.2V}{60\mu A} - R_{NTC}(T1) = 20k\Omega - R_{NTC_T_1} \quad \text{(EQ. 14)}$$

Once R_{NTCTo} and R_s is designed, the actual NTC resistance at T_2 and the actual T_2 temperature can be found in Equations 15 and 16:

$$R_{NTC_T_2} = 2.96k\Omega + R_{NTC_T_1} \quad \text{(EQ. 15)}$$

$$T_{2_actual} = \frac{1}{\frac{1}{b}\ln\left(\frac{R_{NTC_T_2}}{R_{NTCTo}}\right) + 1/(273 + To)} - 273 \quad \text{(EQ. 16)}$$

For example, if using Equations 12, 13 and 14 to design a thermal throttling circuit with the temperature hysteresis +100°C to +105°C, since T_1 = +105°C and T_2 = +100°C, and if we use a Panasonic NTC with b = 4700, Equation 12 gives the required NTC nominal resistance as R_{NTC_To} = 459kΩ.

In fact, the data sheet gives the resistor ratio value at +100°C to +105°C, which is 0.03956 and 0.03322 respectively. The b value 4700kΩ in the Panasonic data sheet only covers to +85°C. Therefore, using Equation 13 is more accurate for +100°C design, the required NTC nominal resistance at +25°C is 467kΩ. The closest NTC resistor value from the manufacturer is 467kΩ. The series resistance is given by Equation 17 as follows:

$$R_S = 20k\Omega - R_{NTC_105°C} = 20k\Omega - 15.65k\Omega = 4.35k\Omega \quad \text{(EQ. 17)}$$

The closest standard resistor to this result is 4.42kΩ. The NTC resistance at T_2 is given by Equation 18.

$$R_{NTC_T2} = 2.96k\Omega + R_{NTC_T1} = 18.16k\Omega \quad \text{(EQ. 18)}$$

Therefore, the NTC branch is designed to have a 470kΩ NTC and 4.42kΩ resistor in series. The part number of the NTC thermistor is ERTJ0EV474J in an 0402 package. The NTC thermistor should be placed in the spot that provides the best indication of the voltage regulator circuit temperature.

Static Mode of Operation - Static Droop Using DCR Sensing

As previously mentioned, the ISL6266A has a differential amplifier that provides precision voltage monitoring at the processor die for both single-phase and two-phase operation. This enables the ISL6266A to achieve an accurate load line in accordance with the IMVP-6+ specification.

DESIGN EXAMPLE

The process of compensation for DCR resistance variation to achieve the desired load line droop has several steps and may be iterative.

A two-phase solution using DCR sensing is shown in Figure 37. There are two resistors connecting to the terminals of inductor of each phase. These are labeled RS and RO. These resistors are used to obtain the DC voltage drop across each inductor. The DC current flowing through each inductor will create a DC voltage drop across the real winding resistance (DCR). This voltage is proportional to the average inductor current by Ohm's Law. When this voltage is summed with the other channel's DC voltage, the total DC load current can be derived.

R_O is typically 1Ω to 10Ω. This resistor is used to tie the outputs of all channels together and thus create a summed average of the local CORE voltage output. R_S is determined

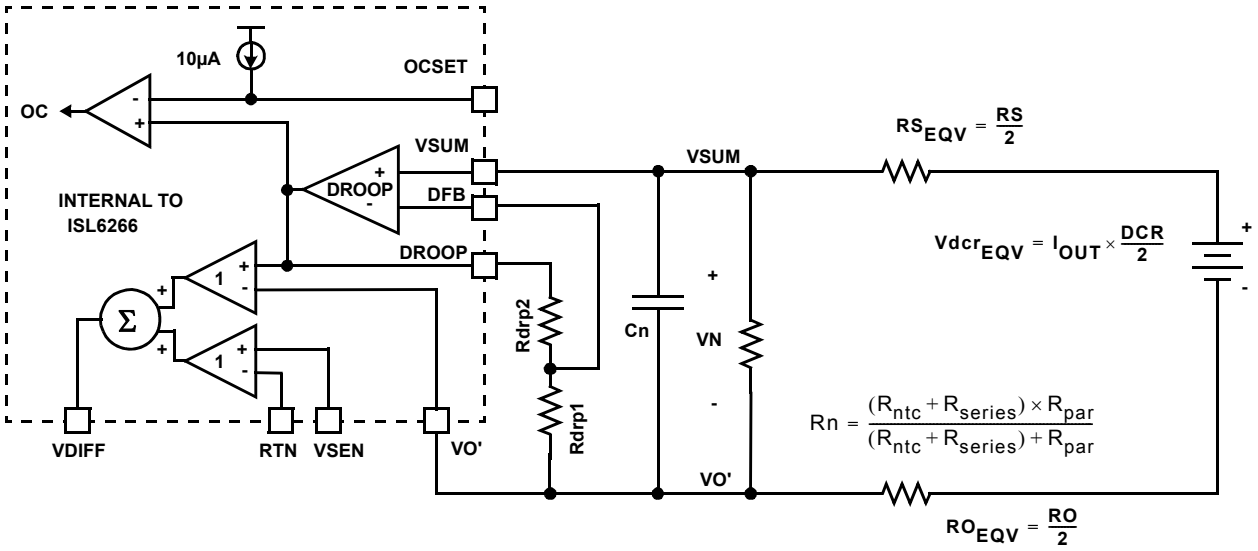


FIGURE 40. EQUIVALENT MODEL FOR DROOP AND DIE SENSING USING DCR SENSING

through an understanding of both the DC and transient load currents. This value will be covered in the next section. However, it is important to keep in mind that the outputs of each of these R_S resistors are tied together to create the VSUM voltage node. With both the outputs of R_O and R_S tied together, the simplified model for the droop circuit can be derived. This is presented in Figure 40.

Figure 40 shows the simplified model of the droop circuitry. Essentially, one resistor can replace the R_O resistors of each phase and one R_S resistor can replace the R_S resistors of each phase. The total DCR drop due to load current can be replaced by a DC source, the value of which is given by Equation 19:

$$V_{DCR_EQU} = \frac{I_{OUT} \bullet DCR}{2} \quad \text{(EQ. 19)}$$

For the convenience of analysis, the NTC network comprised of R_{ntc}, R_{series} and R_{par}, given in Figure 37, is labeled as a single resistor R_N in Figure 40.

The first step in droop load line compensation is to adjust R_N, RO_{EQV} and RS_{EQV} such that sufficient droop voltage exists even at light loads between the VSUM and VO' nodes. As a rule of thumb, we start with the voltage drop across the R_N network, Vn, to be 0.5x to 0.8x V_{DCR_EQU}. This ratio provides for a fairly reasonable amount of light load signal from which to arrive at droop.

The resultant NTC network resistor value is dependent on the temperature and given by Equation 20.

$$R_n(T) = \frac{(R_{series} + R_{ntc}) \bullet R_{par}}{R_{series} + R_{ntc} + R_{par}} \quad \text{(EQ. 20)}$$

For simplicity, the gain of Vn to the V_{DCR_EQU} is defined by G1, also dependent on the temperature of the NTC thermistor.

$$G_1(T) \overset{\Delta}{=} \frac{R_n(T)}{R_n(T) + RS_{EQV}} \quad \text{(EQ. 21)}$$

$$DCR(T) = DCR_{25°C} \bullet (1 + 0.00393*(T-25)) \quad \text{(EQ. 22)}$$

Therefore, the output of the droop amplifier divided by the total load current can be expressed as shown in Equation 23, where R_{droop} is the realized load line slope and 0.00393 is the temperature coefficient of the copper.

$$R_{droop} = G_1(T) \bullet \frac{DCR_{25}}{2} \bullet (1 + 0.00393*(T-25)) \bullet k_{droopamp} \quad \text{(EQ. 23)}$$

How to achieve the droop value independent of the inductor temperature is expressed by Equation 24.

$$G_1(T) \bullet (1 + 0.00393*(T-25)) \cong G_{1target} \quad \text{(EQ. 24)}$$

The non-inverting droop amplifier circuit has the gain $K_{droopamp}$ expressed as Equation 25:

$$k_{droopamp} = 1 + \frac{R_{drp2}}{R_{drp1}} \quad \text{(EQ. 25)}$$

$G_{1target}$ is the desired gain of Vn over I_{OUT} • DCR/2. Therefore, the temperature characteristics of gain of Vn is described by Equation 26.

$$G_1(T) = \frac{G_{1target}}{(1 + 0.00393*(T-25))} \quad \text{(EQ. 26)}$$

For the $G_{1target}$ = 0.76:
R_{ntc} = 10kΩ with b = 4300,
R_{series} = 2610Ω, and
R_{par} = 11kΩ

RS_{EQV} = 1825Ω generates a desired G1, close to the feature specified in Equation 26.

The actual G1 at +25°C is 0.769. A design file is available to generate the proper values of R_{ntc}, R_{series}, R_{par}, and RS_{EQV} for values of the NTC thermistor and G1 that differ from the example provided here.

The individual resistors from each phase to the VSUM node, labeled R_{S1} and R_{S2} in Figure 37, are then given by Equation 27.

$$Rs = 2 \bullet RS_{EQV} \quad \text{(EQ. 27)}$$

So, R_S = 3650Ω. Once we know the attenuation of the R_S and R_N network, we can then determine the droop amplifier gain required to achieve the load line. Setting R_{drp1} = 1k_1%, then R_{drp2} can be found using Equation 28.

$$R_{drp2} = \left(\frac{2 \bullet R_{droop}}{DCR \bullet G1(25°C)} - 1\right) \bullet R_{drp1} \quad \text{(EQ. 28)}$$

Droop Impedance (R_{droop}) = 0.0021 (V/A) as per the Intel IMVP-6+ specification. Using DCR = 0.0008Ω typical for a 0.36µH inductor, R_{drp1} = 1kΩ and the attenuation gain (G1) = 0.77, R_{drp2} is then given by Equation 29:

$$R_{drp2} = \left(\frac{2 \bullet R_{droop}}{0.0008 \bullet 0.769} - 1\right) \bullet 1k\Omega \approx 5.82k\Omega \quad \text{(EQ. 29)}$$

Note, we choose to ignore the R_O resistors because they do not add significant error.

These designed values in R_n network are very sensitive to the layout and coupling factor of the NTC to the inductor. As only one NTC is required in this application, this NTC should be placed as close to the Channel 1 inductor as possible and PCB traces sensing the inductor voltage should route directly to the inductor pads.

Due to layout parasitics, small adjustments may be necessary to accurately achieve the full load droop voltage. This can be easily accomplished by allowing the system to achieve thermal equilibrium at full load, and then adjusting R_{drp2} to obtain the appropriate load line slope.

To see whether the NTC has compensated the temperature change of the DCR, the user can apply full load current and wait for the thermal steady state and see how much the output voltage will deviate from the initial voltage reading. A good compensation can limit the drift to 2mV. If the output voltage is decreasing with temperature increase, the ratio between the NTC thermistor value and the rest of the resistor divider network has to be increased. The user is strongly encouraged to use the evaluation board values and layout to minimize engineering time.

The 2.1mV/A load line should be adjusted by R_{drp2} based on maximum current. The droop gain might vary slightly between small steps (e.g. 10A). For example, if the max current is 40A and the load line 2.1mΩ, the user load the converter to 40A and look for 84mV of droop. If the droop voltage is less than 84mV (e.g. 80mV) the new value will be calculated by Equation 30:

$$R_{drp2_new} = \frac{84mV}{80mV}(R_{drp1} + R_{drp2}) - R_{drp1} \quad \text{(EQ. 30)}$$

For the best accuracy, the effective resistance on the DFB and VSUM pins should be identical so that the bias current of the droop amplifier does not cause an offset voltage. In the previous example, the resistance on the DFB pin is R_{drp1} in parallel with R_{drp2}, that is, 1kΩ in parallel with 5.82kΩ or 853Ω. The resistance on the VSUM pin is R_n in parallel with RS_{EQV} or 5.87kΩ in parallel with 1.825kΩ, which equals 1392Ω. The mismatch in the effective resistances is 1404 - 53 = 551Ω. The mismatch cannot be larger than 600Ω. To reduce the mismatch, multiply both R_{drp1} and R_{drp2} by the appropriate factor. The appropriate factor in this example is 1404/853 = 1.65. In summary, the predicted load line with the designed droop network parameters based on the Intersil design tool is shown in Figure 41.

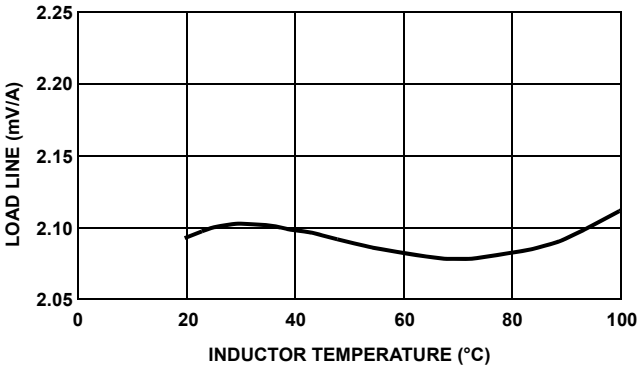


FIGURE 41. LOAD LINE PERFORMANCE WITH NTC THERMAL COMPENSATION

Dynamic Mode of Operation - Dynamic Droop Using DCR Sensing

Droop is very important for load transient performance. If the system is not compensated correctly, the output voltage could sag excessively upon load application and potentially create a system failure. The output voltage could also take a long period of time to settle to its final value, which could be problematic if a load dump were to occur during this time. This situation would cause the output voltage to rise above the no load setpoint of the converter and could potentially damage the CPU.

The L/DCR time constant of the inductor must be matched to the R_n*C_n time constant as shown in Equation 31.

$$\frac{L}{DCR} = \frac{R_n \bullet RS_{EQV}}{R_n + RS_{EQV}} \bullet C_n \quad \text{(EQ. 31)}$$

Solving for C_n we now have Equation 32.

$$C_n = \frac{\frac{L}{DCR}}{\frac{R_n \bullet RS_{EQV}}{R_n + RS_{EQV}}} \quad \text{(EQ. 32)}$$

Note, R_O was neglected. As long as the inductor time constant matches the C_n, R_n and R_s time constants as given previously, the transient performance will be optimum. As in the static droop case, this process may require a slight adjustment to correct for layout inconsistencies. For the example of L = 0.36µH with 0.8mΩ DCR, C_n is calculated in Equation 33.

$$C_n = \frac{\frac{0.36\mu H}{0.0008}}{\text{parallel}(5.823K, 1.825K)} \approx 330nF \quad \text{(EQ. 33)}$$

The value of this capacitor is selected to be 330nF. As the inductors tend to have 20% to 30% tolerances, this capacitor generally will be tuned on the board by examining the transient voltage. If the output voltage transient has an initial dip lower than the voltage required by the load line and slowly increases back to steady state, the capacitor is too small and vice versa. It is better to have the capacitor value a little bigger to cover the tolerance of the inductor to prevent the output voltage from going lower than the spec. This capacitor needs to be a high grade capacitor like X7R with low tolerance. There is another consideration in order to achieve better time constant match mentioned previously. The NPO/COG (class-I) capacitors have only 5% tolerance and very good thermal characteristics. However, these capacitors are only available in small capacitance values. In order to use such capacitors, the resistors and thermistors surrounding the droop voltage sensing and droop amplifier has to be resized up to 10x larger to reduce the capacitance by 10x. Careful attention must be paid in balancing the impedance of droop amplifier in this case.

Dynamic Mode of Operation - Compensation Parameters

Considering the voltage regulator as a black box with a voltage source controlled by VID and a series impedance, in order to achieve the 2.1mV/A load line, the impedance needs to be 2.1mΩ. The compensation design has to target the output impedance of the converter to be 2.1mΩ. There is a mathematical calculation file available to the user. The power stage parameters such as L and Cs are needed as the input to calculate the compensation component values. Attention must

be paid to the input resistor to the FB pin. Too high of a resistor will cause an error to the output voltage regulation because of bias current flowing in the FB pin. It is better to keep this resistor below 3kΩ when using this file.

Static Mode of Operation - Current Balance Using DCR or Discrete Resistor Current Sensing

Current Balance is achieved in the ISL6266A by measuring the voltages present on the ISEN pins and adjusting the duty cycle of each phase until they match. R_L and C_L around each inductor, or around each discrete current resistor, are used to create a rather large time constant such that the ISEN voltages have minimal ripple voltage and represent the DC current flowing through each channel's inductor. For optimum performance, R_L is chosen to be 10kΩ and C_L is selected to be 0.22µF. When discrete resistor sensing is used, a capacitor most likely needs to be placed in parallel with R_L to properly compensate the current balance circuit.

ISL6266A uses an RC filter to sense the average voltage on phase node and forces the average voltage on the phase node to be equal for current balance. Even though the ISL6266A forces the ISEN voltages to be almost equal, the inductor currents will not be exactly equal. Using DCR current sensing as an example, two errors have to be added to find the total current imbalance.

1. Mismatch of DCR: If the DCR has a 5% tolerance, the resistors could mismatch by 10% worst case. If each phase is carrying 20A, the phase currents mismatch by 20A*10% = 2A.
2. Mismatch of phase voltages/offset voltage of ISEN pins: The phase voltages are within 2mV of each other by the current balance circuit. The error current that results is given by 2mV/DCR. If DCR = 1mΩ then the error is 2A.

In the previous example, the two errors add to 4A. For the two phase DC/DC, the currents would be 22A in one phase and 18A in the other phase. In the previous analysis, the current balance can be calculated with 2A/20A = 10%. This is the worst case calculation. For example, the actual tolerance of two 10% DCRs is 10%*√(2) = 7%.

There are provisions to correct the current imbalance due to layout or to purposely divert current to certain phase for better thermal management. The Customer can put a resistor in parallel with the current sensing capacitor on the phase of interest in order to purposely increase the current in that phase.

If the PC board trace resistance from the inductor to the microprocessor are significantly different between two phases, the current will not be balanced perfectly. Intersil has a proprietary method to achieve the perfect current sharing in cases of severely imbalanced layouts.

When choosing the current sense resistor, both the tolerance of the resistance and the TCR are important. Also, the current sense resistor's combined tolerance at a wide temperature range should be calculated.

Droop Using Discrete Resistor Sensing - Static/Dynamic Mode of Operation

Figure 42 shows the equivalent circuit of a discrete current sense approach. Figure 33 shows a more detailed schematic of this approach. Droop is solved the same way as the DCR sensing approach with a few slight modifications.

First, because there is no NTC required for thermal compensation, the R_n resistor network in the previous section is not required. Second, because there is no time constant matching required, the C_n component is not matched to the L/DCR time constant. This component does indeed provide noise immunity and therefore is populated with a 39pF capacitor.

The R_S values in the previous section, R_S = 1.5k_1%, are sufficient for this approach.

Now the input to the droop amplifier is essentially the V_{rsense} voltage. This voltage is given by Equation 34.

$$Vrsense_{EQV} = \frac{R_{sense}}{2} \bullet I_{OUT} \quad \text{(EQ. 34)}$$

The gain of the droop amplifier, $K_{droopamp}$, must be adjusted for the ratio of the R_{sense} to droop impedance, R_{droop} by using Equation 35.

$$K_{droopamp} = \frac{R_{droop}}{(R_{sense}/2)} \quad \text{(EQ. 35)}$$

Solving for the R_{drp2} value, R_{droop} = 0.0021(V/A) as per the Intel IMVP-6+ specification, R_{sense} = 0.001Ω and R_{drp1} = 1kΩ, Equation 36 is obtained:

$$R_{drp2} = (K_{droopamp} - 1) \bullet R_{drp1} = 3.2k\Omega \quad \text{(EQ. 36)}$$

Because these values are extremely sensitive to layout, some tweaking may be required to adjust the full load droop. This is fairly easy and can be accomplished by allowing the system to achieve thermal equilibrium at full load, and then adjusting R_{drp2} to obtain the desired droop value.

Fault Protection - Overcurrent Fault Setting

As previously described, the overcurrent protection of the ISL6266A is related to the droop voltage. Previously the droop voltage was calculated as I_{Load}*R_{droop}, where R_{droop} is the load line slope specified as 0.0021 (V/A) in the Intel IMVP-6+ specification. Knowing this relationship, the overcurrent protection threshold can be programmed as an equivalent droop voltage droop. Knowing the voltage droop level allows the user to program the appropriate drop across the R_{OC} resistor. This voltage drop will be referred to as V_{OC}. Once the droop voltage is greater than V_{OC}, the PWM drives will turn off and PGOOD will go low.

The selection of R_{OC} is given in Equation 37. Assuming an overcurrent trip level, I_{OC}, of 55A, and knowing from the Intel

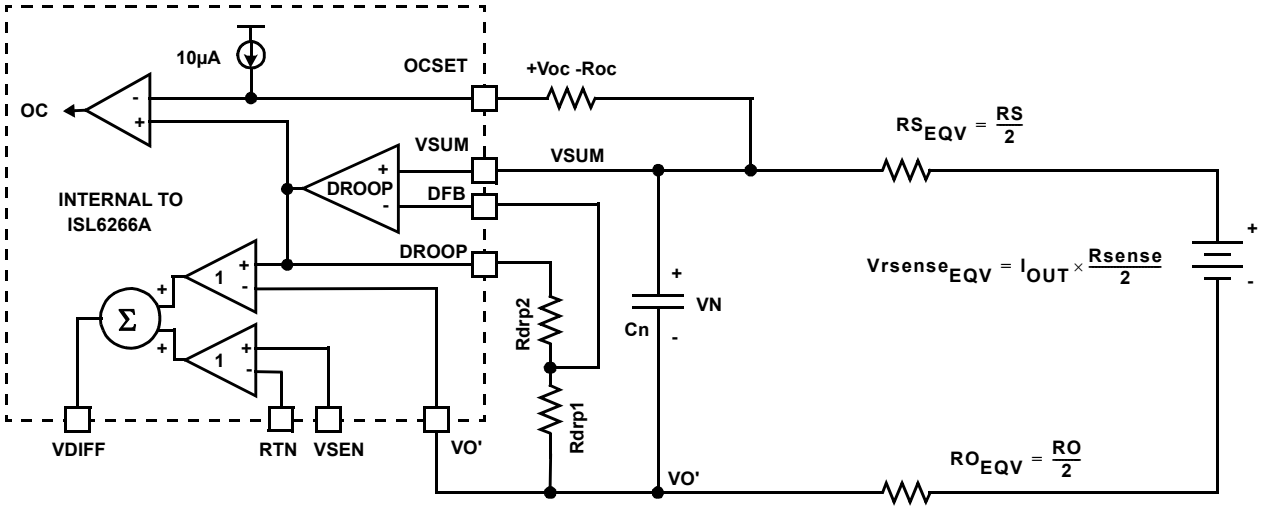


FIGURE 42. EQUIVALENT MODEL FOR DROOP AND DIE SENSING USING DISCRETE RESISTOR SENSING

specification of the load line slope, R_{droop} = 0.0021 (V/A), R_{OC} is calculated by Equation 37.

$$R_{OC} = \frac{I_{OC} \bullet R_{droop}}{10\mu A} = \frac{55 \bullet 0.0021}{10 \bullet 10^{-6}} = 11.5k\Omega \qquad \text{(EQ. 37)}$$

Note, if the droop load line slope is not -0.0021 (V/A) in the application, the overcurrent setpoint will differ from predicted. In addition, due to the saturation limitations of the DROOP amplifier, there is a maximum way-overcurrent (WOC) set point for each VID code. The maximum OC set point that will ensure WOC can be reached is expressed in Equation 38:

$$I_{OC} = \frac{1.75 - VID}{2.5 \cdot R_{DROOP}} \qquad \text{(EQ. 38)}$$

The WOC limitation is only problematic at very high VID settings (~1.350V and above).

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 25, 2015	FN6398.4	Updated Ordering Information table on page 1. Added Revision History and About Intersil sections. Updated Package Outline Drawing L48.7X7 to the latest revision. -Revision 4 to Revision 5 changes - Corrected Note 4 from: "Dimension b applies to.." to: "Dimension applies to.." and enclosed Notes #'s 4, 5 and 6 in a triangle.

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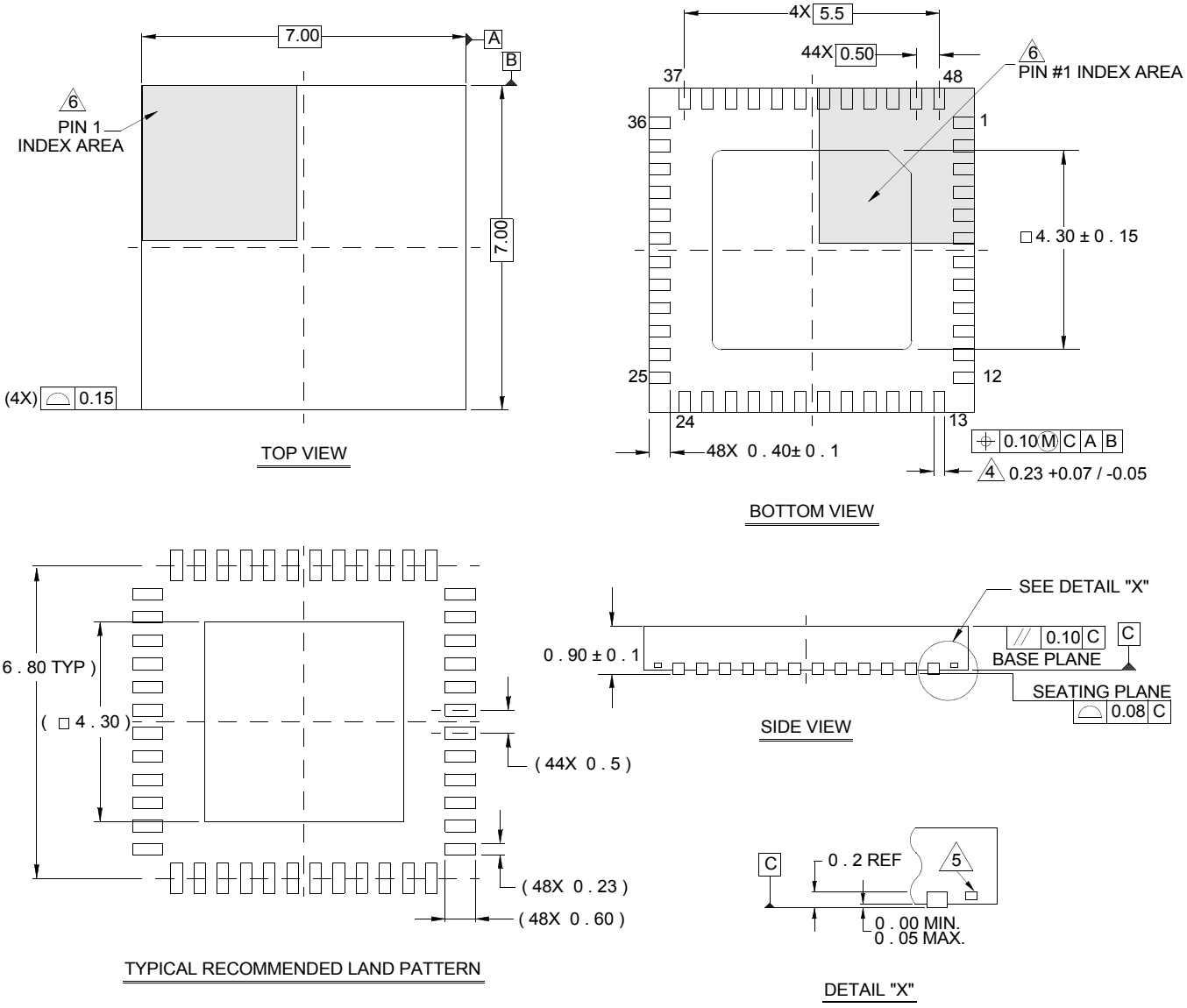
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Package Outline Drawing

L48.7x7

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 4/10



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.