Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

CY74FCT16500T
CY74FCT162500T

18-Bit Registered Transceivers

SCCS056 - August 1994 - Revised March 2000

Features

- **FCT-C speed at 4.6 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of –40˚C to +85˚C**
- **V_{CC} = 5V ± 10%**

CY74FCT16500T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162500T Features:

- **Balanced 24 mA output drivers**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25˚C**

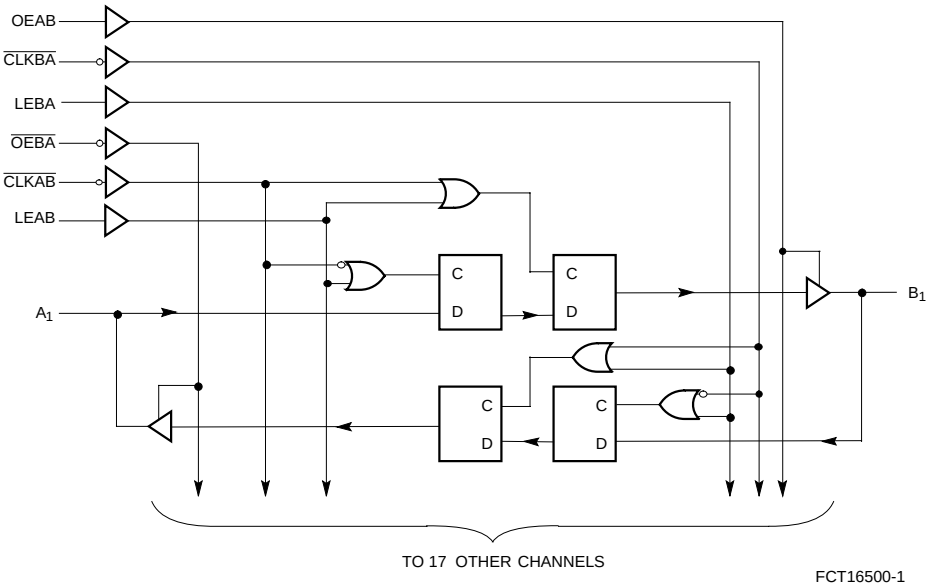
Functional Description

These 18-bit universal bus transceivers can be operated in transparent, latched, or clock modes by combining D-type latches and D-type flip-flops. Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA), and clock inputs ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if $\overline{\text{CLKAB}}$ is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{\text{CLKAB}}$. OEAB performs the output enable function on the B port. Data flow from B-to-A is similar to that of A-to-B and is controlled by $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output buffers are designed with power-off disable feature that allows live insertion of boards.

The CY74FCT16500T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162500T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162500T is ideal for driving transmission lines.

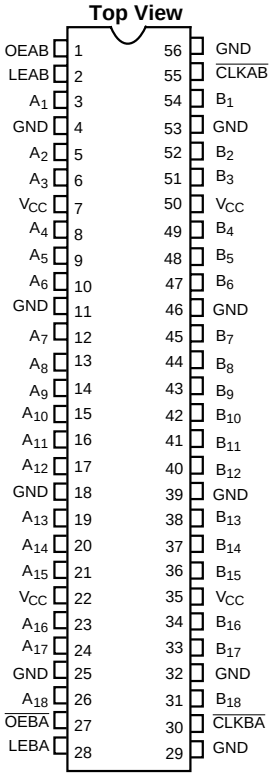
Logic Block Diagram



FCT16500-1

Pin Configuration

SSOP/TSSOP
Top View



FCT16500-2

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Pin Summary

Name	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{CLKAB}$	A-to-B Clock Input (Active LOW)
$\overline{CLKBA}$	B-to-A Clock Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Function Table[1, 2]

Inputs				Outputs
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B[3]
H	L	L	X	B[4]

Maximum Ratings[5, 6]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied..... Com'l −55°C to +125°C

DC Input Voltage .....−0.5V to +7.0V

DC Output Voltage .....−0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....−60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[7]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[8]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND.			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[9]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[9]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V[10]			±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance. ↓ = HIGH-to-LOW Transition.
2. A-to-B data flow is shown, B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was LOW before LEAB went LOW.
5. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
6. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
7. Typical values are at V_{CC}= 5.0V, T_A= +25°C ambient.
8. This parameter is specified but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
10. Tested at +25°C.

Output Drive Characteristics for CY74FCT16500T

Parameter	Description	Test Conditions	Min.	Typ.[7]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=–15 mA	2.4	3.5		
		V_{CC}=Min., I_{OH}=–32 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162500T

Parameter	Description	Test Conditions	Min.	Typ.[7]	Max.	Unit
I_{ODL}	Output LOW Current[9]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[9]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[8] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[7]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[7]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	V_{IN}≤0.2V, V_{IN}≥V_{CC}–0.2V	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[11]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[12]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OEAB=$\overline{OEBA}$=V_{CC} or GND	V_{IN}=V_{CC} or V_{IN}=GND	75	120	µA/MHz
I_C	Total Power Supply Current[13]	V_{CC}=Max., f_0=10 MHz ($\overline{CLKAB}$), f_1=5 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, OEAB=$\overline{OEBA}$=V_{CC} LEAB=GND	V_{IN}=V_{CC} or V_{IN}=GND	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	1.3	3.2	mA
		V_{CC}=Max., f_0=10 MHz, f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Eighteen Bits Toggling, OEAB=$\overline{OEBA}$=V_{CC} LEAB=GND	V_{IN}=V_{CC} or V_{IN}=GND	3.8	6.5[14]	mA
			V_{IN}=3.4V or V_{IN}=GND	8.5	20.8[14]	mA

Notes:

11. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
14. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[15]

Parameter	Description		CY74FCT162500AT		CY74FCT16500CT/ CY74FCT162500CT		Unit	Fig. No.[16]
			Min.	Max.	Min.	Max.		
f_{MAX}	$\overline{CLKAB}$ or $\overline{CLKBA}$ frequency			150		150	MHz	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A		1.5	5.1	1.5	4.6	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LEBA to A, LEAB to B		1.5	5.6	1.5	5.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLKBA}$ to A, $\overline{CLKAB}$ to B		1.5	5.6	1.5	5.3	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to A, OEAB to B		1.5	6.0	1.5	5.4	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to A, OEAB to B		1.5	5.6	1.5	5.2	ns	1, 7, 8
t_{SU}	Set-Up Time, HIGH or LOW A to $\overline{CLKAB}$, B to $\overline{CLKBA}$		3.0		3.0		ns	9
t_H	Hold Time, HIGH or LOW A to $\overline{CLKAB}$, B to $\overline{CLKBA}$		0		0		ns	9
t_{SU}	Set-Up Time, HIGH or LOW A to LEAB, B to LEBA	Clock HIGH	3.0		3.0		ns	4
		Clock LOW	1.5		1.5		ns	4
t_H	Hold Time, HIGH or LOW A to LEAB, B to LEBA		1.5		1.5		ns	4
t_W	LEAB or LEBA Pulse Width HIGH		3.0		2.5		ns	5
t_W	$\overline{CLKAB}$ or $\overline{CLKBA}$ Pulse Width HIGH or LOW		3.0		3.0		ns	5
$t_{SK(O)}$	Output Skew[17]			0.5		0.5	ns	

Ordering Information CY74FCT16500T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT16500CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16500CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	

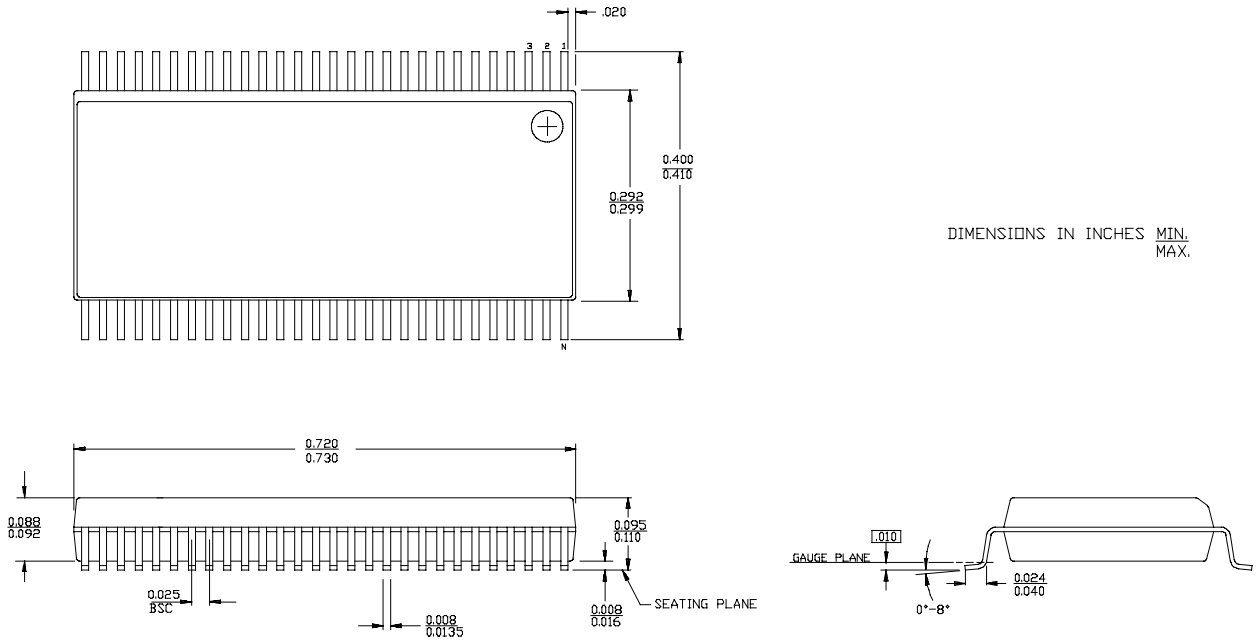
Ordering Information CY74FCT162500T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT162500CTPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162500CTPVCT	O56	56-Lead (300-Mil) SSOP	
5.1	CT74FCT162500ATPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162500ATPVCT	O56	56-Lead (300-Mil) SSOP	

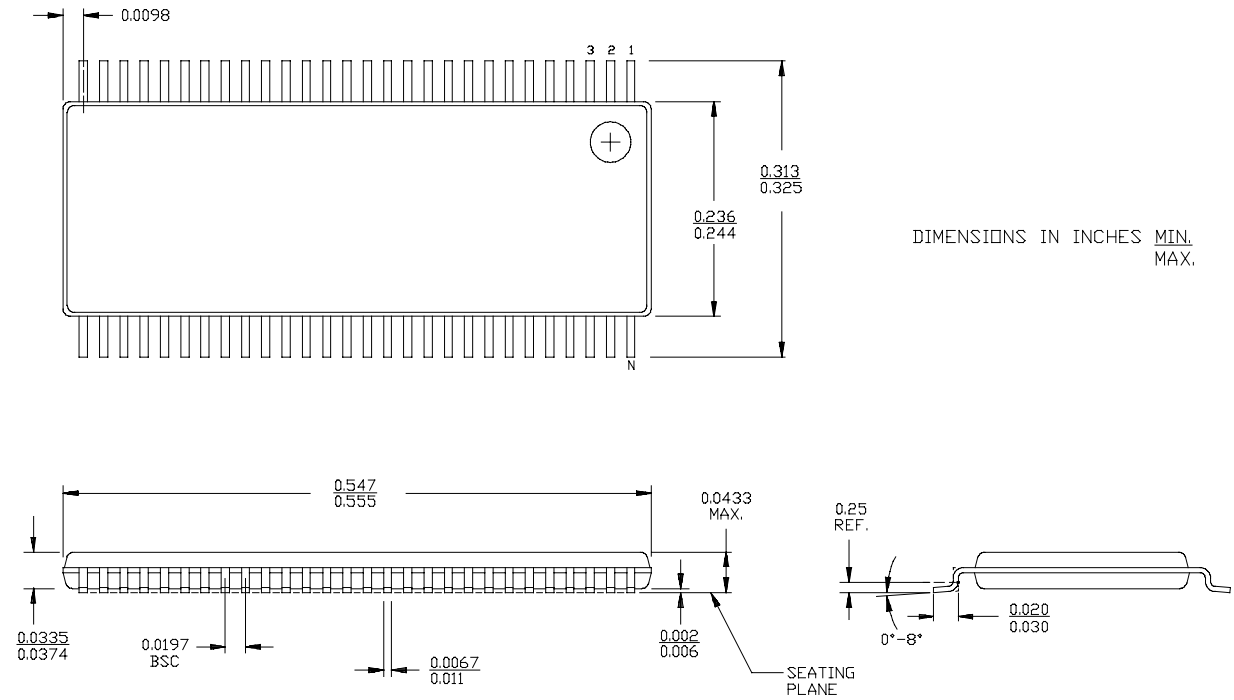
Notes:
15. Minimum limits are specified but not tested on Propagation Delays.
16. See “Parameter Measurement Information” in the General Information section.
17. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56



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