FAIRCHILD SEMICONDUCTOR®

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FDH44N50

44A, 500V, 0.12 Ohm, N-Channel SMPS Power MOSFET

Applications

Switch Mode Power Supplies(SMPS), such as

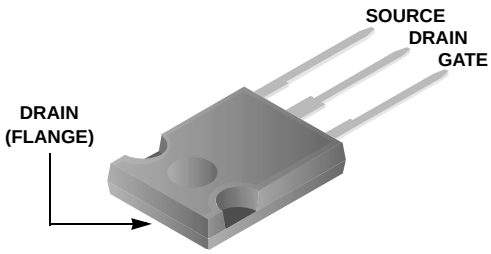
- PFC Boost
- Two-Switch Forward Converter
- Single Switch Forward Converter
- Flyback Converter
- Buck Converter
- High Speed Switching

Features

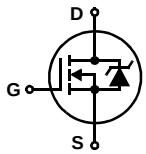
- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and High Reapplied dv/dt Ruggedness
- Reduced $r_{DS(ON)}$
- Reduced Miller Capacitance and Low Input Capacitance
- Improved Switching Speed with Low EMI
- 175°C Rated Junction Temperature

Package

JEDEC TO-247



Symbol



Absolute Maximum Ratings $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	500	V
V_{GS}	Gate to Source Voltage	±30	V
I_D	Drain Current		
	Continuous ($T_C = 25^oC$, $V_{GS} = 10V$)	44	A
	Continuous ($T_C = 100^oC$, $V_{GS} = 10V$)	32	A
	Pulsed[1]	176	A
P_D	Power dissipation	750	W
	Derate above 25^oC	5	$W/^oC$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	^oC
	Soldering Temperature for 10 seconds	300 (1.6mm from case)	^oC
	Mounting Torque, 8-32 or M3 Screw	10ibf*in (1.1N*m)	

Thermal Characteristics

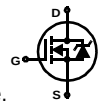
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.2	$^oC/W$
$R_{\theta CS}$	Thermal Resistance Case to Sink, Flat, Greased Surface	0.24	$^oC/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	40	$^oC/W$

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Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDH44N50	FDH44N50	TO-247	-	-	30

Electrical Characteristics T_J = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Statics							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V		500	-	-	V
$\Delta B_{VDSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	Reference to 25°C, ID = 1mA		-	0.61	-	V/°C
$r_{DS(ON)}$	Drain to Source On-Resistance	V_{GS} = 10V, I_D = 22A		-	0.11	0.12	Ω
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA		2	3.15	4	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V	T_C = 25°C	-	-	25	μA
		V_{GS} = 0V	T_C = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA
Dynamics							
g_{fs}	Forward Transconductance	V_{DS} = 50V, I_D = 22A		11	-	-	S
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 10V, V_{DS} = 400V, I_D = 44A		-	90	108	nC
Q_{gs}	Gate to Source Gate Charge			-	24	29	nC
Q_{gd}	Gate to Drain “Miller” Charge			-	31	37	nC
$t_{d(ON)}$	Turn-On Delay Time	V_{DD} = 250V, I_D = 44A, R_G = 2.15Ω, R_D = 5.68Ω		-	16	-	ns
t_r	Rise Time			-	84	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time			-	45	-	ns
t_f	Fall Time			-	79	-	ns
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	5335	-	pF
C_{OSS}	Output Capacitance			-	645	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	40	-	pF
Avalanche Characteristics							
E_{AS}	Single Pulse Avalanche Energy[2]			1500	-	-	mJ
I_{AR}	Avalanche Current			-	-	44	A
Drain-Source Diode Characteristics							
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode. 		-	-	44	A
I_{SM}	Pulsed Source Current[1] (Body Diode)			-	-	176	A
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 44A		-	0.900	1.2	V
t_{rr}	Reverse Recovery Time	I_{SD} = 44A, dI_{SD}/dt = 100A/μs		-	920	1100	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 44A, dI_{SD}/dt = 100A/μs		-	14	18	μC

Notes:
1: Repetitive rating; pulse width limited by maximum junction temperature
2: Starting T_J = 25°C, L = 1.61mH, I_{AS} = 44

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Typical Characteristic

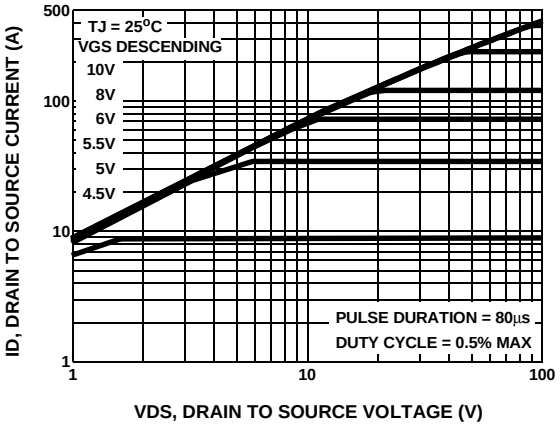


Figure 1. Output Characteristics

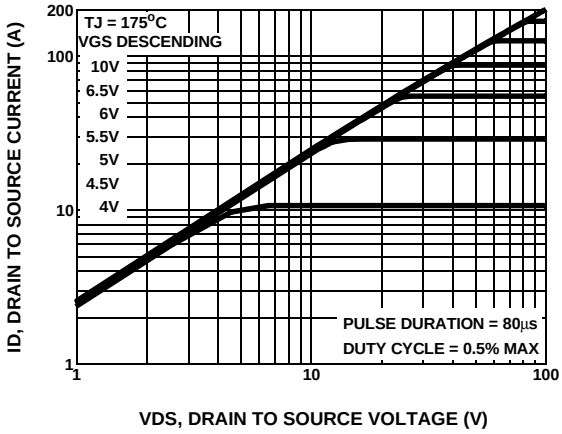


Figure 2. Output Characteristics

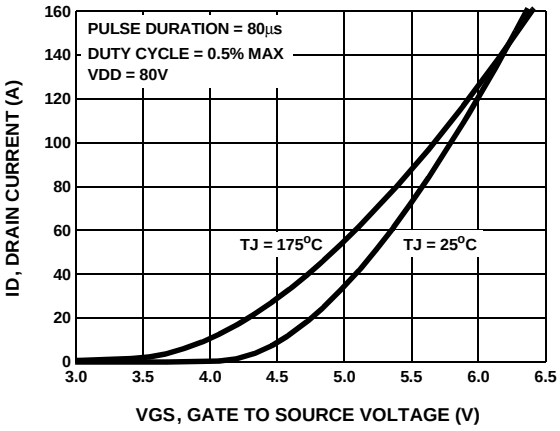


Figure 3. Transfer Characteristics

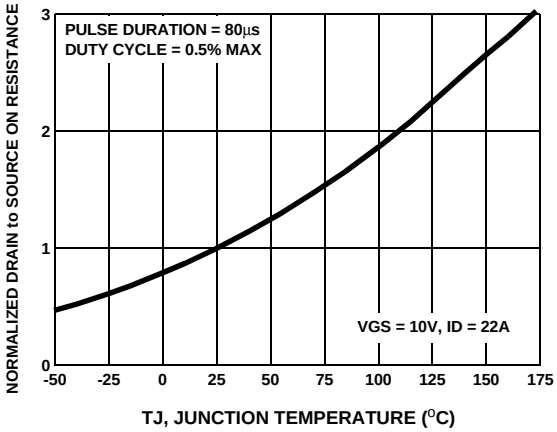


Figure 4. Normalized Drain To Source On Resistance vs Junction Temperatrue

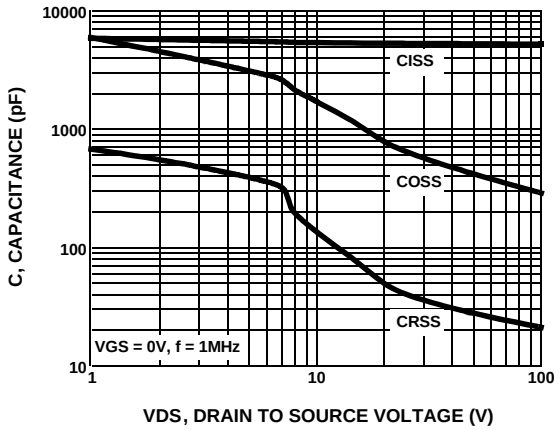


Figure 5. Capacitance vs Drain To Source Voltage

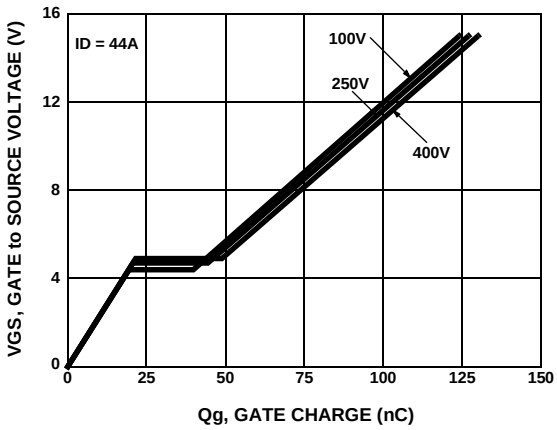


Figure 6. Gate Charge Waveforms For Constant Gate Current

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Typical Characteristic (Continued)

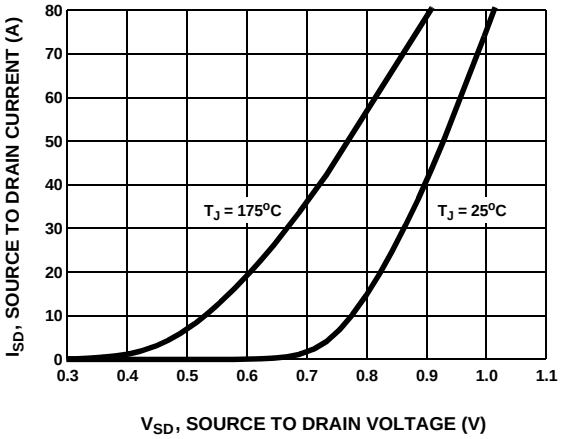


Figure 7. Body Diode Forward Voltage vs Body Diode Current

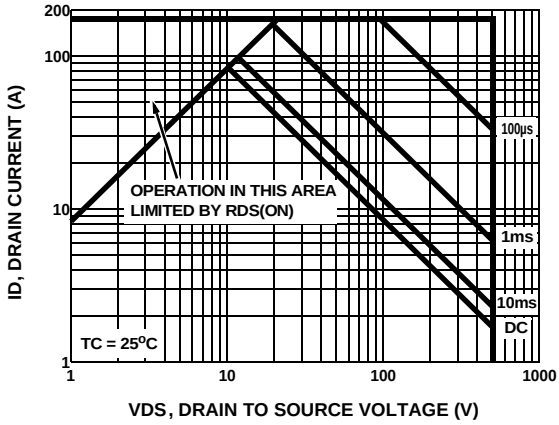


Figure 8. Maximum Safe Operating Area

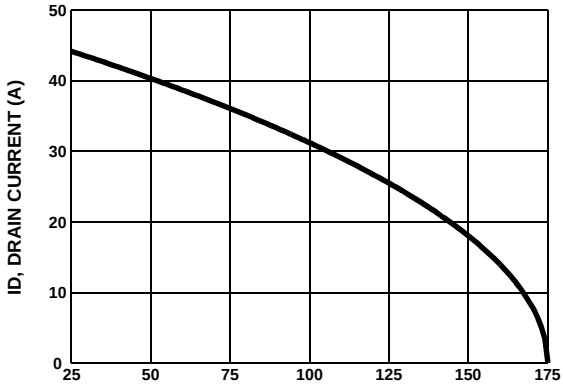


Figure 9. Maximum Drain Current vs Case Temperature

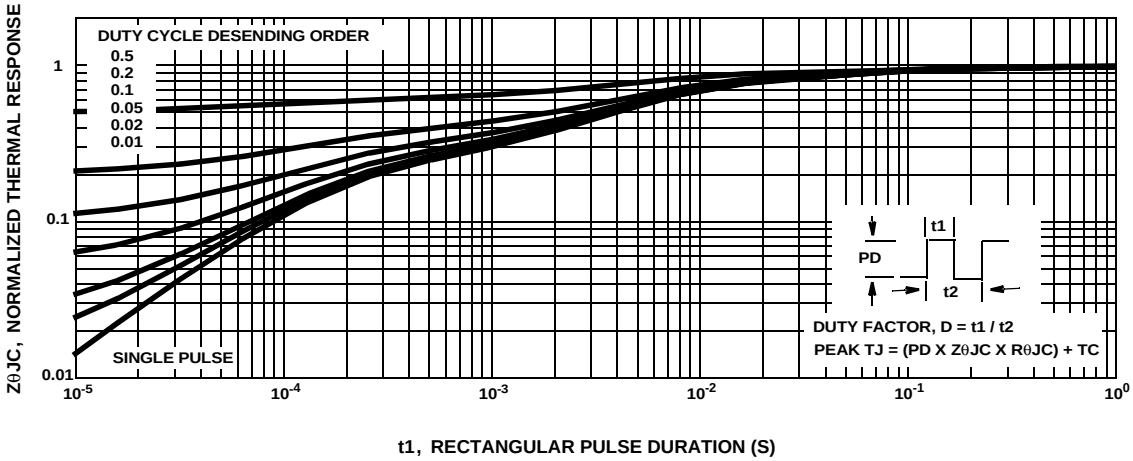


Figure 10. Normalized Transient Thermal Impedance, Junction to Case

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Test Circuits and Waveforms

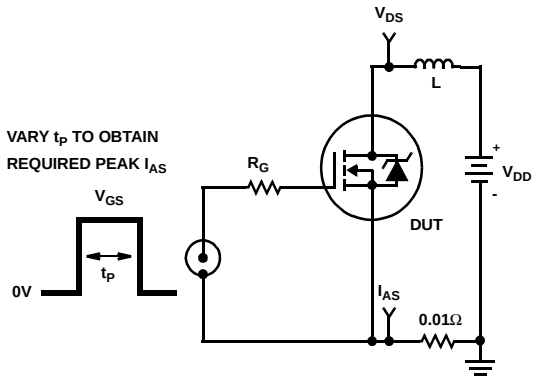


Figure 11. Unclamped Energy Test Circuit

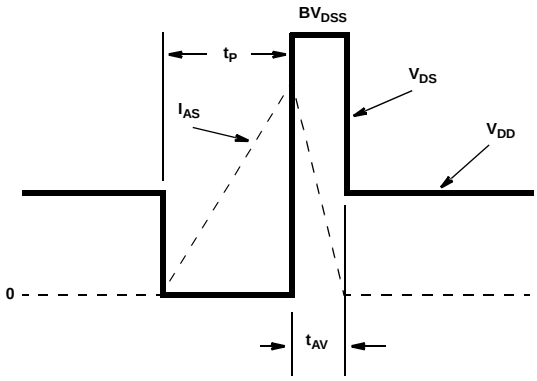


Figure 12. Unclamped Energy Waveforms

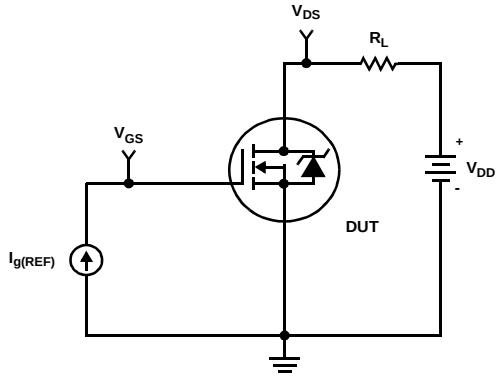


Figure 13. Gate Charge Test Circuit

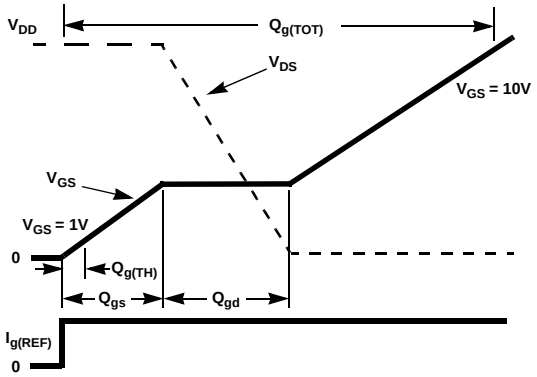


Figure 14. Gate Charge Waveforms

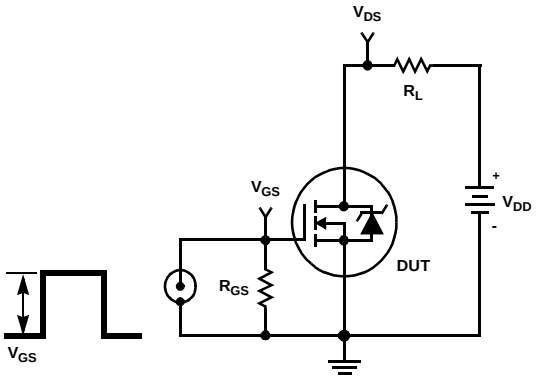


Figure 15. Switching Time Test Circuit

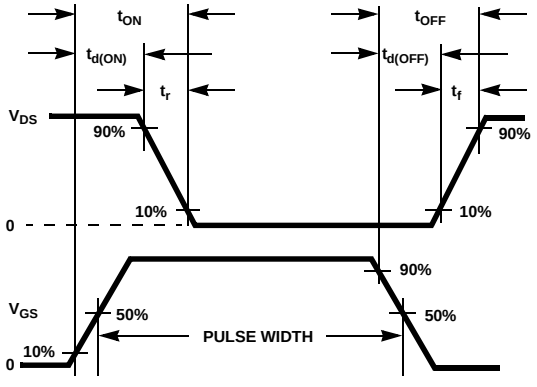


Figure 16. Switching Time Waveform

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CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
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