Si2456/Si2433/Si2414

V.90, V.34, V.32bis ISOmodem™ with Integrated Global DAA

Features

- Data modem formats
  - ITU-T, Bell
  - 300 bps up to 56 kbps
  - V.42, V.42bis, MNP2-5
  - Automatic rate negotiation
- Caller ID decode
- 3.3 V power
- No external ROM or RAM required
- UART with flow control
- AT command set support
- Integrated DAA
  - Capacitive isolation
  - Parallel phone detect
  - Globally-compliant line interface
  - Overcurrent detection
- Fast connect
- Parallel interface
- Call progress support
- Firmware upgradeable

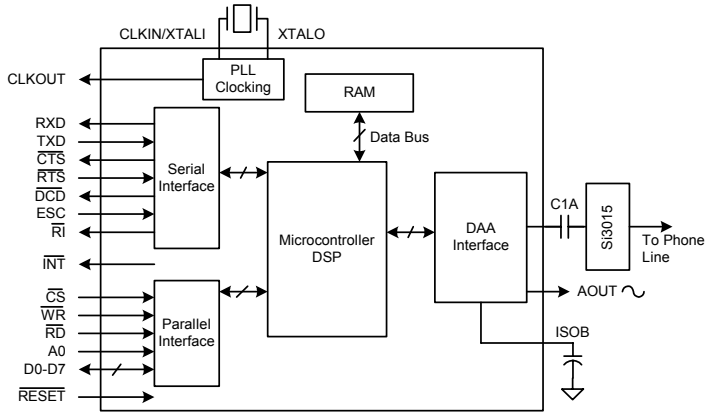
Applications

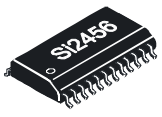
- Set-top boxes
- Email terminals
- Point-of-sale terminals
- PVRs
- Security systems
- Remote monitoring

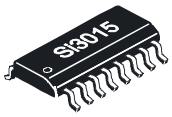
Description

The Si2456 is a complete, ITU-V.90-compliant, 56 kbps modem chipset with integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements with a single design. Available in two small packages, it eliminates the need for a separate DSP data pump, external RAM and ROM, modem controller, analog front end (AFE), isolation transformer, relays, opto-isolators, and 2- to 4-wire hybrid. The ISOmodem™ is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance. The Si2433 and Si2414 products offer all the same features as the Si2456 with connect rates of up to 33.6 kbps and 14.4 kbps, respectively.

Functional Block Diagram





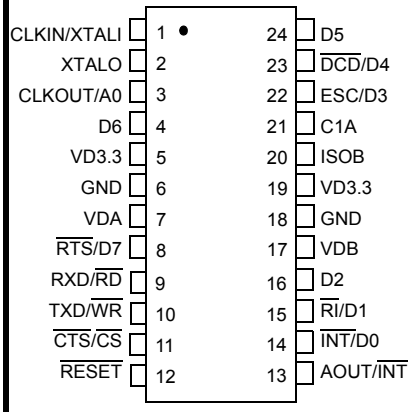


Ordering Information

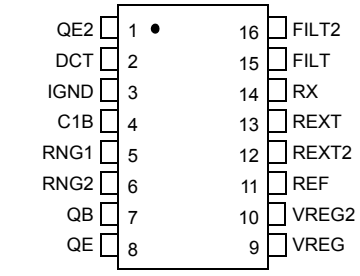
This data sheet is valid only for those chipset combinations listed on page 81.

Pin Assignments

Si2456/33/14



Si3015



Patents pending

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Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	K-Grade	0	25	70	°C
Si2456/33/14 Supply Voltage, Digital[3]	V_D		3.0	3.3	3.6	V

Notes:

1. The Si2456/33/14 specifications are guaranteed when the typical application circuit (including component tolerance) and any Si2456/33/14 and any Si3015 are used. See page 11 for typical application circuit.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. The digital supply, V_D, operates from 3.0 to 3.6 V. The Si2456/33/14 interface supports 5 V logic (CLKIN/XTALI supports 3.3 V logic only).

Table 2. DAA Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT[1] = 1 DCT = 11 (CTR21)	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 42 mA, ACT = 1 DCT = 11 (CTR21)	—	—	14.5	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, ACT = 1 DCT = 11 (CTR21)	—	—	40	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ACT = 1 DCT = 11 (CTR21)	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 0 DCT = 01 (Japan)	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 100 mA, ACT = 0 DCT = 01 (Japan)	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 0 DCT = 10 (FCC)	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 100 mA, ACT = 0 DCT = 10 (FCC)	9	—	—	V
On-Hook Leakage Current	I_{LK}	V_{TR} = –48 V	—	—	7	µA
Operating Loop Current	I_{LP}	FCC/Japan Modes	13	—	120	mA
Operating Loop Current	I_{LP}	CTR21	13	—	60	mA
DC Ring Current[2]		DC flowing through ring detection circuitry	—	—	7	µA
Ring Detect Voltage[3]	V_{RD}	RT = 0	11	—	22	V_{rms}
Ring Detect Voltage[3]	V_{RD}	RT = 1	17	—	33	V_{rms}
Ring Frequency	F_R		15	—	68	Hz
Ringer Equivalence Number[4]	REN		—	—	0.2	

Notes:

1. ACT = U67, bit 5; DCT = U67, bits 3:2; RT = U67, bit 0; RZ = U67, bit 1.
2. R25 and R26 installed.
3. The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.
4. C15, R14, Z2, and Z3 not installed. RZ = 0.

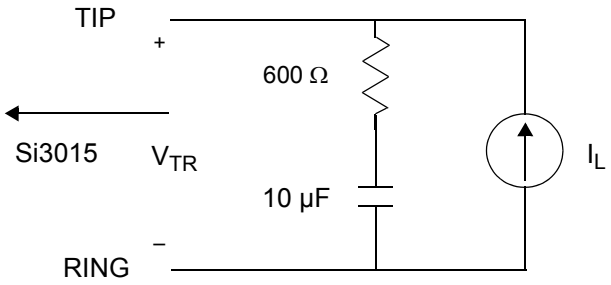


Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, V_D = 3.3 V

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.35	V
Input Leakage Current	I_L		–10	—	10	µA
Pullup Resistance Pins 9, 11, 13, 16	R_{PU}		100	300	420	kΩ
Total Supply Current*	I_D	V_{D33} pin	—	26	35	mA
Total Supply Current, Powerdown*	I_D	PDN = 1	—	35	100	µA

***Note:** All inputs at 0 or V_D. All inputs held static except clock and all outputs unloaded (Static I_{OUT} = 0 mA).

Table 4. DAA AC Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate	Fs		—	9.6	—	kHz
Crystal Oscillator Frequency	F_{XTL}		—	4.9152	—	MHz
Transmit Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Receive Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Transmit Full Scale Level[1]	V_{FS}		—	1	—	V_{PEAK}
Receive Full Scale Level[1]	V_{FS}		—	1	—	V_{PEAK}
Dynamic Range[2,3,4]	DR	ACT[5] = 0, DCT[5] = 10 (FCC) I_L=100 mA	—	82	—	dB
Dynamic Range[2,3,6]	DR	ACT = 0, DCT = 01 (Japan) I_L = 20 mA	—	83	—	dB
Dynamic Range[2,3,4]	DR	ACT = 1, DCT = 11(CTR21) I_L = 60 mA	—	84	—	dB
Transmit Total Harmonic Distortion[4,7]	THD	ACT = 0, DCT = 10 (FCC) I_L = 100 mA	—	–85	—	dB
Transmit Total Harmonic Distortion[5,7]	THD	ACT = 0, DCT = 01 (Japan) I_L = 20 mA	—	–76	—	dB
Receive Total Harmonic Distortion[6,7]	THD	ACT = 0, DCT = 01 (Japan) I_L = 20 mA	—	–74	—	dB
Receive Total Harmonic Distortion[4,7]	THD	ACT = 1, DCT = 11 (CTR21) I_L = 60 mA	—	–82	—	dB
AOUT Dynamic Range		VIN = 1 kHz	—	40	—	dB
AOUT THD		VIN = 1 kHz	—	40	—	dB
AOUT Full Scale Level			—	$0.7V_{DD}$	—	V_{PP}
AOUT Mute Level			—	60	—	dB

Notes:

1. Measured at TIP and RING with 600 Ω termination at 1 kHz.
2. DR = 20 x log |Vin| + 20 x log (RMS signal/RMS noise).
3. Measurement is 300 to 3400 Hz. Applies to transmit and receive paths.
4. Vin = 1 kHz, –3 dBFS, Fs = 10300 Hz.
5. ACT = U67, bit 5; DCT = U67, bits 3:2.
6. Vin = 1 kHz, –6 dBFS, Fs = 10300 Hz.
7. THD = 20 x log (RMS distortion/RMS signal).

Table 5. Absolute Maximum Ratings

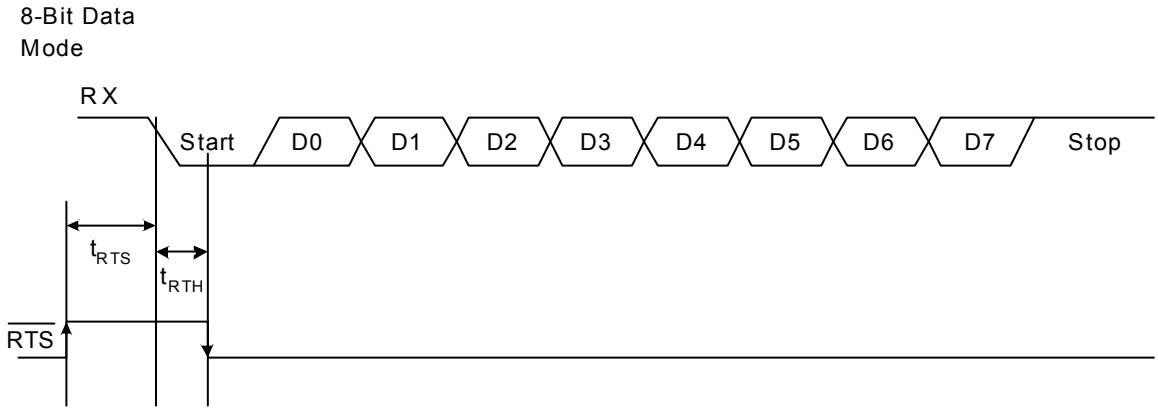
Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	4.1	V
Input Current, Si2456/33/14 Digital Input Pins	I_{IN}	±10	μA
Digital Input Voltage	V_{IND}	–0.3 to 5.3	V
CLKIN/XTALI Input Voltage	V_{XIND}	–0.3 to (V_D + 0.3)	V
Operating Temperature Range	T_A	–10 to 100	°C
Storage Temperature Range	T_{STG}	–40 to 150	°C
Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.			

Table 6. Switching Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
CLKOUT Output Clock Frequency		2.4576	—	39.3216	MHz
Baud Rate Accuracy	t_{BD}	–1	—	1	%
Start Bit ↓ to $\overline{RTS}$ ↓	t_{RTH}	—	1/(2 x Baud Rate)	—	ns
$\overline{CTS}$ or $\overline{RTS}$ ↑ High to Start Bit↓	t_{RTS}	10	—	—	ns
Stop Bit ↑ to $\overline{CTS}$ ↑	t_{CTH}	—	—	—	ns
$\overline{RESET}$ ↓ to $\overline{RESET}$ ↑	t_{RS}	5.0	—	—	ms
$\overline{RESET}$ ↑ to 1st AT Command	t_{AT}	300	—	—	ms
Address Setup	t_{AS}	15	—	—	ns
Address Hold	t_{AH}	0	—	—	ns
$\overline{WR}$ Low Pulse Width	t_{WL}	50	—	—	ns
Write Data Setup Time	t_{WDSU}	20	—	—	ns
Write Cycle Time	t_{WC}	120	—	—	ns
Chip Select Setup	t_{CSS}	10	—	—	ns
Chip Select Hold	t_{CSH}	0	—	—	ns
$\overline{RD}$ Low Pulse Width	t_{RL}	50	—	—	ns
$\overline{RD}$ Low to Data Driven Time	t_{RLDD}	—	—	20	ns
Data Hold	t_{DH}	10	—	—	ns
$\overline{RD}$ High to Hi-Z Time	t_{DZ}	—	—	30	ns
Read Cycle Time	t_{RC}	120	—	—	ns
Note: All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_D – 0.4 V, V_{IL} = 0.4 V					

UART Time for Modem Receive Path (8N1 Mode)



UART Timing for Modem Transmit Path (9N1 Mode with 9th Bit Escape)

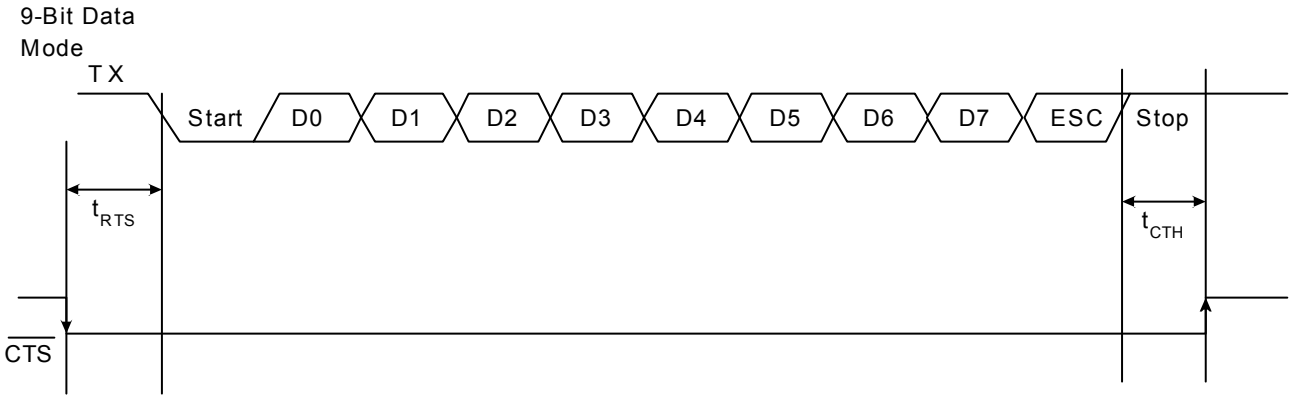


Figure 2. Asynchronous UART Serial Interface Timing Diagram

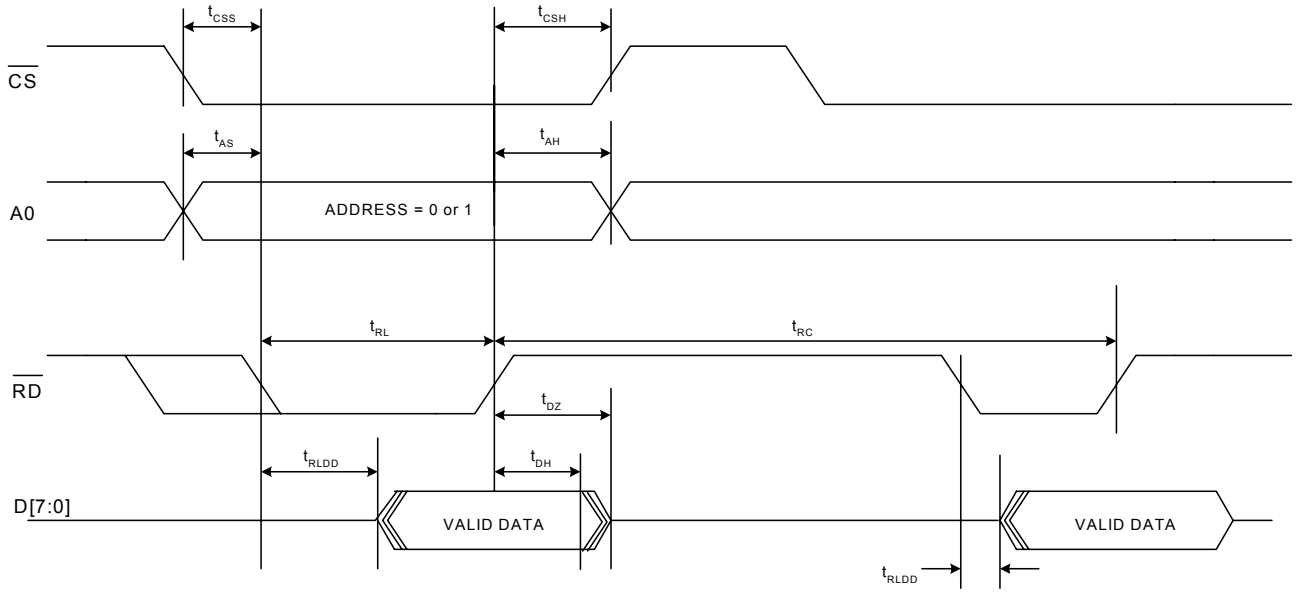


Figure 3. Parallel Interface Read Timing

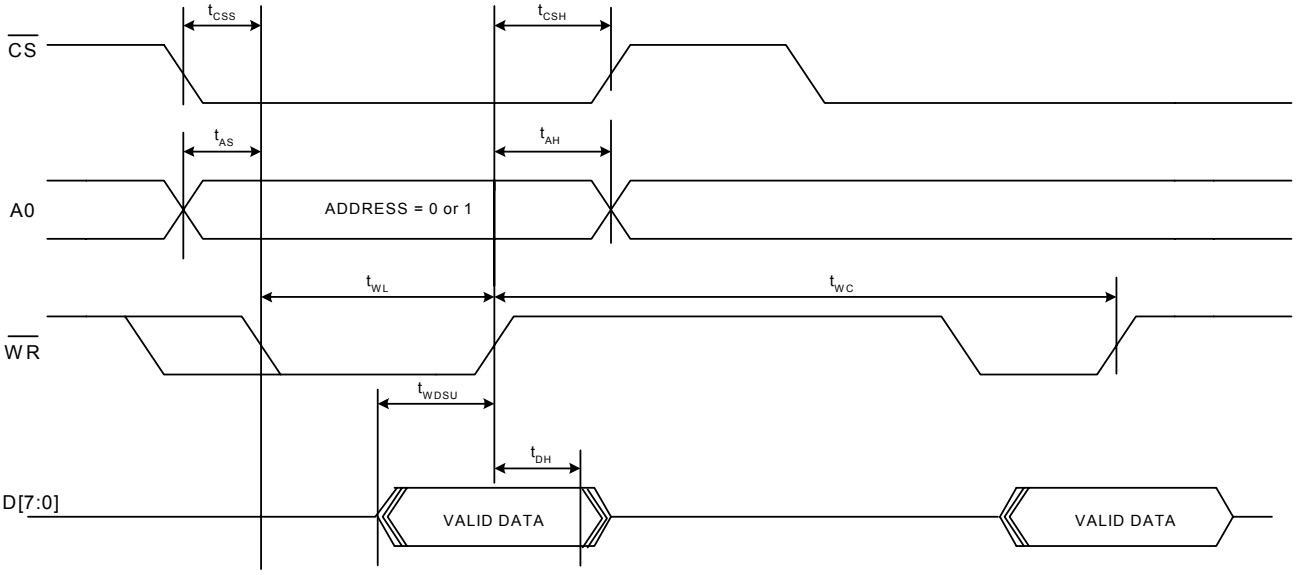
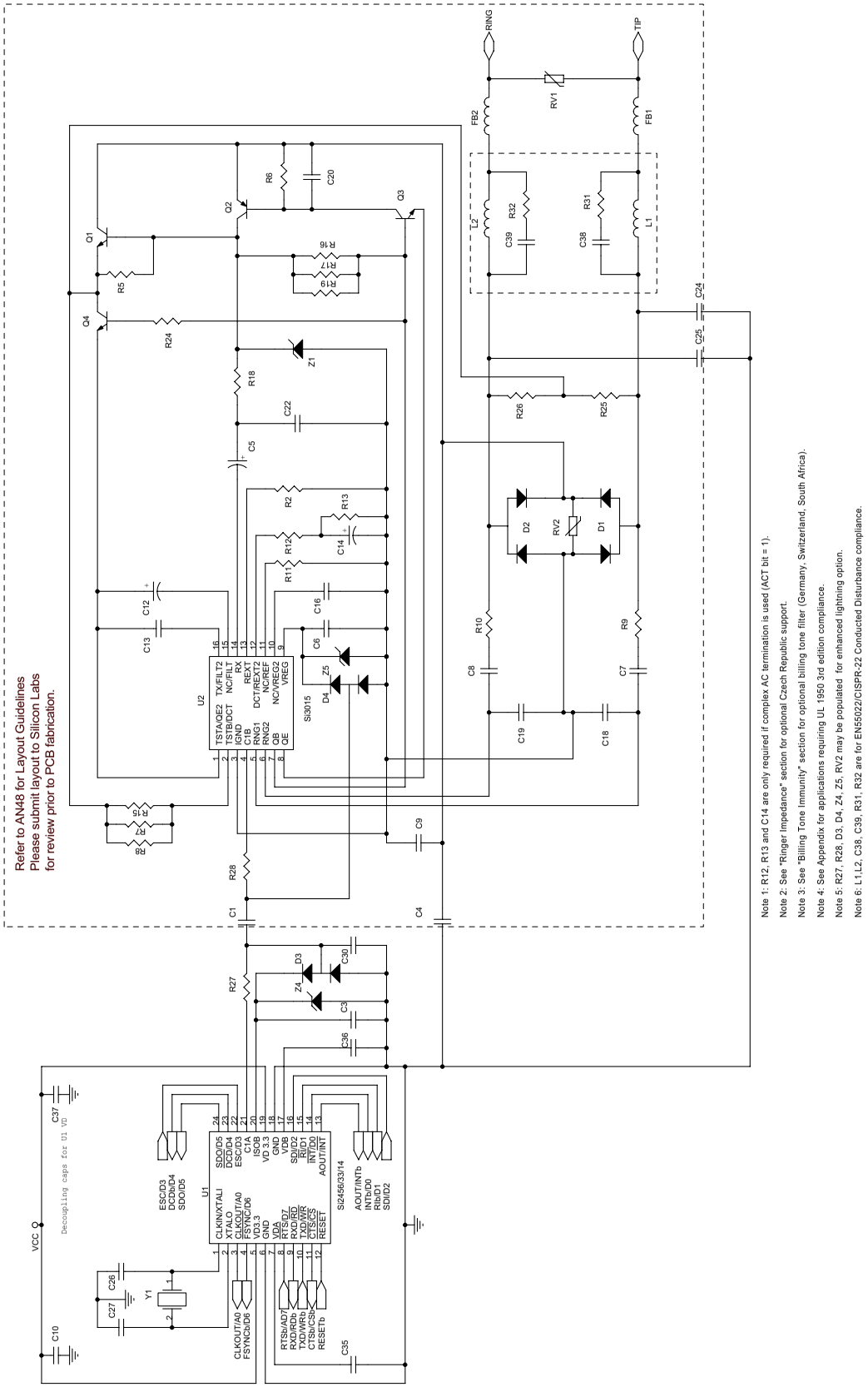


Figure 4. Parallel Interface Write Timing

Typical Application Circuit



Bill of Materials: Si2456/33/14 Chipset

Component	Value	Supplier(s)
C1,C4[1]	150 pF, 3 kV, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C3,C13,C35,C36	0.22 µF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C5[2]	0.1 µF, 50 V, Elec/Tant, ±20%	Venkel, Johanson, Murata, Panasonic
C6,C10,C16,C37	0.1 µF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata
C7,C8[3]	560 pF, 250 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C9	22 nF, 250 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C12	1.0 µF, 16 V, Tant, ±20%	Venkel, Panasonic
C14[2]	0.68 µF, 16 V, X7R/Elec/Tant, ±20%	Novacap, Venkel, AUX, Murata, Panasonic
C18,C19[3]	3.9 nF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata
C20	0.01 µF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata
C22[4]	1800 pF, 50 V, X7R, ±20%	Not installed
C24,C25[1]	1000 pF, 3 kV, X7R, ±10%	Novacap, Venkel, Johanson, Murata, Panasonic
C26,C27	33 pF, 16 V, NPO, ±5%	Novacap, Venkel, Johanson, Murata
C30[4]	10 pF, 16 V, NPO, ±10%	Not Installed
C38,C39[2,5]	47 pF, 16 V, X7R, ±10%	Venkel
D1,D2[6]	Dual Diode, 300 V, 225 mA	Central Semiconductor
D3,D4[1]	BAV99 Dual Diode, 70 V, 350 mW	Diodes Inc., OnSemiconductor, Fairchild
FB1,FB2	Ferrite Bead, 600 Ω, ±25%, 200 mA	Murata
L1,L2[2,5]	68 µH, 120 mA, 4 Ω max, ±10%	Murata, Panasonic
Q1,Q3	A42, NPN, 300 V	OnSemiconductor, Fairchild, Zetex
Q2	A92, PNP, 300 V	OnSemiconductor, Fairchild, Zetex

Notes:

1. The Si2456/33/14 design survives up to 3500 V longitudinal surges without R27, R28, D3, D4, Z4, and Z5. Adding the R27, R28, D3, D4, Z4, and Z5 enhanced lightning options increases longitudinal surge survival to greater than 6600 V. The isolation capacitors, C1, C4, C24, and C25, must also be rated to greater than the surge voltage. Y-class capacitors are recommended for highest surge survival.
2. For FCC-only designs, C14, C38, C39, R12, R13, R31, and R32 are not required (leave Si3015 pin 12 unconnected); L1 and L2 may be replaced with a short; R2 may be ±5%; with Z1 rated at 18 V, C5 may be rated at 16 V; also see Note 9.
3. If the auto answer, ring detect, and caller ID features are not used, R9, R10, C7, C8, C18, and C19 may be removed. In this case, connect the RNG1 and RNG2 pins of the Si3015 to the IGND pin.
4. C22 and C30 may provide an additional improvement in emissions/immunity, depending on design and layout. Population option recommended. See "Emissions/Immunity" on page 67.
5. Compliance with EN55022 and/or CISPR-22 conductance disturbance tests requires the following: L1, L2, C38, C39, R31, and R32; D1 and D2 must be 400 V rated; and RV2 must be populated. See also “EN55022 and CISPR-22 Compliance” in “Appendix A—DAA Operation”.
6. Several diode bridge configurations are acceptable (suppliers include General Semi., Diodes Inc.)
7. Q4 may require copper on board to meet 1/2 W power requirement. (Contact manufacturer for details.)
8. RV2 can be installed to improve performance for multiple longitudinal surges.
9. The R7, R8, R15, and R16, R17, R19 resistors may each be replaced with a single resistor of 1.78 kΩ, 3/4 W, ±1%. For FCC-only designs, 1.78 kΩ, 1/16 W, ±5% resistors may be used.
10. If the parallel phone detection feature is not used, R25 and R26 may be removed.
11. To ensure compliance with ITU specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70 °C, and capacitive loading.

Component	Value	Supplier(s)
Q4[7]	BCP56, NPN, 60 V, 1/2 W	OnSemiconductor, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, ST Microelectronics, Microsemi, TI
RV2[8]	270 V, MOV	Not Installed
R2[2]	402 Ω, 1/16 W, ±1%	Venkel, Panasonic
R5	100 kΩ, 1/16 W, ±1%	Venkel, Panasonic
R6	120 kΩ, 1/16 W, ±5%	Venkel, Panasonic
R7,R8,R15,R16,R17,R19[9]	5.36 kΩ, 1/4 W, ±1%	Venkel, Panasonic
R9,R10[3]	56 kΩ, 1/10 W, ±5%	Venkel, Panasonic
R11	9.31 kΩ, 1/16 W, ±1%	Venkel, Panasonic
R12[2]	78.7 Ω, 1/16 W, ±1%	Venkel, Panasonic
R13[2]	215 Ω, 1/16 W, ±1%	Venkel, Panasonic
R18	2.2 kΩ, 1/10 W, ±5%	Venkel, Panasonic
R24	150 Ω, 1/16 W, ±5%	Venkel, Panasonic
R25,R26[10]	10 MΩ, 1/16 W, ±5%	Venkel, Panasonic
R27,R28[1]	10 Ω, 1/10 W, ±5%	Venkel, Panasonic
R31,R32[2,5]	470 Ω, 1/16 W, ±5%	Venkel, Panasonic
U1	Si2456/33/14	Silicon Labs
U2	Si3015	Silicon Labs
Y1[11]	4.9152 MHz, 20 pF, 50 ppm, 150 ESR	Not Installed
Z1[2]	Zener Diode, 43 V, 1/2 W	Vishay, OnSemiconductor, Rohm
Z4,Z5[1]	Zener Diode, 5.6 V, 1/2 W	Vishay, OnSemiconductor, Rohm

Notes:

1. The Si2456/33/14 design survives up to 3500 V longitudinal surges without R27, R28, D3, D4, Z4, and Z5. Adding the R27, R28, D3, D4, Z4, and Z5 enhanced lightning options increases longitudinal surge survival to greater than 6600 V. The isolation capacitors, C1, C4, C24, and C25, must also be rated to greater than the surge voltage. Y-class capacitors are recommended for highest surge survival.
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10. If the parallel phone detection feature is not used, R25 and R26 may be removed.
11. To ensure compliance with ITU specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70 °C, and capacitive loading.

Analog Output

Figure 5 illustrates an optional application circuit to support the analog output capability of the Si2456/33/14 for call progress monitoring purposes.

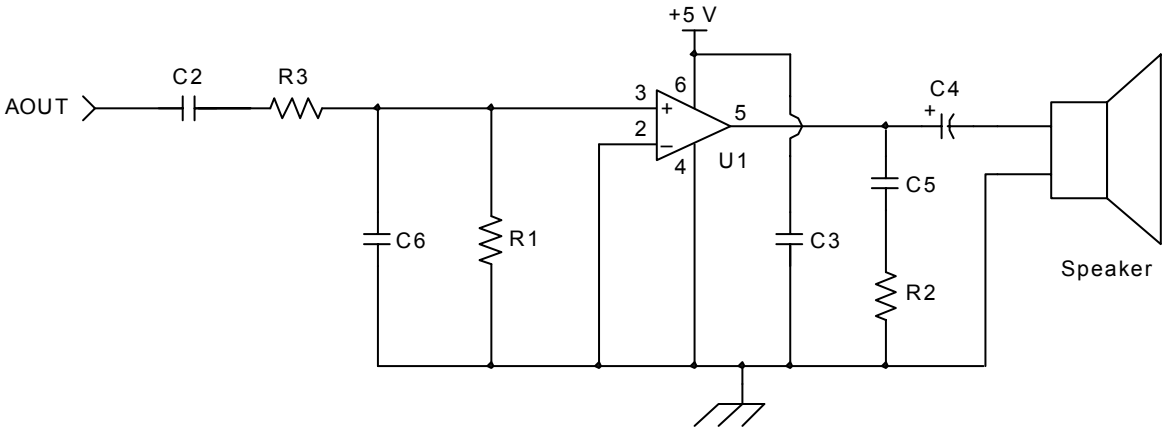


Figure 5. Optional Connection to AOUT for a Monitoring Speaker

Table 7. Component Values—Optional Connection to AOUT

Symbol	Value
C2, C3, C5	0.1 µF, 16 V, ±20%
C4	100 µF, 16 V, Elec. ±20%
C6	820 pF, 16 V, ±20%
R1	10 kΩ, 1/10 W, ±5%
R2	10 Ω, 1/10 W, ±5%
R3	47 kΩ, 1/10 W, ±5%
U1	LM386

Table 8. Protocol Characteristics

Item	Specification
Data Rate	
56 kbps[1]	ITU-T V.90[1]
54.666 kbps[1]	ITU-T V.90[1]
53.333 kbps[1]	ITU-T V.90[1]
52 kbps[1]	ITU-T V.90[1]
50.666 kbps[1]	ITU-T V.90[1]
49.333 kbps[1]	ITU-T V.90[1]
48 kbps[1]	ITU-T V.90[1]
46.666 kbps[1]	ITU-T V.90[1]
45.333 kbps[1]	ITU-T V.90[1]
44 kbps[1]	ITU-T V.90[1]
42.666 kbps[1]	ITU-T V.90[1]
41.333 kbps[1]	ITU-T V.90[1]
40 kbps[1]	ITU-T V.90[1]
38.666 kbps[1]	ITU-T V.90[1]
37.333 kbps[1]	ITU-T V.90[1]
36 kbps[1]	ITU-T V.90[1]
34.666 kbps[1]	ITU-T V.90[1]
33.333 kbps[1]	ITU-T V.90[1]
32 kbps[1]	ITU-T V.90[1]
30.666 kbps[1]	ITU-T V.90[1]
29.333 kbps[1]	ITU-T V.90[1]
28 kbps[1]	ITU-T V.90[1]
33.6 kbps[2]	ITU-T V.34[2]
31.2 kbps[2]	ITU-T V.34[2]
28.8 kbps[2]	ITU-T V.34[2]
26.4 kbps[2]	ITU-T V.34[2]
24.0 kbps[2]	ITU-T V.34[2]
21.6 kbps[2]	ITU-T V.34[2]
19.2 kbps[2]	ITU-T V.34[2]
16.8 kbps[2]	ITU-T V.34[2]
14.4 kbps	ITU-T V.34 or V.32bis
12.0 kbps	ITU-T V.34 or V.32bis
9600 bps	ITU-T V.34 or V.32bis
7200 bps	ITU-T V.34 or V.32bis
4800 bps	ITU-T V.34 or V.32bis
2400 bps	ITU-T V.34, V.32 bis, or V.22bis
1200 bps	ITU-T V.22bis, V.23, or Bell 212A
300 bps	ITU-T V.21
300 bps	Bell 103

Notes:
1. Supported on Si2456 only.
2. Supported on Si2456 and Si2433 only.

Table 8. Protocol Characteristics (Continued)

Item	Specification
Data Format Bit asynchronous	Selectable 8, 9, 10, or 11 bits per character
Compatibility	ITU-T V.90[1], V.34[1], V.32bis, V.32, V.23, V.22bis, V.22, V.21, Bell 212A, and Bell 103
Operating Mode Switched network	Two-wire full duplex
Data Modulation 28 to 56 kbps[1] 2.4 to 33.6 kbps[2] 14.4 kbps 12.0 kbps 9600 kbps 9600 kbps 7200 kbps 4800 kbps 2400 kbps 1200 kbps 0 to 300 kbps	 V.90 as specified by ITU-T V.34 as specified by ITU-T 128-level TCM/2400 Baud ±0.01% 64-level TCM/2400 Baud ±0.01% 32-level TCM/2400 Baud ±0.01% 16-level QAM/2400 Baud ±0.01% 16-level TCM/2400 Baud ±0.01% 4-level QAM/2400 Baud ±0.01% 16-level QAM/600 Baud ±0.01% 4-level PSK/600 Baud ±0.01% FSK 0–300 Baud ±0.01%
Answer Tone ITU-T V.32bis, V.32, V.22bis, V.22, and V.21 modes Bell 212A and 103 modes	 2100 Hz ±3 Hz 2225 Hz ±3 Hz
Transmit Carrier V.90[1] V.34[2] ITU-T V.32bis ITU-T V.32 ITU-T V.22, V.22bis/Bell 212A Originate mode Answer mode ITU-T V.21 Originate mode Answer mode Bell 103 Originate mode Answer mode	 As specified by ITU-T As specified by ITU-T 1800 Hz ±0.01% 1800 Hz ±0.01% 1200 Hz ±0.5 Hz 2400 Hz ±1 Hz Mark (980 Hz ±12 Hz) Space (1180 Hz ±12 Hz) Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz) Mark (1270 Hz ±12 Hz) Space (1070 Hz ±12 Hz) Mark (2225 Hz ±12 Hz) Space (2025 Hz ±12 Hz)
Output Level Permissive—Switched network	–9 dBm maximum

Notes:
1. Supported on Si2456 only.
2. Supported on Si2456 and Si2433 only.

Table 8. Protocol Characteristics (Continued)

Item	Specification
Receive Carrier	
ITU-T V.90[1]	As specified by ITU-T
ITU-T V.34[2]	As specified by ITU-T
ITU-T V.32bis	1800 Hz ±7 Hz
ITU-T V.32	1800 Hz ±7 Hz
ITU-T V.22, V.22bis/Bell 212A	
Originate mode	2400 Hz ±7 Hz
Answer mode	1200 Hz ±7 Hz
ITU-T V.21	
Originate mode	Mark (980 Hz ±12 Hz) Space (1180 Hz ±12 Hz)
Answer mode	Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz)
Bell 103	
Originate mode	Mark (2225 Hz ±12 Hz) Space (2025 Hz ±12 Hz)
Answer mode	Mark (1270 Hz ±12 Hz) Space (1070 Hz ±12 Hz)
Carrier Detect (level for ITU-T V.22bis, V.22, V.21, 212, 103) in Switched Network	Acquisition (–43 dBm) Release (–48 dBm)
Hysteresis	2 dBm minimum
Note: ITU-T V.90[1], V.34[2], V.32/V.32bis are echo canceling protocols that use signal quality as criteria for maintaining connection. They also provide for self-training detection to force disconnect.	
DTE Interface	EIA/TIA-232-E (ITU-T V.24/V.28/ISO 2110)
Line Equalization	Automatic Adaptive
Connection Options	Loss of Carrier in ITU-T V.22bis and lower
Phone Types	500 (rotary dial), 2500 (DTMF dial)
Dialing	Pulse and Tone
DTMF Output Level	Per Part 68
Pulse Dial Ratio	Make/Break: 39/61%
Ring Cadence	On 2 seconds; Off 4 seconds
Call Progress Monitor	BUSY CONNECT (rate) NO ANSWER NO CARRIER NO DIALTONE OK RING RINGING
Notes: **1.** Supported on Si2456 only. **2.** Supported on Si2456 and Si2433 only.	

Functional Description

The Si2456/33/14 ISOmodem™ is a complete embedded modem chipset with integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements. Available in two small packages, this solution includes a DSP data pump, a modem controller, on-chip RAM and ROM, an analog front end (AFE), a DAA, and an analog output.

The Si2456/33/14 accepts standard modem AT commands and provides connect rates up to 56/33.6/14.4 kbps full-duplex over the Public Switched Telephone Network (PSTN). The Si2456/33/14 features a complete set of modem protocols, including all ITU-T standard formats up to 56 kbps.

The ISOmodem provides numerous additional features for embedded modem applications. The modem includes full caller ID detection and decoding for global standards. Call progress is supported through echoing result codes and is also programmable to meet global settings. Because the Si2456/33/14 ISOmodem integrates the DAA, analog features, such as parallel phone detect, overcurrent detection, and global PTT compliance with a single design, are included.

This device is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance. The Si2456/33/14 solution includes a silicon DAA using Silicon Laboratories' proprietary ISOcap™ technology. This highly-integrated DAA can be programmed to meet worldwide PTT specifications for ac termination, dc termination, ringer impedance, and ringer threshold. In addition, the Si2456/33/14 has been designed to meet the most stringent worldwide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

The Si2456/33/14 is designed to be rapidly incorporated into existing modem applications. The device interfaces directly through either a serial UART to a microcontroller or through a standard RS-232 transceiver. This interface allows for PC evaluation of the modem immediately upon powerup via the AT commands using standard terminal software. The Si2456/33/14 also provides an 8-bit parallel port.

The Si2456/33/14 solution requires only a few low-cost discrete components to achieve global compliance. See the "Typical Application Circuit" on page 11. Table 8 on page 15 outlines the functional modes of the Si2456/33/14 modem. For additional information, see the Si2456/33/14 Programmer's Guide.

Digital Interface

The Si2456/33/14 digital I/O can be configured as either a serial UART interface with flow control or as a parallel 8-bit interface.

Selection of a serial or parallel I/O interface is determined by the state of AOUT/$\overline{\text{INT}}$ (Si2456/33/14, pin 13) during the rising edge of $\overline{\text{RESET}}$. An internal pullup resistor forces the default state to serial mode operation. An external 10 kΩ pulldown resistor can be connected to AOUT/$\overline{\text{INT}}$ to force selection of parallel mode. Additionally, when selecting parallel mode, $\overline{\text{CS}}$ should remain high until after the rising edge of $\overline{\text{RESET}}$. Configuration of pins 3, 4, 8–11, 13–16, and 22–24 is determined by this interface selection.

Serial Interface

This section describes the basic operation of the Si2456/33/14 serial UART interface. The Si2456/33/14 supports DTE rates up to 307.2 kbps with the standard serial UART format. Upon powerup, the UART defaults to a 19.2 kbps baud rate. If a pulldown resistor ≤ 10 kΩ is placed between D2 (Si2456/33/14, pin 16) and GND (Si2456/33/14, pin 6), the DTE rate is 2400 bps 8N1 after reset. This rate may be changed through the extended AT\Tn commands listed in Table 14 on page 30. Immediately after the AT\Tn command is sent, the host must program its UART to the new baud rate.

The UART interface synchronizes on the start bits of incoming characters and samples the data bit field and stop bits. The interface is designed to accommodate character lengths of 8, 9, 10, and 11 bits giving data fields of 6, 7, 8, or 9 bits. The Si2456/33/14 defaults to a character length of 8 (8N1), and the character length can be set via the \Bn command. Under some \Bn options, parity may be set using the \Pn command.

The serial interface provides a hardware pin, $\overline{\text{DCD}}$ (data carrier detect), which remains low as long as the ISOmodem is connected. This and other signals can also be monitored via the I/O Control 0 register (U70).

The $\overline{\text{INT}}$ interrupt pin can be programmed to alert the host of changes in $\overline{\text{DCD}}$ and the other interrupts listed in I/O Control 0 (U70). After an interrupt has been received by the host via the $\overline{\text{INT}}$ pin, the host should issue the AT:I command. This command causes a read-clear of the CID, OCD, PPD, and RI bits of the U70 register and raises (deactivates) the $\overline{\text{INT}}$ pin.

Parallel Interface

The parallel interface is an 8-bit data bus with a single bit address. Figure 3 on page 10 shows the required timing for the parallel interface.

If A0 = 0, the data bus represents a read/write to the "Parallel Interface 0 (0x00)" register on page 65. If A0 = 1, the data bus represents a read/write to the "Parallel Interface 1 (0x01)" register on page 66).

The parallel port may be read/written by the host in blocks by monitoring the receive/transmit FIFOs on the Si2456/33/14. The transmit and receive FIFOs are 14 and 12 characters deep, respectively. The FIFOs can be guaranteed to never fill/empty as long as TXE and RXF are polled (and the TX/RX register is written/read appropriately). The FIFOs can also be serviced on interrupts by using the $\overline{INT}$ pin and setting the INTM bit 3 in the "Parallel Interface 1 (0x01)" register. Additionally, the $\overline{CTS}$ and the $\overline{RTS}$ bits are used to control flow.

The $\overline{INT}$ pin in parallel mode operates differently than in serial mode. In parallel mode, the pin is used primarily to monitor and control the I/O FIFO. By default, the $\overline{INT}$ function is triggered by a low-to-high transition on RXF, TXE, or INT in the Parallel Interface 1 register. The INT bit in the "Parallel Interface 1 (0x01)" register is set by the events selected in U70. If the INTM bit is set, these events cause a high-to-low transition on the $\overline{INT}$ pin. Contact Silicon Labs Technical Support for detailed parallel interface applications information.

Command Mode

Upon reset, the ISOmodem is in Command mode and accepts "AT" commands. An outgoing modem call can be made using the "ATDT#" (tone dial) or "ATDP#" (pulse dial) command after the device is configured. If the handshake is successful, the modem responds with the response codes detailed in Table 16 on page 33. The Si2456/33/14 does not enter Data mode until after the protocol result code. In Data mode, "AT" commands are not accepted. The Si2456/33/14 reverts to Command mode if the modem connection is terminated. However, there are three "escape" methods that may be used to return the ISOmodem to Command mode from Data mode. See I/O Control 0 (U70).

- "+++"—The escape sequence is a sequence of three escape characters that are set in S-register S2 ("+" characters by default). If the ISOmodem detects the "+++" sequence and detects no activity on the UART before or after the "+++" sequence for a time period set by S-register S12, it returns to Command mode. This is enabled by setting U70[13] (TES) = 1_b (default).
- "ESC pin"—This feature is enabled by setting U70[15] (HES) = 1_b. A high level detected on this pin returns the modem to Command mode. In parallel mode, the ESC pin is replaced functionally by the ESC bit in the Parallel Interface 1 register. The ESC pin is level-sensitive and should be left high until the "OK/" result code indicates that the modem is in Command mode.
- "9th bit"—If 8-bit data format with escape is programmed, a 1 detected on bit 9 returns the modem to Command mode. (See Figure 2 on page 9.) This is enabled via the \B6 AT command.

The "ATO" command can be used to re-enter Data mode no matter which "escape" method is used.

Flow Control

Flow control settings are configured with the "AT\Q" commands. Possible settings are no flow control, CTS-only flow control, RTS/CTS flow control, and XON/XOFF. $\overline{RTS}$ is the flow control signal from the host. When $\overline{RTS}$ is low, RXD serial transmission operates normally. When $\overline{RTS}$ goes high, no more characters are transmitted after the current character, and RXD is clamped to mark (1). This state persists until $\overline{RTS}$ goes low. Normal serial transmission resumes within one character-time.

The $\overline{CTS}$ output pin controls flow from the Si2456/33/14 to the host. When $\overline{CTS}$ is low, the Si2456/33/14 is ready to accept a character. While $\overline{CTS}$ is high, no data should be sent to the Si2456/33/14 on TXD. Figure 2 on page 9 shows the timing for flow control and the serial interface.

The ISOmodem default setting configures it to automatically retrain to a lower line rate depending on line conditions. However, the UART speed remains fixed as set by the "AT\Tn" command.

Data Mode

The Si2456/33/14 ISOmodem is in Data mode while it has a telephone line connection to another modem or is in the process of establishing a connection.

In Command and Data mode, the Si2456/33/14 operates in asynchronous mode only. Data protocols are available to provide error correction to improve reliability (V.42 and MNP2-4) and data compression to increase throughput (V.42bis and MNP5).

Each connection between two modems in Data mode begins with a handshaking sequence. During that sequence, the modems determine the line speed, data protocol, and related parameters for the data link. Configuration through AT commands determines the range of choices available to the modem in the negotiation process. Most configuration options in the Si2456/33/14 act to limit the range over which a

parameter can be negotiated rather than making specific assignments.

The host can cause the Si2456/33/14 to enter Data mode and initiate dialing by issuing an AT command to dial.

Fast Connect

The Si2456/33/14 supports a Fast Connect mode of operation to reduce the time of a connect sequence in originate mode. The Fast Connect modes are enabled via U7A. Each of the stages (answer tone detect time, unscrambled ones detect time, etc.) in the connect sequence may be shortened. The amount that each of these is shortened when in Fast Connect mode depends on the modulation. (See Table 9.)

Transparent HDLC/ Synchronous DCE Mode

The Si2456/33/14 also supports a "transparent HDLC" mode of operation, which operates with an asynchronous DTE and a synchronous DCE. The Si2456/33/14 performs HDLC frame packing and unpacking, frame opening and closing, flag generation and detection, CRC computation and checking, and 0 insertion and deletion. To use this mode, the DTE rate must be greater than the DCE rate, and either CTS or /Q and /S must be used. (See Table 10 on page 21.)

Table 9. Fast Connect/Transparent HDLC

Protocol	DCE	Register Settings
All	Normal, Asynchronous	&Hn
V.22, Bell212, V.22bis	Normal, Transparent HDLC	&H6, 7, 8 U7A = 0002 \N0
Bell103, V.21	Fast connect, Asynchronous	&H9, 10 U7A = 0001 \N0
V.22, Bell212	Fast connect, Asynchronous	&H7, 8 U7A = 0001 \N0
V.22, Bell212	Fast connect, Transparent HDLC	&H7, 8 U7A = 0003 \N0
V.22bis	Transparent HDLC	&H6 U7A = 0002 \N0

On the transmit side, if no data is received on TXD, the Si2456/33/14 continually transmits HDLC flags at the DCE. As soon as there are 10 characters sent into the transmit buffer, the Si2456/33/14 begins an HDLC frame at the DCE. The reason for this 10-character “headstart” is to reduce the likelihood of an underrun once the HDLC frame has begun at the DCE. As long as the host continues to send data, the Si2456/33/14 continues to zero insert, update the CRC value, and send data within an HDLC frame. To properly end the frame, the host must send a /Zn (see Table 10) indicating to the Si2456/33/14 the end of the frame. Once the Si2456/33/14 encounters the /Zn, it computes and sends the final CRC and begins transmitting HDLC flags. If an HDLC frame is smaller than the 10-character “head start”, the HDLC frame is started at the DCE upon receipt of the /Zn character. The /Tn metacharacter is sent to the host to provide an indication that an HDLC frame was sent successfully. The “n” in the /Zn and /Tn is a host-defined tag that can be used to track multiple HDLC frames. To facilitate transmit flow control, the modem sends the /S and /Q metacharacters to the host. If the transmit buffer (512 bytes) is three-quarters full, the /S metacharacter is sent to the host. The host must then stop transmitting. When the transmit buffer empties down to half full, the /Q metacharacter is sent to the host to indicate that it is okay to begin transmitting again. If a transmit underrun occurs, the current frame is aborted, and a /Un is sent to the host. All data from the underrun to the receipt of the /Zn metacharacter is discarded by the modem. A design goal of the host software should be to eliminate any occurrence of the /Un metacharacter.

Because the “/” is an escape character, the host must send a “//” when a “/” appears in the transmit data stream. The Si2456/33/14 removes one “/” for each instance of “// ” that appears on TXD.

On the receive side, as long as HDLC flags are received by the Si2456/33/14 at the DCE, it does not pass data out RXD. Once the first non-flag word is detected, the Si2456/33/14 performs zero deletion, calculates the CRC value, and passes the data out RXD. The Si2456/33/14 continues in this manner until detecting the HDLC flags, which indicate the end of the frame. At this point, the HDLC frame is complete, and the Si2456/33/14 calculates the final CRC and compares it to the CRC value received in the frame. If the CRC matches, the Si2456/33/14 passes /G to the host. If the CRC does not match, the Si2456/33/14 passes /B to the host.

Because the / is an escape character, the Si2456/33/14 sends a // when a / appears in the receive data stream. The host must remove one / for each instance of // that appears on RXD. Table 10 on page 21 lists additional escape characters that are used to control the flow of data between the Si2456/33/14 and the host in the "transparent HDLC" mode.

Table 10. Synchronous DCE Mode Metacharacters

Character	Direction	Description
/Z*n*	TX	Follows the last character of a transmit frame. Once the frame has been sent, a /T , metacharacter is sent to the host. *n* denotes a frame tag. *n* is echoed back later with the /U or /T metacharacters to make frame tracking easier.
//	TX	A forward slash character is to be transmitted.
/E	TX	Escape back to Command mode. Si2456/33/14 returns to Command mode.
/U*n*	RX	A transmit underrun has occurred, but a /Z metacharacter was not received. When an underrun occurs, the current frame is aborted, and a /U*n* is sent to host where *n* is the frame tag. All data following the underrun, up to the /Z metacharacter, is discarded by the modem.
/T*n*	RX	The transmit frame *n* has been sent. The *n* from the /Z is echoed with the /T*n* to allow tracking frames.
/G	RX	The previous receive frame CRC check was successful.
/B	RX	The previous receive frame CRC check was unsuccessful.
/S	RX	Transmit buffer is almost full, and the host must pause transmission to prevent an overflow. If hardware flow control is used, the host may ignore this metacharacter.
/Q	RX	The host may begin transmitting again after a /S (pause) has been sent. If hardware flow control is used, the host may ignore this metacharacter.
//	RX	A forward slash character was received.
/A	RX	Received frame was aborted.

Clocking/Low Power Modes

The Si2456/33/14 contains an on-chip phase-locked loop (PLL) and clock generation. Using either a single crystal or master clock input, the Si2456/33/14 can generate all the internal clocks required to support the featured modem protocols. Either a 4.9152 MHz clock (3.3 V max input—see Table 5 on page 8) on XTALI or a 4.9152 MHz (±100 ppm max) crystal across XTALI and XTALO form the master clock for the ISOmodem. This clock source is sent to an internal PLL that generates all necessary internal system clocks including the DSP clock. Figure 6 shows a block diagram of how the DSP clock and the CLKOUT are derived.

The DSP clock is generated from the 78.6432 MHz clock via the N1 clock divider. N1 is programmed through U6E[1:0] (N1) and defaults to 2 giving a DSP clock rate of 39.3216 MHz. This DSP clock rate is necessary to run the Si2456/33/14 in all modes described in the data sheet.

Using the S24 S-register, the Si2456/33/14 can be set to automatically enter sleep mode after a pre-programmed time of inactivity with either the DTE or the remote modem. The sleep mode is entered after (S24) seconds have passed since the TX FIFO has been empty. The ISOmodem remains in the sleep state until either a 1 to 0 transition on TXD (serial mode) or a 1 to 0 transition on $\overline{CS}$ (parallel mode) occurs.

Additionally, the Si2456/33/14 may be placed in a complete powerdown mode or wake-on-ring mode. Complete powerdown is accomplished via U65[13] (PDN). Once the PDN bit is written, the Si2456/33/14 completely powers down and can only be powered back on via the $\overline{RESET}$ pin.

A 78.6432 MHz/(R1 + 1) clock is produced on the CLKOUT pin that may be used as an external system clock. R1 may be programmed via U5E to any value between 1 and 31 (default value = 31).

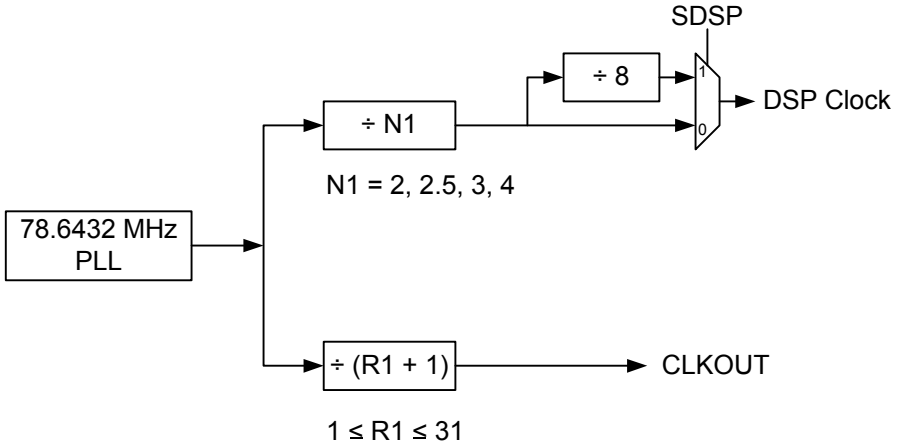


Figure 6. DSP Clock Divider and CLKOUT Generation

AT Commands

At powerup, the Si2456/33/14 is in the AT Command mode. In Command mode, the modem monitors the input (serial or parallel) checking constantly for a valid command (AT commands are described in Table 11).

Command Syntax

An AT command takes the form of a single letter or combination of a letter and a modified character, often followed by one or more numeric characters. The modem interprets the AT command as a direction to set a parameter or perform an action. The command (letter or letter and modifier) identifies the parameter or action, and the numeric value specifies (from a pre-determined range of choices) how the parameter is to be set or how the action is to be performed. Issuing any AT command strings that are not listed in Table 11 may result in unpredictable behavior.

AT commands are issued to the modem in the form of a "command line." Each command line is preceded by the letters AT, contains one or more commands, and ends with a carriage return. The letters AT stand for "ATtention" and signal the modem that a command (or commands) follows.

It is possible to enter multiple commands on a single line (up to a maximum of 48 characters). The commands may be separated by space or line-feed characters to improve readability. The modem ignores space and line-feed characters; so, they are not counted as part of the line's 48 characters. A carriage-return character must be entered at the end of a command line to signal the modem to process the commands.

Command Buffer

Once the command line is issued to the modem, it is loaded into an internal command buffer with a capacity of 48 characters. The AT prefix, spaces, line-feed characters, and carriage return are not loaded into the buffer. If a command line is more than 48 characters long, the modem does not act on any characters.

Table 11. Basic AT Command Set (Command Defaults in Bold)

Command	Action	
$	Display AT Command mode settings.	
A	Answer incoming call	
A/	Re-execute last command. This is the only command not preceded by "AT" or followed by a <CR>.	
Dn	Dial The dial command, followed by 1 or more dial command modifiers, manually dials a phone number:	
	Modifier	**Function**
	! or &	Flash hook switch for FHT (U4F) ms (default: 500 ms)
	, or <	Pause before continuing for S8 seconds (default: 2 seconds)
	;	Return to AT Command mode
	P	Pulse (rotary) dialing—pulse digits: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9
	T	Tone (DTMF) dialing—DTMF digits: *, #, A, B, C, D, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9
	W	Wait for dial tone before continuing for S14 seconds (default: 12 seconds). Blind dialing modes X0, X1 and X3 do not affect the W command. If the DOP bit (U7A, bit 7) is set, the "ATDTW" command will cause the ISOmodem to pause dialing and either report an "OK" if a dialtone is detected or "NO DIALTONE" if a dial tone is not detected.
En	Local DTE echo	
E0	Disable	

Table 11. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action	
E1	**Enable**	
Hn	Hook switch.	
H0	Go on-hook (hang up modem).	
H1	Go off-hook.	
In	Identification and checksum.	
I0	Display Si2456/33/14 revision code. B: Revision B C: Revision C, etc.	
I1	Display Si2456/33/14 firmware revision code (numeric).	
I3	Display line-side revision code. 15D = Si3015 revision D	
I6	Display the ISOmodem model number. “2414” = Si2414 “2433” = Si2433 “2456” = Si2456	
I7	Diagnostic Results 1. **Format** RX <rx_rate>,TX <tx_rate> PROTOCOL: <protocol> LOCAL NAK <rre> REMOTE NAK <rte> RETRN/RR <rn> DISC REASON <dr>	 **Description** Receive/transmit data rate in bps Error correction/data compression protocol. Number of V.42 receive errors Number of V.42 transmit errors Number of retrains Disconnect reason code (see Table 15 on page 32)
I8	Diagnostic Results 2. **Format** RX LEVEL <rx_level> TX LEVEL <tx_level> EFFECTIVE S/N <esn> RESIDUAL ECHO <re>	 **Description** Receive level power in dBm Transmit level power in dBm. Effective signal-to-noise ratio in dB Ratio of residual echo to signal in dB
Mn	Speaker operation (via AOUT).	
M0	**Speaker is always off.**	
M1	Speaker is on while dialing and handshaking; off in Data mode.	
M2	Speaker is always on.	
M3	Speaker is off while dialing, on during handshaking and retraining.	
On	Return to Data mode from Command mode operation.	
O0	Return to Data mode.	
O1	Return to Data mode and perform a full retrain (at any speed except 300 bps).	
O2	Return to Data mode and perform rate renegotiation.	
Qn	Response mode.	
Q0	**Enable result codes (see Table 16 on page 33)**	
Q1	Disable result codes (enable quiet mode).	
R	Initiate V.23 reversal.	

Table 11. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action
Sn	S-register operation (see Table 20 on page 40).
S$	List contents of all S registers.
Sn?	Display contents of S-register n.
Sn=x	Set S-register n to value x (where n and x are decimal values).
Vn	Result code type (see Table 16 on page 33).
V0	Numeric result codes.
V1	**Verbal result codes**
Xn	Call Progress Monitor (CPM)—This command controls which CPM signals are monitored and reported to the host from the Si2456/33/14. (See Table 16 on page 33.)
X0	Basic results; disable CPM—Blind dial (does not wait for dial tone). CONNECT message does not include speed.
X1	Extended results; disable CPM—Blind dial. CONNECT message includes speed.
X2	Extended results and detect dial tone only—Add dial tone detection to X1 mode. Does not blind dial.
X3	Extended results and detect busy only—Add busy tone detection to X1 mode.
X4	**Extended results, full CPM—Full CPM enabled, CONNECT message includes speed.**
X5	Extended results—Full CPM enabled including ringback detection. Adds ringback detection to X4 mode.
Yn	Long space disconnect—Modem hangs up after 1.5 seconds or more of continuous space while on-line.
Y0	**Disable.**
Y1	Enable.
Z	Hard Reset—This command is functionally equivalent to pulsing the $\overline{\text{RESET}}$ pin low. (See t_{AT} in Table 6 on page 8.)
:I	Interrupt Read—This command causes the ISOmodem to report the lower 8 bits of the interrupt register I/O Control 0 (U70). The CID, OCD, PPD, and RI bits also are cleared, and the $\overline{\text{INT}}$ pin (INT bit in parallel mode) is deactivated on this read.
:P	Program RAM Write—This command is used to upload firmware supplied by Silicon Labs to the Si2456/33/14. The format for this command is AT:Paaaa,xxxx,yyyy,.... where aaaa is the first address in hexadecimal and xxxx,yyyy,.... is data in hexadecimal. Only one :P command is allowed per AT command line. No other commands can be concatenated in the :P command line. This command is *only* for use with special files provided by Silicon Laboratories. Do not attempt to use this command for any other purpose.
:R	User-Access Register Read—This command allows the user to read from the user-access registers. (See pages 42–62.) The format is “AT:Raa”, where aa = user-access address in hexadecimal. The “AT:R” command causes all the U- registers to be displayed.
:U	User-Access Register Write—This command allows the user to write to the 16-bit user-access registers. (See page 42.) The format is “AT:Uaa,xxxx,yyyy,zzzz,...” where aa = user-access address in hexadecimal. xxxx = data in hexadecimal to be written to location aa. yyyy = data in hexadecimal to be written to location (aa + 1). zzzz = data in hexadecimal to be written to location (aa + 2). etc.

Table 11. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action
+VCID = X	Caller ID Enable. X Mode **0 Off** 1 On—formatted 2 On—raw data format
+VCDT = X	Caller ID Type. X Mode **0 After ring only** 1 Always on 2 UK 3 Japan

Extended AT Commands

The extended AT commands are supported by the Si2456/33/14 and are described in Tables 12 through 14.

Table 12. Extended AT& Command Set (Command Defaults in Bold)

Command	Action
&$	Display AT& current settings.
&Gn	Line connection rate limit—This command sets a lower limit on the line speed that the Si2456/33/14 can connect. Note that the &Hn commands may limit the line speed as well (&Gn not used for &H0 or &H1).
&G5	4.8 kbps max
&G6	7.2 kbps max
&G7	9.6 kbps max
&G8	12 kbps max
&G9	**14.4 kbps max (default for Si2414)**
&G10	16.8 kbps max
&G11	19.2 kbps max
&G12	21.6 kbps max
&G13	24 kbps max
&G14	26.4 kbps max
&G15	28.8 kbps max
&G16	31.2 kbps max
&G17	**33.6 kbps max (default for Si2456 and Si2433)**
&Hn	Switched network handshake mode—&Hn commands must be on a separate command line from ATD, ATA, or ATO commands.
&H0	**V.90 with automatic fallback (56 kbps to 300 bps) (default for Si2456)**
&H1	V.90 only (56 kbps to 28 kbps)
&H2	**V.34 with automatic fallback (33.6 kbps to 300 bps) (default for Si2433)**
&H3	V.34 only (33.6 kbps to 2400 bps)
&H4	**ITU-T V.32bis with automatic fallback (14.4 kbps to 300 bps) (default for Si2414)**
&H5	ITU-T V.32bis only (14.4 kbps to 4800 bps)
&H6	ITU-T V.22bis only (2400 bps or 1200 bps)
&H7	ITU-T V.22 only (1200 bps)
&H8	Bell 212 only (1200 bps)
&H9	Bell 103 only (300 bps)
&H10	ITU-T V.21 only (300 bps)
&H11	V.23 1200/75 bps
&Tn	Test Mode
&T0	Cancel Test Mode (Escape to Command mode to issue AT&T0)

Table 12. Extended AT& Command Set (Command Defaults in Bold) (Continued)

Command	Action
&T2	Initiate ITU-T V.54 (ANALOOP) test. Modem mode set by &H AT command. Test loop is through the DSP (Si2456/33/14 device) only. ISOmodem echoes data from TX pin (Register 0 in parallel mode) back to RX pin (Register 0 in parallel mode).
&T3	Initiate ITU-T V.54 (ANALOOP) test. Modem mode set by &H AT command. Test loop is through the DSP (Si2456/33/14), DAA interface section (Si2456/33/14), ISOcap interface (Si3015), and analog hybrid circuit (Si3015). ISOmodem echoes data from TX pin (Register 0 in parallel mode) back to RX pin (Register 0 in parallel mode). Phone line termination required as in Figure 1. To test only the ISOcap link operation, the hybrid and AFE codec can be removed from the test loop by setting the DL bit (U62, bit 1).
&T6	Compute checksum for firmware-upgradeable section of program memory. If no firmware upgrade is installed, &T6 returns 0x0408.

Table 13. Extended AT% Command Set (Command Defaults in Bold)

Command	Action
%$	Display AT% command settings.
%Cn	Data compression
%C0	Disable V.42bis and MNP5 data compression
%C1	**Enable V.42bis in transmit and receive paths. If MNP is selected (\N2), then %C1 enables MNP5 in transmit and receive paths.**
%C2	Enable V.42bis in transmit path only
%C3	Enable V.42bis in receive path only
%On	Answer mode
%O1	**Si2456/33/14 will auto-answer a call in answer mode**
%O2	Si2456/33/14 will auto-answer a call in originate mode

Table 14. Extended AT\ Command Set (Command Defaults in Bold)

Command	Action
\$	Display AT\ command settings.
\Bn	Character length
\B0	6N1—six data bits, no parity, one stop bit, one start bit, eight bits total (\N0 only)
\B1	7N1—seven data bits, no parity, one stop bit, one start bit, nine bits total (\N0 only)
\B2	7P1—seven data bits, parity optioned by \P, one stop bit, one start bit, 10 bits total
\B3	**8N1—eight data bits, no parity, one stop bit, one start bit, 10 bits total**
\B5	8P1—eight data bits, parity optioned by \P, one stop bit, one start bit, 11 bits total (\N0 only)
\B6	8X1—eight data bits, one escape bit, one stop bit, one start bit, 11 bits total (enables ninth-bit escape mode)
\Nn	Asynchronous protocol
\N0	Wire mode (no error correction, no compression)
\N2	MNP Reliable Mode. The Si2456/33/14 attempts to connect with MNP2-4 error correction. If unsuccessful, the call is dropped.
\N3	**V.42 auto-reliable—The Si2456/33/14 attempts to connect with data compression and error correction (V42bis and V.42). If unsuccessful, V.42 only is attempted. If unsuccessful, wire mode is attempted.**
\N4	V.42 (LAPM) reliable mode (or drop call)—Same as \N3 except that the Si2456/33/14 drops the call instead of connecting in wire mode.
\Pn	Parity type
\P0	**Even**
\P1	Space
\P2	Odd
\P3	Mark
\Qn	Modem-to-DTE flow control
\Q0	Disable all flow control—Note that this may only be used if the DTE speed and the VF speed are guaranteed to match throughout the call.
\Q2	**Use CTS only**
\Q3	Use RTS/CTS
\Q4	Use XON/XOFF flow control for modem-to-DTE interface. Does not enable modem-to-modem flow control.
\Tn	DTE speed
\T0	300 bps

Table 14. Extended AT\ Command Set (Command Defaults in Bold) (Continued)

Command	Action
\T1	600 bps
\T2	1200 bps
\T3*	2400 bps
\T4	4800 bps
\T5	7200 bps
\T6	9600 bps
\T7	12.0 kbps
\T8	14.4 kbps
\T9	**19.2 kbps**
\T10	38.4 kbps
\T11	57.6 kbps
\T12	115.2 kbps
\T13	230.4 kbps
\T14	245.760 kbps
\T15	307.200 kbps
\U	Serial mode—causes a low pulse (25 ms) on $\overline{RI}$ and $\overline{DCD}$. $\overline{INT}$ to be the inverse of ESC. $\overline{RTS}$ to be inverse of $\overline{CTS}$. Parallel mode—causes a low pulse (25 ms) on $\overline{INT}$. This command terminates with a $\overline{RESET}$.
\Vn	Connect message type
\V0	**Report connect message and protocol message**
\V2	Report connect message only (exclude protocol message)
***Note:** Default DTE speed when ≤10 kΩ resistor is placed between SDI and GND.	

Table 15. Disconnect Codes

Disconnect Code	Reason
8002	Handshake stalled.
8	No dialtone detected.
8008	No line available.
9	No loop current detected.
8009	Parallel phone pickup disconnect.
A	No ringback.
B	Busy signal detected.
D	V.42 requested disconnect.
E	MNP requested disconnect.
10	Drop dead timer disconnect.
8014	Loop current loss.
8017	Remote modem requested disconnect.
8018, 8019	Soft reset command received.
1a	V.42 Protocol error.
1b	MNP Protocol error.
801c	Loss-of-carrier disconnect.
801e	Long space disconnect.
801f	Character abort disconnect.
802a	Rate request failed.
802b	Answer modem energy not detected.
802c	V.8 negotiation failed.
2d	TX data timeout.

Table 16. Result Codes

Numeric	Meaning	Verbal Response	X0	X1	X2	X3	X4	X5
0	Command was successful	OK	X	X	X	X	X	X
1	Link established at 300 bps or higher	CONNECT	X	X	X	X	X	X
2	Incoming ring detected	RING	X	X	X	X	X	X
3	Link dropped	NO CARRIER	X	X	X	X	X	X
4	Command failed	ERROR	X	X	X	X	X	X
5	Link establish at 1200	CONNECT 1200		X	X	X	X	X
6	Dial tone not present	NO DIALTONE			X		X	X
7	Line busy	BUSY				X	X	X
8	Remote not answering	NO ANSWER	X	X	X	X	X	X
9	Ringback detected	RINGING						X
10	Link established at 2400	CONNECT 2400		X	X	X	X	X
11	Link established at 4800	CONNECT 4800		X	X	X	X	X
12	Link established at 9600	CONNECT 9600		X	X	X	X	X
14	Link established at 19200	CONNECT 19200[1]		X	X	X	X	X
15	Link established at 7200	CONNECT 7200		X	X	X	X	X
16	Link established at 12000	CONNECT 12000		X	X	X	X	X
17	Link established at 14400	CONNECT 14400		X	X	X	X	X
18	Link established at 16800	CONNECT 16800[1]		X	X	X	X	X
19	Link established at 21600	CONNECT 21600[1]		X	X	X	X	X
20	Link established at 24000	CONNECT 24000[1]		X	X	X	X	X
21	Link established at 26400	CONNECT 26400[1]		X	X	X	X	X
22	Link established at 28800	CONNECT 28800[1]		X	X	X	X	X
23	Link established at 31200	CONNECT 31200[1]		X	X	X	X	X
24	Link established at 33600	CONNECT 33600[1]		X	X	X	X	X
30	Caller ID mark detected	CIDM	X	X	X	X	X	X
75	Link established at 75	CONNECT 75		X	X	X	X	X
31	Hookswitch flash detected	FLASH	X	X	X	X	X	X
32	UK CID State Tone Alert Signal detected	STAS	X	X	X	X	X	X
33	Overcurrent condition	X[2]	X	X	X	X	X	X
52	Link established at 56000	CONNECT 56000[3]		X	X	X	X	X
60	Link established at 32000	CONNECT 32000[3]		X	X	X	X	X
61	Link established at 48000	CONNECT 48000[3]		X	X	X	X	X
63	Link established at 28000	CONNECT 28000[3]		X	X	X	X	X
64	Link established at 29333	CONNECT 29333[3]		X	X	X	X	X
65	Link established at 30666	CONNECT 30666[3]		X	X	X	X	X

Notes:

1. This message is only supported on the Si2456 and Si2433.
2. X is the only verbal response code that does not follow the <CR><LF>Result Code<CR><LF> standard. There is no leading <CR><LF>.
3. This message is only supported on the Si2456.

Table 16. Result Codes (Continued)

Numeric	Meaning	Verbal Response	X0	X1	X2	X3	X4	X5
66	Link established at 33333	CONNECT 33333[3]		X	X	X	X	X
67	Link established at 34666	CONNECT 34666[3]		X	X	X	X	X
68	Link established at 36000	CONNECT 36000[3]		X	X	X	X	X
69	Link established at 37333	CONNECT 37333[3]		X	X	X	X	X
70	No protocol	PROTOCOL: NONE	Set with \V0 command.					
77	V.42 protocol	PROTOCOL: V42	Set with \V0 command.					
79	V.42bis protocol	PROTOCOL: V42bis	Set with \V0 command.					
80	MNP2 protocol	PROTOCOL: ALTERNATE, + CLASS 2	Set with \V command.					
81	MNP3 protocol	PROTOCOL: ALTERNATE, + CLASS 3	Set with \V command.					
82	MNP4 protocol	PROTOCOL: ALTERNATE, + CLASS 4	Set with \V command.					
83	MNP5 protocol	PROTOCOL: ALTERNATE, + CLASS 5		X	X	X	X	X
90	Link established at 38666	CONNECT 38666[3]		X	X	X	X	X
91	Link established at 40000	CONNECT 40000[3]		X	X	X	X	X
92	Link established at 41333	CONNECT 41333[3]		X	X	X	X	X
93	Link established at 42666	CONNECT 42666[3]		X	X	X	X	X
94	Link established at 44000	CONNECT 44000[3]		X	X	X	X	X
95	Link established at 45333	CONNECT 45333[3]		X	X	X	X	X
96	Link established at 46666	CONNECT 46666[3]		X	X	X	X	X
97	Link established at 49333	CONNECT 49333[3]		X	X	X	X	X
98	Link established at 50666	CONNECT 50666[3]		X	X	X	X	X
99	Link established at 52000	CONNECT 52000[3]		X	X	X	X	X
100	Link established at 53333	CONNECT 53333[3]		X	X	X	X	X
101	Link established at 54666	CONNECT 54666[3]		X	X	X	X	X
102	DTMF dial attempted on a pulse dial only line	UN–OBTAINABLE NUMBER	X	X	X	X	X	X

Notes:
1. This message is only supported on the Si2456 and Si2433.
2. X is the only verbal response code that does not follow the <CR><LF>Result Code<CR><LF> standard. There is no leading <CR><LF>.
3. This message is only supported on the Si2456.

The connect messages shown in Tables 14 and 16 are sent when link negotiation is complete.

Data Compression

The modem can achieve DTE (host-to-ISOmodem) speeds greater than the maximum DCE (modem-to-modem) speed through the use of a data compression protocol. The compression protocols available are the ITU-T V.42bis and MNP5 protocols. Data compression attempts to increase throughput by compressing the information to be sent before actually sending it. The modem is, thus, able to transmit more data in a given period of time. Table 17 details the Si2456/33/14 error correction and data compression modes of operation.

Table 17. Enabling Error Correction/Data Compression

To Enable	Use AT Commands
V.42 (LAPM) V.42bis Wire	\N3 and %C1 (default)
V.42 and V.42bis only	\N4 and %C1
V.42 only	\N4 and %C0
MNP2-4 only	\N2
MNP2-5 only	\N2 and %C1
No data compression and no error correction	\N0 and %C0

Error Correction

The Si2456/33/14 ISOmodem can employ error correction (reliable) protocols to ensure error-free delivery of asynchronous data sent between the host and the remote end. The error control methods are based on grouping data into frames with checksums determined by the contents of each frame. The receiving modem checks the frames and sends acknowledgments to the transmitting modem. When it detects a faulty frame, the receiving modem requests a retransmission. Frame length varies according to the amount of data transmitted or the number of retransmissions requested from the opposite end.

The Si2456/33/14 supports V.42 and MNP2-4 error correction protocols. V.42 (LAPM) is most commonly used and is enabled in \N3 and \N4 modes. In the default mode (\N3), the Si2456/33/14 attempts to connect with V.42 error correction and V.42bis data compression and falls back to either V.42 only or no error correction (wire mode) if necessary. In \N4 mode, the Si2456/33/14 hangs up if a V.42 connection cannot be established. If the ISOmodem hangs up in V.42 mode after all data is successfully sent, the result code is “OK”. If the modem hangs up before all data is successfully sent, the result code is “No Carrier”. The “No Carrier” result code will also be given in the \N4 mode if V.42 negotiation is unsuccessful.

The V.42 specification allows an alternate error correction protocol, MNP2-4. MNP2-4 is enabled in \N2 mode. In \N2 mode, the Si2456/33/14 hangs up if an MNP2, 3, or 4 connection cannot be established.

Wire Mode

Wire mode (\N0) is used to communicate with standard non-error correcting modems. When optioned with \N3, the Si2456/33/14 falls back to wire mode if it fails in an attempt to negotiate a V.42 link with the remote modem. Error correction and data compression are not active in wire mode.

Caller ID Operation

The Si2456/33/14 supports full caller ID detection and decode for the US Bellcore and European ETSI protocols.

The Si2456/33/14 detects the first ring burst signal and echoes “RING” to the host. The device starts searching for the caller ID preamble sequence after the appropriate time-out. When 50 continuous mark bits have been detected, the “CIDM” response is echoed to indicate that the mark has been detected and that caller ID data follows. If enabled (via the +VCID and +VCDT AT commands), the $\overline{\text{INT}}$ pin goes active.

At this point, the algorithm looks for the first start bit, assemble the characters, and transmits them to the host as they are detected. When the caller ID burst finishes, the carrier is lost, and the modem echoes a “NO CARRIER” to indicate that the carrier is lost.

At this point, the Si2456/33/14 continues detecting ring bursts and echoing “RING” for each burst and answers automatically after the correct number of rings.

UK Caller ID Operation

When the Si2456/33/14 detects a line reversal, it echoes a “FLASH” to the host, and, if enabled, the $\overline{\text{INT}}$ pin activates.

The ISOmodem begins searching for the Idle State Tone Alert Signal. When this signal has been detected, it echoes “STAS” to the host. After the Idle State Tone Alert Signal is completed, the ISOmodem applies the wetting pulse for the required 15 ms by quickly going off-hook and on-hook. From this point on, the algorithm is identical to that of Bellcore in that it searches for the channel seizure signal and the marks before echoing “CIDM” and reports the decoded caller ID data.

Japan Caller ID Operation

After a polarity reversal and the first ring burst are detected, the Si2456/33/14 is taken off-hook, and, if

enabled, the $\overline{INT}$ pin is activated. After 40 1s (marks) have been detected, the Si2456/33/14 searches for a start bit, echo “CIDM”, and begins assembling characters and transmitting them out through the serial port. When the carrier is lost, the Si2456/33/14 immediately hangs up and echoes “No Carrier”.

Force Caller ID Monitor (Always On)

The Si2456/33/14 may be used to continuously monitor the phone line for the caller ID mark (1) FSK data. This can be useful in systems that require detection of caller ID data before the ring signal, voice mail indicator signals, and Type II caller ID support. The +VCDT AT command can be used to force the Si2456/33/14 into this mode.

Parallel Phone Detection

The ISOmodem is able to detect when another telephone, modem, or other device is using the phone line. This allows the host to avoid interrupting another phone call when the phone line is already in use and to intelligently handle an interruption when the ISOmodem is using the phone line.

On-Hook Intrusion Detection

When the ISOmodem is sharing the telephone line with other devices, it is important that it not interrupt a call in progress. To detect whether another device is using the shared telephone line, the host can use the ISOmodem to monitor the TIP-RING dc voltage with the LVCS (Line Voltage and Current Sense) register (U79, bits 4:0). See Figure 7 on page 37.

Set U69[2] (MODE) = 1 to read LVCS while on-hook. Before going off-hook, it is necessary to set U69[2] (MODE) = 0. The commands to accomplish this are listed in Table 18.

Table 18. AT Commands

AT Command	Function
AT:U69,0004<CR>	Sets MODE bit to monitor loop voltage.
AT:R79<CR>	U79[4:0] (LVCS) measures loop voltage.
AT:U69,0000<CR>	Clears MODE bit for modem to go off-hook.

Off-Hook Intrusion Detection

When the ISOmodem is off-hook, an algorithm is implemented in the ISOmodem to automatically monitor the TIP-RING loop current via the LVCS register. Because the TIP-RING voltage drops significantly when off-hook, TIP-RING current is a better indicator of intrusion than TIP-RING voltage. When the ISOmodem is off-hook, the LVCS register switches from representing the TIP-RING voltage to representing the TIP-RING current. (See Figure 8 on page 38.) Upon detecting an intrusion, the ISOmodem alerts the host of the condition via the $\overline{INT}$ pin (the INT bit in parallel mode). The host must unmask this interrupt by setting the PPDM bit (U70, bit 10). After detecting the interrupt, the host should then issue the AT:I command to verify the reason for the interrupt was a parallel phone intrusion and to clear the PPD bit (U70, bit 2). The ISOmodem may be set to automatically hang up on a PPD interrupt by setting the HOI bit (U77, bit 11).

The off-hook intrusion algorithm monitors the value of LVCS (U79, bits 4:0) at a sample rate determined by the OHSR (U76, bits 15:9) register (40 ms units). The algorithm compares each LVCS sample to the reference value in the ACL register (U76, bits 4:0). If LVCS is lower than ACL by an amount greater than DCL (U76, bits 7:5), the algorithm waits for another LVCS sample, and if the next LVCS sample is also lower than ACL by an amount greater than DCL, a PPD interrupt occurs. This helps the ISOmodem avoid a false PPD interrupt due to glitches on the phone line. The ACL is continually updated with the value of LVCS as outlined below. If desired, the host may force ACL to a fixed value by setting the FACL bit (U76, bit 8). The algorithm can be outlined as follows:

If LVCS(t) = LVCS(t – 40 ms x OHSR)
and
LCVS(t) – ACL > DCL
then ACL = LVCS(t)
If (ACL – LVCS[t – 40 ms x OHSR]) > DCL)
and
(ACL – LVCS[t]) > DCL)
then PPD = 1 and $\overline{INT}$ (INT bit in parallel mode) is asserted.

The very first sample of LVCS the algorithm uses after going off-hook does not have any previous samples for comparison. If LVCS was measured during a previous call, this value of LVCS may be used as an initial reference. ACL may be written by the host with this known value of LVCS. If ACL is non-zero, the ISOmodem uses ACL as the first valid LVCS sample in the off-hook intrusion algorithm. If ACL is 0 (default after

reset), the ISOmodem ignores the register and does not begin operating the algorithm until two LVCS samples have been received. Additionally, immediately after a modem call, the ISOmodem is updated automatically ACL with the last valid LVCS value before a PPD intrusion or going back on-hook.

The off-hook intrusion algorithm does not begin to operate immediately after going off-hook. This is to avoid triggering a PPD interrupt due to transients resulting from the ISOmodem itself going from on-hook to off-hook. The time from when the ISOmodem goes off-hook to when the intrusion algorithm begins defaults to 1 second and may be adjusted via the IST register (U77, bits 15:12). If ACL is written to a non-zero value before going off-hook, a parallel phone intrusion that occurs during this IST interval and sustains through the end of the interval triggers a PPD interrupt.

The off-hook intrusion algorithm may, additionally, be disabled for a period of time after dialing begins via the IB register (U78, bits 15:14). This avoids triggering a PPD interrupt due to pulse dialing, open-switch intervals, or line transients from central office switching. Intrusion may be disabled from the start of dialing to the end of dialing (IB = 1), from the start of dialing to the timeout of the IS (U78, bits 7:0) register (IB = 2), or from the start of dialing to the connect result code (CONNECT XXX, NO DIALTONE, or NO CARRIER) (IB = 3). The off-hook intrusion algorithm is only suspended (not disabled) during this IB interval. Therefore, any intrusion that occurs during the IB interval and sustains through the end of the interval triggers a PPD interrupt.

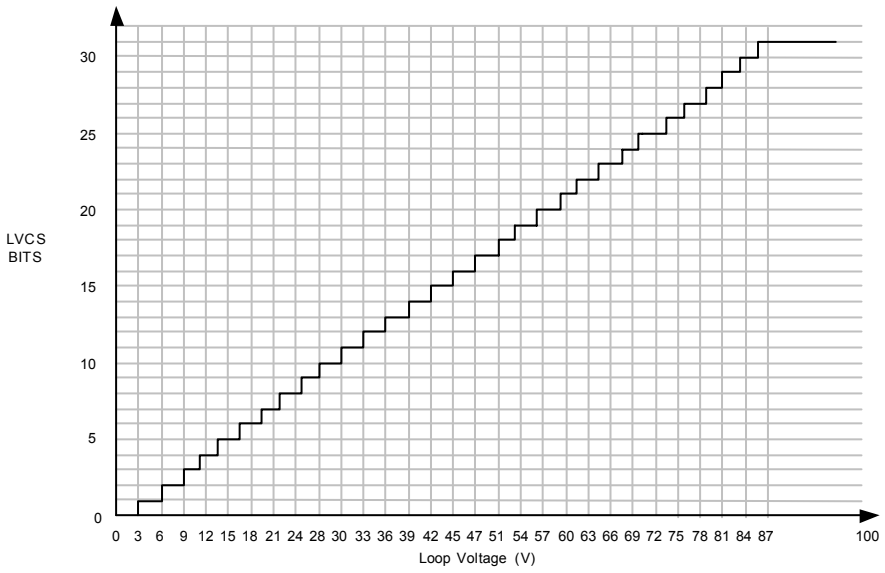


Figure 7. Loop Voltage

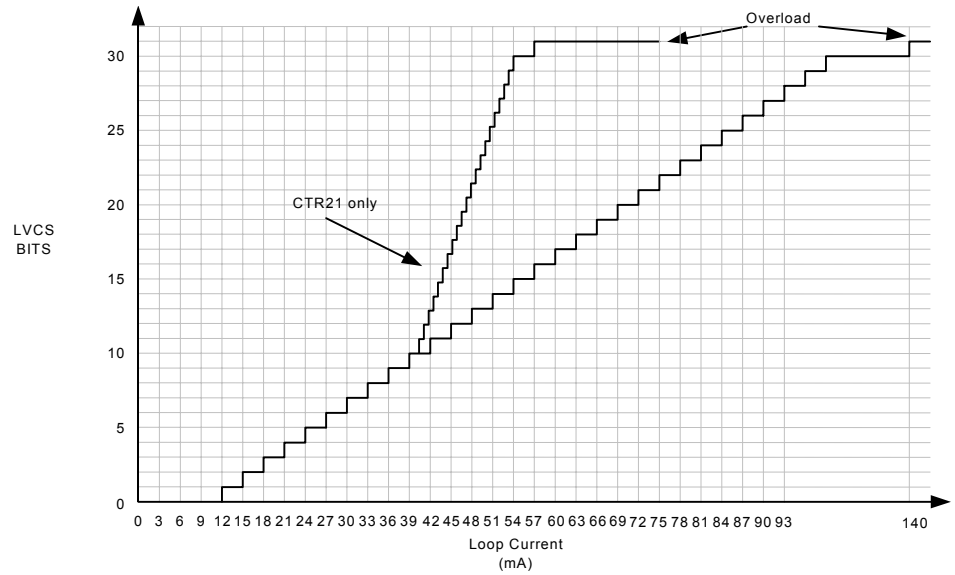


Figure 8. Loop Current

Overcurrent Detection

The Si2456/33/14 includes an overcurrent detection feature that measures the loop current at a programmable time after the Si2456/33/14 goes off-hook. This allows the Si2456/33/14 to detect if it is connected to an improper telephone line (such as a digital PBX) that may damage the DAA. The overcurrent detection feature may be enabled by setting the OCDM bit (U70, bit 11). OHT (U77, bits 8:0) sets the delay after off-hook until the loop current is measured. If OCDM is enabled and excessive current is detected, the Si2456/33/14 will send the "X" result code and trigger an interrupt by asserting the INT pin (or set the INT bit in parallel mode). After an interrupt, the host should issue the AT:I command to verify the OCD interrupt and clear OCD bit (U70, bit 3). The host should hang up the modem with the ATH command immediately after an overcurrent is detected in order to avoid damaging the DAA.

In the CTR21 mode of operation (see Table 19), the overcurrent detection can trip unnecessarily for loop current values greater than 55 mA. Therefore, if the ISOmodem is in CTR21 mode and an overcurrent condition is detected, the host should switch the ISOmodem into FCC mode and check the LVCS register for a valid overcurrent value equal to 0x1F.

Global Operation

The Si2456/33/14 chipset contains an integrated silicon direct access arrangement (Silicon DAA) that provides a programmable line interface to meet international telephone line interface requirements. Table 19 on page 39 gives the DAA register settings required to meet international PTT standards.

Additionally, the user-access registers (via the AT:U and AT:R commands) may be programmed for country-specific settings, such as dial tone, ring, ringback, and busy tone. Table 21 on page 42 contains a listing of these U-register settings for many countries. Additional settings may easily be implemented by following the U-register descriptions.

Firmware Upgrades

The Si2456/33/14 contains an on-chip program ROM that includes the firmware required for the features listed in this data sheet. In addition, the Si2456/33/14 contains on-chip program RAM to accommodate minor changes to the ROM firmware. This allows Silicon Labs to provide future firmware updates to optimize the characteristics of new modem designs and those already deployed in the field.

The firmware upgrade (provided by Silicon Labs) is a file loaded into the Si2456/33/14 after a reset using the AT:P command. Once loaded, the upgrade status can be read using the ATI1 command to verify the firmware revision number. The entire firmware upgrade in RAM is always cleared on reset. To reload the file after a reset or powerdown, the host simply rewrites the file using the "AT:P" command. (See Table 11 on page 23.)

A CRC can be run on the file loaded into on-chip RAM, with the AT&T6 command to verify that the upgrade was correctly written to the on-chip memory. The CRC value obtained from executing the AT&T6 command should match the CRC value provided with the upgrade code.

Table 19. Country-Specific Register Settings

Register	U67					U68	U69		U4D
Country	**OHS**	**ACT**	**DCT**	**RZ**	**RT**	**LIM**	**VOL**	**FLVM**	**LLC**
Australia[1]	1	1	01	0	0	0	0	0	0
Brazil[2]	0	0	01	0	0	0	0	0	0
CTR21[1, 3, 4]	0	1	11	0	0	1	0	0	1
Czech Republic	0	1	10	0	0	0	0	0	0
FCC[1, 5]	**0**	**0**	**10**	**0**	**0**	**0**	**0**	**0**	**0**
Latvia	0	1	11	0	0	1	0	0	0
Malaysia[1,6]	0	0	01	0	0	0	0	0	0
New Zealand	0	1	10	0	0	0	0	0	0
Nigeria	0	1	11	0	0	1	0	0	0
Philippines[1]	0	0	01	0	0	0	0	1	0
Poland[7], Slovenia	0	0	10	1	1	0	0	0	0
South Africa[7]	1	0	10	1	0	0	0	0	0
South Korea[7]	0	0	01	1	0	0	0	0	0

Note:

1. See "DC Termination" on page 68 for more information.
2. The following countries require the same settings as Brazil: Armenia, China, Egypt, Georgia, Japan, Jordan, Kazakhstan, Kyrgyzstan, Muldova, Oman, Pakistan, Qatar, Russia, Syria, Taiwan, Thailand, and Ukraine.
3. The following countries require the same settings as CTR21: Austria, Bahrain, Belgium, Bulgaria, Croatia, Cyprus, Denmark, Estonia, European Union, Finland, France, Germany, Greece, Guadeloupe, Iceland, Ireland, Israel, Italy, Lebanon, Liechtenstein, Luxembourg, Malta, Martinique, Morocco, Netherlands, Norway, Polynesia (French), Portugal, Reunion, Spain, Sweden, Switzerland, Turkey, and the United Kingdom.
4. When changing into or out of CTR21 Mode, LLC should be written first.
5. The following countries require the same settings as FCC: Argentina, Brunei, Canada, Chile, Columbia, Dubai, Equador, El Salvador, Guam, Hong Kong, Hungary, India, Indonesia, Kuwait, Macao, Mexico, Peru, Puerto Rico, Romania, Saudi Arabia, Singapore, Slovakia, Tunisia, UAE, USA, Venezuela, and Yemen.
6. Supported for loop current $\geq$ 20 mA.
7. SF5[1] (RZ) should only be set for Poland, South Africa, and South Korea if the ringer impedance network (C15, R14, Z2, Z3) is not populated.

S-Registers

The S command allows reading (Sn?) or writing (Sn=x) the S-registers. The S-registers store values for functions that typically are rarely changed, such as timers or counters, and the ASCII values of control characters, such as carriage return. Table 20 summarizes the S-register set.

Table 20. S-Register Description

Definition				
S-Register (Decimal)	**Function**	**Default (Decimal)**	**Range**	**Units**
0	Automatic answer—Number of rings the Si2456/33/14 must detect before answering a call. 0 disables auto answer.	0	0–255	Rings
1	Ring counter.	0	0–255	Rings
2	ESC code character.	43 (+)	0–255	ASCII
3	Carriage return character.	13 (CR)	0–255	ASCII
4	Line feed character.	10 (LF)	0–255	ASCII
5	Backspace character.	08 (BS)	0–255	ASCII
6	Dial tone wait timer—Number of seconds the Si2456/33/14 waits before blind dialing. Only applicable if blind dialing is enabled (X0, X1, X3).	02	0–255	seconds
7	Carrier wait timer—Number of seconds the Si2456/33/14 waits for carrier before timing out. This register also sets the number of seconds the modem waits for ring-back when originating a call before hanging up.	60	0–255	seconds
8	Dial pause timer for , and < dial command modifiers.	02	0–255	seconds
9	Carrier presence timer—Time after a loss of carrier that a carrier must be detected before reactivating $\overline{\text{DCD}}$. S9 is referred to as “carrier loss debounce time.”	06	1–255	0.1 second
10	Carrier loss timer—Time the carrier must be lost before the Si2456/33/14 disconnects. Setting 255 disables disconnect entirely. If S10 is less than S9, even a momentary loss of carrier causes a disconnect.	14	1–255	0.1 second
12	Escape code guard timer—Minimum guard time required before and after “+++” for the Si2456/33/14 to recognize a valid escape sequence.	50	1–255	0.02 second
14	Wait for dial tone delay value (in relation to the W dial modifier). Starts when “W” is executed in the dial string.	12	0–255	seconds

Table 20. S-Register Description (Continued)

Definition				
S-Register (Decimal)	**Function**	**Default (Decimal)**	**Range**	**Units**
24	Sleep Inactivity Time—Sets the time that the modem operates in normal power mode with no activity on the serial port, parallel port, or telephone line before entering low-power sleep mode. This feature is disabled if the timer is set to 0.	0	0–255	seconds
30	Disconnect Activity Timer—Sets the length of time that the modem stays online before disconnecting with no activity on the serial port, parallel port, or telephone line (Ring, hookswitch flash, or caller ID). This feature is disabled if set to 0.	0	0–255	minutes
38	Hang Up Delay Time—Maximum delay between receipt of ATH0 command and hang up. If time out occurs before all data can be sent, the NO CARRIER (3) result code is sent (operates in V.42 mode only). “OK” response is sent if all data is transmitted before timeout. S38 = 255 disables timeout and modem disconnects only if data is successfully sent or carrier is lost.	20	0–255	seconds

User-Access Registers (U-Registers)

The :U AT command is used to write these 16-bit U-registers, and the :R command is used to read them. U-registers are identified by a hexidecimal (hex) address.

Table 21. U-Register Description

Register	Address (Hex)	Name	Description	Default
U00	0x0000	DT1A0	DT1 registers set the coefficients for stage 1 of the Dial Tone Detect filter. Biquad coefficients can be programmed as 16-bit 2s complement values scaled as 1.0 = 0xC000 with the formula: $H(z) = \frac{A0 + A1z^{-1} + A2z^{-2}}{1 + B1z^{-1} + B2z^{-2}}$ Default is for FCC countries. See "Appendix C—User-Access Register Settings" on page 73 for other country settings.	0x0800
U01	0x0001	DT1B1		0x0000
U02	0x0002	DT1B2		0x0000
U03	0x0003	DT1A2		0x0000
U04	0x0004	DT1A1		0x0000
U05	0x0005	DT2A0	Dial tone detect filters stage 2 biquad coefficients.	0x00A0
U06	0x0006	DT2B1		0x6EF1
U07	0x0007	DT2B2		0xC4F4
U08	0x0008	DT2A2		0xC000
U09	0x0009	DT2A1		0x0000
U0A	0x000A	DT3A0	Dial tone detect filters stage 3 biquad coefficients.	0x00A0
U0B	0x000B	DT3B1		0x78B0
U0C	0x000C	DT3B2		0xC305
U0D	0x000D	DT3A2		0x4000
U0E	0x000E	DT3A1		0xB50A
U0F	0x000F	DT4A0	Dial tone detect filters stage 4 biquad coefficients.	0x0400
U10	0x0010	DT4B1		0x70D2
U11	0x0011	DT4B2		0xC830
U12	0x0012	DT4A2		0x4000
U13	0x0013	DT4A1		0x80E2
U14	0x0014	DTK	Dial tone detect filter output scaler.	0x0009
U15	0x0015	DTON	Dial tone detect ON threshold.	0x00A0
U16	0x0016	DTOF	Dial tone detect OFF threshold.	0x0070

Table 21. U-Register Description (Continued)

Register	Address (Hex)	Name	Description	Default
U17	0x0017	BT1A0	BT1 registers set the coefficients for stage 1 of the Busy Tone Detect filter. Default is for FCC countries. See "Appendix C—User-Access Register Settings" on page 73 for other country settings.	0x0800
U18	0x0018	BT1B1		0x0000
U19	0x0019	BT1B2		0x0000
U1A	0x001A	BT1A2		0x0000
U1B	0x001B	BT1A1		0x0000
U1C	0x001C	BT2A0	Busy tone detect filter stage 2 biquad coefficients.	0x00A0
U1D	0x001D	BT2B1		0x6EF1
U1E	0x001E	BT2B2		0xC4F4
U1F	0x001F	BT2A2		0xC000
U20	0x0020	BT2A1		0x0000
U21	0x0021	BT3A0	Busy tone detect filter stage 3 biquad coefficients.	0x00A0
U22	0x0022	BT3B1		0x78B0
U23	0x0023	BT3B2		0xC305
U24	0x0024	BT3A2		0x4000
U25	0x0025	BT3A1		0xB50A
U26	0x0026	BT4A0	Busy tone detect filter stage 4 biquad coefficients.	0x0400
U27	0x0027	BT4B1		0x70D2
U28	0x0028	BT4B2		0xC830
U29	0x0029	BT4A2		0x4000
U2A	0x002A	BT4A1		0x80E2
U2B	0x002B	BTK	Busy tone detect filter output scaler.	0x0009
U2C	0x002C	BTON	Busy tone detect ON threshold.	0x00A0
U2D	0x002D	BTOF	Busy tone detect OFF threshold.	0x0070

Table 21. U-Register Description (Continued)

Register	Address (Hex)	Name	Description	Default
U2E	0x002E	BMTT	Busy cadence minimum total time in seconds multiplied by 7200. Country-specific settings for busy, ringback, and dialtone cadences are specified by a range for ON time (minimum ON and maximum ON) and a range for OFF time (minimum OFF and maximum OFF). The Si2456/33/14 uses three registers to fully specify this range: MTT, DLT, and MOT. MTT is the minimum total time and is equal to the minimum ON time plus the minimum OFF time. DLT is the allowable delta. This is equal to maximum total time (maximum ON time plus the maximum OFF time) minus the minimum total time (MTT). MOT is simply the minimum ON time. Example: A country specifies a busy tone with ON time from 1–2 seconds and OFF time from 3–4 seconds. Thus, minimum ON time = 1 sec, maximum ON time = 2 sec, minimum OFF time = 3 sec, and maximum OFF time = 4 sec. BMTT = 1 + 3 = 4 seconds, maximum total time = 2 + 4 = 6 seconds, so BDLT = 6 – 4 = 2 seconds, and BMOT = 1.	0x0870
U2F	0x002F	BDLT	Busy cadence delta in seconds multiplied by 7200.	0x25F8
U30	0x0030	BMOT	Busy cadence minimum on time in seconds multiplied by 7200.	0x0438
U31	0x0031	RMTT	Ringback cadence minimum total time in seconds multiplied by 7200.	0x4650
U32	0x0032	RDLT	Ringback cadence delta in seconds multiplied by 7200.	0xEF10
U33	0x0033	RMOT	Ringback cadence minimum on time in seconds multiplied by 7200.	0x1200
U34	0x0034	DTWD	Window to look for dialtone in seconds multiplied by 1000.	0x1B58
U35	0x0035	DMOT	Minimum dialtone on time in seconds multiplied by 7200.	0x2D00
U37	0x0037	PD0	Number of pulses to dial 0.	0x000A
U38	0x0038	PD1	Number of pulses to dial 1.	0x0001
U39	0x0039	PD2	Number of pulses to dial 2.	0x0002
U3A	0x003A	PD3	Number of pulses to dial 3.	0x0003
U3B	0x003B	PD4	Number of pulses to dial 4.	0x0004
U3C	0x003C	PD5	Number of pulses to dial 5.	0x0005
U3D	0x003D	PD6	Number of pulses to dial 6.	0x0006
U3E	0x003E	PD7	Number of pulses to dial 7.	0x0007
U3F	0x003F	PD8	Number of pulses to dial 8.	0x0008
U40	0x0040	PD9	Number of pulses to dial 9.	0x0009
U42	0x0042	PDBT	Pulse dial break time (ms units).	0x003D

Table 21. U-Register Description (Continued)

Register	Address (Hex)	Name	Description	Default
U43	0x0043	PDMT	Pulse dial make time (ms units).	0x0027
U45	0x0045	PDIT	Pulse dial interdigit time (ms units).	0x0320
U46	0x0046	DTPL	DTMF power level—16-bit format is 0x0(H)(L)0 where H is the (–)dBm level of the high-frequency DTMF tone and L is the (–)dBm level of the low-frequency DTMF tone. Note that twist may be specified here.	0x09B0
U47	0x0047	DTNT	DTMF on time (ms units).	0x0064
U48	0x0048	DTFT	DTMF off time (ms units).	0x0064
U49	0x0049	RGFH	Ring frequency high—Maximum frequency ring to be considered a valid ring. RGFH = 2400/(maximum ring frequency).	0x0022
U4A	0x004A	RGFD	Ring delta $RGFD = 2400\ \text{Hz} \times \left(\frac{1}{\text{min ring freq (Hz)}}\right) - \left(\frac{1}{\text{max ring freq (Hz)}}\right)$	0x007A
U4B	0x004B	RGMN	Ring cadence minimum ON time in seconds multiplied by 2400.	0x0258
U4C	0x004C	RGNX	Ring cadence maximum total cadence in seconds multiplied by 2400.	0x6720
U4D	0x004D	MOD1	This is a bit-mapped register.	0x0000
U4E	0x004E	PRDD	Pre-dial delay-time after ATD command that modem waits to dial (ms units). The Si2456/33/14 stays on-hook during this time.	0x0000
U4F	0x004F	FHT	Flash Hook Time. Time corresponding with “!” or “&” dial modifier that the Si2456/33/14 goes on-hook during a flash hook (ms units).	0x01F4
U50	0x0050	LCDN	Loop current debounce on time (ms units).	0x015E
U51	0x0051	LCDF	Loop current debounce off time (ms units).	0x00C8
U52	0x0052	XMTL	Transmit level (1 dB units)—Sets the modem data pump transmitter level. Default level of 0 corresponds to –9.85 dBm. Transmit level = –(9.85 + XMTL) dBm. Range = –9.85 to –48.	0x0000
U53	0x0053	MOD2	This is a bit-mapped register.	0x0000
U62	0x0062	DAAC1	This is a bit-mapped register.	0x0804
U65	0x0065	DAAC4	This is a bit-mapped register.	0x00E0
U66	0x0066	DAAC5	This is a bit-mapped register.	0x0040
U67	0x0067	ITC1	This is a bit-mapped register.	0x0008
U68	0x0068	ITC2	This is a bit-mapped register.	0x0000
U69	0x0069	ITC3	This is a bit-mapped register.	0x0000

Table 21. U-Register Description (Continued)

Register	Address (Hex)	Name	Description	Default
U6A	0x006A	ITC4	This is a bit-mapped register.	n/a
U6E	0x006E	CK1	This is a bit-mapped register.	0x1F20
U70	0x0070	IO0	This is a bit-mapped register.	0x2B00
U71	0x0071	IO1	This is a bit-mapped register.	0x0000
U76	0x0076	GEN1	This is a bit-mapped register.	0x3240
U77	0x0077	GEN2	This is a bit-mapped register.	0x401E
U78	0x0078	GEN3	This is a bit-mapped register.	0x0000
U79	0x0079	GEN4	This is a bit-mapped register.	0x0000
U7A	0x007A	GENA	This is a bit-mapped register.	0x0000

Table 22. Bit-Mapped U-Register Summary

Reg.	Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
U4D	MOD1		TOCT		NHFP	NHFD	CLPD	CCAD	FTP	SPDM		GT18	GT55	CTE		LLC	
U53	MOD2	REV															
U62	DAAC1														FOH	DL	
U65	DAAC4	PWM	PWMG	PDN									PDL				
U66	DAAC5										FDT						
U67	ITC1									OFF	OHS	ACT		DCT		RZ	RT
U68	ITC2												LIM		BTE	ROV	BTD
U69	ITC3										DIAL	FJM	VOL	FLVM	MODE		
U6A	ITC4														OVL		
U6E	CK1				R1								RST		SDSP	N1	
U70	IO0	HES		TES	CIDM	OCDM	PPDM	RIM	DCDM				CID	OCD	PPD	RI	DCD
U76	GEN1	OHSR							FACL	DCL			ACL				
U77	GEN2	IST				HOI		AOC	OHT								
U78	GEN3	IB								IS							
U79	GEN4												LVCS				
U7A	GENA									DOP					V22HD	HDLC	FAST
U7C	GENC												RIGPO				RIG-POEN
U7D	GEND						LLV	AUSDC									FDP

Bit-Mapped U-Register Detail (defaults in bold)

U4D MOD1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		TOCT		NHFP	NHFD	CLPD	CCAD	FTP	SPDM		GT18	GT55	CTE		LLC	
Type	R/W			R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W		R/W	

Reset settings = 0x0000

Bit	Name	Function
15	Reserved	Read returns zero.
14	TOCT	**Turn Off Calling Tone.** **0 = Disable.** 1 = Enable.
13	Reserved	Read returns zero.
12	NHFP	**No Hook Flash Pulse.** **0 = Disable.** 1 = Enable.
11	NHFD	**No Hook Flash Dial.** **0 = Disable.** 1 = Enable.
10	CLPD	**Check Loop Current Before Dialing.** **0 = Ignore.** 1 = Check.
9	CCAD	**Check Carrier at Data (confirm carrier before entering Data mode).** **0 = Disable.** 1 = Enable.
8	FTP	**Force Tone or Pulse.** **0 = Disable.** 1 = Enable.
7	SPDM	**Skip Pulse Dial Modifier.** **0 = No.** 1 = Yes.
6	Reserved	Read returns zero.
5	GT18	**1800 Hz Guard Tone Enable.** **0 = Disable.** 1 = Enable.
4	GT55	**550 Hz Guard Tone Enable.** **0 = Disable.** 1 = Enable.
3	CTE	**Calling Tone Enable.** **0 = Disable.** 1 = Enable.
2	Reserved	Read returns zero.

Bit	Name	Function
1	LLC	**Low Loop Current Detect (required for CTR21).** **0 = Disabled.** 1 = Enabled.
0	Reserved	Read returns zero.

U53 MOD2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REV															
Type	R/W															

Reset settings = 0x0000

Bit	Name	Function
15	REV	**V.23 Reversing.** **0 = Disable.** 1 = Enable.
14:0	Reserved	Read returns zero.

U62 DAAC1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	1	0	0	0	0	0	0	0	0	FOH	DL	0
Type														R/W	R/W	

Reset settings = 0x0804

Bit	Name	Function
15:12	Reserved	Must be set 0.
11	Reserved	Must be set 1.
10:3	Reserved	Must be set 0.
2	FOH	**Fast Off-Hook.** 0 = Automatic Calibration Time set to 426 ms **1 = Automatic Calibration Time set to 106 ms**
1	DL	**Isolation Digital Loopback (see the AT&T commands).** **0 = Loopback occurs beyond the ISOcap interface, out to and including the analog hybrid circuit.** 1 = Enables digital loopback mode across isolation barrier only.
0	Reserved	Must be set 0.

U65 DAAC4

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PWM	PWMG	PDN									PDL				
Type	R/W	R/W	R/W									R/W				

Reset settings = 0x00E0

Bit	Name	Function
15	PWM	**PWM Mode.** **0 = Normal. Classic PWM output waveform.** 1 = Scrambled mode. Low distortion mode if used with output circuit shown in Figure 5 on page 14.
14	PWMG	**PWM Gain.** **0 = No gain.** 1 = 6 dB gain applied to AOUT.
13	PDN	**Powerdown.** Completely powerdown the Si2456/33/14 and Si3015. Once set to 1, the Si2456/33/14 must be reset to power on. **0 = Normal.** 1 = Powerdown.
12:8	Reserved	Read returns zero.
7:5	Reserved	Must not change in a read-modify-write.
4	PDL*	**Powerdown Line-Side Chip.** **0 = Normal operation.** 1 = Places the Si3015 in powerdown mode.
3:0	Reserved	Must not change in a read-modify-write.
***Note:** Typically used only for board-level debug.		

U66 DAAC5

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name										FDT						
Type	R															

Reset settings = 0x0040

Bit	Name	Function
15:7	Reserved	Read returns zero.
6	FDT*	**Frame Detect.** 0 = Indicates ISOcap has not established frame lock. 1 = Indicates ISOcap frame lock has been established.
5:4	Reserved	Read returns zero.
3:0	Reserved	Do not modify.
***Note:** Typically used only for board-level debug.		

U67 ITC1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name									OFF	OHS	ACT		DCT		RZ	RT
Type									R/W	R/W	R/W		R/W		R/W	R/W

Reset settings = 0x0008

Bit	Name	Function
15:8	Reserved	Read returns zero.
7	OFF	**DC Termination Off.** **0 = Normal operation.** The OFF bit must always be set to 0 when on-hook. 1 = DC termination disabled and the device presents an 800 Ω dc impedance to the line, which is used to enhance operation with an off-hook parallel phone.
6	OHS[1,2]	**On-Hook Speed.** **0 = The Si2456/33/14 will execute a fast on-hook.** 1 = The Si2456/33/14 will execute a slow controlled on-hook.
5	ACT[1,2]	**AC Termination Select.** **0 = Selects the real impedance.** 1 = Selects the complex impedance.
4	Reserved	Read returns zero.
3:2	DCT[1,2]	**DC Termination Select.** 00 = Low Voltage mode (Transmit level = –13.85 dBm). 01 = Japan mode (Transmit level = –11.85 dBm). **10 = FCC mode. Standard voltage mode (Transmit level = –9.85 dBm).** 11 = CTR21 mode. Current limiting mode (Transmit level = –9.85 dBm).
1	RZ[1,2]	**Ringer Impedance.** **0 = Maximum (high) ringer impedance.** 1 = Synthesize ringer impedance. C15, R14, Z2, and Z3 must not be installed when setting this bit. See "Ringer Impedance" on page 69.
0	RT[1,2]	**Ringer Threshold Select.** Used to satisfy country requirements on ring detection. Signals below the lower level does not generate a ring detection; signals above the upper level are guaranteed to generate a ring detection. **0 = 11 to 22 VRMS.** 1 = 17 to 33 V_{RMS}.

Notes:
1. See Table 19 on page 39
2. See "Appendix A—DAA Operation" on page 67

U68 ITC2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name												LIM		BTE	ROV	BTD
Type												R/W		R/W	R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15:8	Reserved	Read returns zero.
7:5	Reserved	Do not modify.
4	LIM[1,2]	**Current Limit.** **0 = All other modes.** 1 = CTR21 mode.
3	Reserved	Do not modify.
2	BTE[2]	**Billing Tone Protect Enable.** **0 = Disabled.** 1 = Enabled. When set, the DAA responds automatically to a collapse of the line-derived power supply during a billing tone event. When off-hook, if BTE = 1 and BTD goes high, the dc termination is released (800 Ω presented to line). If BTE and RIM (U70, bit 9) are set, an RI (U70, bit 1) interrupt also occurs when BTD goes high.
1	ROV[2]	**Receive Overload.** The bit is set when the receive input (i.e., receive pin goes below ground) has an excessive input level. This bit is cleared by writing a 0 to this location. **0 = Normal receive input level.** 1 = Excessive receive input level.
0	BTD[2]	**Billing Tone Detected.** This bit is set if a billing tone is detected. This bit is cleared by writing a 0 to this location. 0 = No billing tone. 1 = Billing tone detected.

Notes:
1. See Table 19 on page 39
2. See "Appendix A—DAA Operation" on page 67

U69 ITC3

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name										DIAL	FJM	VOL	FLVM	MODE		
Type										R/W	R/W	R/W				

Reset settings = 0x0000

Bit	Name	Function
15:8	Reserved	Read returns zero.
7	Reserved	Do not modify. Must be set to zero.
6	DIAL	**DTMF Dialing Mode.** This bit should be set during DTMF dialing in CTR21 mode if LVCS < 12. **0 = Normal operation.** 1 = Increase headroom for DTMF dialing.
5	FJM	**Force Japan DC Termination Mode.** **0 = Normal Gain.** 1 = When DCT = 2 (FCC mode), setting this bit forces Japan dc termination mode while allowing for a transmit level of –1 dBm. See "DTMF Dialing" on page 69.
4	VOL[1,2]	**Line Voltage Adjust.** When set, this bit adjusts the TIP-RING line voltage. Lowering this voltage improves margin in low voltage countries. Raising this voltage may improve large signal distortion performance. **0 = Normal operation.** 1 = Lower DCT voltage.
3	FLVM[1,2]	**Force Low Voltage Mode.** When DCT (U67, bits 3:2) = 10 (FCC mode), setting FLVM forces the Low Voltage mode (see DCT = 00) while allowing for a transmit level of –1 dBm. **0 = Disable.** 1 = Enable.
2	MODE	**Mode.** MODE = 1_b enables on-hook line monitor. MODE must be disabled (MODE = 0_b) before the modem can go off-hook, dial, or answer a call. **0 = Disable.** 1 = Enable.
1:0	Reserved	Do not modify.

Notes:
1. See Table 19 on page 39
2. See "Appendix A—DAA Operation" on page 67

U6A ITC4

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name														OVL		
Type														R		

Reset settings = N/A

Bit	Name	Function
15:3	Reserved	Read returns zero.
2	OVL*	**Overload Detected.** This bit has the same function as ROV, but clears itself after the overload has been removed. See "Billing Tone Detection" on page 69. This bit is not affected by the BTE bit.
1:0	Reserved	Do not modify.
***Note:** See "Appendix A—DAA Operation" on page 67.		

U6E CK1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name				R1								RST		SDSP	N1	
Type	R/W											R/W		R/W	R/W	

Reset settings = 0x1F00

Bit	Name	Function
15:13	Reserved	Do not modify.
12:8	R1*	**R1** **CLKOUT Divider** 0 CLKOUT off. R1 R1 + 1 (default R1 = 31; 2.4576 MHz). R1 = 31 required for proper codec interface operation.
7:5	Reserved	Read returns zero.
4	RST	**Hardware Reset.** This bit functions exactly as the digital inverse of the $\overline{\text{RESET}}$ pin. Writing this bit to 1 causes a hardware reset.
3	Reserved	Read returns zero.
2	SDSP*	**Slow DSP.** **0 = No divider.** 1 = Extra divide-by-8 on DSP clock.
1:0	N1*	**N1** **DSP_CLK Divider** **0** **2** 1 2.5 2 3 3 4
Note: See Figure 6 on page 22.		

U70 IO0

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	HES		TES	CIDM	OCDM	PPDM	RIM	DCDM				CID	OCD	PPD	RI	DCD
Type	R/W		R/W	R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W	R/W

Reset settings = 0x2700

Bit	Name	Function
15	HES	**Hardware Escape Pin.** **0 = Disable.** 1 = Enable.
14	Reserved	Read returns zero.
13	TES	**Enable "+++" Escape.** 0 = Disable. **1 = Enable.**
12	CIDM	**Caller ID Mask.** **0 = Change in CID will not affect INT.** 1 = A low to high transition in CID activates $\overline{\text{INT}}$.
11	OCDM	**Overcurrent Detect Mask.** **0 = Change in OCD does not affect INT.** ("X" result code is not generated in Command mode.) 1 = A low to high transition in OCD will activate INT. ("X" result code is generated in Command mode.)
10	PPDM	**Parallel Phone Detect Mask.** 0 = Change in PPD does not affect $\overline{\text{INT}}$. **1 = A low to high transition in PPD will activate INT.**
9	RIM	**Ring Indicator.** 0 = Change in RI does not affect $\overline{\text{INT}}$. **1 = A low to high transition in RI activates INT.**
8	DCDM	**Data Carrier Detect Mask.** 0 = Change in DCD does not affect $\overline{\text{INT}}$. **1 = A high to low transition in DCD (U70, bit 0), which indicates loss of carrier, activates INT.**
7	Reserved	Must be set to zero.
6:5	Reserved	Read returns zero.
4	CID	**Caller ID (sticky).** Caller ID preamble has been detected; data will soon follow. Clears on :I read.
3	OCD	**Overcurrent Detect (sticky).** Overcurrent condition has occurred. Clears on :I read.
2	PPD	**Parallel Phone Detect (sticky).** Parallel phone detected since last off-hook event. Clears on :I read.

Bit	Name	Function
1	RI	**Ring Indicator.** Active high bit when the Si2456/33/14 is on-hook, indicates ring event has occurred. Clears on :I read.
0	DCD	**Data Carrier Detect (status).** Active high bit indicates carrier detected (equivalent to inverse of $\overline{\text{DCD}}$ pin).

U76 GEN1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OHSR							FACL	DCL			ACL				
Type	R/W							R/W				R/W				

Reset settings = 0x3240

Bit	Name	Function
15:9	OHSR	**Off-Hook Sample Rate (40 ms units)** Sets the sample rate for the off-hook intrusion algorithms (1 second default).
8	FACL	**Force ACL.** **0 = While off-hook, ACL is automatically updated with LVCS.** 1 = While off-hook, ACL does not change from the value written to it while on-hook.
7:5	DCL	**Differential Current Level (3 mA units).** Sets the differential level between ACL and LVCS that will trigger an off-hook PPD interrupt (default = 2).
4:0	ACL	**Absolute Current Level (3 mA units, see Figure 7 on page 37).** ACL represents the value of LVCS current when the ISOmodem is off-hook and all parallel phones are on-hook. If ACL = 0, then it is ignored by the off-hook intrusion algorithm.The ISOmodem will also write ACL with the contents of LVCS before an intrusion and before going on-hook (default = 0).

U77 GEN2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IST				HOI		AOC	OHT								
Type	R/W				R/W		R/W	R/W								

Reset settings = 0x401E

Bit	Name	Function
15:12	IST	**Intrusion Settling Time (250 ms units).** Delay between when the ISOmodem goes off-hook and the off-hook intrusion algorithm begins. Default is 1 second.
11	HOI	**Hang-Up On Intrusion.** **0 = ISOmodem will not automatically hang up when an off-hook PPD interrupt occurs.** 1 = ISOmodem automatically hangs up on a PPD interrupt.
10	Reserved	Read returns zero.
9	AOC	**Overcurrent Protection.** Enable Overcurrent protection. **0 = Disable.** 1 = Enable. **Note:** AOC may falsely detect an overcurrent condition in the presence of line reversals or other transients. Therefore, this feature should not be used in applications or locations (such as Japan) where line reversals are common or may be expected.
8:0	OHT	**Off-Hook Time (1 ms units).** Time before LVCS is checked for overcurrent condition after going off-hook (30 ms default).

U78 GEN3

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IB								IS							
Type	R/W								R/W							

Reset settings = 0x0000

Bit	Name	Function
15:14	IB	**Intrusion Blocking** Defines the method used to block the off-hook intrusion algorithm from operation after dialing has begun. **0 = No intrusion blocking.** 1 = Intrusion disabled from start of dial to end of dial. 2 = Intrusion disabled from start of dial to IS register time-out. 3 = Intrusion disabled from start of dial to connect (“CONNECT XXX”, “NO DIALTONE”, or “NO CARRIER”).
13:8	Reserved	Read returns zero.
7:0	IS	**Intrusion Suspend (500 ms units).** When IB = 2, this register sets the length of time from when dialing begins that the off-hook intrusion algorithm is blocked (suspended) (default = 00000000_b).

U79 GEN4

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name												LVCS				
Type	R															

Reset settings = 0x0000

Bit	Name	Function
15:5	Reserved	Read returns zero.
4:0	LVCS	**Line Voltage Current Sense.** Represents either the line voltage, loop current, or on-hook line monitor depending on the state of the MODE, OFHK, and ONHM bits. **On-Hook Voltage Monitor (2.75 V/bit ±20%) (see Figure 7 on page 37).** 00000 = No line connected. 00001 = Minimum line voltage (V_{MIN} = 3.0 V ± 0.5 V). 11111 = Maximum line voltage (87 V ± 20%). The line voltage monitor full scale may be modified by changing R5 as follows: $V_{MAX} = V_{MIN} + 4.2\ (10M + R5 + 1.6k)/(R5 + 1.6k)/5$ U69[2] (MODE) must be set to 1_b before reading LVCS while the ISOmodem is on-hook. See MODE on page 54. U69[2] (MODE) must be disabled (MODE = 0_b) before the ISOmodem can go off-hook, dial, or answer a call. **Off-Hook Loop Current Monitor (3 mA/bit) (see Figure 8 on page 38).** 00000 = No loop current. 00001 = Minimum loop current. 11110 = Maximum loop current. 11111 = Loop current is excessive (overload). Overload > 140 mA in all modes except CTR21 Overload > 54 mA in CTR21 mode

U7A GENA

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name									DOP					V22HD	HDLC	FAST
Type																

Reset settings = 0x0000

Bit	Name	Function
15:8	Reserved	Read returns to zero.
7	DOP	**Dial or Pulse.** **0 = Normal ATDTW operation** 1 = Use ATDTW for Pulse/Tone Dial Detection (see also ATDW command)
6:3	Reserved	Read returns to zero.
2	V22HD	**V.22bis Synchronous Mode.*** **0 = Normal asynchronous mode.** 1 = Transparent HDLC mode.
1	HDLC	**Synchronous Mode.*** **0 = Normal asynchronous mode.** 1 = Transparent HDLC mode.
0	FAST	**Fast Connect.*** **0 = Normal modem handshake timing per ITU/Bellcore standards.** 1 = Fast connect modem handshake timing.
***Note:** When V22HD, HDLC, or FAST bits are set, \N0 (wire mode) must be used.		

U7C GENC

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name												RIGPO				RIGPOEN
Type												R				R/W

Reset settings = 0x0000

Bit	Name	Function
15:5	Reserved	Reads returns to zero.
4	RIGPO	**RI** RI (pin 15), follows this bit when RIGPIOEN = 1_b.
3:1	Reserved	Reads returns to zero.
0	RIGPOEN	**0 = RI indicates valid ring signal. (Normal ring-indicator mode)** 1 = RI (Pin 15) can be used as a general purpose output and follows U7C[4] (RIGPO).

U7D GENC

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name						LLV	AUSDC									FDP
Type						R/W	R/W									

Reset settings = 0x0000

Bit	Name	Function
15:11	Reserved	Reads returns to zero.
10	LLV	**0 = Normal operation.** 1 = Enables an optional algorithm for countries, such as Japan and Malaysia, with low loop voltage. Also set U67[3:2] (DCT) = 00_b, U69[4] VOL = 1_b, and U52 = 0x0002 before going off-hook. When the modem goes off-hook, it samples LVCS and changes DCT and VOL as necessary to maximize transmit levels and optimize distortion.
9	AUSDC	**0 = Normal operation.** 1 = Causes the modem to go off-hook in Japan mode and then revert to FCC mode after 500 ms. This allows the modem to meet the Australian line seizure requirements while allowing the maximum transmit power (optional for Australia and when DCT = 01_b).
0	FDP	**FSK Data Processing.** **0 = FSK data processing stops when carrier is lost.** 1 = FSK data processing continued for 2 bytes after carrier is lost.

Parallel Interface Registers

Parallel Interface 0 (0x00)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TX/RX							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	TX/RX	**Parallel Interface Transmit/Receive.** This register functions similarly to the serial port TX pin on writes to the parallel port, and similarly to the serial port RX pin on reads from the parallel port.

Parallel Interface 1 (0x01)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXF	TXE	REM	INTM	INT	ESC	$\overline{RTS}$	$\overline{CTS}$
Type	R	R	R	R/W	R	R/W	R/W	R

Reset settings = 0110_0011

Bit	Name	Function
7	RXF	**Receive FIFO Almost Full (status).** 0 = Receive FIFO (12 deep) contains three or more empty locations (RXF ≤ 9). 1 = Receive FIFO contains two or less empty locations (RXF ≥ 10). Requires servicing within xx ms to avoid overflow.
6	TXE	**Transmit FIFO Almost Empty (status).** 0 = Transmit FIFO (14 deep) contains three or more characters (TXF ≥ 3). 1 = Transmit FIFO contains two or less characters (TXF ≤ 2). Requires servicing within xx ms to avoid underflow.
5	REM	**Receive FIFO Empty.** 0 = Receive FIFO has valid data. 1 = Receive FIFO empty.
4	INTM	**Interrupt Mask.** 0 = In parallel mode, the $\overline{INT}$ pin is triggered by a rising edge on RXF or TXE only (default). 1 = In parallel mode, the $\overline{INT}$ pin is triggered by a rising edge on RXF, TXE, or INT.
3	INT	**Interrupt.** 0 = No interrupt has occurred. 1 = Indicates that an interrupt (CID, OCD, PPD, RI, or DCD from U70) has occurred. This bit is cleared via the AT:I command.
2	ESC	**Escape.** Operation of this bit in parallel mode is functionally equivalent to the ESC pin in serial mode.
1	$\overline{RTS}$	**Request-to-Send.** Operation of this bit in parallel mode is functionally equivalent to the $\overline{RTS}$ pin in serial mode. Use of the $\overline{CTS}$ and $\overline{RTS}$ bits (as opposed to the TXE and RXF bits) allows the flow control between the host and the ISOmodem to operate 1 byte at a time, rather than in blocks.
0	$\overline{CTS}$	**Clear-to-Send.** Operation of this bit in parallel mode is functionally equivalent to the $\overline{CTS}$ pin in serial mode. Use of the $\overline{CTS}$ and $\overline{RTS}$ bits (as opposed to the TXE and RXF bits) allows the flow control between the host and the ISOmodem to operate 1 byte at a time, rather than in blocks.

APPENDIX A—DAA OPERATION

Introduction

This appendix describes the detailed functionality of the integrated DAA included in the Si2456/33/14//Si3015 chipset.

DAA Isolation Barrier

The Si2456/33/14 chipset consists of the Si3015 line side device and the Si2456/33/14 modem device. The Si2456/33/14 achieves an isolation barrier through a low-cost high-voltage capacitor in conjunction with Silicon Laboratories' proprietary ISOcap signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common mode interference, or noise coupling. As shown in the "Typical Application Circuit" on page 11, the C1, C4, C24, and C25 capacitors isolate the Si2456/33/14 (DSP-side) from the Si3015 (line-side). All transmit, receive, and control data are communicated through this barrier.

Emissions/Immunity

The Si2456/33/14 chipset and recommended DAA schematic are fully-compliant with and pass all international electromagnetic emissions and conducted immunity tests (includes FCC part 15,68; EN50082-1). Careful attention to the "Bill of Materials: Si2456/33/14 Chipset" on page 12, "Typical Application Circuit" schematic on page 11, and layout guidelines ensure compliance with these international standards. In designs with difficult layout constraints, the addition of the C22 and C30 capacitors to the C24 and C25 recommended capacitors may improve modem performance on emissions and conducted immunity. For such designs, a population option for C22 and C30 may allow additional flexibility for optimization after the printed circuit board has been completed.

EN55022 and CISPR-22 Compliance

Pending ratification in July 2001 of the CISPR-22 standard, effective August 1, 2001, compliance to the EN55022:1998 standard is necessary to conform to the European Union's EMC Directive and display the CE mark on designs intended for sale in the European Union. However, EN55022 and CISPR-22 compliance is currently under review. Consequently, as of June 2001, compliance requirements may change, and the compliance date may be extended beyond August 2001. Additionally, some countries may require compliance to the CISPR-22 specification. The "Typical Application Circuit" schematic on page 11 and global "Bill of Materials: Si2456/33/14 Chipset" on page 12 contained in this data sheet are designed to be compliant to these standards. It should be noted that L1, L2, R31, R32, C38, and C39 are only necessary for those products intended for sale in the European Union or any countries that require CISPR-22 compliance. If this is not the target market, L1 and L2 can be replaced with 0 Ω resistors, and R31, R32, C38, and C39 need not be populated.

While this population option achieves EN55022 and CISPR-22 compliance, there are several system-dependent and country-dependent issues worth considering. The first relates to the direct current resistance (DCR) of the inductors. If the selected inductors have a DCR of less than 3 Ω each, countries that require 300 Ω or less of dc resistance at TIP and RING with 20 mA of loop current can be satisfied with the Japan DC termination mode (DCT = 01). If the selected inductors have a DCR of greater than 3 Ω but less than 8 Ω each, low voltage dc termination mode (DCT = 00) must be used to satisfy the above requirement. In either case, Silicon Laboratories strongly recommends that users of the ISOmodem adhere to the section, "DC Termination" on page 68, for their dc termination requirements.

The second consideration relates to the power supply of the target system. The recommended values for L1, L2, R31, R32, C38, and C39 assume that the target system provides a direct current connection between the target system's reference ground (Si2456/33/14 GND) and an external ground (often the third prong of a power plug). If there is no direct connection between the reference ground and external ground, smaller inductor values are possible. It should be understood that this consideration is system-dependent, and the impedance between the system ground and the external ground in the range of 500 kHz and 10 MHz should be well known. Please contact a Silicon Laboratories technical representative if you need assistance in analyzing or testing your system for this consideration.

DC Termination

The Si2456/33/14 has four programmable dc termination modes that are selected with DCT (U67, bits 3:2).

FCC mode (DCT = 10), shown in Figure 9, is the default dc termination mode and supports a transmit full-scale level of –1 dBm at TIP and RING. This mode meets FCC requirements in addition to the requirements of many other countries.

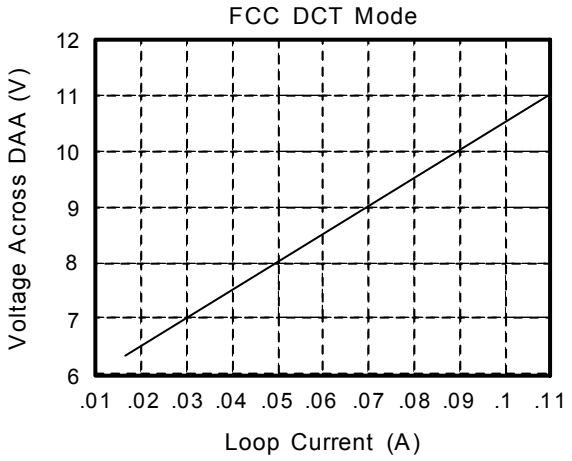


Figure 9. FCC Mode I/V Characteristics

CTR21 mode DCT = 11, shown in Figure 10, provides current limiting while maintaining a transmit full-scale level of –1 dBm at TIP and RING. The dc termination current limits before reaching 60 mA.

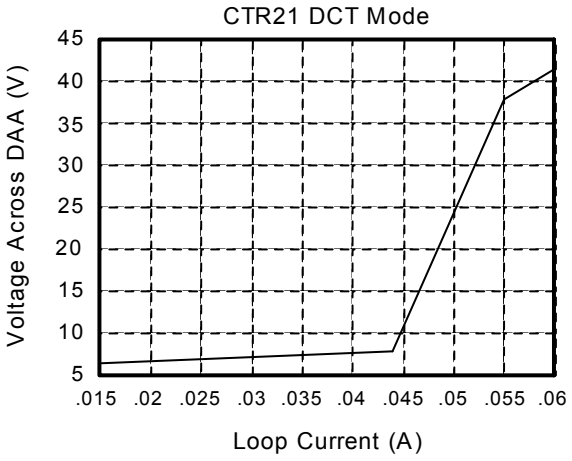


Figure 10. CTR21 Mode I/V Characteristics

Japan mode DCT = 01, shown in Figure 11, is a lower voltage mode and supports a transmit full-scale level of –2.71 dBm. Higher transmit levels for DTMF dialing are also supported. See "DTMF Dialing" on page 69. The low voltage requirement is dictated by countries, such as Japan and Malaysia.

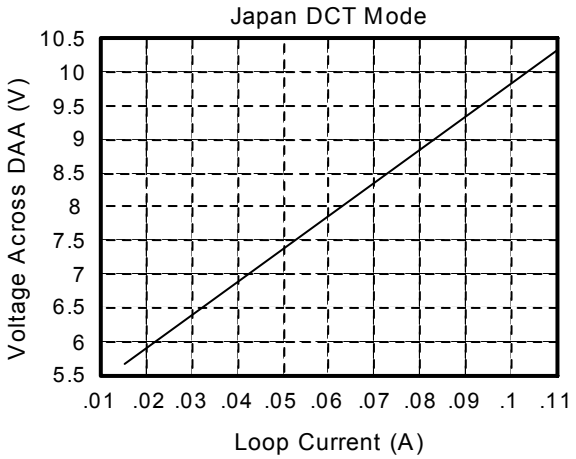


Figure 11. Japan Mode I/V Characteristics

Low Voltage mode (DCT = 00), shown in Figure 12, is the lowest line voltage mode supported on the Si2456/33/14 with a transmit full-scale level of –5 dBm. Higher transmit levels for DTMF dialing are also supported. See "DTMF Dialing" on page 69. This low-voltage mode is offered for situations that require very low line voltage operation. It is important to note that this mode should only be used when necessary because the dynamic range is significantly reduced, and, thus, the ISOmodem is not able to transmit or receive large signals without clipping them.

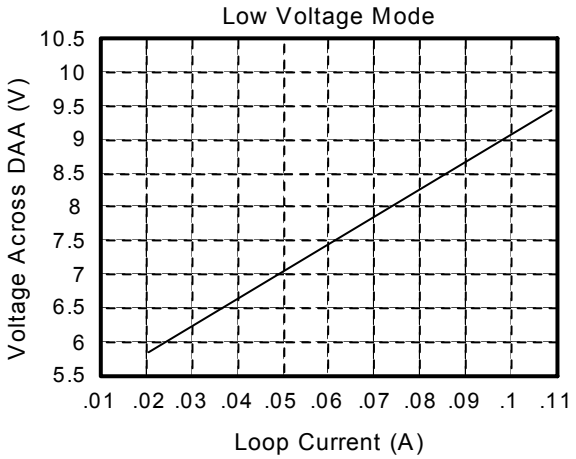


Figure 12. Low Voltage Mode I/V Characteristics

AC Termination

The Si2456/33/14 has two ac Termination impedances that are selected with the ACT bit (U67, bit 5).

ACT = 0 is a real nominal 600 Ω termination, which satisfies the impedance requirements of FCC part 68, JATE, and other countries. This real impedance is set by circuitry internal to the Si3015 as well as the resistor R2 connected to the REXT pin.

ACT = 1 is a complex impedance, which satisfies the impedance requirements of Australia, New Zealand, South Africa, CTR21, and some European NET4 countries, such as the UK and Germany. This complex impedance is set by circuitry internal to the Si3015 as well as the complex network formed by R12, R13, and C14 connected to the REXT2 pin.

Ringer Impedance

The ring detector in a typical DAA is ac-coupled to the line with a large 1 μF, 250 V decoupling capacitor. The ring detector on the Si2456/33/14 is also capacitively-coupled to the line, but it is designed to use smaller, less expensive 1.8 nF capacitors. Inherently, this network produces a high ringer impedance to the line of approximately 800–900 kΩ. This value is acceptable for most countries including FCC and CTR21.

Several countries including the Czech Republic, Poland, South Africa, and South Korea require a maximum ringer impedance. For Poland, South Africa, and South Korea, the maximum ringer impedance specification can be met with an internally-synthesized impedance by setting the RZ bit (U67, bit 1).

Pulse Dialing

Pulse dialing is accomplished by going off- and on-hook to generate make and break pulses. The nominal rate is 10 pulses per second. Some countries have very tight specifications for pulse fidelity including make and break times, make resistance, and rise and fall times. In a traditional solid-state dc holding circuit, there are a number of issues in meeting these requirements.

The Si2456/33/14 dc holding circuit has active control of the on-hook and off-hook transients to maintain pulse dialing fidelity.

Spark quenching requirements in countries, such as Italy, the Netherlands, South Africa, and Australia deal with the on-hook transition during pulse dialing. These tests provide an inductive dc feed resulting in a large voltage spike. This spike is caused by the line inductance and the sudden decrease in current through the loop when going on-hook. The traditional way of dealing with this problem is to put a parallel RC shunt across the hookswitch relay. The capacitor is large (~1 μF, 250 V) and expensive. In the Si2456/33/14, the OHS bit (U67, bit 6) can be used to slowly ramp down the loop current to pass these tests without requiring additional components.

DTMF Dialing

In CTR21 dc termination mode, the DIAL bit (U69, bit 6) should be set during DTMF dialing if LVCS ≤ 12. Setting this bit increases headroom for large signals. This bit should only be used during dialing and if LVCS < 11.

In Japan dc termination mode (DCT [U67, bits 3:2] = 01), the ISOmodem attenuates the transmit output by 1.7 dB to meet headroom requirements. Similarly, in Low Voltage mode (DCT = 00), the ISOmodem attenuates the transmit output by 4 dB. However, when DTMF dialing is desired in these modes, this attenuation must be removed. This is achieved by entering the FCC dc termination mode and setting the FJM bit (U69, bit 5). When in the FCC dc termination modes, these bits enable the respective lower loop current termination modes without the associated transmit attenuation. Increased distortion may be observed, which is acceptable during DTMF dialing. After DTMF dialing is complete, the attenuation should be enabled by returning to either the Japan dc termination mode (DCT = 01) or the Low Voltage termination mode (DCT = 00). The FJM and the FLVM bits have no effect in any other termination mode other than the FCC dc termination mode.

Billing Tone Detection

“Billing tones” or “metering pulses” generated by the central office can cause modem connection difficulties. The billing tone is typically a 12 kHz or 16 kHz signal and is sometimes used in Germany, Switzerland, and South Africa. Depending on line conditions, the billing tone may be large enough to cause major modem errors. The Si2456/33/14 chipset can provide feedback when a billing tone occurs and when it ends.

Billing tone detection is enabled by setting the BTE bit (U68, bit 2). Billing tones less than 1.1 V_{PK} on the line are filtered out by the low-pass digital filter on the Si2456/33/14. The ROV bit (U68, bit 1) is set when a line signal is greater than 1.1 V_{PK} indicating a receive overload condition. The BTD bit is set when a line signal (billing tone) is large enough to excessively reduce the line-derived power supply of the line-side device (Si3015). When the BTD bit is set, the dc termination is changed to an 800 Ω dc impedance. This ensures minimum line voltage levels even in the presence of billing tones.

The OVL bit should be polled following billing tone detection. When the OVL bit returns to 0, indicating that

the billing tone has passed, the BTE bit should be written to 0 to return the dc termination to its original state. It takes approximately one second to return to normal dc operating conditions. The BTD and ROV bits are sticky, and they must be written to 0 to be reset. After the BTE, ROV, and BTD bits are all cleared, the BTE bit can be set to re-enable billing tone detection.

Certain line events, such as an off-hook event on a parallel phone or a polarity reversal, may trigger the ROV or the BTD bits, after which the billing tone detector must be reset. Look for multiple events before qualifying if billing tones are actually present.

Although the DAA remains off-hook during a billing tone event, the received data from the line is corrupted (or a modem disconnect or retrain may occur) in the presence of large billing tones. To receive data through a billing tone, an external LC filter must be added. A modem manufacturer can provide this filter to users in the form of a dongle that connects on the phone line before the DAA. This keeps the manufacturer from having to include a costly LC filter internal to the modem when it may only be necessary to support a few countries/ customers.

Alternatively, when a billing tone is detected, the host software may notify the user that a billing tone has occurred. This notification can be used to prompt the user to contact the telephone company and have the billing tones disabled or to purchase an external LC filter.

Billing Tone Filter (Optional)

To operate without degradation during billing tones in Germany, Switzerland, and South Africa, an external LC notch filter is required. (The Si3015 can remain off-hook during a billing tone event, but modem data is lost (or a modem disconnect or retrain may occur) in the presence of large billing tone signals.) The notch filter design requires two notches, one at 12 kHz and one at 16 kHz. Because these components are expensive and few countries supply billing tone support, this filter is typically placed in an external dongle or added as a population option for these countries. Figure 13 shows an example billing tone filter.

L3 must carry the entire loop current. The series resistance of the inductors is important to achieve a narrow and deep notch. This design has more than 25 dB of attenuation at 12 and 16 kHz.

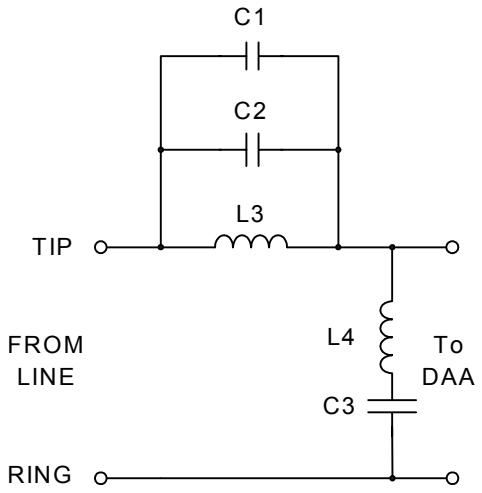


Figure 13. Billing Tone Filter

Table 23. Component Values—Optional Billing Tone Filters

Symbol	Value
C1,C2	0.027 μF, 50 V, ±10%
C3	0.01 μF, 250 V, ±10%
L3	3.3 mH, >120 mA, <10 Ω, ±10%
L4	10 mH, >40 mA, <10 Ω, ±10%

In-Circuit Testing

The Si2456/33/14's advanced design provides the system manufacturer with increased ability to determine system functionality during production line tests as well as support for end-user diagnostics. In addition to the local echo, a loopback mode exists allowing increased coverage of system components. For the loopback test mode, a line-side power source is required. While a standard phone line can be used, the test circuit in Figure 1 on page 6 is adequate.

To test communication with the Si2456/33/14 across the UART, the local echo may by used immediately after powerup.

The DSP loopback test mode tests the functionality and data transfer from the host to the Si2456/33/14 DSP filters out to the DAA and hybrid, back through the DSP, and back to the host.

This is the most comprehensive test and can be executed via the AT&T3 command. Once the AT command is issued, the ISOmodem goes off-hook and

runs the ITU V.54 loopback test 3 via the hybrid path in the DAA. After a connection is complete, the ISOmodem issues the “CONNECT xxx” response, and data is passed from the TXD pin, out the loop, and back to the RXD pin. This loopback test is a very complete line test. If desired, further testing is possible by connecting the ISOmodem to a dummy phone line and running any variety of functional tests.

A test of the ISOcap link only may be initiated by setting the DL bit (U62, bit 1) = 1 and issuing the AT&T3 command. This test implements the ITU V.54 loopback test 3 but eliminates the hybrid from the path. Finally, a digital-only loopback that does not involve the line-side device (Si3015) may be initiated via the AT&T2 command. This test is also the ITU V.54 loopback test 3.

The billing tone filter affects the ac termination and return loss. The current complex ac termination passes worldwide return loss specifications with and without the billing tone filter by at least 3 dB. The ac termination is optimized for frequency response and hybrid cancellation while having greater than 4 dB of margin with or without the dongle for South African, Australian, CTR21, German, and Swiss country-specific specifications.

APPENDIX B—UL1950 3RD EDITION

Introduction

Designs using the Si2456/33/14 pass all overcurrent and overvoltage tests for UL1950 3rd Edition compliance with a couple of considerations.

Figure 14 shows the designs that can pass the UL1950 overvoltage tests as well as electromagnetic emissions. The top schematic of Figure 14 shows the configuration in which the ferrite beads (FB1, FB2) are on the unprotected side of the sidactor (RV1). For this configuration, the current rating of the ferrite beads must be 6 A.

The bottom schematic of Figure 14 shows the configuration in which the ferrite beads (FB1, FB2) are on the protected side of the sidactor (RV1). For this design, the ferrite beads can be rated at 200 mA.

In a cost-optimized design, it is important to remember that compliance to UL1950 does not always require overvoltage tests. It is best to plan ahead and know which overvoltage test applies to your system. System-level elements in the construction, such as fire enclosure and spacing requirements, need to be considered during the design stages. Consult with your Professional Testing Agency during the design of the product to determine which tests apply to your system.

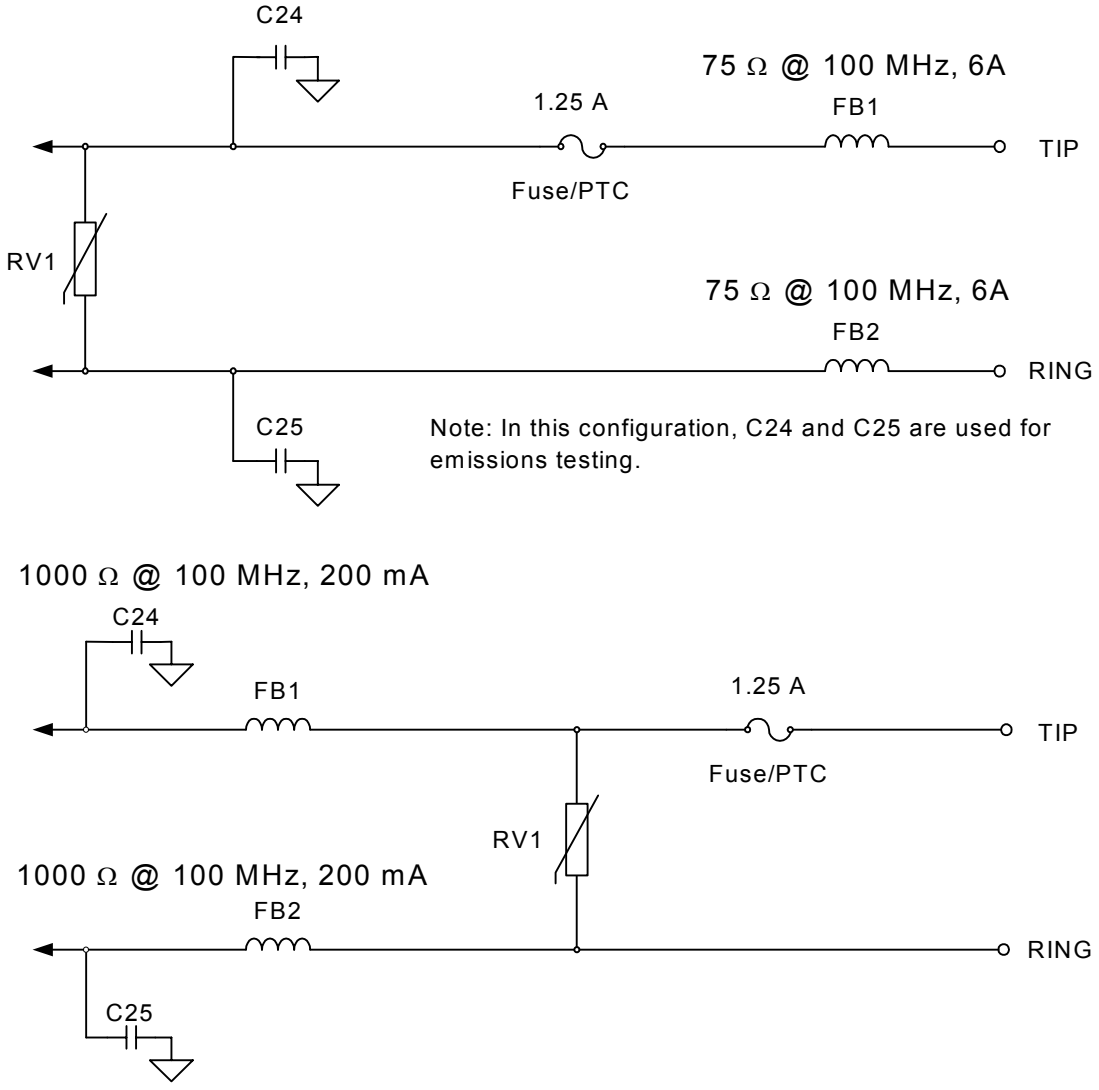


Figure 14. Circuits that Pass all UL1950 Overvoltage Tests

APPENDIX C—USER-ACCESS REGISTER SETTINGS

Introduction

This appendix outlines many of the user-access register settings required for international homologation.

Table 24. User-Access Register Values

Country	Dial Tone Call Progress Filter (Table 25)	Busy Tone Call Progress Filter (Table 25)	DTON (U15)	DTOF (U16)	BTON (U2C)	BTOF (U2D)
USA and UK like countries*, Australia, Austria, Cyprus, Czechoslovakia, Denmark, Greece, Hungary, Israel, Japan, Korea, Malaysia, New Zealand, Poland, Singapore, Slovakia, Taiwan	310/510	310/510	0x00A0	0x0070	0x00A0	0x0070
Norway	310/510	310/510	0x00A0	0x0070	0x00B0	0x0080
Switzerland, Finland	325/550	325/550	0x0580	0x0550	0x0580	0x0550
Sweden	325/550	325/550	0x0A80	0x0A50	0x0230	0x0200
The Netherlands	100/550	325/550	0x0300	0x02D0	0x0700	0x06D0
Germany, Slovenia	300/480	300/480	0x0150	0x0120	0x0070	0x0040
France	300/480	300/480	0x0190	0x0160	0x00AA	0x007A
Portugal	300/480	300/480	0x0258	0x0258	0x0258	0x0258
Belgium	400/440	400/440	0x0150	0x0120	0x0060	0x0030
Italy	400/440	400/440	0x0060	0x0030	0x0060	0x0030
Spain	320/630	320/630	0x0055	0x0035	0x0072	0x0042

***Note:** USA-like countries: Argentina, Bolivia, Brazil, Canada, Chile, Colombia, Costa Rica, India, Indonesia, Guatemala, Panama, Peru, Puerto Rico, Russia, Thailand, Trinidad, Uruguay, USA, and Venezuela.
UK-like countries: Bahrain, China, Ecuador, Egypt, Hong Kong, Ireland, Kuwait, Lebanon, Oman, Philippines, Saudi Arabia, South Africa, Turkey, UAE, and the UK.

Table 25. BPF Biquad Values

BPF Biquad Values	Stage 1	Stage 2	Stage 3	Stage 4	Output Scalar
310/510					
A0	0x0800	0x00A0	0x00A0	0x0400	—
B1	0x0000	0x6EF1	0x78B0	0x70D2	—
B2	0x0000	0xC4F4	0xC305	0xC830	—
A2	0x0000	0xC000	0x4000	0x4000	—
A1	0x0000	0x0000	0xB50A	0x80E2	—
K	—	—	—	—	0x0009
300/480					
A0	0x0800	0x01A0	0x01A0	0x03A0	—
B1	0x0000	0x6E79	0x7905	0x7061	—
B2	0x0000	0xC548	0xC311	0xC8EF	—
A2	0x0000	0xC000	0x4000	0x4000	—
A1	0x0000	0x0000	0xA7BE	0x8128	—
K	—	—	—	—	0x0009
320/630					
A0	0x0078	0x0210	0x0330	0x0330	—
B1	0x67EF	0x79E0	0x68C0	0x7235	—
B2	0xC4FA	0xC252	0xCB6C	0xC821	—
A2	0x4000	0x4000	0x4000	0x4000	—
A1	0x0214	0x8052	0xB1DC	0x815C	—
K	—	—	—	—	0x0008
325/550					
A0	0x0100	0x0600	0x0600	0x0600	—
B1	0x71CC	0x78EF	0x69B9	0x68F7	—
B2	0xC777	0xC245	0xC9E4	0xC451	—
A2	0x4000	0x4000	0x4000	0x4000	—
A1	0x81C2	0x806E	0xAFE9	0xFCA6	—
K	—	—	—	—	0x0009
100/550					
A0	0x0800	0x01C0	0x01C0	0x01C0	—
B1	0x7DAF	0x5629	0x7E3F	0x6151	—
B2	0xC1D5	0xCF51	0xC18A	0xDC9B	—
A2	0x4000	0xC000	0x4000	0x4000	—
A1	0x8000	0x0000	0xB96A	0x8019	—

Table 25. BPF Biquad Values (Continued)

BPF Biquad Values	Stage 1	Stage 2	Stage 3	Stage 4	Output Scalar
K	—	—	—	—	0x0005
400/440					
A0	0x0020	0x0200	0x0400	0x0040	—
B1	0x7448	0x7802	0x73D5	0x75A7	—
B2	0xC0F6	0xC0CB	0xC2A4	0xC26B	—
A2	0x4000	0x4000	0x4000	0x4000	—
A1	0x96AB	0x8359	0x8D93	0x85C1	—
K	—	—	—	—	0x0008

APPENDIX D—TYPICAL MODEM APPLICATIONS EXAMPLES

Introduction

Steps required to configure the Si2456/33/14 for modem operation under typical examples are outlined below. The ISOmodem has been designed to be easy to use and flexible. The Si2456/33/14 has many features and modes that add to the complexity of the device but are not required for a typical modem configuration. The following examples help the user quickly make a modem connection and begin evaluation of the Si2456/33/14 under various operational scenarios.

Example 1: V.90 in FCC Countries

1. Power on reset.
2. Set host UART to 19.2 kbps.
3. AT\T12 - set ISOmodem UART to 115.2 kbps.
4. Set host UART to 115.2 kbps.
5. ATDT15128675309<CR>
   Si2456 may echo:
   BUSY - busy tone detection
   NO CARRIER - no carrier detected
   CONNECT 56000 - connect at 56 kbps
6. Next byte after “CONNECT 56000" is modem data!

Example 2: 33600 bps in Norway

1. Power on reset.
2. Set host UART to 19.2 kbps.
3. AT\T12 - set ISOmodem UART to 115.2 kbps.
4. Set host UART to 115.2 kbps.
5. AT&H2 - limit Si2456 to V.34.
6. AT:U2C,00B0,0080 -Busy tone cadence set for Norway.
7. AT:U67,000C,0010,0004:U4D,0001 - DAA PTT settings for Norway.
8. ATDT15128675309<CR>
   Si2456/33 may echo:
   BUSY - busy tone detection
   NO CARRIER - no carrier detected
   CONNECT 33600 - connect at 33600 bps
9. Next byte after “CONNECT 33600" is modem data!

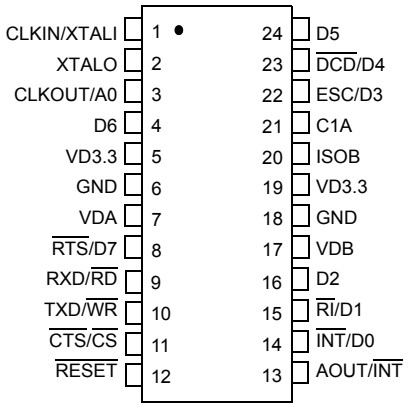
Example 3: V.22 in Australia with Parallel Phone Detection

1. Power on reset.
2. Set host UART to 19.2 kbps.
3. AT&H7 - limit Si2456/33/14 to V.22 only.
4. AT:U67,0064 - DAA PTT settings for Australia.
5. AT:U70,2400 - Enable off-hook intrusion interrupt.
6. AT:R79 - Check for phone in-use before dial.
7. ATDT15128675309<CR>
   Si2456/33/14 may echo:
   BUSY - busy tone detection
   NO CARRIER - no carrier detected
   CONNECT 1200 - connect at 1200 bps
8. Next byte after “CONNECT 1200" is modem data!

Example 4: V.32bis in South Korea with Japan Caller ID

1. Power on reset.
2. Set host UART to 19.2 kbps.
3. AT:U67,0006 - DAA PTT settings for South Korea.
4. AT&H4 - limit Si2456/33/14 to V.32bis
5. AT+VCST=3 - enable Japan caller ID.
6. ATDT15128675309<CR>
   Si2456/33/14 may echo:
   BUSY - busy tone detection
   NO CARRIER - no carrier detected
   CONNECT 14400 - connect at 14.4 kbps
7. Next byte after “CONNECT 14400" is modem data!

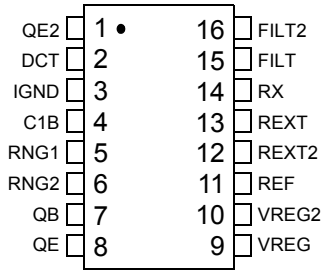
Pin Descriptions: Si2456/33/14



Pin #	Pin Name	Description
1	CLKIN/XTALI	**Clock Input/Crystal Oscillator Pin.** This pin provides support for parallel resonant, AT cut crystals. XTALI also acts as an input in the event that an external clock source is used in place of a crystal. A 4.9152 MHz crystal or 4.9152 MHz clock is required.
2	XTALO	**Crystal Oscillator Pin.** This pin provides support for parallel-resonant AT-cut crystals. XTALO serves as the output of the crystal amplifier.
3	CLKOUT/A0	**Clock Output/Address Bit 0.** Clock output in serial mode. Address Enable in parallel mode.
4	D6	**Data Bit.** Bidirectional parallel bus data bit 6 in parallel mode.
5, 19	VD3.3	**Digital Supply Voltage.** Provides the 3.3 V digital supply voltage to the Si2456/33/14.
6, 18	GND	**Ground.** Connects to the system digital ground.
7,17	VDA, VDB	**Digital Rail.** Pin provides additional power supply voltage to the Si2456/33/14.
8	$\overline{\text{RTS}}$/D7	**Request-to-Send/Data Bit.** Request-to-send (for flow control) in serial mode. Bidirectional parallel bus data bit 7 in parallel mode.
9	RXD/$\overline{\text{RD}}$	**Receive Data/Read Enable.** Data output to DTE RXD pin in serial mode. Active low read enable pin in parallel mode.
10	TXD/$\overline{\text{WR}}$	**Transmit Data/Write Enable.** Data input from DTE TXD pin in serial mode. Active low write enable pin in parallel mode.

Pin #	Pin Name	Description
11	$\overline{\text{CTS}}$/$\overline{\text{CS}}$	**Clear-to-Send/Chip Select.** Active low clear-to-send (for flow control) in serial mode. Active low chip select in parallel mode.
12	$\overline{\text{RESET}}$	**Reset Input.** An active low input that is used to reset all control registers to a defined initialized state.
13	AOUT/$\overline{\text{INT}}$	**Analog Output/Interrupt Output.** Analog output in serial mode. Active low interrupt output in parallel mode.
14	$\overline{\text{INT}}$/D0	**Interrupt Output/Data Bit.** Active low interrupt output in serial mode. Bidirectional parallel bus data bit 0 in parallel mode.
15	$\overline{\text{RI}}$/D1	**Ring Indicator/Data Bit.** The $\overline{\text{RI}}$ on (active low) indicates the presence of an ON segment of a ring signal on the telephone line. Bidirectional parallel bus data bit 1 in parallel mode.
16	D2	**Data Bit.** Bidirectional parallel bus data bit 2 in parallel mode.
20	ISOB	**Isolink Bias Voltage.** This pin should be connected via the C3 capacitor.
21	C1A	**Isolation Capacitor 1A.** Connects to one side of the isolation capacitor, C1.
22	ESC/D3	**Escape/Data Bit.** Hardware escape in serial mode. Bidirectional parallel bus data bit 3 in parallel mode.
23	$\overline{\text{DCD}}$/D4	**Carrier Detect/Data Bit.** Active low carrier detect in serial mode. Bidirectional parallel bus data bit 4 in parallel mode.
24	D5	**Data Bit.** Bidirectional parallel bus data bit 5 in parallel mode.

Pin Descriptions: Si3015



Pin #	Pin Name	Description
1	QE2	**Transistor Emitter 2.** Connects to the emitter of Q4.
2	DCT	**DC Termination.** Provides dc termination to the telephone network.
3	IGND	**Isolated Ground.** Connects to ground on the line-side interface. Also connects to capacitor C2.
4	C1B	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1.
5	RNG1	**Ring 1.** Connects through a capacitor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the modem.
6	RNG2	**Ring 2.** Connects through a capacitor to the RING lead of the telephone line. Provides the ring and caller ID signals to the modem.
7	QB	**Transistor Base.** Connects to the base of transistor Q3.
8	QE	**Transistor Emitter.** Connects to the emitter of transistor Q3.
9	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
10	VREG2	**Voltage Regulator 2.** Connects to an external capacitor to provide bypassing for an internal power supply.
11	REF	**Reference.** Connects to an external resistor to provide a high-accuracy reference current.
12	REXT2	**External Resistor 2.** Sets the complex ac termination impedance.
13	REXT	**External Resistor.** Sets the real ac termination impedance.

Pin #	Pin Name	Description
14	$\overline{RX}$	**Receive Input.** Serves as the receive side input from the telephone network.
15	FILT	**Filter.** Provides filtering for the dc termination circuits.
16	FILT2	**Filter 2.** Provides filtering for the bias circuits.

Ordering Guide

Chipset	Region	Power Supply	Digital	Line	Temperature
Si2456	Global	3.3 V Digital	Si2456-KT	Si3015-KS	0 to 70 °C
Si2456	Global	3.3 V Digital	Si2456-BT	Si3015-BS	–40 to 85 °C
Si2433	Global	3.3 V Digital	Si2433-KT	Si3015-KS	0 to 70 °C
Si2433	Global	3.3 V Digital	Si2433-BT	Si3015-BS	–40 to 85 °C
Si2414	Global	3.3 V Digital	Si2414-KT	Si3015-KS	0 to 70 °C
Si2414	Global	3.3 V Digital	Si2414-BT	Si3015-BS	–40 to 85 °C

Package Outline: TSSOP

Figure 15 illustrates the package details for the Si2456/33/14. Table 26 lists the values for the dimensions shown in the illustration.

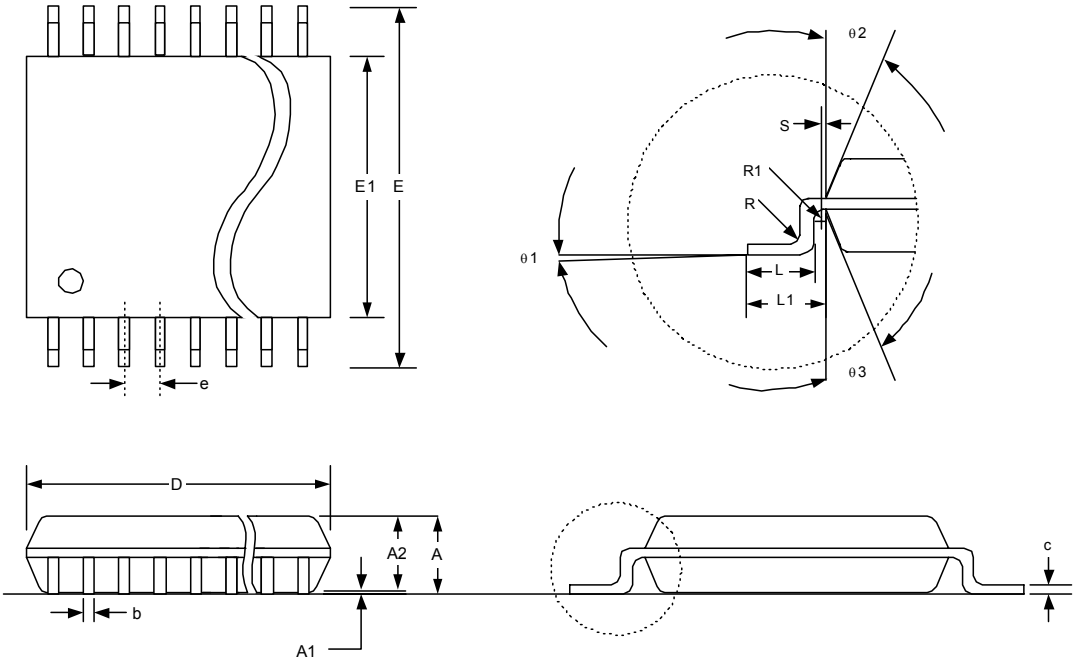


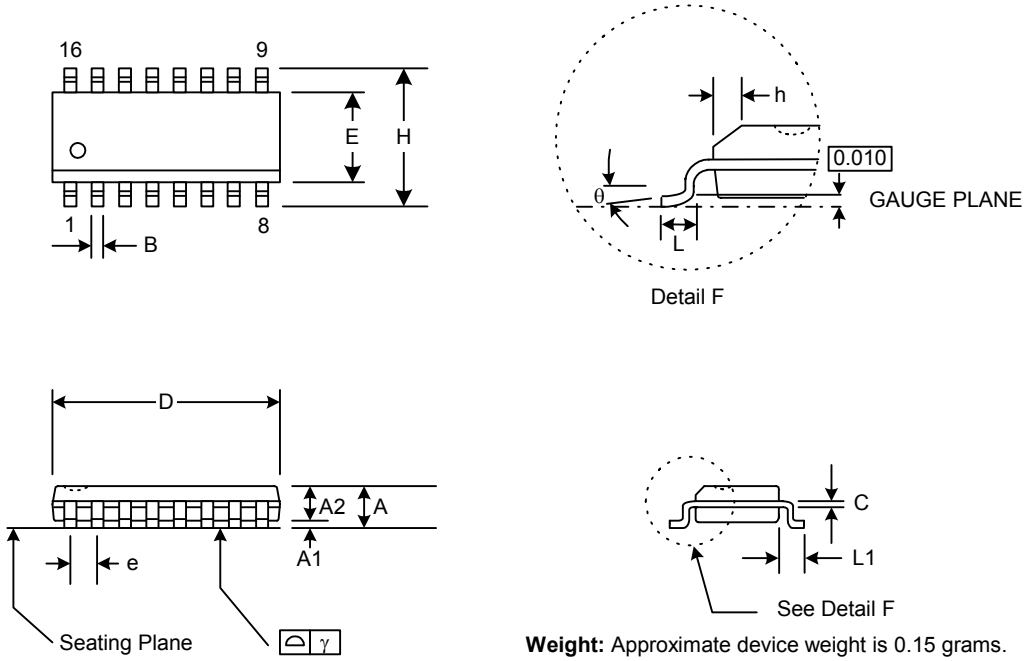
Figure 15. 24-Pin Thin Small Shrink Outline Package (TSSOP)

Table 26. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	—	1.10	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	7.70	7.80	7.90
e	0.65 BSC		
E	6.40 BSC		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1	1.00 REF		
R	0.09	—	—
R1	0.09	—	—
S	0.20	—	—
θ1	0	—	8
θ2	12 REF		
θ3	12 REF		

Package Outline: SOIC

Figure 16 illustrates the package details for the Si3015. Table 27 lists the values for the dimensions shown in the illustration.



Weight: Approximate device weight is 0.15 grams.

Figure 16. 16-Pin Small Outline Integrated Circuit (SOIC) Package

Table 27. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	.10	.25
A2	1.30	1.50
B	.33	.51
C	.19	.25
D	9.80	10.01
E	3.80	4.00
e	1.27 BSC	—
H	5.80	6.20
h	.25	.50
L	.40	1.27
L1	1.07BSC	—
γ	—	0.10
θ	0º	8º

Document Change List

Revision 0.81 to Revision 0.9.

- Removed Wake-on-Ring mode (AT&Z) and associated I_D specification in Table 3.
- Removed FULL bit (U69, bit 7).
- Added \N0 commands to Table 9.
- Added V.22bis Transparent HDLC mode to Table 9.
- Removed PCM mode and associated U71 register.
- Removed :Dn and :Fn commands.
- Simplified some Parallel Phone Detection text.
- Removed RST bit (U70, bit 5).
- Added V22HD bit (U7A, bit 2).
- Removed Ringer Impedance and Billing Tone notes, tables, and figures for Czech Republic in “Appendix A—DAA Operation”.
- Added DOP bit (U7A, bit 7)
- Added U7A, U7C registers
- Added FOH bit (U62, bit 2)
- Added /A metacharacter (Table 10)

Notes:

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