2A 23V Synchronous PWM/PSM Step-Down Converter with High Light-load Efficiency

FEATURES

- 2A Continuous Output Current
- Wide 4.75V to 23V Operating Input Range
- Ouput Adjustable from 0.925V to 12V
- Up to 89% Efficiency for Heavy Load (Vin=12V, Vout=3.3V, Iout=2.0A)
- Up to 92% Efficiency for Moderate Load (Vin=12V, Vout=3.3V, Iout=1.0A)
- Up to 81% Efficiency for Light Load (Vin=12V, Vout=3.3V, Iout=20mA)
- Low Rds(on) Internal Switches: 140mΩ and 120mΩ
- <3μA Supply Current in Shutdown Mode
- 340KHz/550KHz Frequency
- Programmable Soft Start
- Thermal Shutdown
- Cycle by Cycle Over Current Protection
- Under Voltage Lockout
- Short Circuit Protection
- Over Voltage Protection

APPLICATIONS

- Networking Systems such as Modems & Routers
- Distributed Power Systems
- Pre-Regulator for Linear Regulators
- Set-top Box

DESCRIPTION

The AIC2862 is a 2A synchronous-rectified Buck converter with integrated low Rds(on) power MOSFETs. The AIC2862, designed with a current-mode control scheme, can convert wide input voltage to the adjustable output voltage to provide excellent output voltage regulation. It is stable with low ESR output ceramic capacitors.

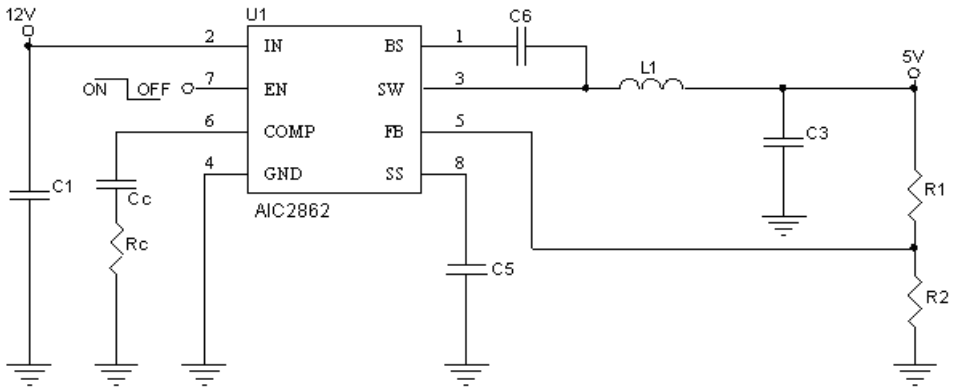
For high efficiency over all load current range, the

AIC2862 is equipped with an automatic PSM/PWM modeoperation. At light load, the IC operates in the PSM (Pulse Skipping Mode) to reduce switching losses. At heavy load, the IC works in PWM mode to provide high efficiency and excellent output voltage regulation.

The AIC2862 is also equipped with softstart and whole protections (under-voltage, over-voltage, over-temperature, short circuit and current-limit) into a single package.

This device, available in SOP-8 package, provides a very compact system solution with minimal external components and PCB area.

TYPICAL APPLICATIONS CIRCUIT



Typical Application Circuit

PIN CONFIGURATION

AIC2862-XXXXXX

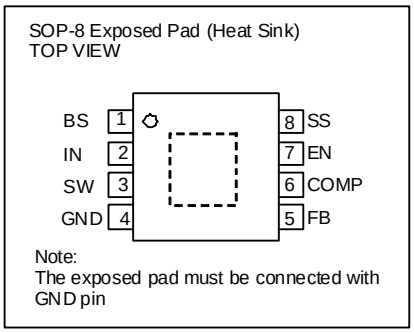
- PACKING TYPE
  TR: TAPE & REEL
  TB: TUBE
- PACKAGING TYPE
  R8: SOP-8 Exposed Pad (Heat Sink)
- G: GREEN PACKAGE
- 3: fs=340KHz
  5: fs=550KHz

Example:

AIC2862-3GR8TR

→ 340KHz with GREEN SOP-8 Exposed Pad (Heat Sink) Package and TAPE & REEL Packing Type

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN})…… - 0.3V to 26V

SW Pin Voltage (Vsw) …… -1V to V_{IN} + 0.3V

BS Pin Voltage ……Vsw – 0.3V to Vsw + 6V

EN Pin Voltage…….... - 0.3V to V_{IN}

All Other Pins Voltage……..… - 0.3V to 6V

Operating Ambient Temperature Range T_A……..... - 40°C ~ 85°C

Operating Maximum Junction Temperature T_J……..... 150°C

Storage Temperature Range T_{STG} ..... -65ºC~150ºC

Lead Temperature (Soldering 10 Sec.)…… 260°C

Thermal Resistance Junction to Case SOP-8 Exposed Pad*……..15°C/W

Thermal Resistance Junction to Ambient SOP-8 Exposed Pad*……..60°C/W
(Assume no Ambient Airflow)

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

*The package is place on a two layers PCB with 2 ounces copper and 2 square inch, connected by 8 vias.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, unless otherwise specified. Typical values are at TA=+25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range			4.75		23	V
Under Voltage Lockout Threshold		V_{IN} Rising	3.7	4.05		V
UVLO Hysteresis				210		mV
Shutdown Supply Current		V_{EN} = 0V		0.3	3	μA
Standby Current (Switching)		V_{EN} = 3.0V; SW = NC		0.7	1.5	mA
Reference Voltage	V_{REF}		0.900	0.925	0.95	V
Feedback Over Voltage Threshold		V_{FB} Rising		123		%
EN Shutdown Threshold Voltage		V_{EN} Rising	1.1	1.5	2.2	V
EN Shutdown Hysteresis				220		mV
High-Side Switch On-Resistance	$R_{DS(ON)1}$			140		mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)2}$			120		mΩ
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V		0	10	μA
High-Side Switch Current Limit		Peak Current	2.7	3.4		A
Oscillation Frequency fs=340KHz	fs		300	340	380	KHz
Oscillation Frequency fs=550KHz	fs		485	550	615	KHz
Short Circuit Oscillation Frequency		V_{FB} = 0V		110		KHz
Maximum Duty Cycle	D_{MAX}			90		%
Minimum On Time	T_{ON}			220		ns
Soft-Start Current		V_{SS} = 0V		6		μA
Soft-Start Period		V_{SS} = 0.1μF		15		ms
Thermal Shutdown		Trip Point		160		°C

Note 1: Specifications are production tested at T_A=25°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

TYPICAL PERFORMANCE CHARACTERISTICS

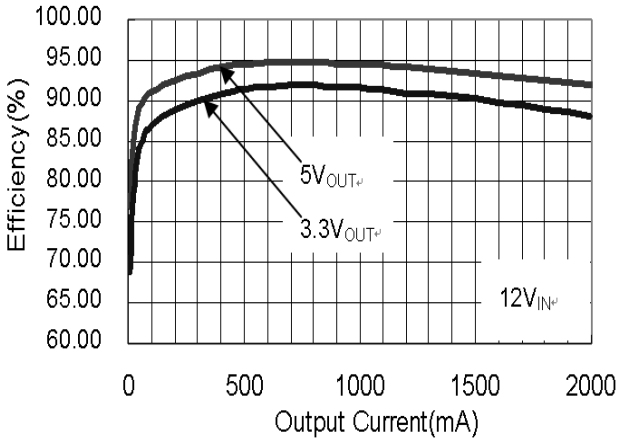


Fig. 1 Efficiency vs. Load Current at V_{IN} = 12V

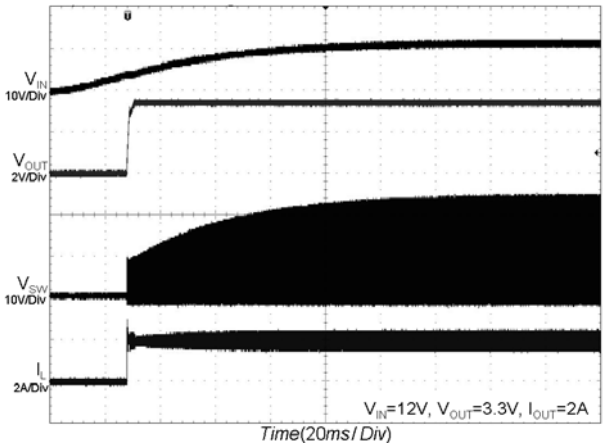


Fig. 2 Start-Up Waveform at V_{OUT}=3.3V, I_{OUT}=2A

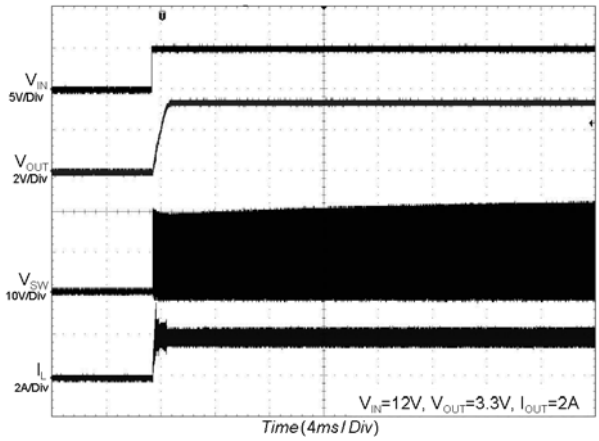


Fig. 3 Start-Up Waveform at V_{OUT}=3.3V, I_{OUT}=2A

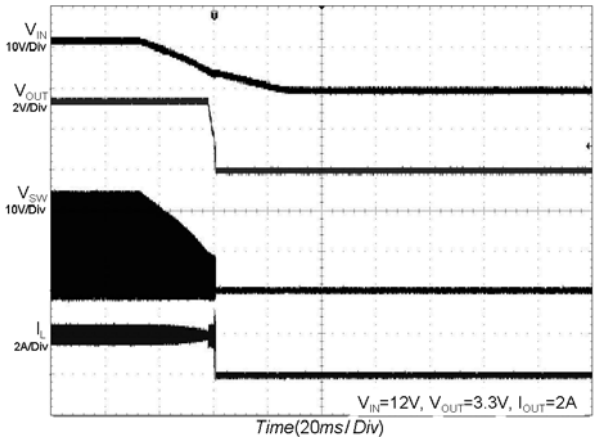


Fig. 4 Shutdown Waveform at V_{OUT}=3.3V, I_{OUT}=2A

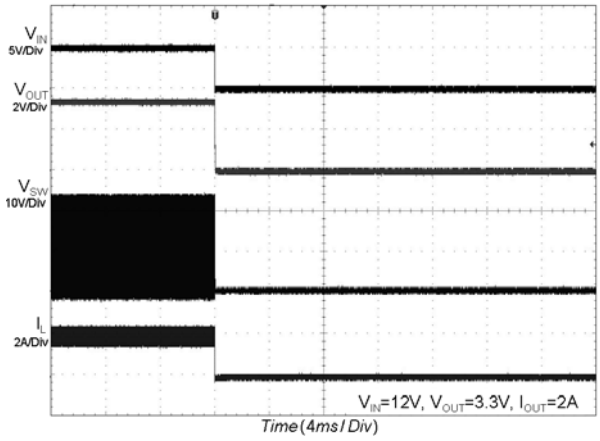


Fig. 5 Shutdown Waveform at V_{OUT}=3.3V, I_{OUT}=2A

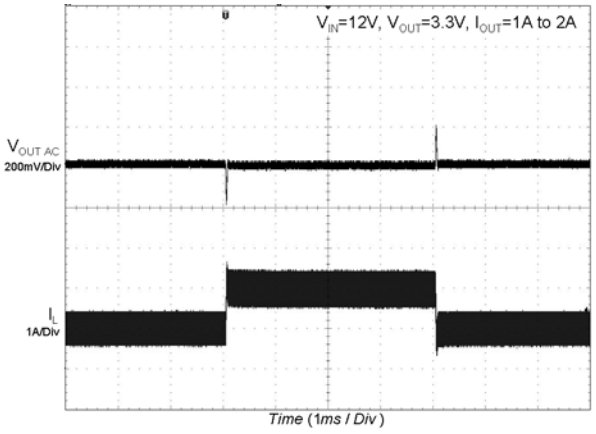


Fig. 6 Load Transient at V_{OUT}=3.3V, I_{OUT}=1A to 2A

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

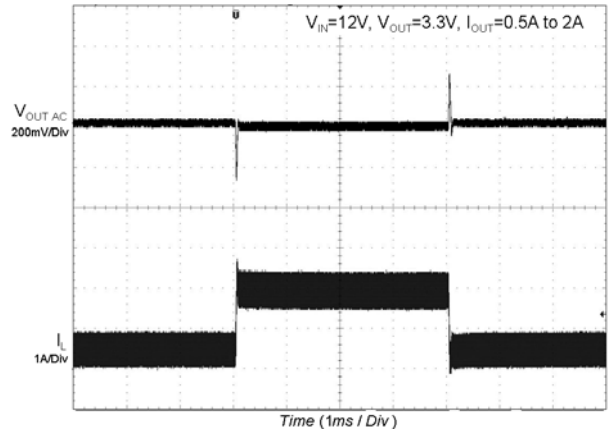


Fig. 7 Load Transient at V_{OUT}=3.3V, I_{OUT}=0.5A to 2A

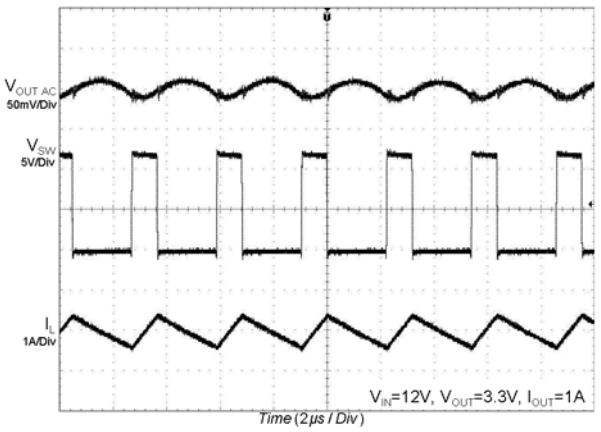


Fig. 8 Stability Waveform at V_{OUT}=3.3V, I_{OUT}=1A

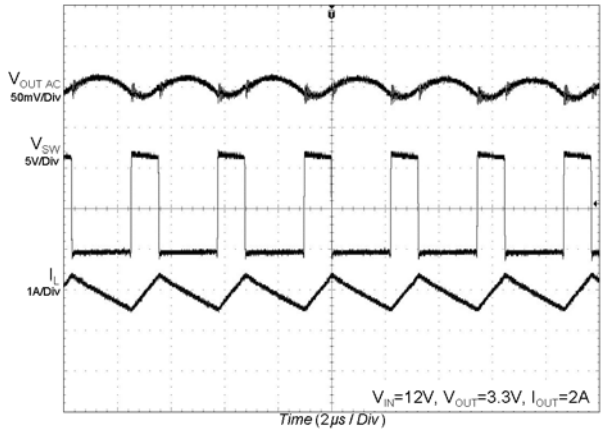
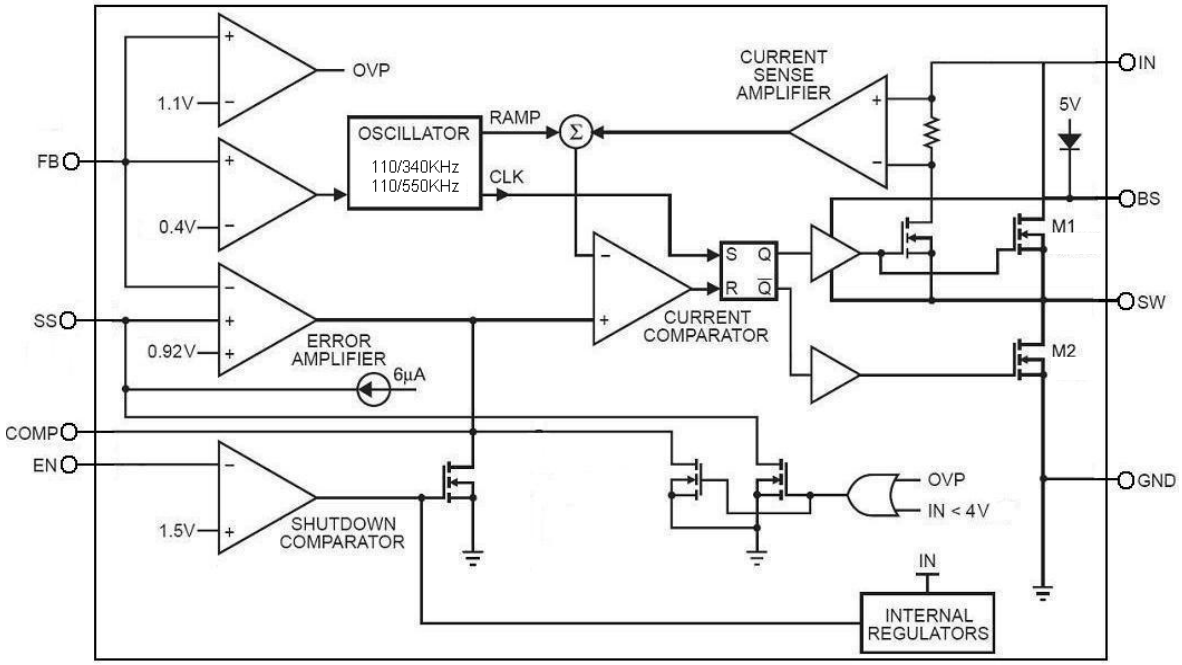


Fig. 9 Stability Waveform at V_{OUT}=3.3V, I_{OUT}=2A

BLOCK DIAGRAM



Functional Block Diagram of AIC2862

PIN DESCRIPTIONS

Pin No.	Pin Name	Pin Function
1	BS	High Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 10nF or greater capaitor from SW to BS to power the high-side switch.
2	IN	Power Input. IN supplies power to the IC, as well as the step-down converter switches. By pass IN to GND with a suitabley large capacitor to eliminate noise on the input to the IC.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from switch to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground. Connect the exposed pad on backside to Pin 4.
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive feedback with a resistive voltage divider from the output voltage.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network form COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator. Drive it low to turn it off. For automatic strat-up, attach to IN with a 100kΩ pull up resistor.
8	SS	Soft Star Contol Input. SS controls the soft star period. Connect a capacitor from SS to GND to set the soft-star period. To disable the soft-star feature, leave the SS pin unconnected.

APPLICATION INFORMATIONS

The AIC2862 is a synchronous high voltage buck converter that can support the input voltage range from 4.75V to 23V and the output current can be up to 2A.

Setting the Output Voltage

The output voltage is set using a resistive voltage divider connected from the output voltage to FB. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Thus the output voltage is:

$$V_{OUT} = 0.925 \times \frac{R1+R2}{R2}$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 26.1kΩ.

Inductor

The inductor selection depends on the current ripple of inductor, the input voltage, and the output voltage.

$$L \geq \frac{V_{OUT}}{f_{OSC} \cdot \Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Accepting a large current ripple of inductor allows the use of a smaller inductance. However, higher current ripple of inductor can cause higher output ripple voltage and large core loss. By setting an acceptable current ripple of inductor, a suitable inductance can be obtained from above equation.

In addition, it is important to ensure the inductor saturation current exceeds the peak value of inductor current in application to prevent core saturation. The peak value of inductor current can be calculated according to the following equation.

$$I_{PEAK} = I_{OUT(max)} + \frac{V_{OUT}}{2 \times f_{OSC} \cdot L}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Soft-Start

The AIC2862 provides the soft-start function. Initially, the voltage at SS pin is 0V. Then an internal current source of 6μA (typ.) charges an external soft-start capacitor. During the soft-start period, the voltage at SS pin will limit the feedback threshold voltage at FB pin. When the voltage at SS pin is higher than 0.925V, the feedback threshold voltage at FB pin reaches the desired value. The soft-start time can be calculated in accordance with the following equation.

$$t_{SS} = C5 \times \frac{0.925V}{6\mu A}$$

The soft-start capacitor is discharged to GND when the EN pin is connected to GND.

Optional Schottky Diode

A Schottky diode with low forward drop voltage and fast reverse recovery is the ideal choice for better efficiency. The forward drop voltage of a Schottky diode will result in the conduction losses in the diode, and the diode capacitance (C_T or C_D) will cause the switching losses. Therefore, it is necessary to consider both forward voltage drop and diode capacitance for diode selection. In addition, the rating of selected Schottky diode should be able to handle the input voltage and the maximum peak diode current.

Input Capacitor and Output Capacitor

To prevent the high input voltage ripple and noise resulted from high frequency switching, the use of low ESR ceramic capacitor for the maximum RMS current is recommended. The approximated RMS current of the input capacitor can be calculated according to the following equation.

$$I_{CINRMS} \approx \sqrt{I_{OUT(MAX)}^2 \times \frac{V_{OUT}(V_{IN}-V_{OUT})}{V_{IN}^2} + \frac{\Delta I_L^2}{12}}$$

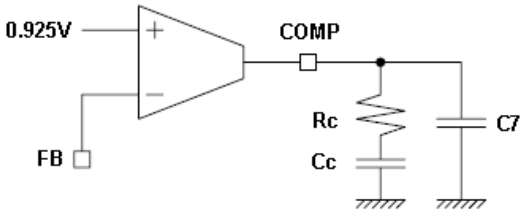
The selection of output capacitor depends on the required output voltage ripple. The output voltage ripple can be expressed as:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times f_{OSC} \times C3} + ESR \quad \Delta I_L$$

For lower output voltage ripple, the use of low ESR ceramic capacitor is recommended. The tantalum capacitor can also be used well, but its ERS is larger than that of ceramic capacitor.

When choosing the input and output ceramic capacitors, X5R and X7R types are recommended because they retain their capacitance over wider ranges of voltage and temperature than other types.

Loop Compensation



In order to avoid the poor output voltage ripple and low efficiency caused by instability, AIC2862 requires a proper external compensation network to compensate its feedback loop. In this external compensation network, the compensation resistor, R_C, and the compensation capacitor, C_C, are used to set the high-frequency integrator gain and the integrator zero. C7 is used to cancel the zero caused by the output capacitor and it's ESR. While using the ceramic capacitor as the output capacitor, C7 can be omitted due to the small ESR.

The system has one pole of importance, due to the output capacitor, C3 and the load resistor. This poles is located at:

$$F_{P1} = \frac{1}{2\pi \times C3 \times R_{LOAD}}$$

The system has one zero of importance, due to the compensation capacitor, Cc and the compensation resistor, Rc. This zero is located at:

$$F_{Z1} = \frac{1}{2\pi \times Cc \times Rc}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$F_{ESR} = \frac{1}{2\pi \times C3 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor, C7 and the compensation resistor, Rc is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$F_{P2} = \frac{1}{2\pi \times C7 \times Rc}$$

※The values of the compensation components are given in the AIC2862 demo board user manual.

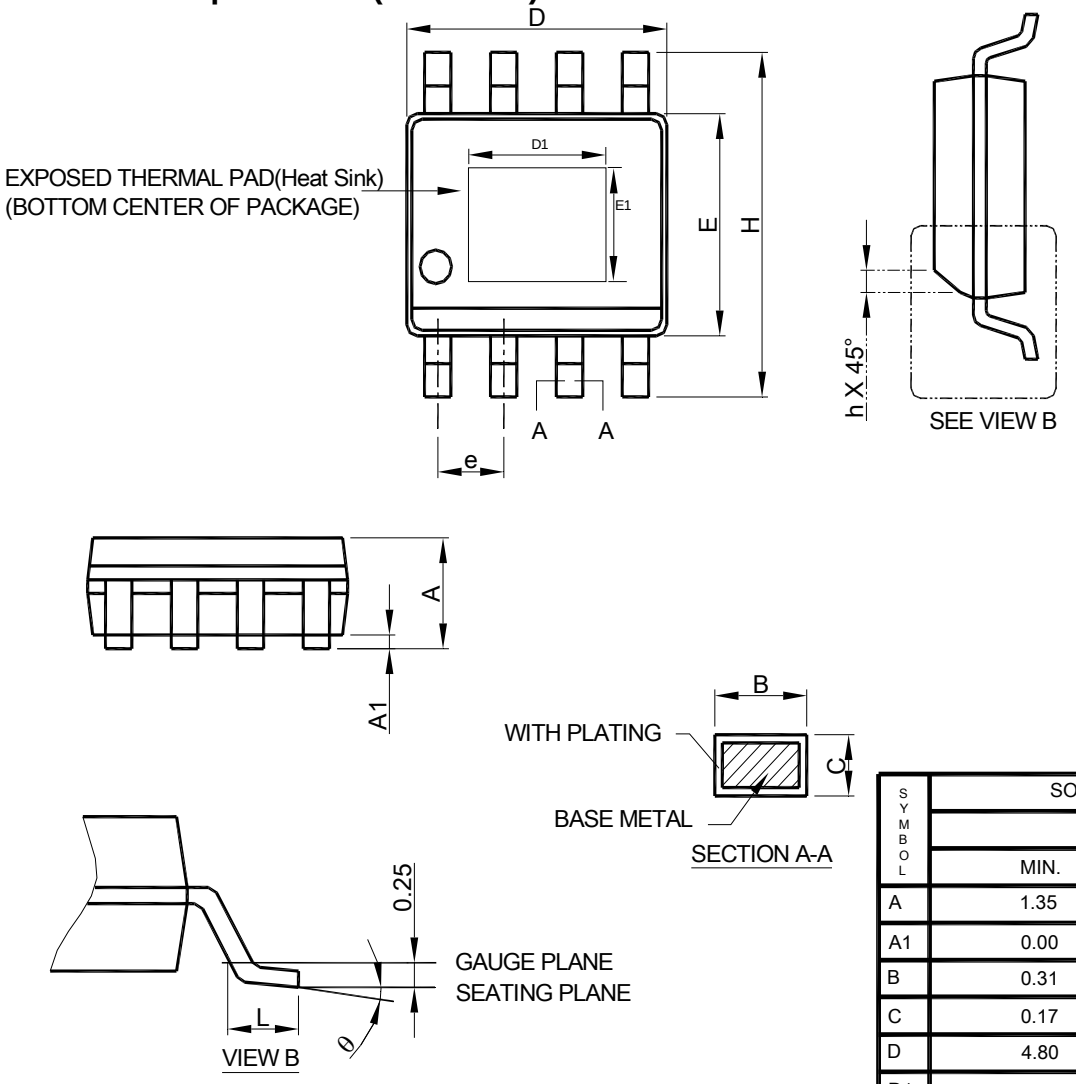
Layout Consideration

In order to ensure a proper operation of AIC2862, the following points should be managed comprehensively.

1. The input capacitor and V_{IN} should be placed as close as possible to each other to reduce the input voltage ripple and noise.
2. The output loop, which is consisted of the inductor, the internal power switch, the Schottky diode and the output capacitor, should be kept as small as possible.
3. The routes with large current should be kept short and wide.
4. Logically the large current on the converter should flow at the same direction.
5. In order to prevent the effect from noise, the IC's GND pin should be placed close to the ground of the input bypass capacitor.
6. The FB pin should be connected to the feedback resistors directly and the route should be away from the noise sources.

PHYSICAL DIMENSIONS

- **SOP-8 Exposed Pad(Heat Sink)**



Note : 1. Refer to JEDEC MS-012E.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

SYMBOL	SOP-8 Exposed Pad(Heat Sink)	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.15
B	0.31	0.51
C	0.17	0.25
D	4.80	5.00
D1	1.50	3.50
E	3.80	4.00
E1	1.0	2.55
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°