Flash

4 Gbit (256M x 16)
3.3V NAND Flash Memory

FEATURES

- Voltage Supply
  - V_{CC}: 3.3V (2.7 V ~ 3.6V)
- Organization
  - Page Size: (2K + 128) words
  - Block Size: 64Pages = (128K + 8K) words
  - Number of Planes: 1
  - Number of Block per Die (LUN)= 2048
- Automatic Program and Erase
  - Page Program: (2K + 128) words
  - Block Erase: (128K + 8K) words
- Page Read Operation
  - Random Read: 25us (Max.)
  - Read Cycle: 25ns
- Write Cycle Time
  - Page Program Time: 400us (Typ.)
    700us (Max.)
  - Block Erase Time: 3 ms (Typ.)
    10ms (Max.)
- 1bit/cell
- Command/Address/Data Multiplexed DQ Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating Gate Technology
  - ECC Requirement: 8bit / 256words
  - Endurance: 50K-P/E Cycle Times
  - Data Retention: 10year
- Command Register Operation
- Number of partial program cycles in the same page (NOP) : 4
- Automatic Page 0 Read at Power-Up Option
  - Boot from NAND support
  - Automatic Memory Download
- Cache Program Operation for High Performance Program
- Cache Read Operation
- Copy-Back Operation
- EDO mode
- Page copy

ORDERING INFORMATION

Product ID	Speed	Package	Comments
F59L4G161KA -25BCAG2R	25 ns	67 ball BGA	Pb-free

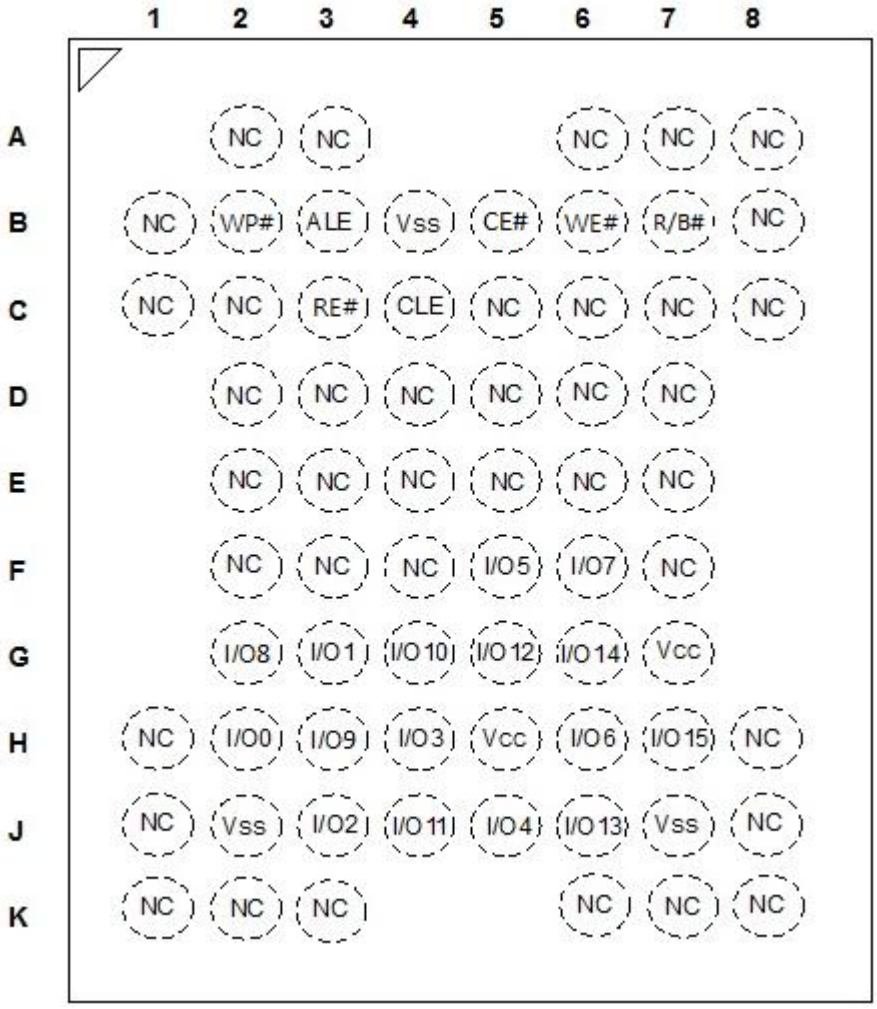
GENERAL DESCRIPTION

The device has 2176-words static registers which allow program and read data to be transferred between the register and the memory cell array in 2176-words increments. The Erase operation is implemented in a single block unit (128Kwords + 8Kwords).

The device is a memory device which utilizes the I/O pins for both address and data input/output as well as command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid state file storage, voice recording, image file memory for still cameras and other systems which require high density non-volatile memory data storage.

BALL CONFIGURATION (TOP VIEW)

(BGA 67 Ball, 6.5mmx8mmx1.0mm Body, 0.8mm Ball Pitch)

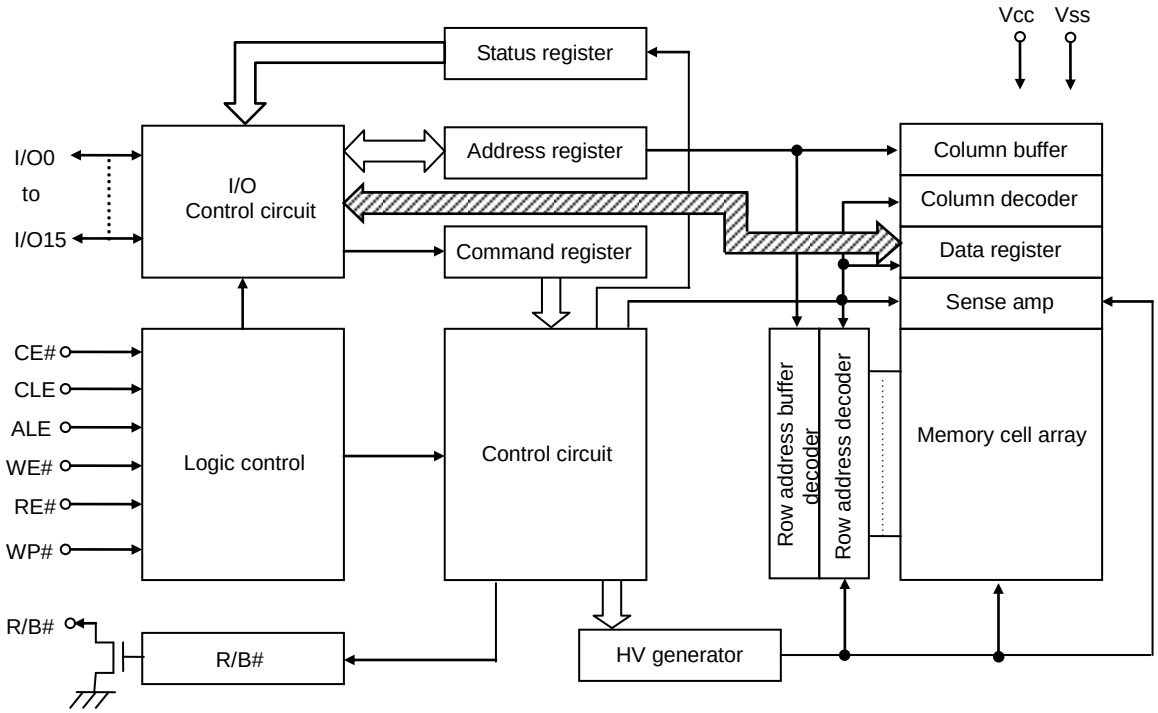


BALL NAMES

Ball Name	Type	Function
V_{CC}	Supply	NAND Power Supply
V_{SS}	Supply	Ground
I/O0 to I/O15	Input/output	**Data inputs/outputs:** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
ALE	Input	**Address latch enable:** The ALE input controls the activating path for addresses sent to the internal address registers. Addresses are latched into the address register through the I/O ports on the rising edge of WE# with ALE high.
CLE	Input	**Command latch enable:** The CLE input controls the activating path for commands sent to the internal command registers. Commands are latched into the command register through the I/O ports on the rising edge of the WE# signal with CLE high.
CE#	Input	**Chip enable:** The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE**#** control during read operation, refer to 'Page read' section of Device operation.
RE#	Input	**Read enable:** The RE# input is the serial data-out control, and when active low, it drives the data onto the I/O bus. Data is valid after t_{REA} of rising edge & falling edge of RE# which also increments the internal column address counter by one.
WE#	Input	**Write enable:** The WE# input controls writes to the I/O ports. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	Input	**Write protect:** The WP# pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	Output	**Ready/busy:** The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
NC	-	**No connect:** Lead is not internally connected.

NOTE: Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs. Do not leave V_{CC} or V_{SS} disconnected.

Block Diagram



Definitions and Abbreviations

LSB
Acronym for the least significant bit.

Address
The address is comprised of a column address 2 cycles and a row address with 3 cycles. The row address identifies the page, block, and LUN to be accessed. The column address identifies the word within a page to access.

Column
The word location within the page register.

Row
Refer to the block and page to be accessed.

Page
The smallest addressable unit for the Read and the Program operations.

Block
Consists of multiple pages and is the smallest unit for the Erase operation.

Page register
Register used to transfer data to and from the Flash Array.

Cache register
Register used to transfer data to and from the Host.

Defect area
The defect area is where the factory defects are marked by the manufacturer. It is a reference for initial invalid block(s).

Device
The packaged NAND unit. A device may contain more than a target.

LUN (Logical Unit Number)
The minimum unit that can independently execute commands and report status. There are one or more LUNs per CE#.

Target
An independent NAND Flash component with its own CE# signal.

SR[x] (Status Read)
SR refers to the status register contained within a particular LUN. SR[x] refers to bit x in the status register for the associated LUN.

Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	-0.6 to +4.6	V
	V_{IN}	-0.6 to +4.6	
	$V_{I/O}$	-0.6 to Vcc+0.3(<4.6V)	
Short Circuit Current	I_{OS}	5	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit
Operating Temperature Range	T_{OPER}	0 to +70	°C
Soldering Temperature (10s)	T_{SOLDER}	260	°C
Storage Temperature	T_{STG}	-55 to +125	°C

Note:

1. Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the NAND.
2. Operating Temperature Range specifies the temperatures where all NAND specifications will be supported. During operation, the NAND case temperature must be maintained between the range specified in the table under all operating conditions.

Recommended Operating Conditions

(Voltage reference to GND, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
High Level Input Voltage	V_{IH}	0.8 V_{CC}	-	V_{CC} + 0.3	
Low Level Input Voltage	V_{IL}	-0.3	-	0.2 V_{CC}	
Ground Voltage	V_{SS}	0	0	0	V

Valid Blocks

Parameter	Symbol	Min	Typ.	Max	Unit
F59L4G161KA (2R)	NVB	2,008	-	2,048	Block

Note:

1. The device may include initial invalid blocks when first shipped. The number of valid blocks is presented as first shipped. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

DC Operation Characteristics

(Recommended operating conditions otherwise noted)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
Operating Current	Page Read with Serial Access	I_{CC1}	CE# = V_{IL}, Iout = 0, t_{RC} = t_{RC}(min)	-	15	30	mA
	Program	I_{CC2}	-	-	15		
	Erase	I_{CC3}	-	-	15		
Stand-by Current (TTL)		I_{SB1}	CE# = V_{IH}, WP# = 0V/V_{CC}	-	-	1	
Stand-by Current (CMOS)		I_{SB2}	CE# = V_{CC}-0.2, WP# = 0V/V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN} = 0 to V_{CC} (max)	-	-	+/-10	
Output Leakage Current		I_{LO}	V_{OUT} = 0 to V_{CC} (max)	-	-	+/-10	
Output High Voltage Level		V_{OH}	I_{OH} = -400uA	2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL} = 2.1mA	-	-	0.4	
Output Low Current (R/B#)		I_{OL} (R/B#)	V_{OL} = 0.4V	8	10	-	mA

Note :

1. Typical value are measured at V_{CC} = 3.3V, T_A = 25°C. Not 100% tested.
2. I_{CC1} and I_{CC2} are without data cache.
3. I_{CC1}, I_{CC2}, I_{CC3}, and I_{SB2} are the values of one chip.

Capacitance

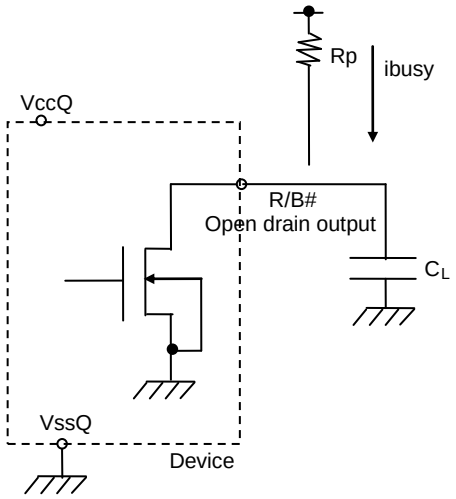
(T_A = 25°C, V_{CC} = 3.3V, f = 1.0MHz)

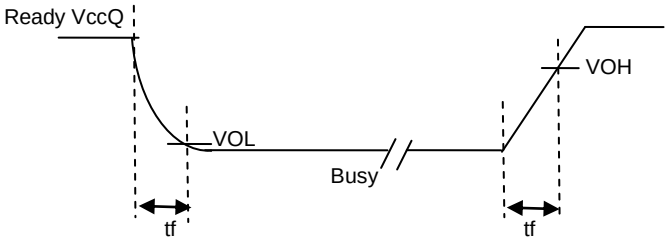
Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	C_{DQ}	V_{OUT} = 0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	10	pF

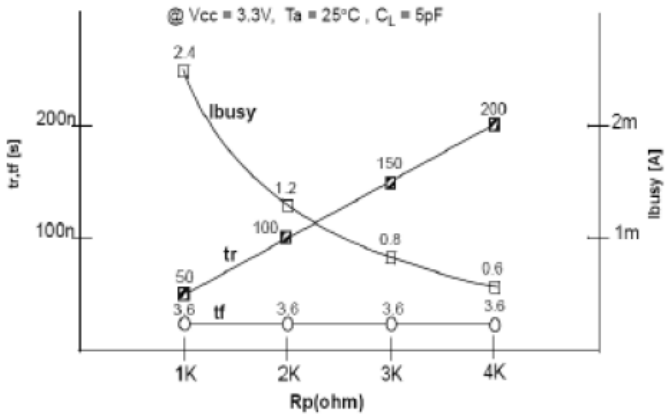
Note: Capacitance is periodically sampled and not 100% tested.

Ready/Busy

R/B# represents the status of the selected target. R/B# goes busy when only a single LUN is busy while rest of LUNs on the same target are idle.

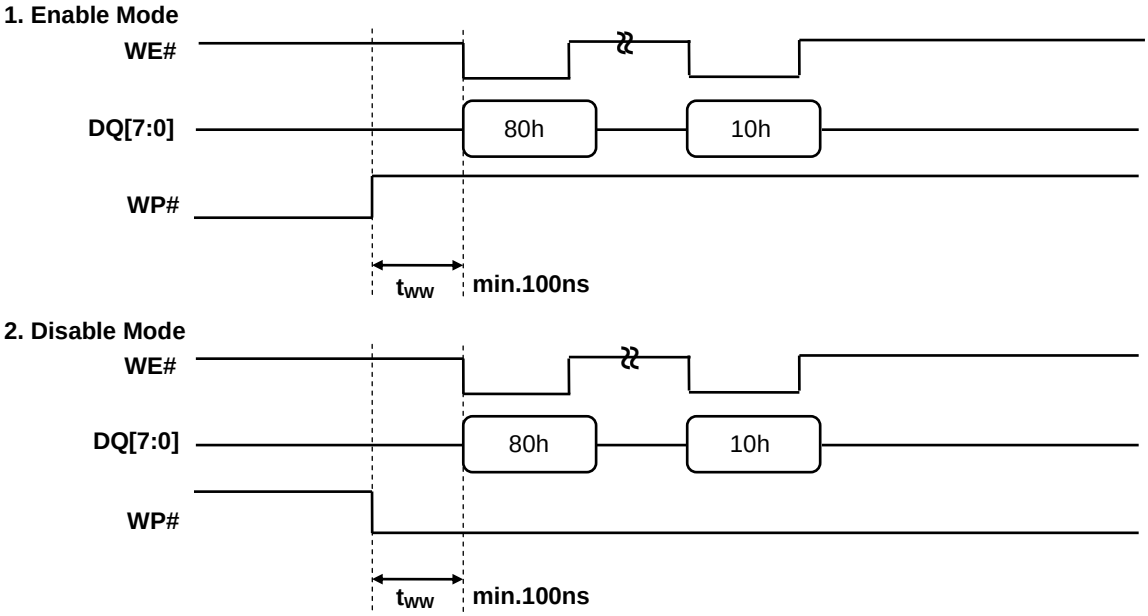




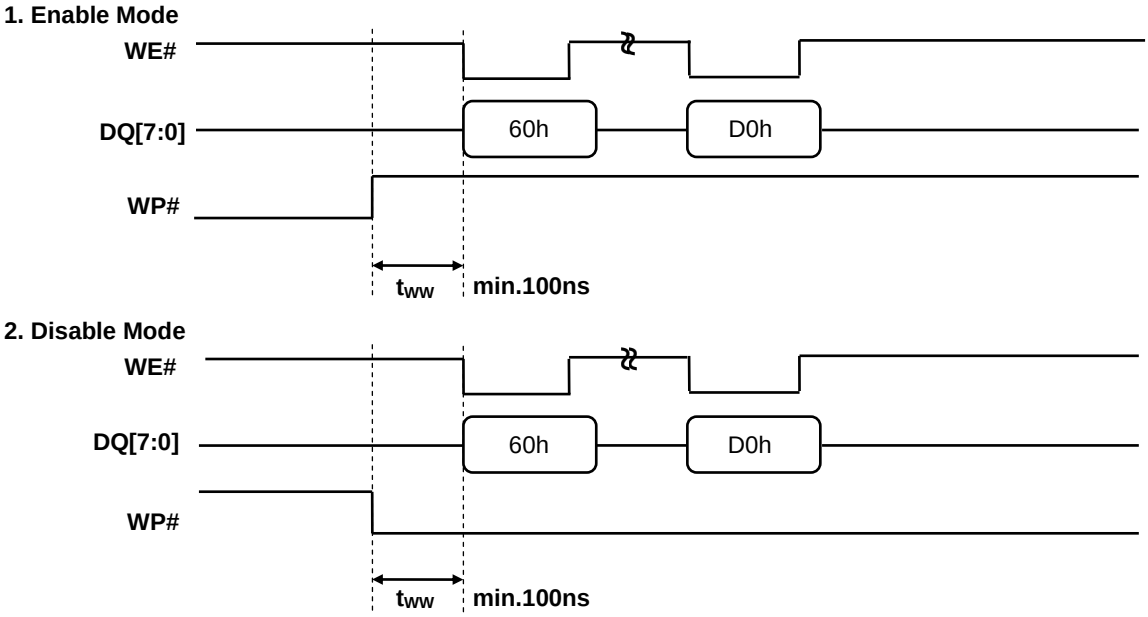


Write Protect

When WP# is enabled, Flash array is blocked from any program and erase operations. This signal shall only transitioned when a target is idle. The host shall be allowed to issue a new command after t_{WW} once WP# is enabled. Figures below describes the t_{WW} timing requirement, shown with the start of a Program command and the start of a Erase command.



Write Protect timing requirements of the Program operation



Write Protect timing requirements of the Erase operation

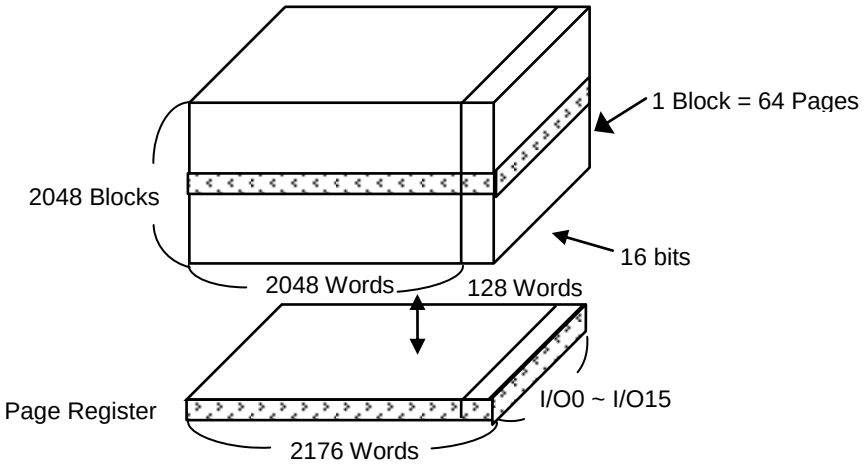
Memory Organization

Addressing

There are two address types used: the column address and the row address. The column address is used to access words within a page, i.e. the column address is the word offset into the page. The row address is used to address pages, blocks, and LUNs.

When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Block Erase. In this case the column addresses shall not be issued.

For both column and row addresses, the first address cycle always contains the least significant bits and the last cycle always contains the most significant bits. If there are bits in the most significant cycles of the column and row addresses that are not used, then they are required to be cleared to zero.



Array Address

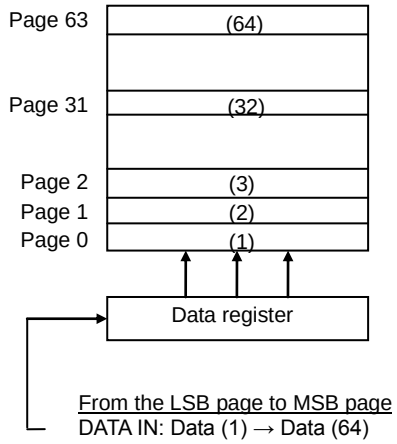
	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	I/O8~I/O15	Address
1st cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	*L	Column Address
2nd cycle	A_8	A_9	A_{10}	A_{11}	*L	*L	*L	*L	*L	Column Address
3rd cycle	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	*L	Row Address
4th cycle	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	*L	Row Address
5th cycle	A_{28}	*L	*L	*L	*L	*L	*L	*L	*L	Row Address

Note:

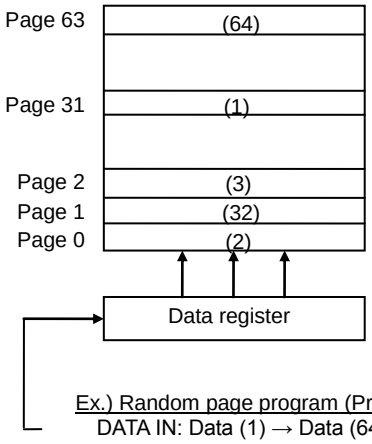
1. Column address: Starting Address of the Register.
2. *L must be set to 'Low'
3. The device ignores any additional input of address cycles than required.
4. A_{12}~A_{17} are for Page Address, A_{18}~A_{28} are for Block Address.

Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.



From the LSB page to MSB page
DATA IN: Data (1) → Data (64)



Ex.) Random page program (Prohibition)
DATA IN: Data (1) → Data (64)

Factory Defect Mapping and Error Management

Mask Out Initial Invalid Block(s)

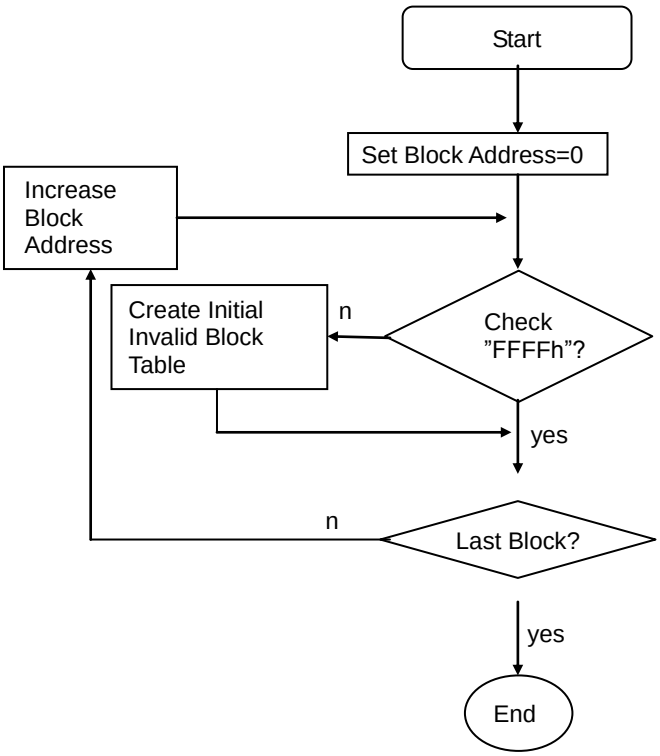
Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

Identifying Initial Invalid Block(s) and Block Replacement Management

If a block is defective, the manufacturer shall mark as defective by setting the Defective Block Marking, as shown in figure, of the first or second page of the defective block to a value of non-FFh. The Defective Block Marking is located on the first word of spare data area in the pages within a block.

The host shall not erase or program blocks marked as defective by the manufacturer, and any attempt to do so yields indeterminate results. Figure below outlines the flow chart how to create an initial invalid block table. It should be performed by the host to create the initial invalid block table prior to performing any erase or programming operations on the target. All pages in non-defective blocks are read FFh with ECC enabled on the controller. A defective block is indicated by the majority of bits being read non-FFh in the Defective Block Marking location of either the first page or second page of the block. The host shall check the Defective Block Marking location of both the first and second page of each block to verify the block is valid prior to any erase or program operations on that block.

Over the lifetime use of a NAND device, the Defective Block Marking of defective blocks may encounter read disturbs that cause bit changes. The initial defect marks by the manufacturer may change value over the lifetime of the device, and are expected to be read by the host and used to create a bad block table during initial use of the part.



Check "FFFFh" at the 1st Word column address in the spare area of the 1st and 2nd page in the block.

Algorithm for Bad Block Scanning

```
For (i=0; i<Num_of_LUs; i++)
{
    For (j=0; j<Blocks_Per_LU; j++)
    {
        Defect_Block_Found=False;


        Read_Page(lu=i, block=j, page=0);
        If (Data[coloumn=First_Word_of_Spare_Area]!=FFFFh) Defect_Block_Found=True;

        Read_Page(lu=i, block=j, page=1);
        If (Data[coloumn=First_Word_of_Spare_Area]!=FFFFh) Defect_Block_Found=True;

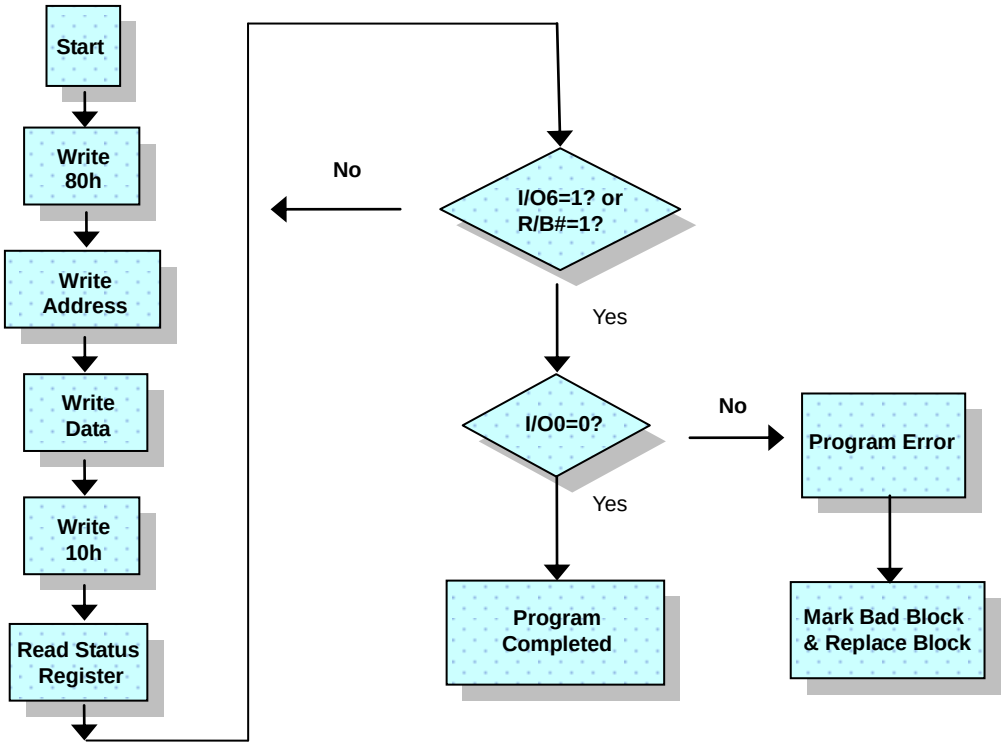
        If (Defect_Block_Found) Mark_Block_as_Defective(lu=i, block=j);
    }
}
```

Errors in Write or Read Operation

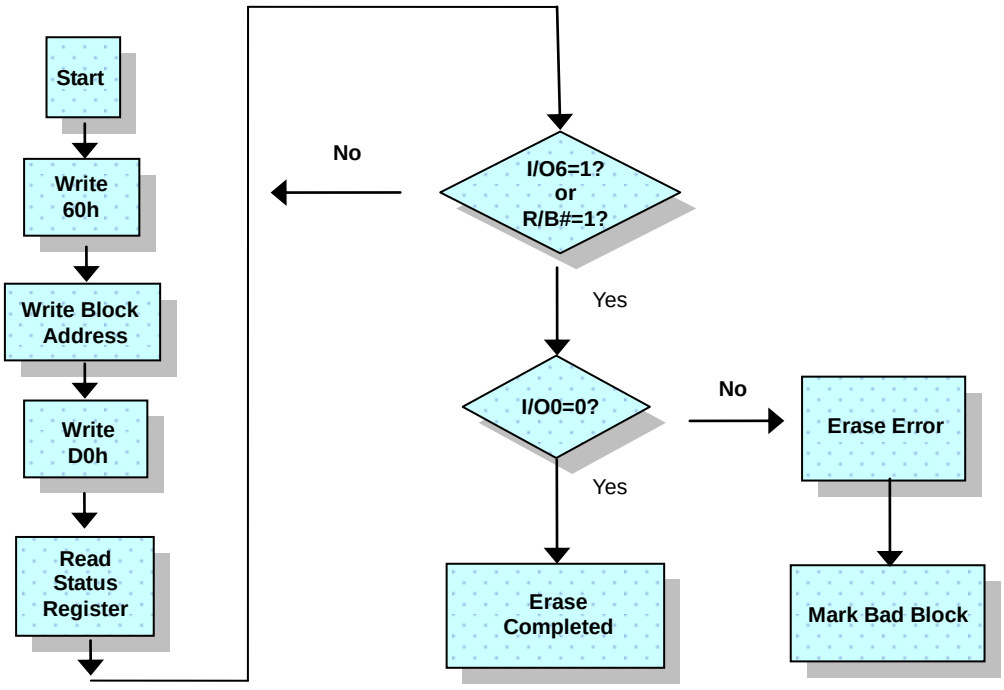
Within its lifetime, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure Sequence
Write	Erase failure	Read Status after Erase → Block Replacement
	Program failure	Read Status after Program → Block Replacement
Read	Up to 8 bits failure	Verify ECC → ECC Correction

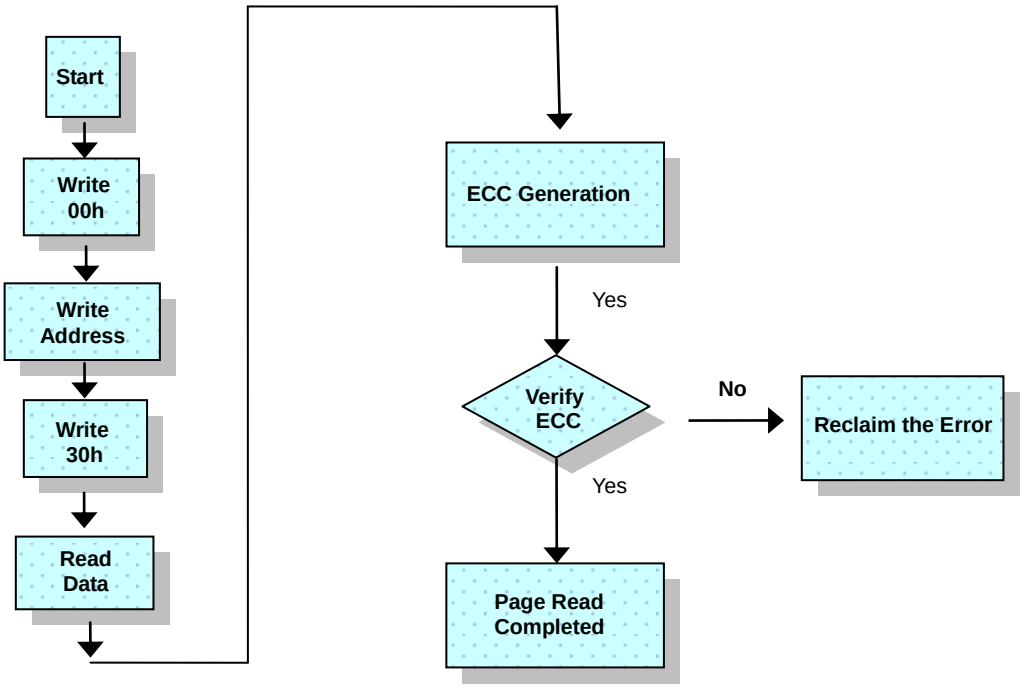
Note: Error Correcting Code → RS Code or BCH Code etc.
Example: 8bit correction / 256Words



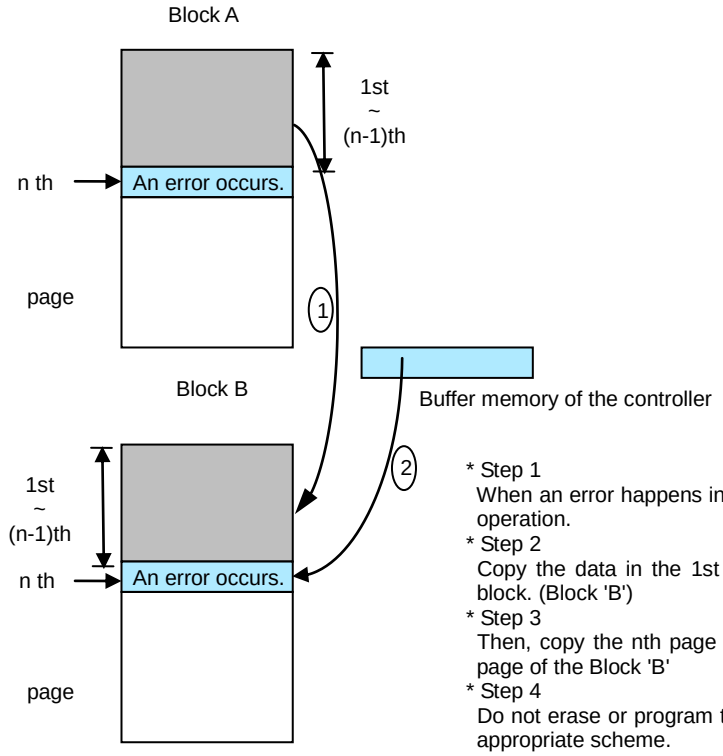
Program Flow Chart



Erase Flow Chart



Read Flow Chart



* Step 1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step 2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step 3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'
* Step 4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

Block Replacement

Function Description

Discovery and Initialization

The device is designed to offer protection from any involuntary program/erase during power transitions. An internal voltage detector disables all functions whenever V_{CC} is below about 2.3V. Max busy time is 5ms after Power-On Reset. During busy time of resetting, the acceptable command is the Read Status (70h).

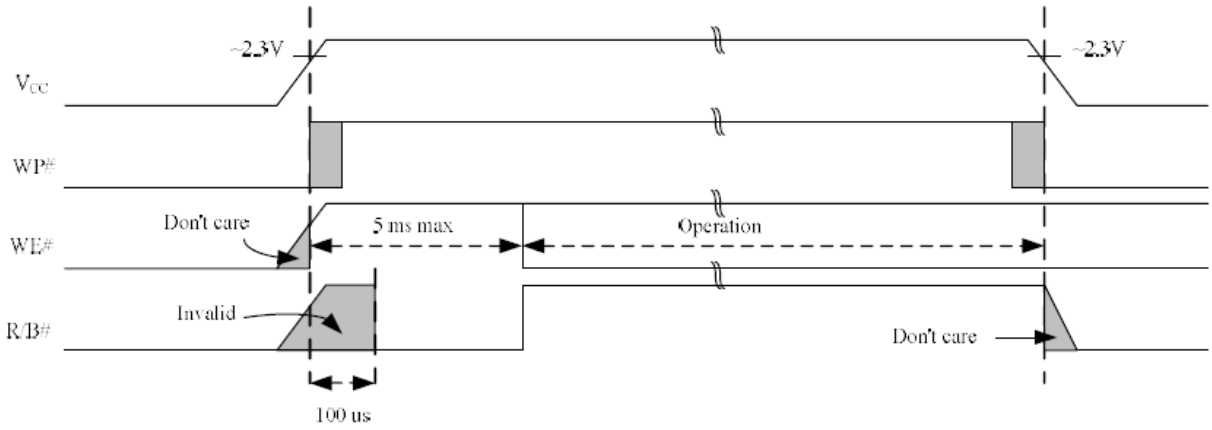
WP# provides hardware protection and is recommended to be kept at V_{IL} during power up and power down. The two step command sequence for program/erase provides additional protection. Figure below defines the Initialization behavior and timings.

Data Protection and Power On Sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device R/B# signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are 70h.

The WP# signal is useful for protecting against data corruption at power on/off.



AC Waveforms for Power Transition

Mode Selection

SDR

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input (5 clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input (5 clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

Note :

1. X can be V_{IL} or V_{IH}.
2. WP# should be biased to CMOS high or CMOS low for standby.

AC Test Condition

(T_A= 0 to 70°C, V_{CC}= 2.7V ~ 3.6V)

Parameter	Single-ended signaling
Input Pulse	0 to V_{CC}
Input Rise and Fall Times	5ns
Input and Output Timing Levels	V_{CC}/2
Output Load*	C_L(50pF) and 1TTL

Note: Refer to Ready/Busy, R/B# output's Busy to Ready time is decided by the pull-up resistor (Rp) tied to the R/B# pin.

Read / Program / Erase Characteristics

(T_A= 0 to 70°C, V_{CC}= 2.7V ~ 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Cell to Register	t_R	-	-	25	us
Program Time	t_{PROG}	-	400	700	us
Last Page Program Time	t_{LPROG}		800	1400	us
Dummy Busy Time for Cache Operation	t_{CBSY}	-	3	750	us
Number of Partial Program Cycles in the Same Page	NOP	-	-	4	cycle
Block Erase Time	t_{BERS}	-	3	10	ms
Data Cache Busy Time in Write Cache (following 15h)	$t_{DCBSYW2}$	-	-	700	us

Note:

1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V Vcc and 25°C temperature.
2. t_{CBSY} max. time depends on timing between internal program completion and data-in.
3. $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.
4. t_{LPROG}=t_{PROG}(last page) + t_{PROG}(last-1 page) – Command load time(last page) – Address load time(last page)-Data load time(last page)

AC Timing Characteristics

SDR (V_{CC} = 2.7~3.6V)

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	t_{CLS}(1)	12	-	ns
CLE Hold Time	t_{CLH}	5	-	ns
CE# Setup Time	t_{CS}(1)	20	-	ns
CE# Hold Time	t_{CH}	5	-	ns
WE# Pulse Width	t_{WP}	12	-	ns
ALE Setup Time	t_{ALS}(1)	12	-	ns
ALE Hold Time	t_{ALH}	5	-	ns
Data Setup Time	t_{DS}(1)	12	-	ns
Data Hold Time	t_{DH}	5	-	ns
Write Cycle Time	t_{WC}	25	-	ns
WE# High Hold Time	t_{WH}	10	-	ns
Address to Data Loading Time	t_{ADL}(2)	70	-	ns
Data Transfer from Cell to Register	t_{R}	-	25	us
ALE to RE# Delay	t_{AR}	10	-	ns
CLE to RE# Delay	t_{CLR}	10	-	ns
Ready to RE# Low	t_{RR}	20	-	ns
Ready to WE# Falling Edge	t_{RW}	20		ns
RE# Pulse Width	t_{RP}	12	-	ns
WE# High to Busy	t_{WB}	-	100	ns
WP# Low to WE# Low (disable mode)	t_{WW}	100	-	ns
WP# High to WE# Low (enable mode)				
Read Cycle Time	t_{RC}	25	-	ns
CE# Low to RE# Low	$\mathbf{t_{CR}}$	9	-	ns
RE# Access Time	t_{REA}	-	20	ns
CE# Access Time	t_{CEA}	-	25	ns
RE# High to Output Hi-Z	t_{RHZ}	-	100	ns
CE# High to Output Hi-Z	t_{CHZ}	-	30	ns
CLE High to Output Hi-Z	$\mathbf{t_{CLHZ}}$	-	30	ns
RE# High to Output Hold	t_{RHOH}	15	-	ns
RE# Low to Output Hold	t_{RLOH}	5		ns
CE# High to Output Hold	t_{COH}	15		ns
RE# High Hold Time	t_{REH}	10	-	ns
Output Hi-Z to RE# Low	t_{IR}	0	-	ns
RE# High to WE# Low	t_{RHW}	100	-	ns
WE# High to CE# Low	t_{WHC}	30		ns

SDR (V_{CC} = 2.7~3.6V)- continued

Parameter		Symbol	Min	Max	Unit
WE# High to RE# Low (Read Status)		t_{WHR1}	60	-	ns
WE# High to RE# Low (Column Address Change in Read)		t_{WHR2}	60	-	ns
Device Resetting Time during…	Ready	t_{RST}	-	5	us
	Read		-	5	us
	Program		-	10	us
	Erase		-	250	us
Data Cache Busy in Read Cache (following 31h and 3Fh)		$t_{DCBSYR1}$		30	us
Data Cache Busy in Page Copy (following 3Ah)		$t_{DCBSYR2}$		30	us

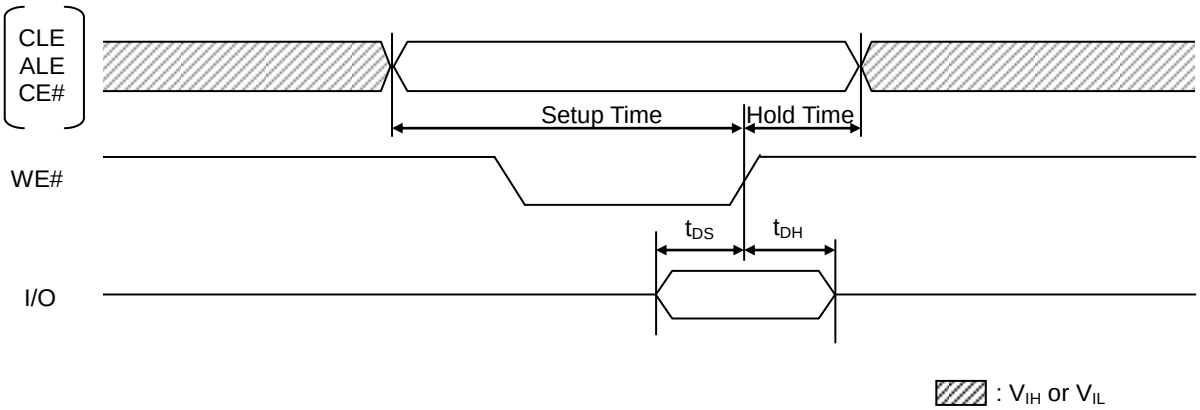
Note:

1. The transition of the corresponding control pins must occur only once while WE# is held low.
2. t_{ADL} is the time from the WE rising edge of final address cycle to the WE# rising edge of first data cycle.

General Timing

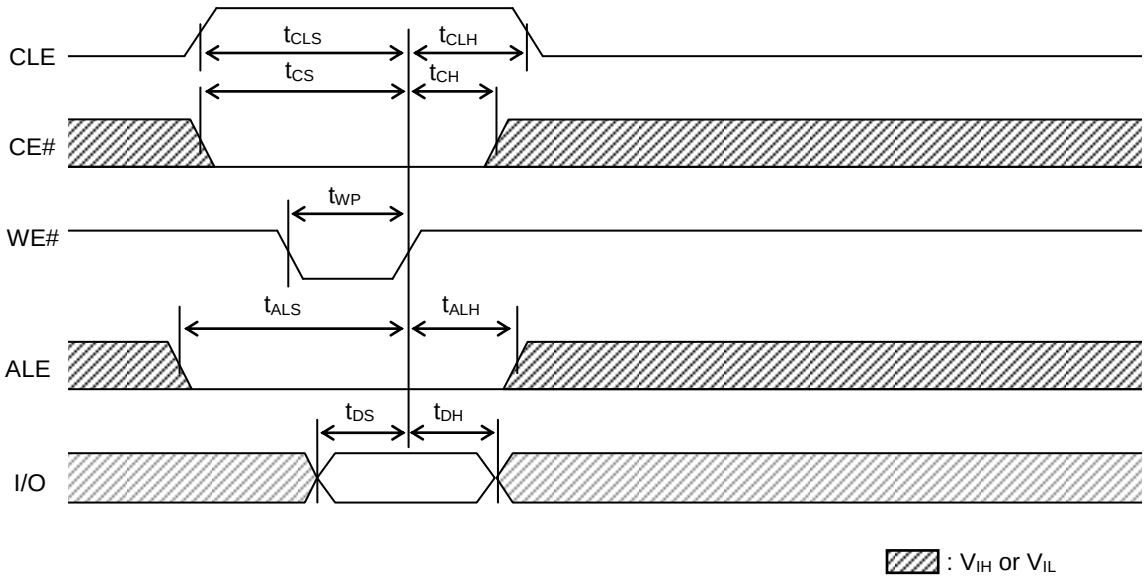
CE bar = CE#
WE bar = WE#
RE bar = RE#
R/ B bar = R/B#

Command/Address/Data Latch Timing



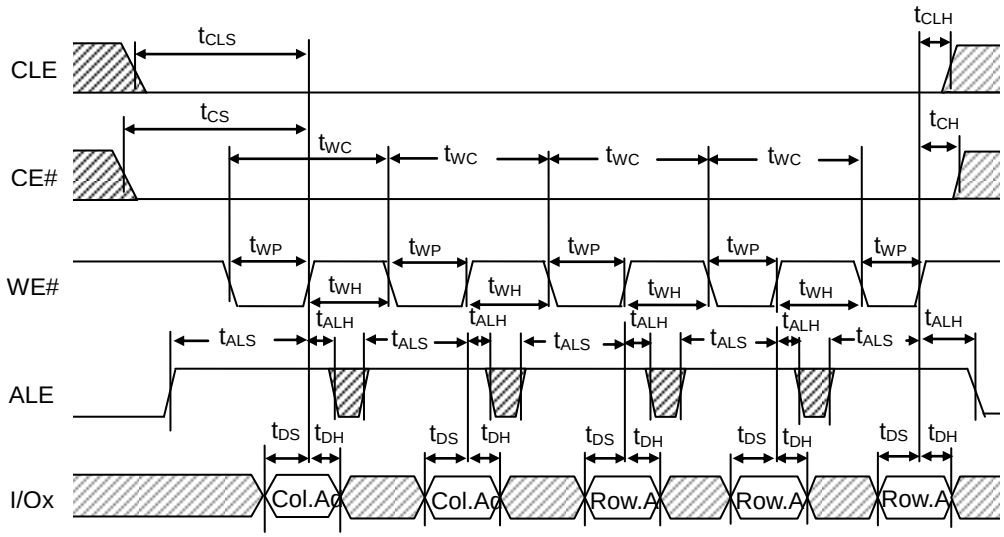
Command/Address/Data Latch Timing

Command Input Cycle



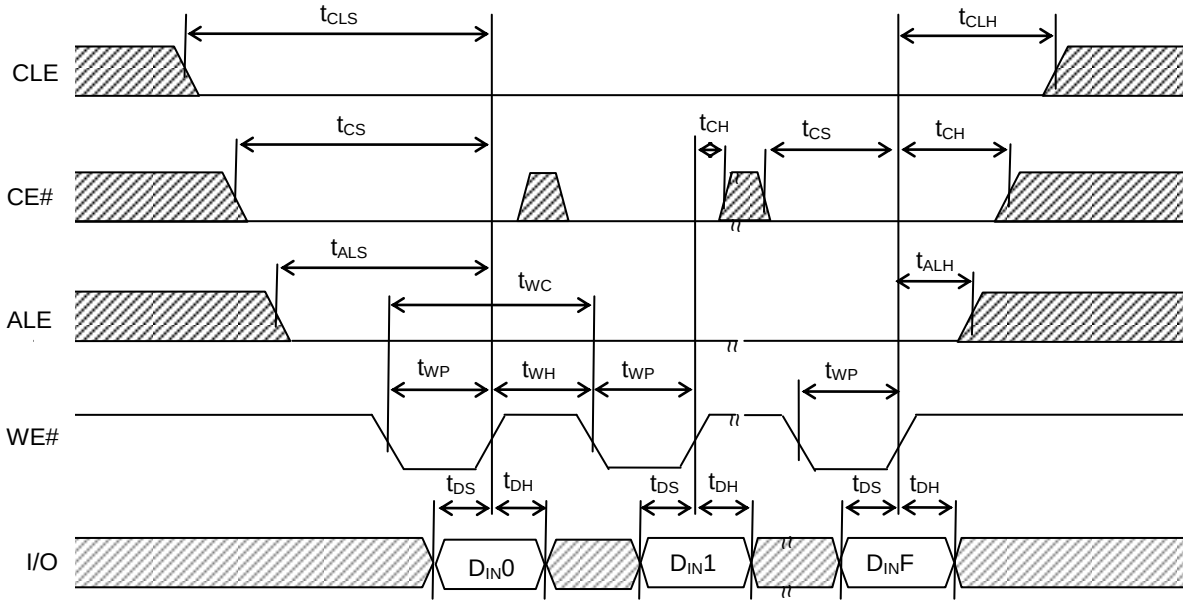
Command Input Cycle Timing

Address Input Cycle



Address Input Cycle Timing

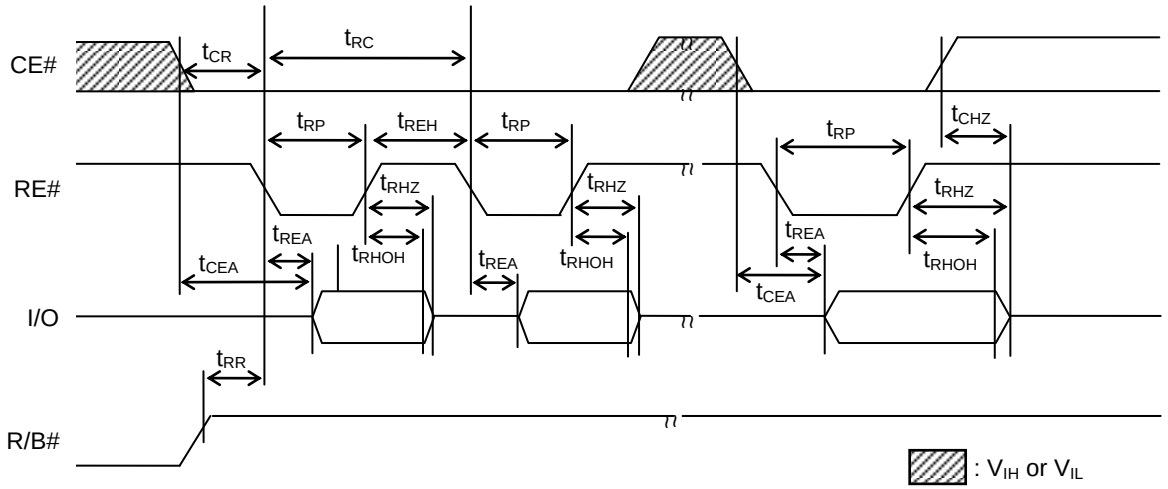
Data Input Cycle



Note: DINF means the Final Data Input.

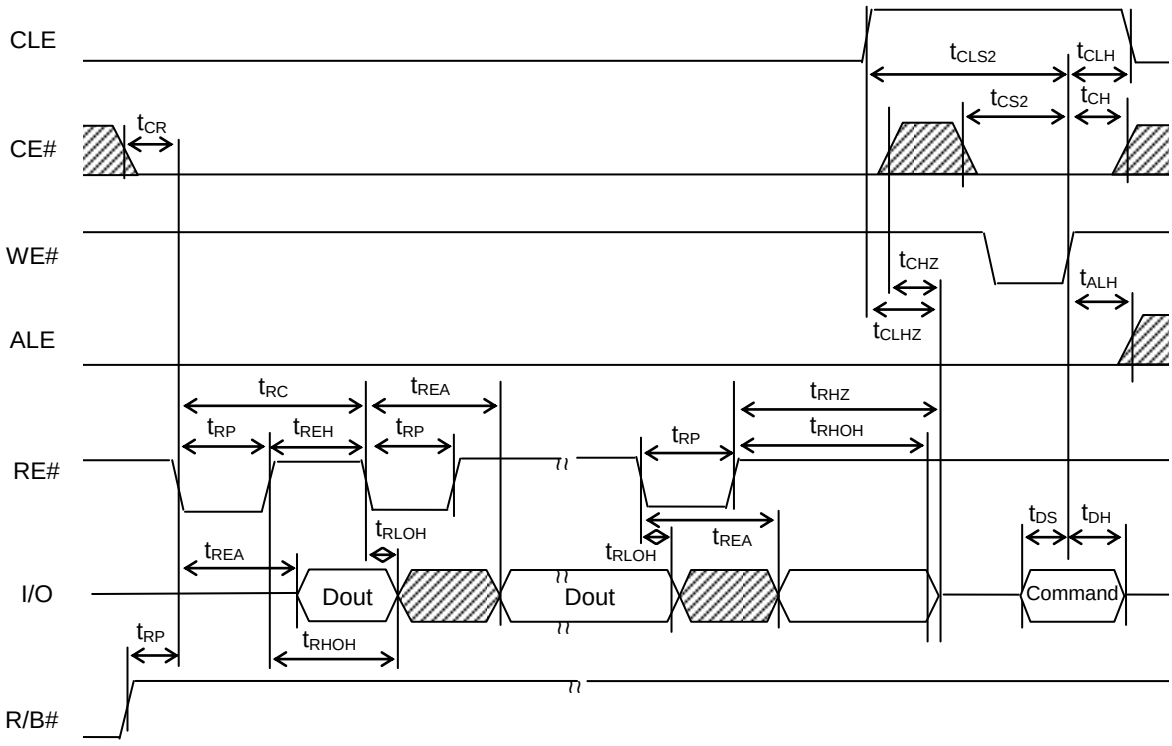
Data Input Cycle Timing

Data Output Cycle



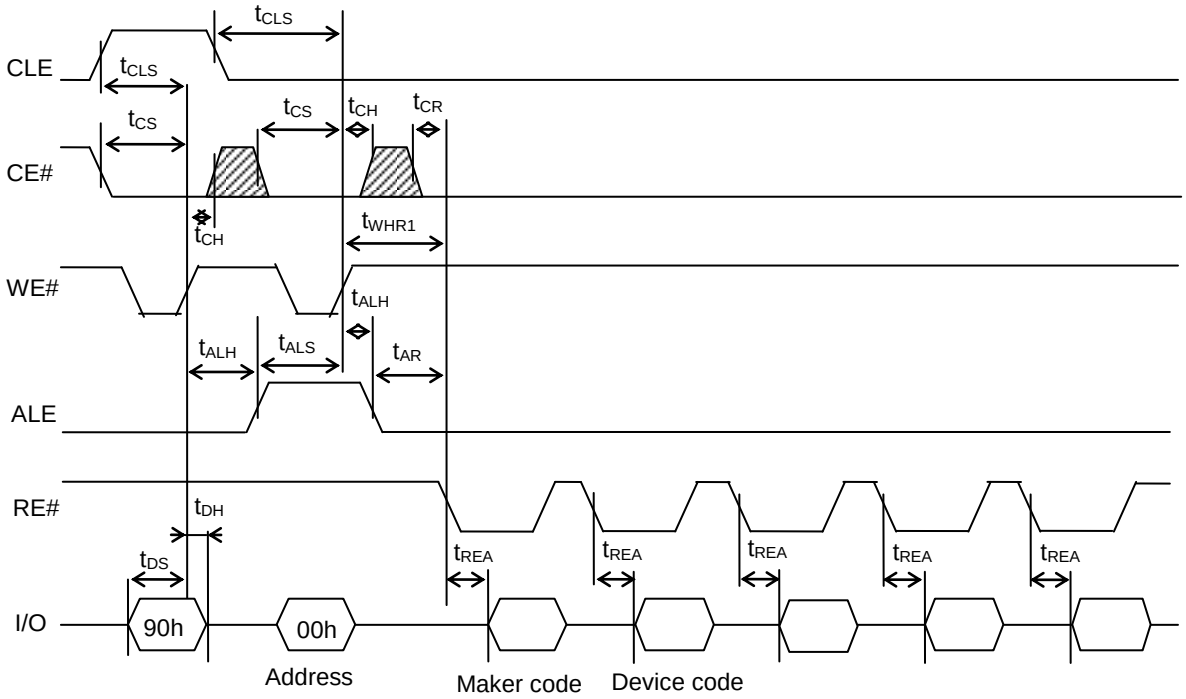
Data Output Cycle Timing

Basic Data Output



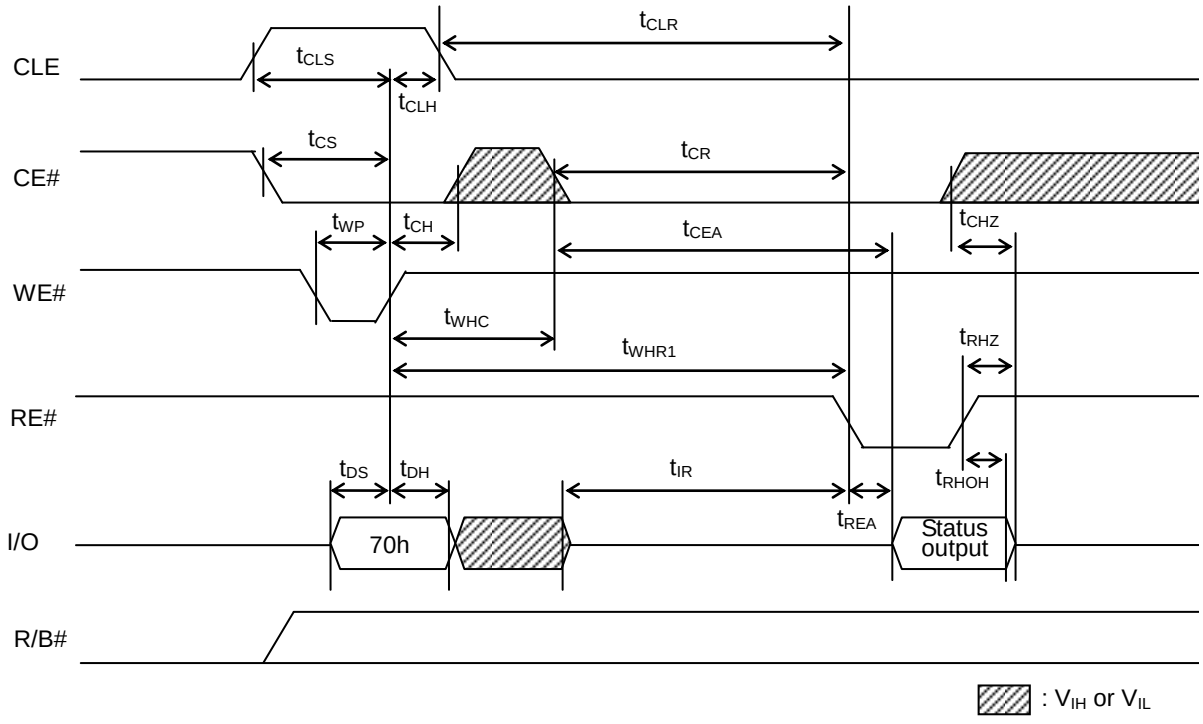
Basic Data Output Timing

Read ID



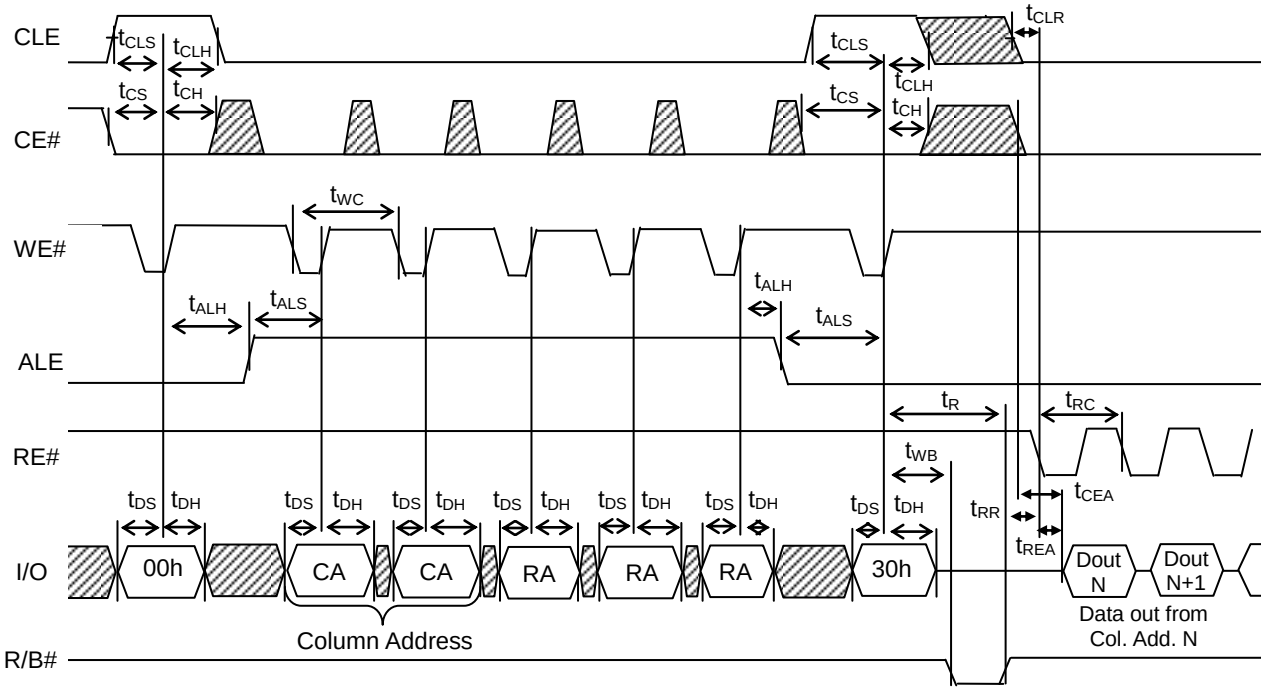
Read ID Operation Timing

Status Read Cycle



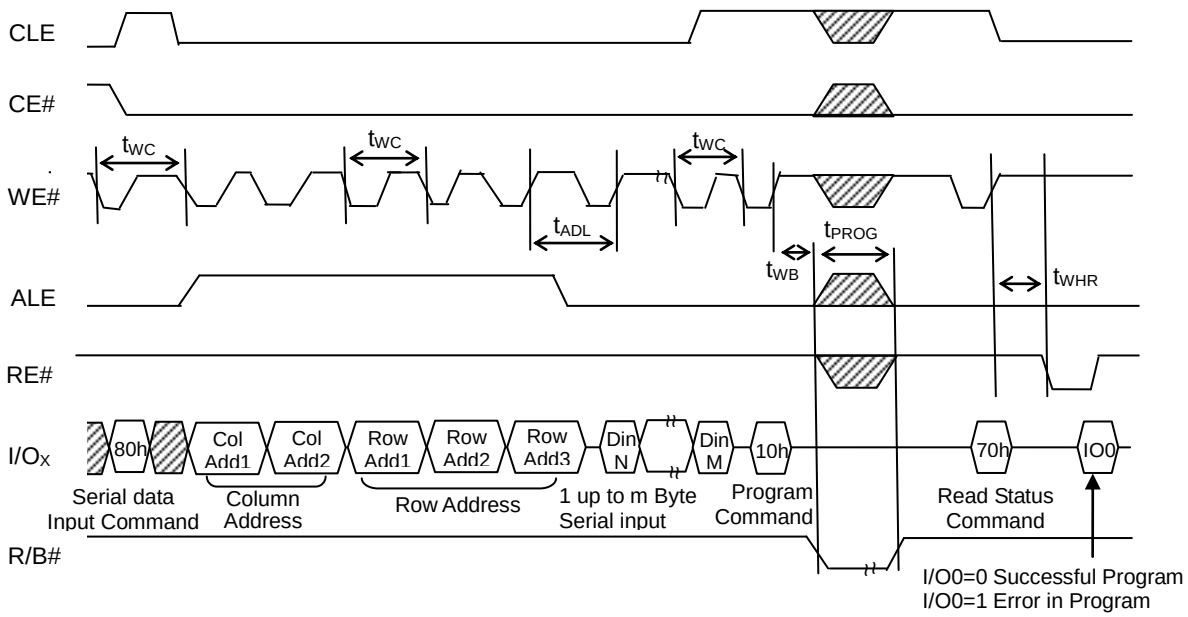
Status Read Cycle Timing

Page Read Operation



Page Read Operation Timing

Page Program Operation



Page Program Operation

Command Description and Device Operation

Command Sets

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy-Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input(1)	85h	-	
Random Data Output(1)	05h	E0h	
Read Status	70h	-	O
Cache Program	80h	15h	
Cache Read	31h	-	
Read Start for Last Page Cache Read	3Fh	-	
Read for Page Copy with Data Out	00h	3Ah	
Auto Program with Data Cache during Page Copy	8Ch	15h	
Auto Program for last page during Page Copy	8Ch	10h	

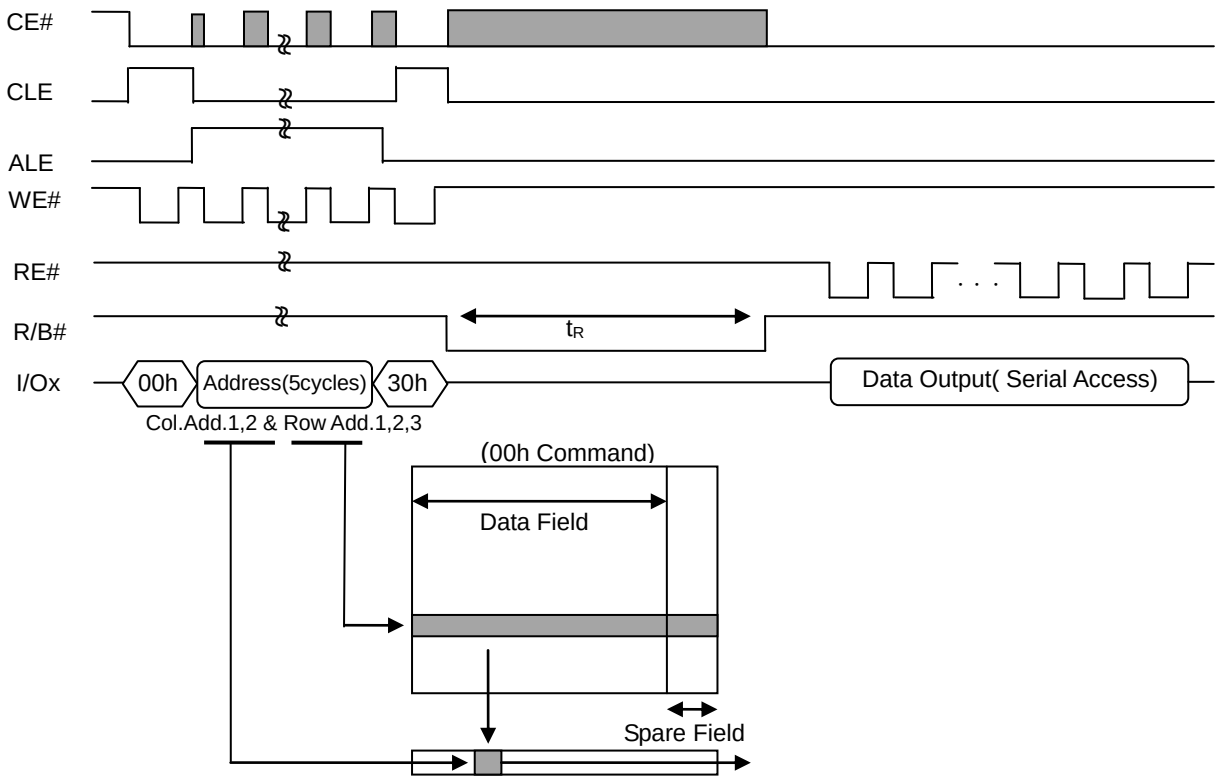
Note:

1. Random Data Input/Output can be executed in a page.

Operations

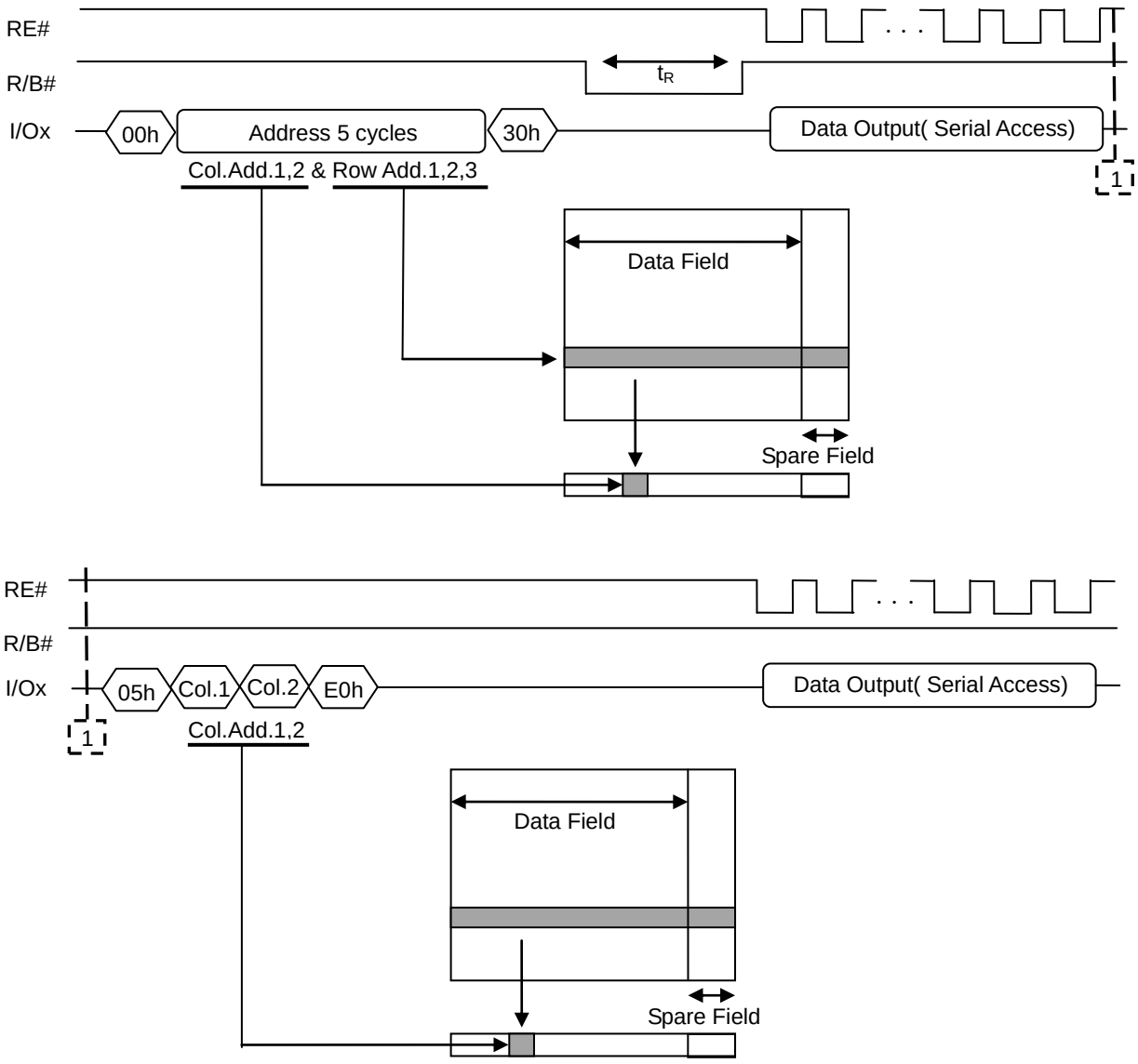
Page Read Operation

The Page Read function reads a page of data identified by row address for the selected LUN. The page of data is made available to be read from the page register starting at the specified column address. Figure below defines the Page Read behavior and timings. Reading beyond the end of a page results in indeterminate values being returned to the host.



Page Read Operation Timing

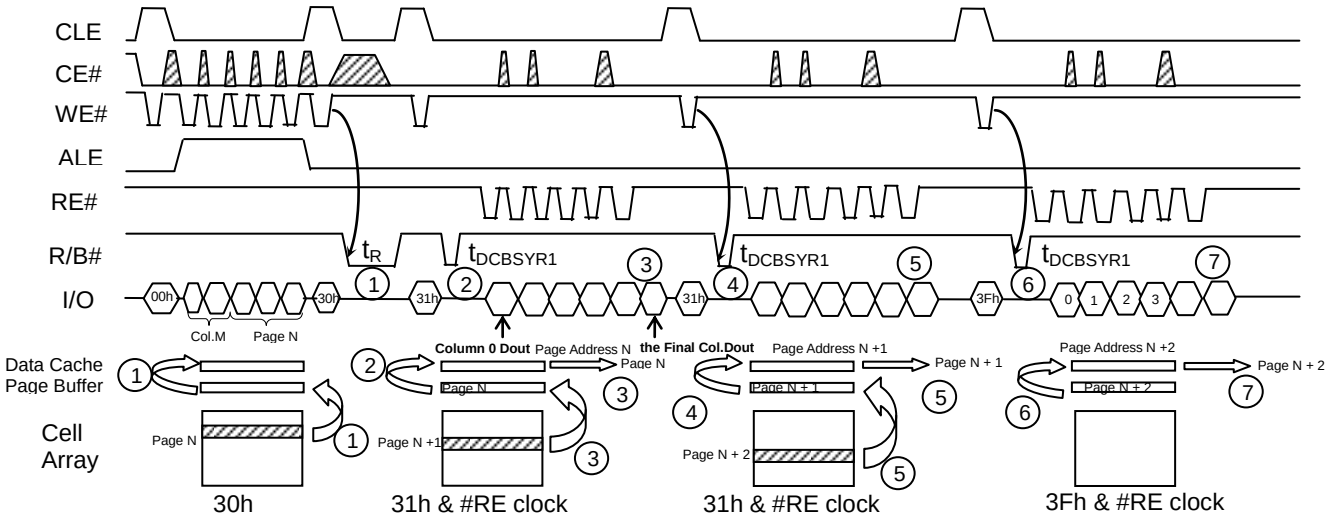
The Random Data Output function changes the column address from which data is being read in the page register for the selected LUN. The Random Data Output command shall only be issued when LUN is in a read idle condition. Figure below defines the Random Data Output behavior and timings. The host shall not read data from the LUN until t_{WHR}(ns) after the second command (i.e. E0h) is written to the LUN.



Random Data Output in a Page Timing

Cache Read Operation

Cache Read is an extension of Page Read, and is available only within a block. The normal Page Read command (00h-30h) is always issued before invoking Cache Read. After issuing the Cache Read command (31h), read data of the designated page (page N) are transferred from data registers to cache registers in a short time period of $t_{DCBSYR1}$, and then data of the next page (page N+1) is transferred to data registers while the data in the cache registers are being read out. Host controller can retrieve continuous data and achieve fast read performance by iterating Cache Read operation. The Read Start for Last Page Cache Read command (3Fh) is used to complete data transfer from memory cells to data registers.



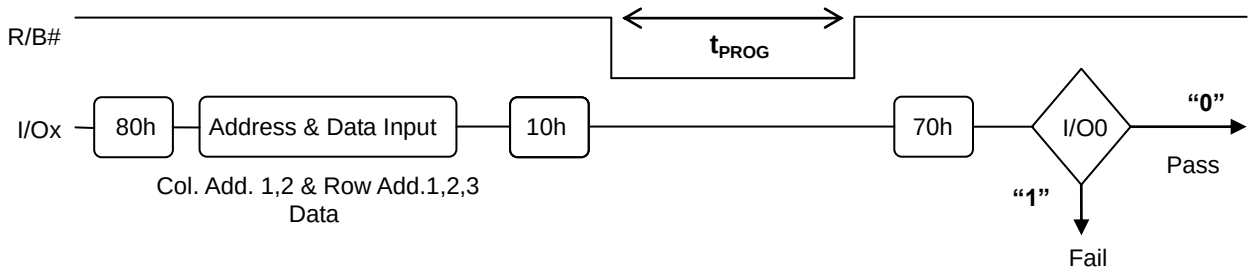
Cache Read Operation Timing

If the 31h command is issued to the device, the data content of the next page is transferred to the Page Buffer during serial data out from the Data Cache, and therefore the t_R (Data transfer from memory cell to data register) will be reduced.

1. Normal read. Data is transferred from Page N to Data cache through Page Buffer. During this time period, the device outputs Busy state for t_R max.
2. After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to Data Cache from Page Buffer again. This data transfer takes $t_{DCBSYR1}$ max and the completion of this time period can be deleted by Ready/Busy signal.
3. Data of Page N + 1 is transferred to Page Buffer from cell while the data of Page N in Data Cache can be read out by /RE clock simultaneously.
4. The 31h command makes data of Page N + 1 transfer to Data Cache from Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for $t_{DCBSYR1}$ max.. This Busy period depends on the combination of the internal data transfer time from cell to Page Buffer and the serial data out time.
5. Data of Page N + 2 is transferred to Page Buffer from cell while the data of Page N + 1 in Data Cache can be read out by /RE clock simultaneously.
6. The 3Fh command makes the data of Page N + 2 transfer to the Data Cache from the Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for $t_{DCBSYR1}$ max.. This Busy period depends on the combination of the internal data transfer time from cell to Page Buffer and the serial data out time.
7. Data of Page N + 2 in Data Cache can be read out, but since the 3Fh command dose not transfer the data from the memory cell to Page Buffer, the device can accept new command input immediately after the completion of serial data out.

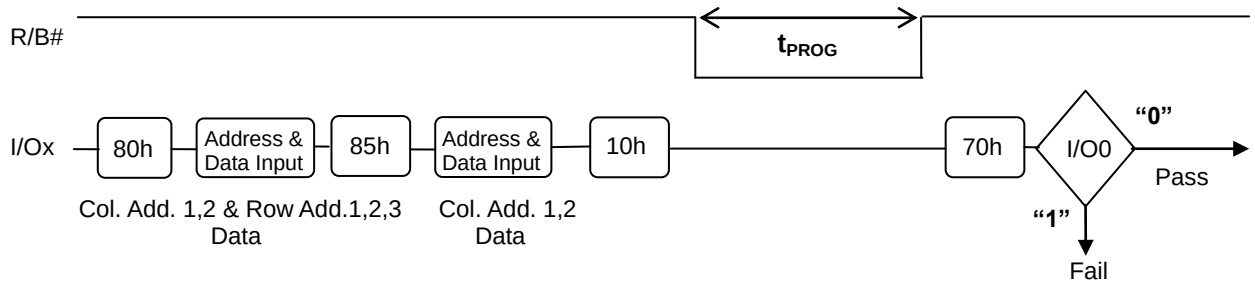
Page Program Operation

The device is programmed basically on a page basis, and each page shall be programmed only one before being erased. The addressing order shall be sequential within a block. The contents of the page register are programmed into the Flash array specified by row address. After t_{PROG} program time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 10h.Figure below defines the Page Program behavior and timings. Writing beyond the end of the page register is undefined.



Program & Read Status Operation Timing

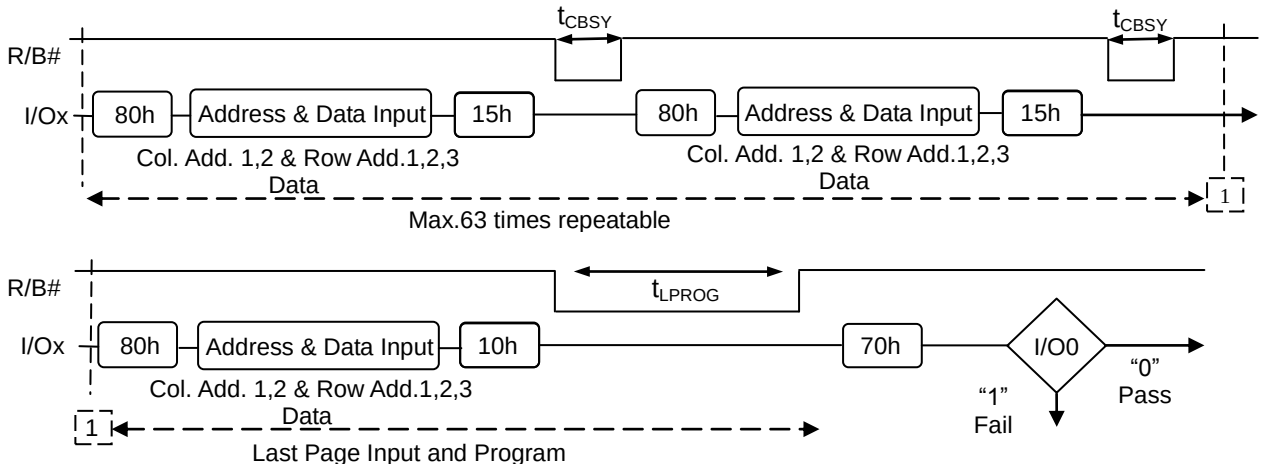
The device supports random data input in a page. The column address for the next data, which will be written, may be changed to the address using Random Data Input command (i.e. 85h). Random data input may be operated multiple times without limitation.



Random Data Input in a Page Timing

Cache Program Operation

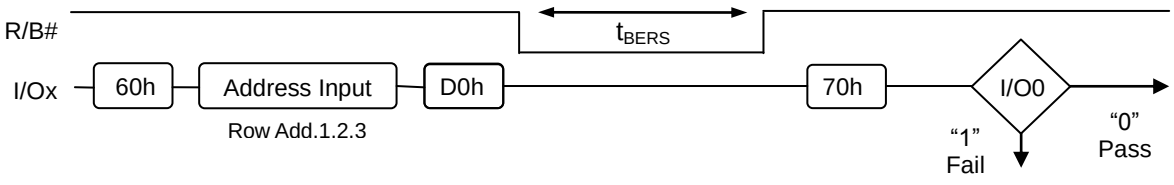
The Cache Program function allows the host to write the next data for another page to the page register while a page of data to be programmed to the Flash array for the selected LUN. When command 15h is issued, R/B# returns high (i.e. ready) when a cache register is ready to be written after data in the cache register is transferred to a page register. However, when command 10h is issued for the final page, R/B# turns to high after outstanding program operation performed by previous Cache Program command and the program operation for the final page is completed. SR[0] is valid for this command after SR[5] transitions from zero to one until the next transition. SR[1] is valid for this command after SR[6] transitions from zero to one, and it is invalid after the first Cache Program command completion since there is no previous Cache Program operation. Cache Program operation shall work only within a block. Figure below defines the Cache Program behavior and timings. Note that t_{LPROG} at the end of the caching operation may be longer than typical as this time also includes completing the programming operation for the previous page. Writing beyond the end of the page register is undefined.



Cache Program Operation Timing

Block Erase Operation

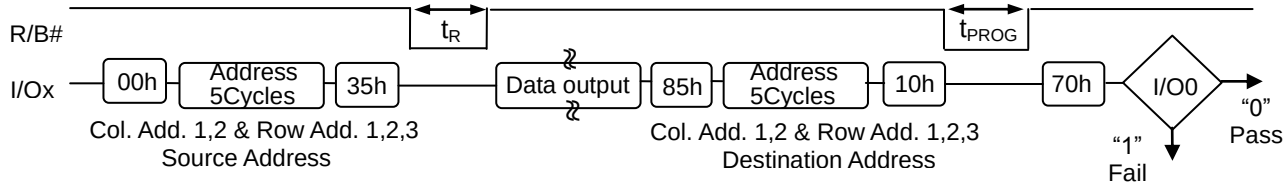
The Block Erase operation is done on a block basis. Only three cycles of row addresses are required for Block Erase operation and a page address within the cycles is ignored while block address are valid. After Block Erase operation passes, all bits in the block shall be set to one. SR[0] is valid for this command after SR[6] transitions from zero to one (i.e. the selected LUN is ready) until the LUN goes in busy state by a next command. Figure below defines the Block Erase behavior and timings.



Block Erase Operation Timing

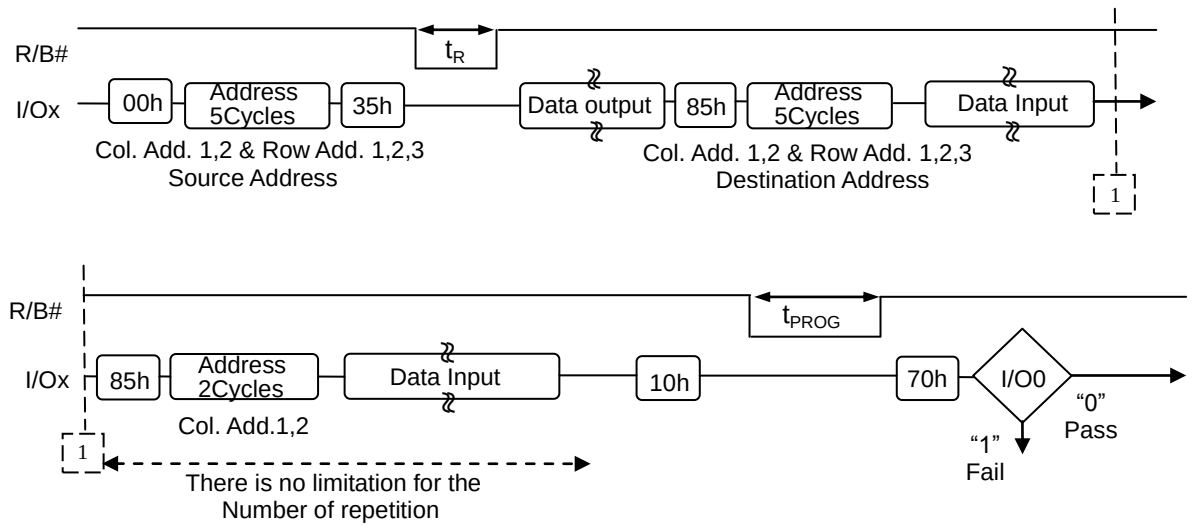
Copy-Back Program Operation

The Copy-Back Program with Read for Copy-Back is configured to efficiently rewrite data stored in a page without data re-loading when no error within the page is found. Since the time consuming re-loading cycles are removed, copy-back operation helps the system performance improve. The benefit is especially obvious when a part of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. A read operation with "35h" command and the address of the source page moves the whole 2,176-word data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status bit(I/O 0) may be checked. The Copy-Back operation consists of Read for Copy-Back and Copy-Back Program. A host reads a page of data from a source page using Read for Copy-Back and copies read data back to a destination page on the same LUN by Copy-Back Program command.



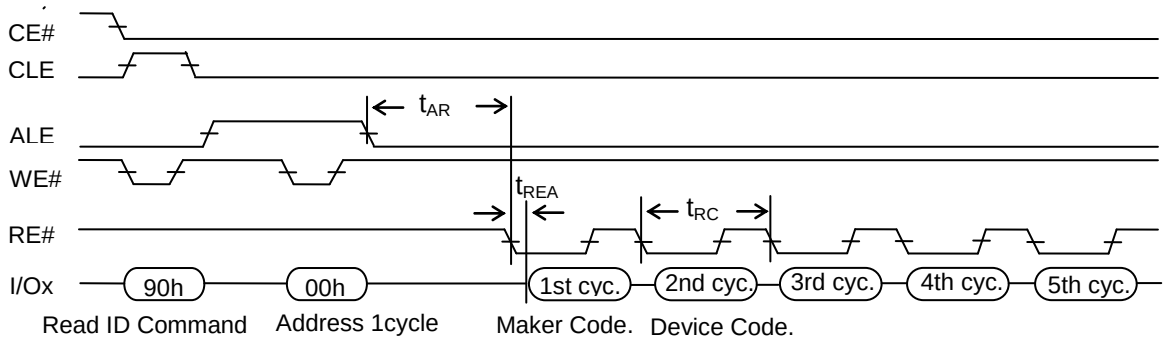
Page Copy-Back Program Operation Timing

After a host completes to read data from a page register, the host may modify data using Random Data Input command if required. Figure below defines Copy-Back Program with Random Data Input behavior and timings.



Page Copy-Back Program Operation with Random Data Input

Read ID



Read ID Timing

Read ID (00h Address ID Cycle)

Users can read six bytes of ID containing manufacturer code, device code and architecture information of the target by command 90h followed by 00h address. The command register remains in Read ID mode until another command is issued.

	Description	X16 device
1st Byte	Maker Code	C8h
2nd Byte	Device Code	ACh
3rd Byte	Internal Chip Number, Cell Type, etc	80h
4th Byte	Page Size, Block Size, etc	1Ah
5th Byte	Plane Number, ECC Level	30h

2nd ID Data

Item	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Density	1Gb					0	0	0	1
	2Gb					1	0	1	0
	4Gb					1	1	0	0
	8Gb					0	0	1	1
	16Gb					0	1	0	1
Voltage	1.8V			0	1				
	3.3V			1	0				
Interface	SPI	0	0						
	X8	0	1						
	X16	1	0						

3rd ID Data

Item	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleave Program Between Multiple Chips	Not Support		0						
	Support		1						
Cache Program	Not Support	0							
	Support	1							

4th ID Data

Item	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Page Size (w/o redundant area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Block Size (w/o redundant area)	128KB	0		0	0				
	256KB	0		0	1				
	512KB	0		1	0				
	1MB	0		1	1				
	Reserved	1		0	0				
	Reserved	1		0	1				
	Reserved	1		1	0				
	Reserved	1		1	1				
Redundant Area Size (Byte / Page Size)	Reserved		0			0	0		
	128B		0			0	1		
	224B		0			1	0		
	400B		0			1	1		
	436B		1			0	0		
	512B		1			0	1		
	640B		1			1	0		
	1KB		1			1	1		

5th ID Data

Item	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Plane Number	1					0	0	0	
	2					0	1	0	
	4					1	0	0	
	8					1	1	0	
	16					1	1	1	
ECC Level	1bit		0	0	0				
	2bit		0	0	1				
	4bit		0	1	0				
	8bit		0	1	1				
	12bit		1	0	0				
	24bit		1	0	1				
	40bit		1	1	0				
	60bit		1	1	1				
Reserved	Reserved	0							0

Read Status

The Read Status function (command 70h) retrieves a status value for the last operation issued in the case of one-plane operations. Both 70h is followed without address setting. Specifically, Read Status return the combined status values of the independent status register bits according to Table below.

Read Status Definition

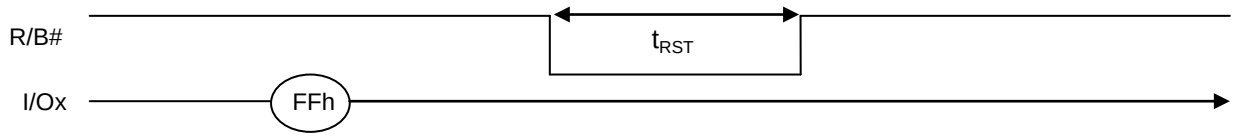
	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
Definition	Pass: 0 Fail: 1	Pass: 0 Fail: 1	Reserved	Reserved	Reserved	Busy: 0 Ready: 1	Busy: 0 Ready: 1	Protected: 0 Not Protected: 1
Read	NA	NA	NA	NA	NA	NA	Busy/Ready	Write Protect
Cache Read	NA	NA	NA	NA	NA	Flash array Busy/Ready	Host Busy/Ready	Write Protect
Page Program	Pass/Fail	NA	NA	NA	NA	NA	Busy/Ready	Write Protect
Cache Program	Pass/Fail	(N-1) Pass/Fail	NA	NA	NA	Flash array Busy/Ready	Host Busy/Ready	Write Protect
Block Erase	Pass/Fail	NA	NA	NA	NA	NA	Busy/Ready	Write Protect

Note:

1. During Block Erase, Page Program or Copy-Back operation, I/O0 is only valid when I/O6 shows the Ready state.
2. During Cache Program operation, I/O0 is only valid when I/O5 shows the Ready state, and I/O1 is only valid when I/O6 shows the Ready state.

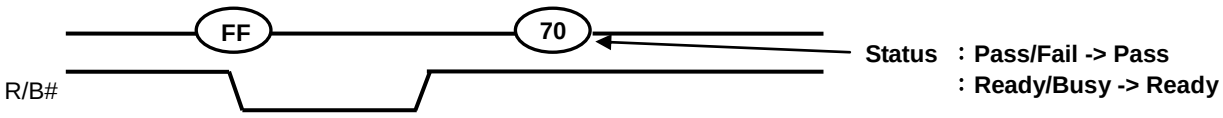
Reset

The device offers a reset function by command FFh. When the device is in 'Busy' state during any operation, the Reset operation will abort these operations except during power-on when Reset shall not be issued until R/B# is set to one (i.e. ready). The contents of memory cells being programmed are no longer valid, as the data will be partially programmed or erased. Although the device is already in process of reset operation, a new Reset command will be accepted.



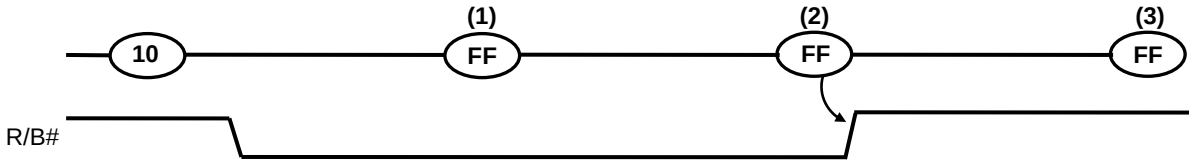
Reset Timing

When Status Read command (70h) is input after Reset Operation



Status Read after Reset operation

When two or more Reset commands are input in succession

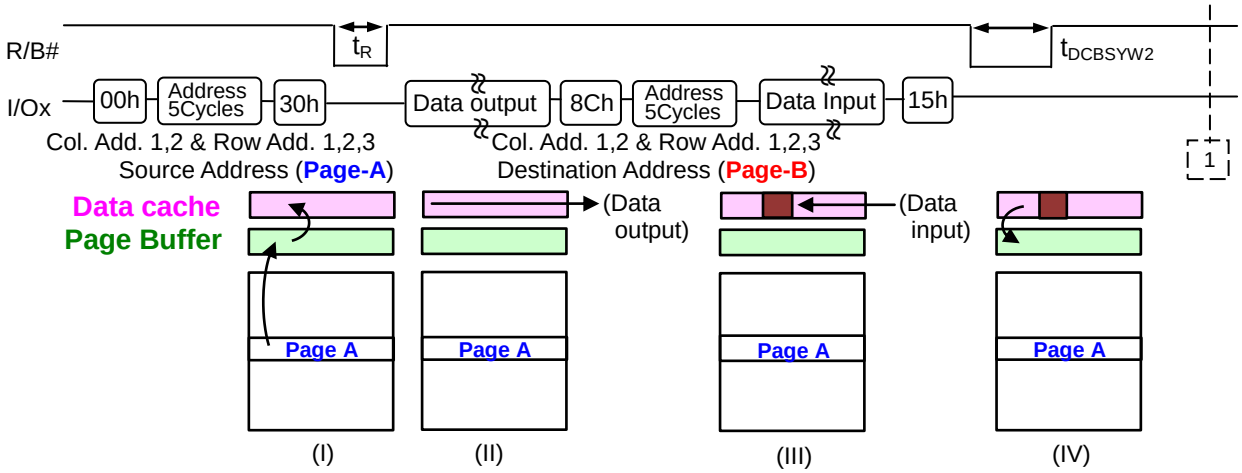


The second FF command is invalid, but the third FF command is valid.

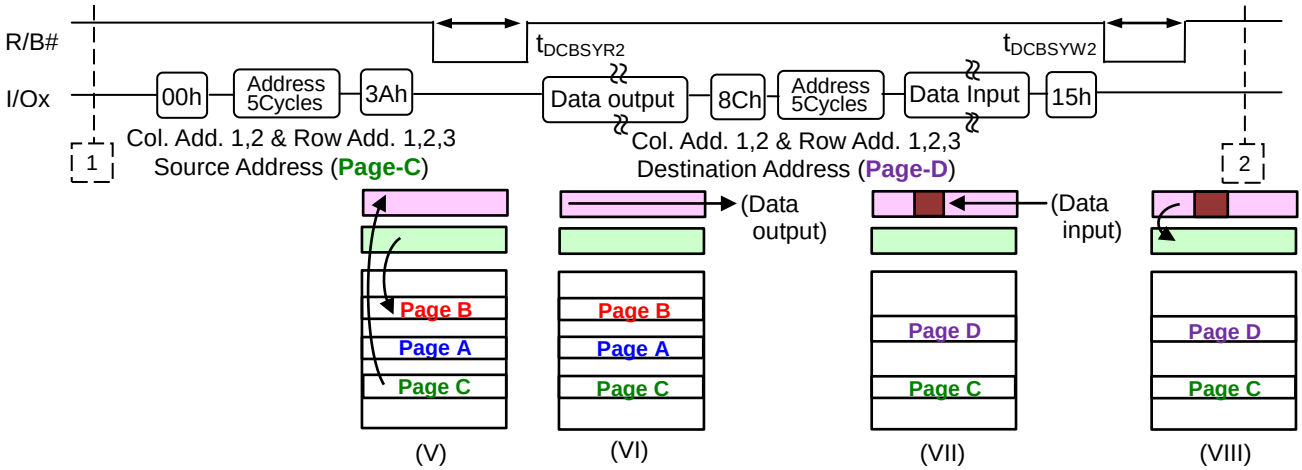
Successive Reset operation

Page Copy

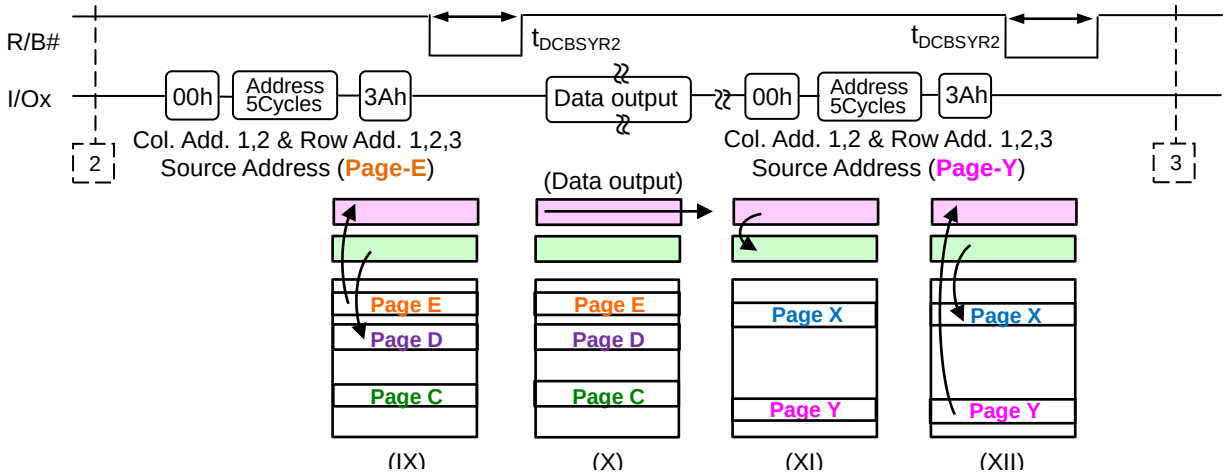
By using Page Copy, data in a page can be copied to another page after the data has been read out. When the block address changes (increments) this sequenced has to be started from the beginning.



I. Data for Page A is transferred to the Data Cache
II. Data for Page A is read out
III. Copy Page address B is input and if the data needs to be changed, changed data is input
IV. Data Cache for Page B is transferred to the Page Buffer



V. Data for Page C is transferred to Data Cache while the data of Page B is being programmed
VI. After the Ready state, Data for Page C is output from the Data Cache
VII. Copy Page address D is input and if the data needs to be changed, changed data is input
VIII. After programming of page B is completed, Data Cache for Page D is transferred to the Page Buffer

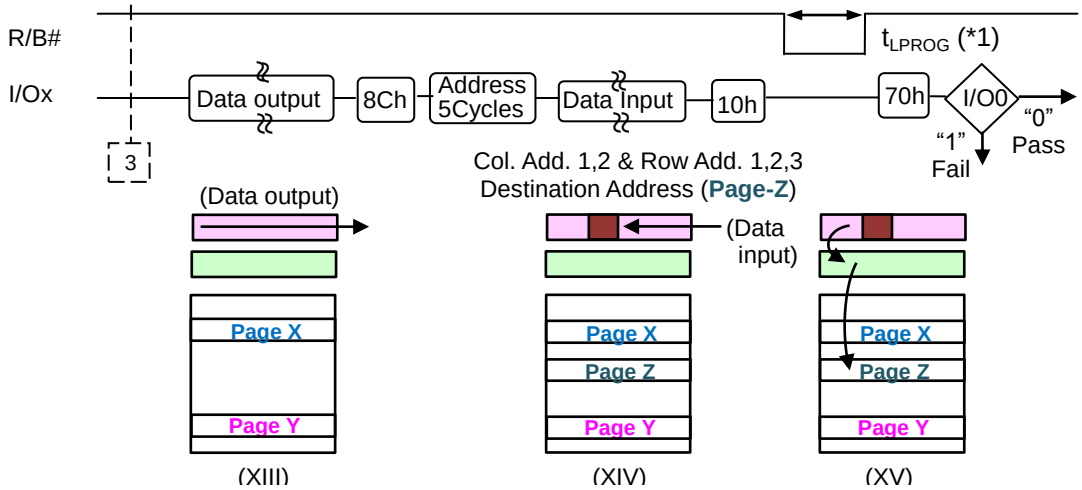


IX. By the 15h command, the data in the Page Buffer is programmed to Page D. Data for Page E is transferred to the Data cache

X. Data for Page E is read out

XI. Data Cache for Page X is transferred to the Page Buffer

XII. The data in the Page Buffer is programmed to Page X. Data for Page Y is transferred to the Data Cache



XIII. After the Ready state, Data for Page Y is output from the Data Cache

XIV. Copy Page address Z is input and if the data needs to be changed, changed data is input

XV. By issuing the 10h command, the data in the Page Buffer is programmed to Page Z

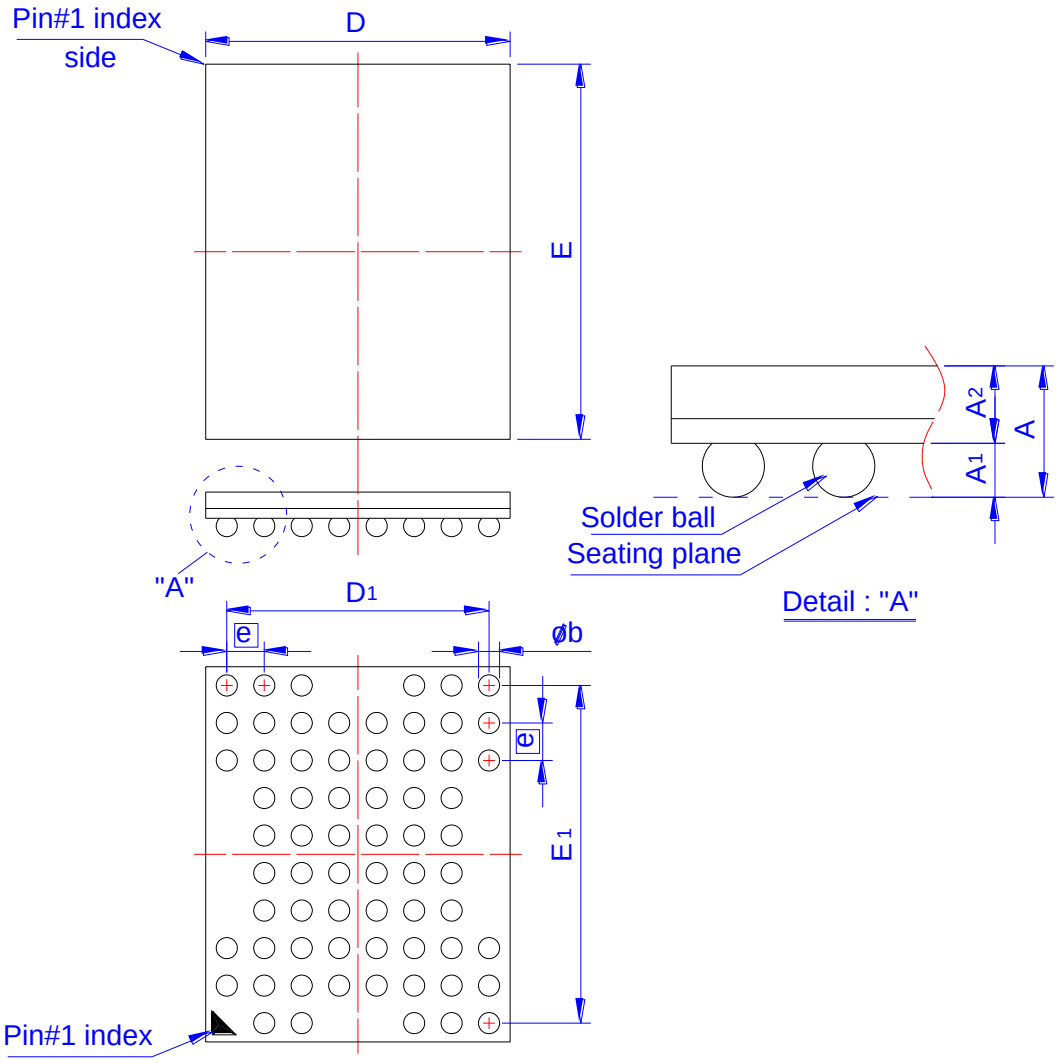
(*1) Since the last page programming by the 10h command is initiated after the previous cache program, the tLPROG here will be expected as the following,
tLPROG = tPROG of the last page + tPROG of the previous page - (command input cycle + address input cycle + data output/input cycle time of the last page)

NOTE)
Data input is required only if previous data output needs to be altered.
If the data has to be changed, locate the desired address with the column and page address input after the 8Ch command, and change only the data that needs be changed.
If the data does not have to be changed, data input cycles are not required.

Make sure WP is held to High level when Page Copy operation is performed.
Also make sure the Page Copy operation is terminated with 8Ch-10h command sequence

PACKING DIMENSIONS

67-BALL (6.5x8 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	---	---	1.00	---	---	0.039
A_1	0.34	---	0.44	0.013	---	0.017
A_2	---	0.56	---	---	0.022	---
Φ_b	0.41	0.46	0.51	0.016	0.018	0.020
D	6.40	6.50	6.60	0.252	0.256	0.260
E	7.90	8.00	8.10	0.311	0.315	0.319
D_1	5.60 BSC			0.220 BSC		
E_1	7.20 BSC			0.283 BSC		
e	0.80 BSC			0.031 BSC		

Controlling dimension : Millimeter.
(Revision date : Nov 02 2019)

Revision History

Revision	Date	Description
0.1	2019.11.27	Original
0.2	2020.01.17	1. Modify Read ID 2. Correct typo

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