

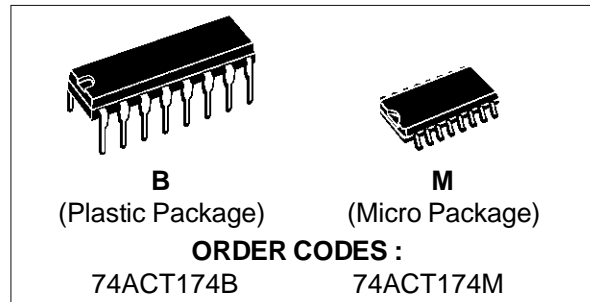
## HEX D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED:  
 $f_{MAX} = 200 \text{ MHz (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 8 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS  
 $V_{IH} = 2\text{V (MIN)}, V_{IL} = 0.8\text{V (MAX)}$
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 24 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC} \text{ (OPR)} = 4.5\text{V to } 5.5\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 174
- IMPROVED LATCH-UP IMMUNITY

### DESCRIPTION

The ACT174 is an high-speed CMOS HEX D-TYPE FLIP FLOP WITH CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power applications maintaining high speed operation similar to equivalent Bipolar Schottky

### PRELIMINARY DATA



TTL.

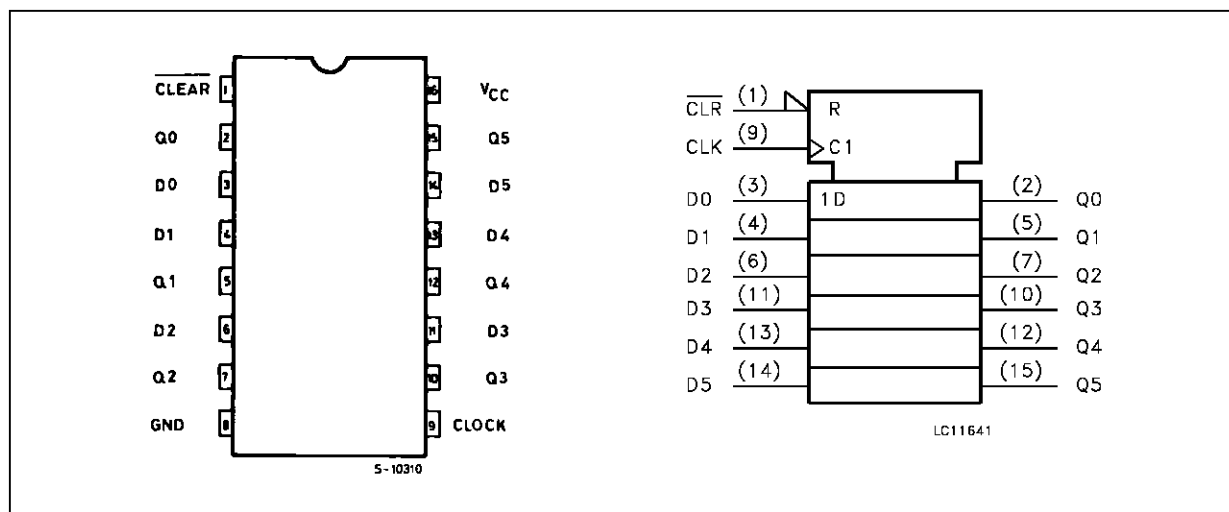
Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse.

When the CLEAR input is held low, the Q outputs are held low independently of the other inputs .

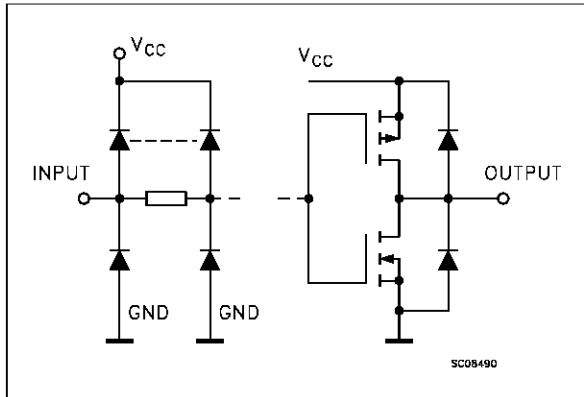
The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

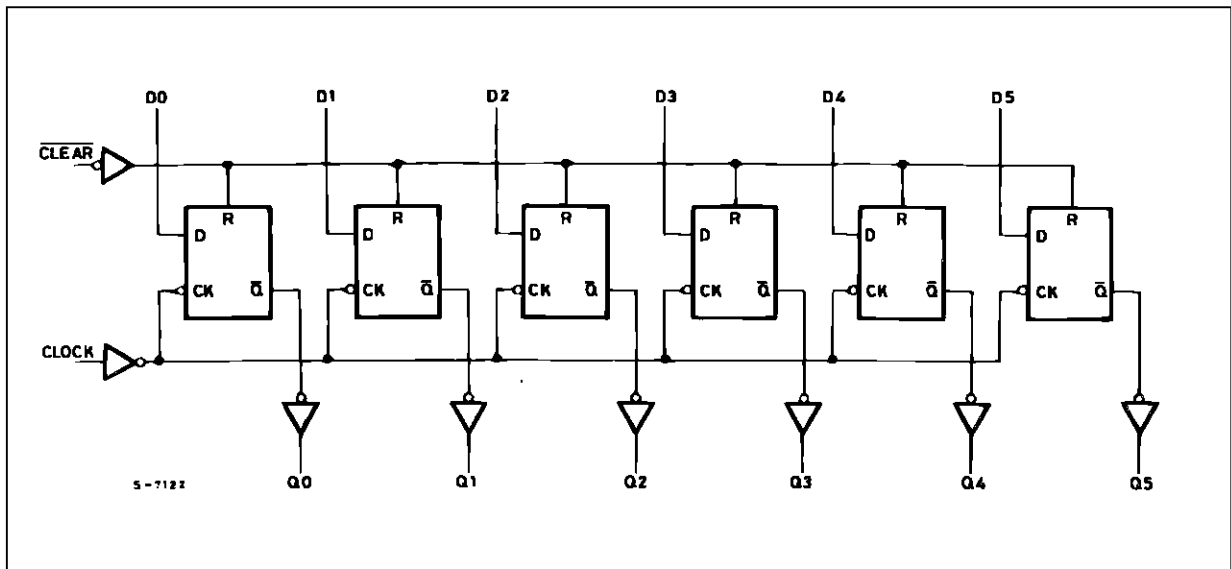
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Asynchronous Master Reset (Active LOW)
2, 5, 7, 10, 12, 15	Q0 to Q5	Flip-Flop Output
3, 4, 6, 11, 13, 14	D0 to D5	Data Inputs
9	CLOCK	Clock Input (LOW-to-HIGH, Edge- Triggered)
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
$\overline{\text{CLEAR}}$	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L		L	
H	H		H	
H	X		Q <sub>n</sub>	NO CHANGE

X: Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
I <sub>OK</sub>	DC Output Diode Current	± 20	mA
I <sub>O</sub>	DC Output Current	± 50	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 300	mA
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	4.5 to 5.5	V
V <sub>I</sub>	Input Voltage	0 to V <sub>CC</sub>	V
V <sub>O</sub>	Output Voltage	0 to V <sub>CC</sub>	V
T <sub>op</sub>	Operating Temperature:	-40 to +85	°C
dt/dv	Input Rise and Fall Time V <sub>CC</sub> = 4.5 to 5.5V (note 1)	8	ns/V

1) V<sub>IN</sub> from 0.8 V to 2.0 V

## DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit	
				V <sub>CC</sub> (V)	T <sub>A</sub> = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	4.5	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V	2.0	1.5		2.0		V	
		5.5		2.0	1.5		2.0			
V <sub>IL</sub>	Low Level Input Voltage	4.5	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V		1.5	0.8		0.8	V	
		5.5			1.5	0.8		0.8		
V <sub>OH</sub>	High Level Output Voltage	4.5	V <sub>I</sub> <sup>(*)</sup> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = -50 μA	4.4	4.49		4.4	V	
		5.5		I <sub>O</sub> = -50 μA	5.4	5.49		5.4		
		4.5		I <sub>O</sub> = -24 mA	3.86			3.76		
		5.5		I <sub>O</sub> = -24 mA	4.86			4.76		
V <sub>OL</sub>	Low Level Output Voltage	4.5	V <sub>I</sub> <sup>(*)</sup> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 50 μA		0.001	0.1	0.1	V	
		5.5		I <sub>O</sub> = 50 mA		0.001	0.1	0.1		
		4.5		I <sub>O</sub> = 24 mA			0.36	0.44		
		5.5		I <sub>O</sub> = 24 mA			0.36	0.44		
I <sub>I</sub>	Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			±0.1		±1	μA	
I <sub>CCT</sub>	Max I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V		0.6			1.5	mA	
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			8		80	μA	
I <sub>OLD</sub>	Dynamic Output Current (note 1, 2)	5.5	V <sub>OLD</sub> = 1.65 V max					75	mA	
I <sub>OHD</sub>			V <sub>OHD</sub> = 3.85 V min					-75	mA	

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50 Ω.

(\*) All outputs loaded.

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ ,  $R_L = 500 \Omega$ , Input  $t_r = t_f = 3 \text{ ns}$ )

Symbol	Parameter	Test Condition		Value					Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time CK to Q	5.0 <sup>(*)</sup>		1.5	7.0	10.5		11.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time CLR to Q	5.0 <sup>(*)</sup>		1.5	6.5	9.5		11.0	ns
t <sub>wL</sub>	CLR pulse Width, LOW	5.0 <sup>(*)</sup>			1.5	3.0		3.5	ns
t <sub>w</sub>	CK pulse Width	5.0 <sup>(*)</sup>			1.5	3.0		3.5	ns
t <sub>s</sub>	Setup Time Q to CK HIGH or LOW	5.0 <sup>(*)</sup>			0.5	1.5		1.5	ns
t <sub>h</sub>	Hold Time Q to CK HIGH or LOW	5.0 <sup>(*)</sup>			1.0	2.0		2.0	ns
t <sub>REM</sub>	Recovery Time CLR to CK	5.0 <sup>(*)</sup>			-1.0	0.5		0.5	ns
f <sub>MAX</sub>	Maximum Clock Frequency	5.0 <sup>(*)</sup>		165	200		140		MHz

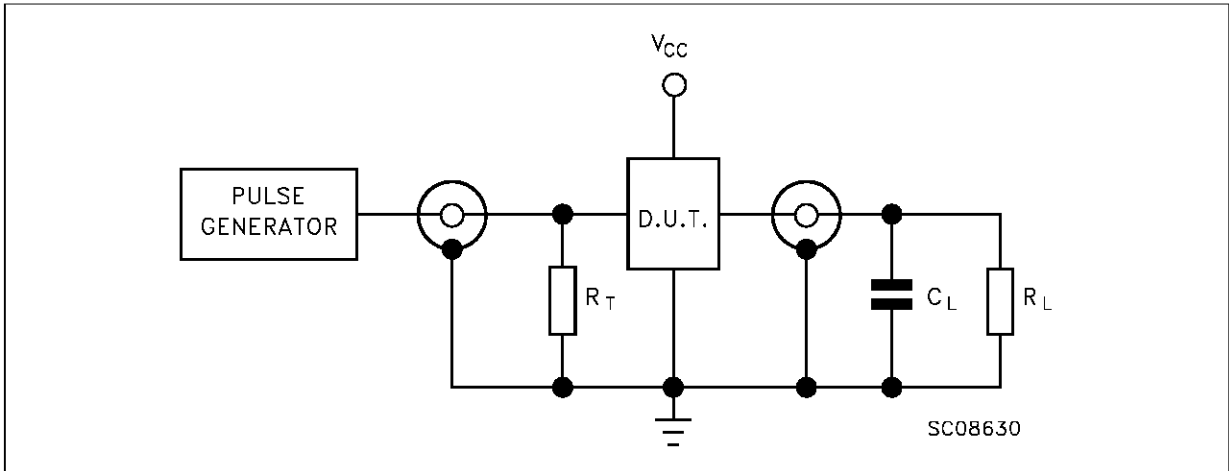
(\*) Voltage range is 5V ± 0.5V

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions		Value					Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C <sub>IN</sub>	Input Capacitance	5.0			4				pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	5.0	f <sub>IN</sub> = 10 MHz		TBD				pF

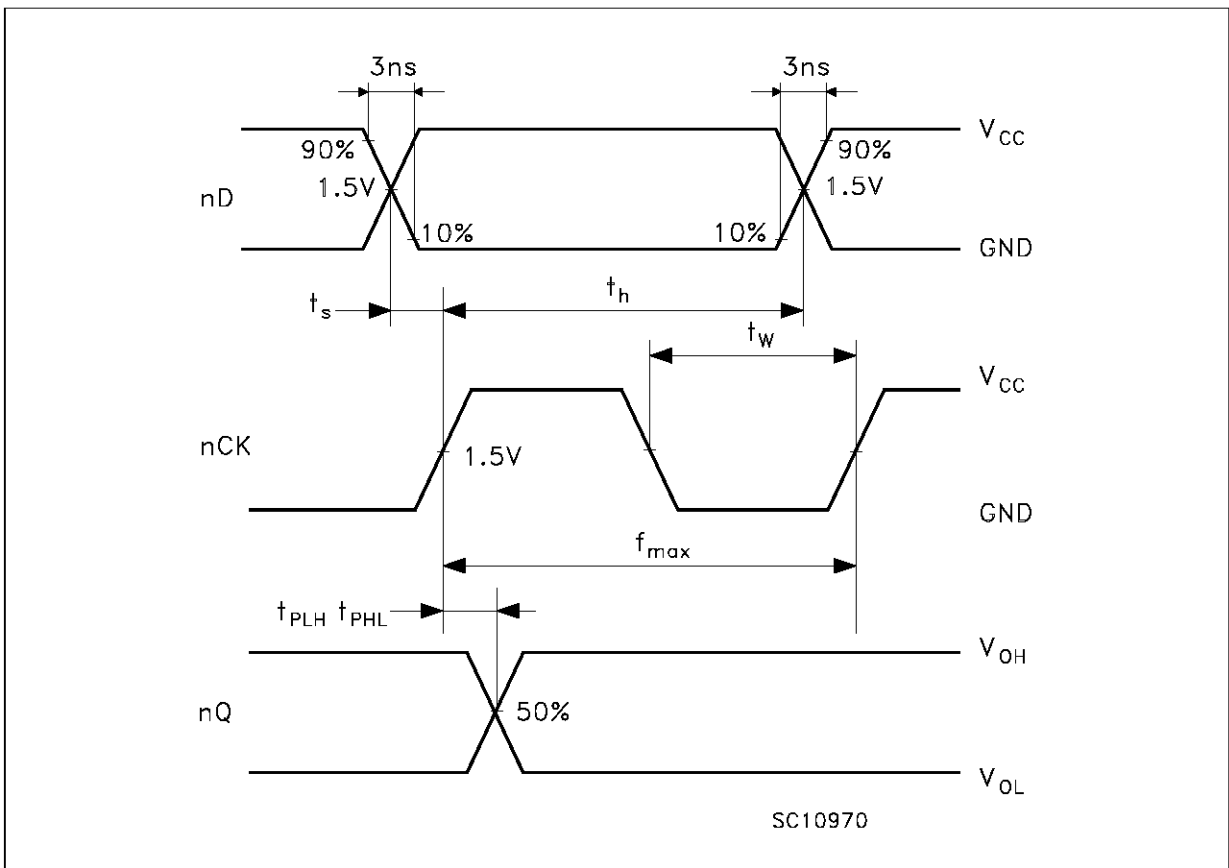
1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/n$  (per circuit)

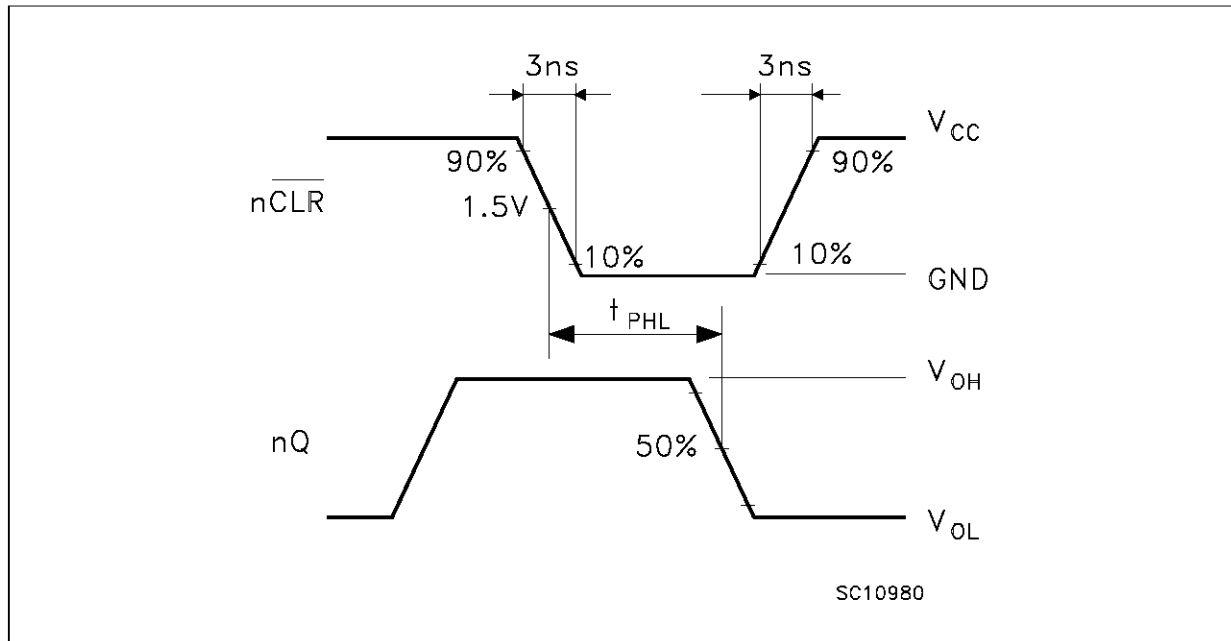
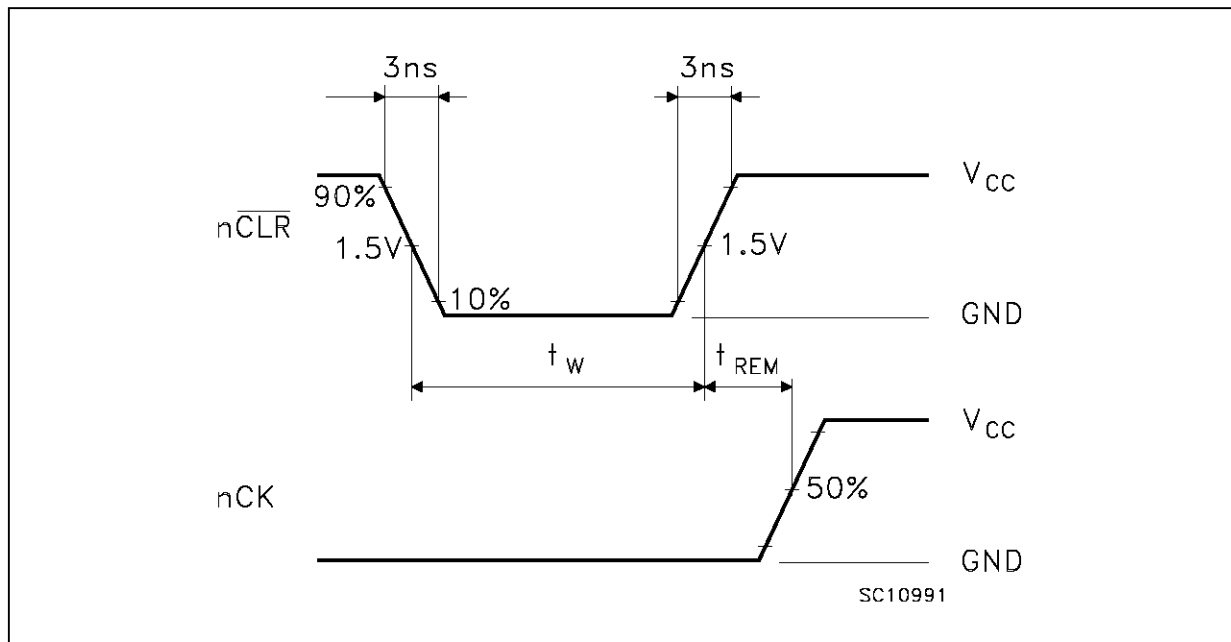
TEST CIRCUIT



$C_L = 50 \text{ pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = R_T = 500\Omega$  or equivalent  
 $R_T = Z_{out}$  of pulse generator (typically  $50\Omega$ )

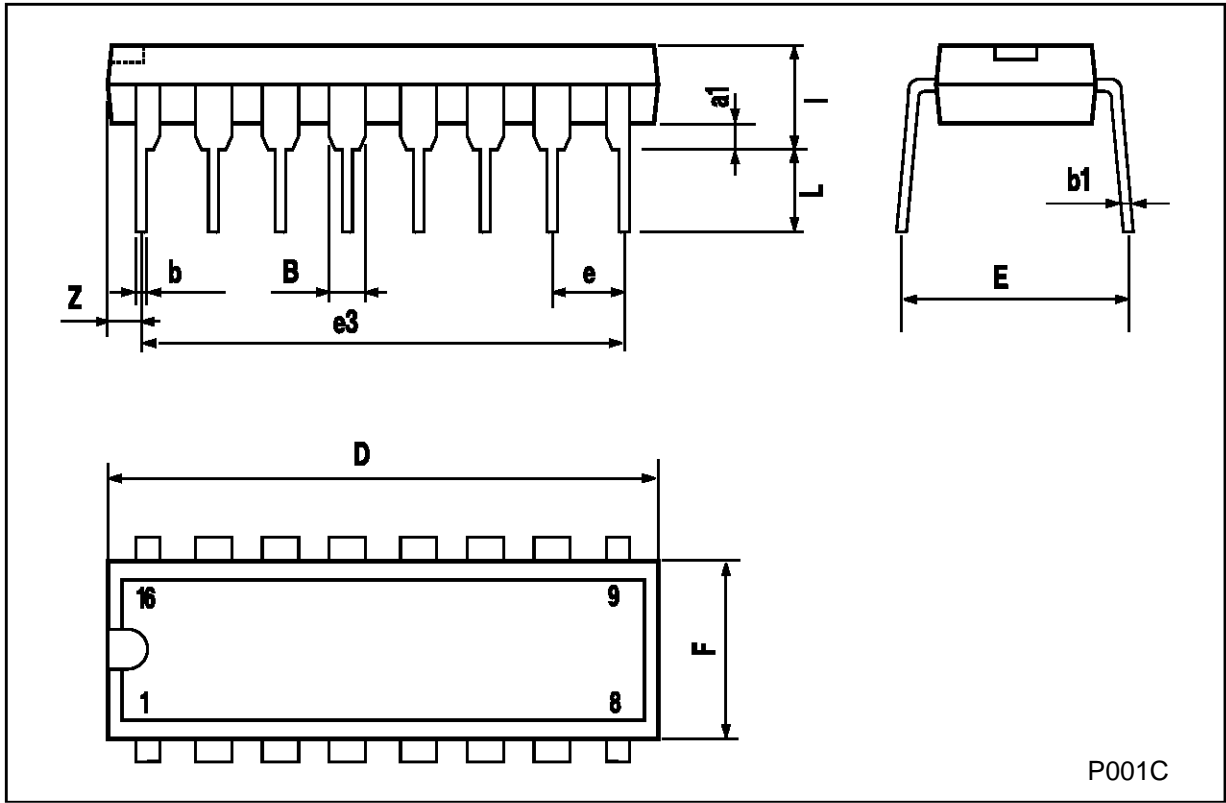
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES ( $f=1\text{MHz}$ ; 50% duty cycle)



**WAVEFORM 2: PROPAGATION DELAYS** ( $f=1\text{MHz}$ ; 50% duty cycle)**WAVEFORM 3: RECOVERY TIME** ( $f=1\text{MHz}$ ; 50% duty cycle)

**Plastic DIP-16 (0.25) MECHANICAL DATA**

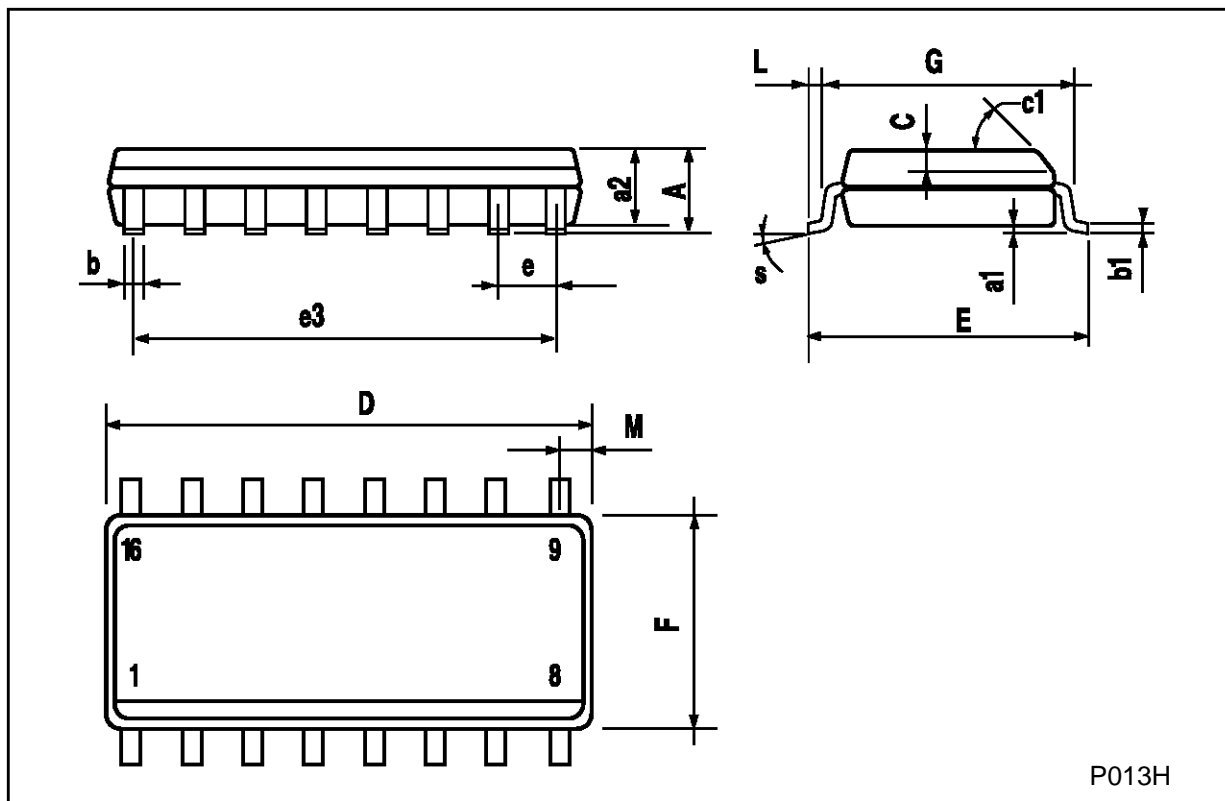
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050





## SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



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