Designing High-Frequency DC-to-DC Converters With the Si9114A Switchmode Controller

INTRODUCTION

Vishay Siliconix's Si9100 monolithic switchmode PWM controller established the standard for low-power, high-efficiency dc-to-dc converters. This versatile device integrates a number of useful features, including a power MOSFET, high-voltage start circuitry, and low power consumption. The Si9114A controller pushes the limits for high-frequency power conversion by further reducing delay times and adding additional features. As a result, dc-to-dc converters can be designed for frequencies up to 1 MHz with simple PWM topologies instead of the complex resonant ones.

The Si9114A uses constant frequency current mode control. By increasing the conversion frequency, power supply designers will be able to:

- reduce the size of energy storage components
- increase reliability by using ceramic capacitors
- produce an all-surface-mount assembly solution
- lower system costs
- simplify the implementation of a distributed power architecture.

Traditionally, distributed power has been regarded as costly and impractical to implement due to the high cost of local power conversion and the perceived complexity of resonant power supplies. But these decision criteria are now being changed by the availability of small-outline control ICs, LITTLE FOOT® MOSFETs, ceramic capacitors, and new magnetic components.

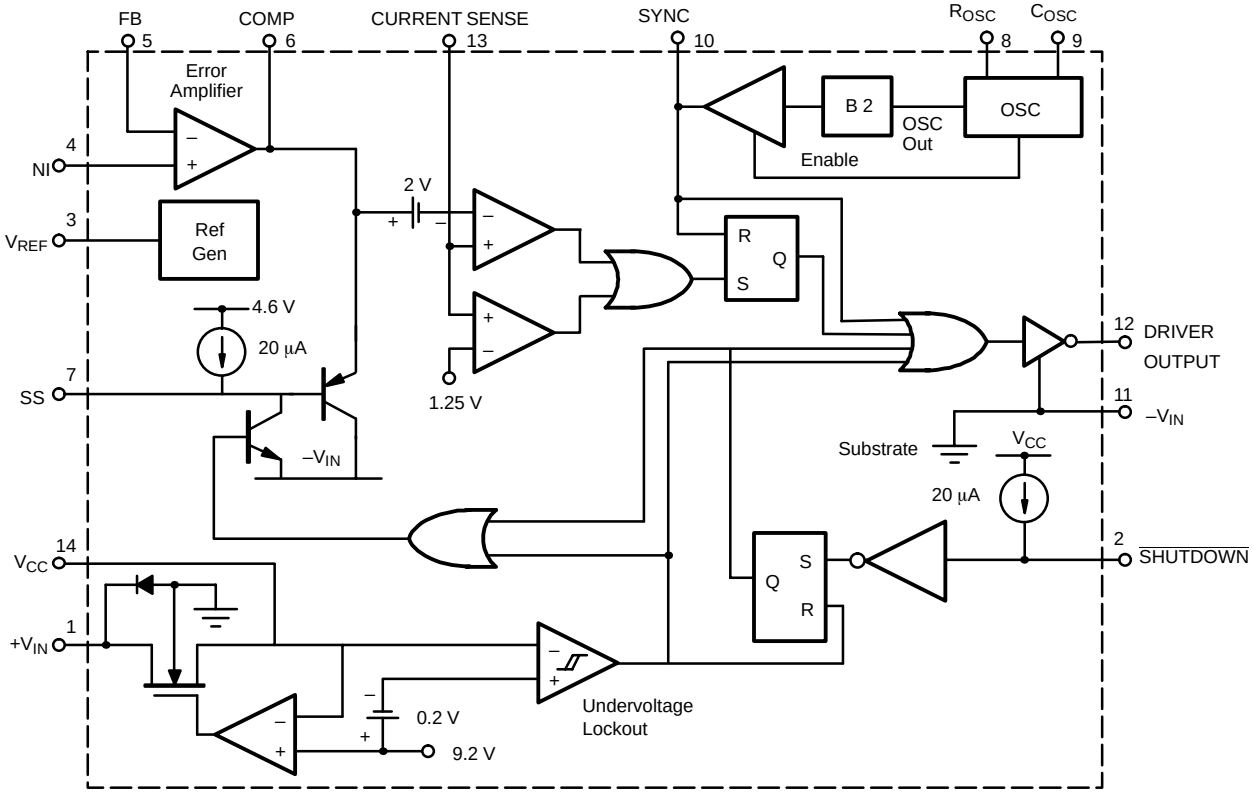


Figure 1 Si9114A Block Diagram

FUNCTIONAL DESCRIPTION OF THE SI9114A BID/CMOS PWM CONTROLLER

The Si9114A controller is similar in configuration to the Si9110. It uses a traditional constant frequency current mode control, the most commonly used architecture. The duty cycle is limited to less than 50% to avoid problems with core reset.

Current mode control is presently the de-facto standard for PWM control circuits. Indeed, it is the only candidate that should be considered, given its many advantages:

- Cycle by cycle current limit protection
- Simple loop compensation, eliminating effect of output inductor
- Excellent fast transient response due to inner control loop
- Automatic input voltage feed-forward compensation

PIN 1 - HIGH VOLTAGE PRE-REGULATOR

All switchmode power supplies face a start-up problem caused by the large difference between dc bus voltage and the V_{CC} power rail for supplying the control circuit. The traditional technique has been to keep the control circuit in “sleep mode,” while a small amount of energy is used to “top up” a large enough electrolytic capacitor to get the circuit started. When the circuit starts operating, a winding on the transformer is then used to power the control circuit. Disadvantages with this type of circuit include delayed start-up and large required capacitances for guaranteed operation over the full voltage range. The Si9114A overcomes these problems by using low power consumption, BiC/DMOS circuitry, and a unique high-voltage depletion mode MOSFET. (See 2)

When power is first applied, the depletion transistor is on, and current flows from the input capacitor C_{IN} into the V_{CC} capacitor C_{VCC} until V_{CC} reaches 9.2 V. The converter transformer will then supply the V_{CC} through a bias winding, which will raise V_{CC} to a level higher than 9.2 V. Ideally this will be between 11 and 13 V, thus turning off the high-voltage depletion mode MOSFET. The 9.2-V threshold has a hysteresis of 300 mV to prevent oscillations when the transition voltage is not clearly defined or when high-line supply impedance is encountered.

For applications where the input dc voltage is not high, and the chip power consumption is not excessive, the feedback winding can be eliminated. In such cases, the pre-regulator circuit will behave just like a linear regulator with 9.2-V output and 10-kΩ series resistance. In this case, the parameters to be considered are the dropout voltage at lowest line condition and the power dissipation at highest voltage. The high-voltage depletion mode MOSFET contains an internal body diode, and in situations where the V_{CC} is being powered from a laboratory supply, care must be taken to avoid loading the $+V_{IN}$ rail beyond the current rating of this device. Typically, the reverse characteristics of the device will generate a voltage of 3.4 V on Pin 1 with 10-kΩ load when powering V_{CC} from a lab supply.

In some applications it is necessary to inhibit the start of a converter until a high enough voltage is present on the supply bus. This is the case for the following reasons:

- Circuitry fed from a high line impedance such as a telephone line will have difficulty starting, since the converter will behave like a negative impedance. As the dc voltage decreases, the input current increases because constant power is drawn. This causes severe oscillations, and can in some instances have a destructive effect on the converter. [4]
- During start-up, the Si9114A will begin operation as soon as the UVLO threshold is reached. Since the converter is designed to operate over a much higher range—for example, from 36 to 72 V—then between 10- and 36-V input the output voltage will be out of regulation and undefined. In some cases, digital circuitry will not accept this mode of operation, and system faults will be encountered without a RESET watchdog circuit.

To overcome these problems, a Zener diode of suitable value V_Z can be placed in series with the $+V_{in}$ pin, preventing start-up until V_Z + 9.2 V is reached.

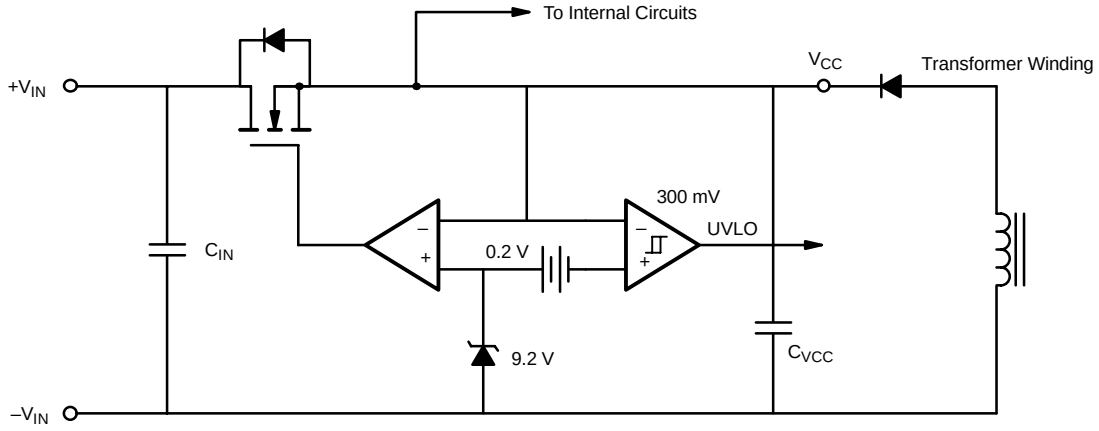


Figure 2 Start Circuit

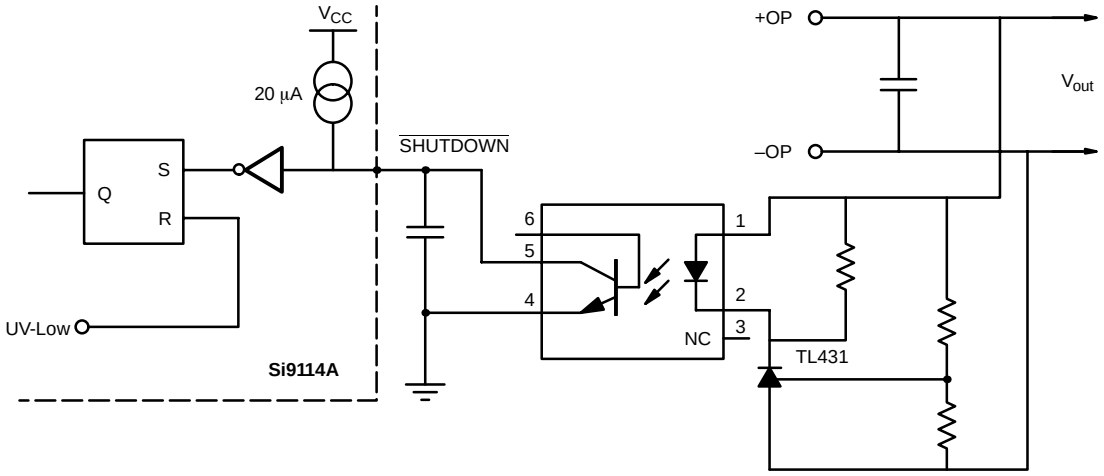


Figure 3 Shutdown

PIN 2: SHUTDOWN

The shutdown pin is configured to allow fast latched termination of the output pulse. The delay from shutdown to output is typically 300 ns. This delay is short enough to allow this pin to be used for over-voltage applications where fast orderly shutdown is desirable: for example, when control of the feedback loop is lost.

Using an opto-coupler and a TL431, interface is easy. (See 3) Once latched, the shutdown can only be reset from the UVLO circuit by re-cycling the power. In the event of an over-voltage, the latch can be reset by momentarily pulling the V_{CC} to a value lower than the UVLO threshold.

This approach will generally be acceptable, since the feedback winding will not be supplying power, and the only power maintaining the latch will be supplied by the depletion start transistor. Note, however, that this action will still be subject to the power dissipation limits of the Si9114A package and should ideally be applied as a short fast pulse.

An internal 20-µA current source pull-up on $\overline{\text{SHUTDOWN}}$ pin is provided. However, if the Si9114A is used in a potentially noisy environment, a 10-kΩ pull-up is recommended from $\overline{\text{SHUTDOWN}}$ to V_{CC} to prevent fault triggering, and to prevent a start-up problem when a fast slew rate power supply (dv/dt > 100 V/ms) is used for $+V_{IN}$ (pin 1).

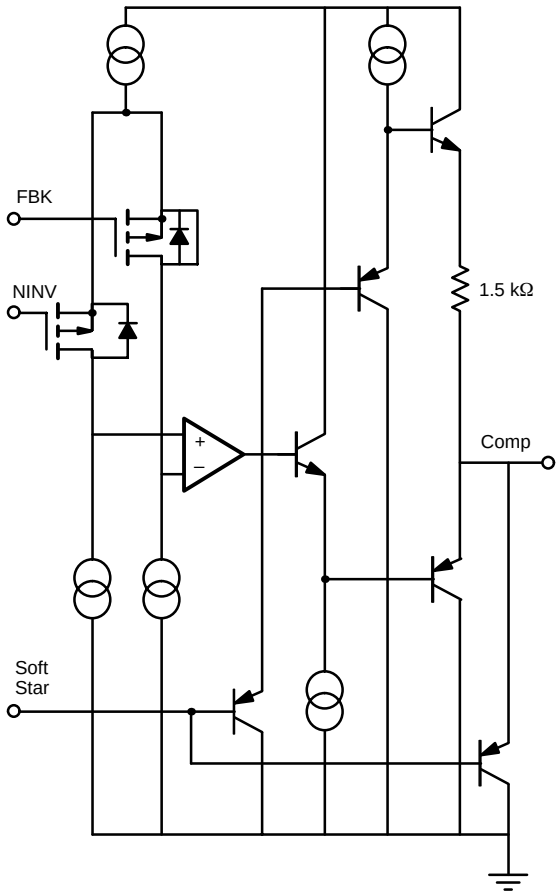


Figure 4 Operational Amplifier

PIN 3: REFERENCE

The reference voltage is a fully buffered band gap type which can source 5 mA over the specified voltage tolerance range. The reference should be well de-coupled to prevent instability and jitter. A ceramic 100 nF or small tantalum is recommended, depending on the de-coupling present on the supply pins.

PINS 4, 5 AND 6: ERROR AMPLIFIER

The error amplifier consists of a PMOS input folded cascade gain stage followed by a class AB unity gain amplifier.

Typical open loop voltage gain is 77 dB, and unity gain bandwidth is typically 2.7 MHz. The soft-start circuit (see Pin 7 description) forces the output to within 0.7 V above ground, and additional clamp diodes limit the positive output excursion to within $2xV_{BE}$ above V_{REF} . Operation at high frequency allows high closed loop bandwidths and permits excellent transient response to both input and output changes. Under normal operation, a small 100 pF bypass capacitor is recommended from N_{INV} to Comp to increase high-frequency noise rejection. This should be calculated, however, in conjunction with the loop dynamics.

PIN 7: SOFT-START

The soft-start circuit is designed to help dc-to-dc converters start in an orderly manner and reduce component stress. The output of the error amplifier is clamped by a PNP transistor.

The external capacitor C_{SS} is supplied by a 20-μA current source and will charge linearly to 4.6 V. In the event of an under-voltage lockout (or during start-up), this capacitor is held low.

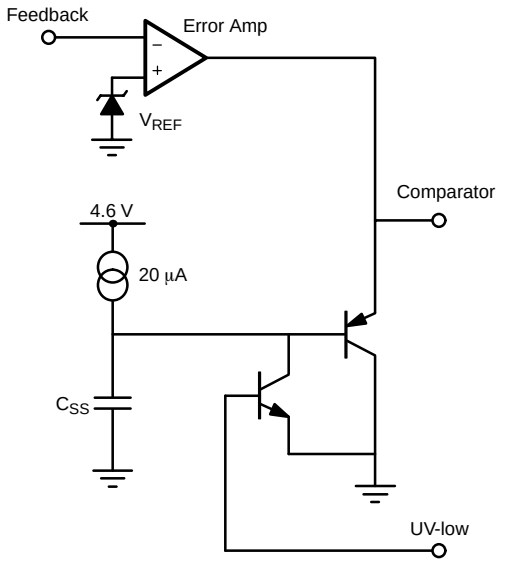


Figure 5 Soft-Start

Soft-start is a very important feature and has many beneficial effects, especially in applications connecting to telecom lines where source impedances are high. In such cases, there is an initial start-up current caused by the input capacitor, followed by a secondary peak caused by the converter running at maximum duty cycle while trying to reach regulation. Where large output capacitances and peak loads are encountered, oscillations may occur. These can be prevented with the use of long soft-start times. The soft-start pin can also be used as a non-latching shutdown pin by connecting it to $–V_{IN}$. This approach allows a shutdown with soft re-start.

PINS 8 AND 9 - OSCILLATOR

The oscillator circuit uses external timing components R_T and C_T. An internal divide-by-two prevents pulses with greater than 50% duty cycle, so that core saturation can be avoided. When the R_T terminal is connected to V_{CC}, comparator C_2 disconnects the oscillator output from the SYNC terminal using SW_1, and allows an external oscillator circuit to take control of the current mode comparator circuit.

The current programmed by R_T defines the charging current of C_T and the on and off times with the following design equations:

$$t_{ON} = \frac{1.025 \times R_T \times C_T}{8} \quad (1)$$

$$t_{OFF} = 5 \times R_{ql} \times C_T \quad \text{where } R_{ql} = 25\ \Omega \quad (2)$$

$$f_{OSC} = \frac{1}{2} \times \frac{1}{(t_{ON} + t_{OFF})} \quad (3)$$

Actual values taken from a prototype board have been plotted (Figure 6), and are a close match (except for 47 pF, where stray parasitics have more significant effect).

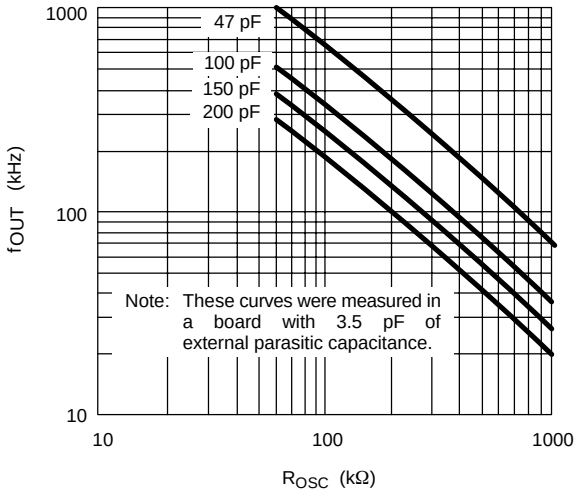


Figure 6 Oscillator Frequency Selection

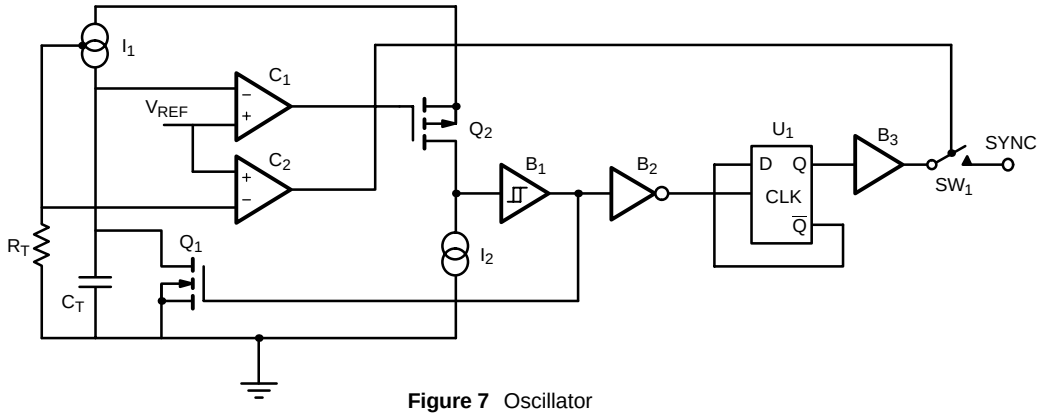


Figure 7 Oscillator

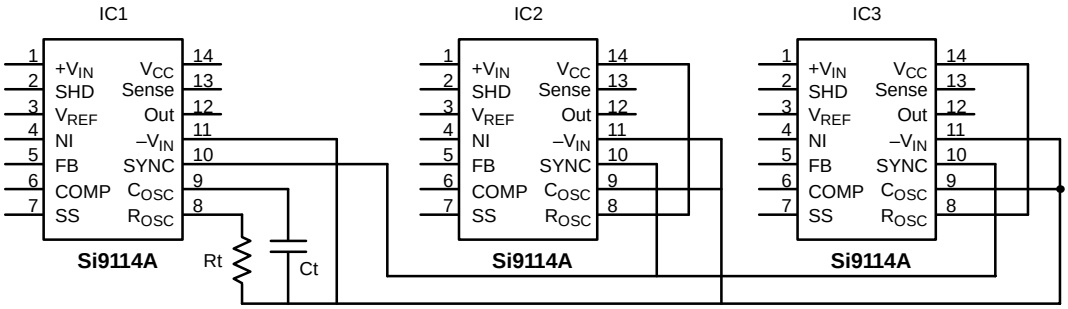
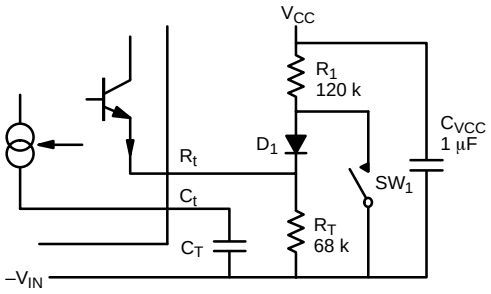


Figure 8 Oscillator Synchronization



SW1 Closed = Frequency High
SW1 Open = Frequency Low

Figure 9 Frequency Shifting Using R_t Current Change

In certain circumstances, such as current limiting, it may be desirable to change the frequency of the converter for a period of time to overcome current tails (see Figure 16 for further explanation). With the Si9114A, this is easily done by adding or subtracting some current into the R_T terminal:

- The charging current in C_T is set by 8 × R_T.
- The voltage at the R_T terminal is 4 V, as supplied by an internal emitter follower from the reference.

The frequency can be changed easily by supplying some of the current into R_T from the V_{CC} rail, thus "starving" the internal current source, and slowing the frequency down.

The current in R_T is set by V = IR where V = 4 V and R = R_T. Using a diode, and some type of switch, the frequency can be easily changed: when SW_1 is closed, D_1 is reverse biased, and has no effect on R_T. When SW_1 is open, current flows through R_1 and D_1 into R_T and removes some of the current supplied by the internal emitter follower.

PIN 10 - SYNCHRONIZATION

The *SYNC* input allows operation from a master clock as the connection is made after the divide-by-two. As a result, synchronization in both frequency and phase is possible. This unique feature is important to systems designers who use multiple converters, where noise caused by an unsynchronized "beating" effect is present and causes difficult EMI/EMC problems. If an external clock is used, duty cycles of >50% are possible due to the position of the *SYNC* pin , after the divide-by-two. Where >50% conduction is used, core reset must be allowed, in order to prevent core saturation. Synchronization is in master/slave mode, with one device (the "master") setting the switching frequency and others (the "slaves") with disabled oscillators locked to it. Alternatively, all devices can be clocked using a master oscillator.

During slave mode, the unused C_T pin should be connected to ground, and the R_T to V_{CC}.

PIN 11 & PIN 14 -V_{IN} & V_{DD}

These pins are used for powering the Si9114A and should consequently be well de-coupled. In selecting the right de-coupling, the MOSFET gate drive requirements should be considered, as the de-coupling capacitor will also have to supply the required peak current. Generally speaking, the best combination would be a 1- to 10-µF electrolytic for bulk energy and a 100-nF ceramic for high-frequency bypass. The V_{CC} rail should be carefully observed at the switch on and off occurrences using ac de-coupling, and the peak voltage spikes should be measured. These should be less than 200 mV. Excessive noise on the V_{CC} will appear on other pins and may cause instability or jitter on the control waveforms.

PIN 12 - OUTPUT DRIVER

The output driver uses complementary n- and p-channel output stages, with break-before-make capability, preventing shoot-through conduction. The output is typically capable of sourcing 400 mA and sinking 700 mA. When driving power MOSFETs, remember that the relevant parameter for sizing the drive requirements is the total gate charge for the applied voltage, not the commonly used input capacitance, C_{ISS}. When driving a MOSFET in common source mode, the Miller effect will significantly affect the drive waveform applied to the gate: in particular, when the driving source impedance is high enough (Figure 10).

As the voltage is applied to the gate, the previously charged C_{gd} will need to discharge, and will thus oppose the application of any voltage to V_{gs}. Many designers commonly overestimate the drive requirements of the MOSFET and cause excessive noise in the converter by overdriving the MOSFET. To prevent this, designs typically require snubbers or other additional noise attenuation devices. The voltage that will be applied to the drain just prior to driving of the gate will need to be considered. In practice, most manufacturers are unable to publish this data for all voltages, so designers should use the curve nearest to the actual voltage applied.

The Si9420DY LITTLE FOOT MOSFET is designed specifically for converters in the 5- to 25-W power range. It has a 200-V V_{DS} rating with 1-Ω $r_{DS(on)}$. Using the Gate charge curve, for a gate drive of 12 V from the Si9114A, the total gate charge for 100-V V_{DS} will be 10 nC. From Q = i x t, it is easy to deduce that with 400 mA gate drive, a time of 50 ns will be obtained—which is more than adequate for this size MOSFET. To supply 400 mA, the gate drive circuit resistor will need to be 12 V/400 mA = 30 Ω (Figure 11).

PIN 13 - CURRENT SENSE

The current sense comparator performs the current mode control function by comparing the output of the error amplifier (V_C) with the current in the output inductor.

It is impractical to measure the output inductor current, but the rising slope of the current can supply all the necessary information if sampled in the MOSFET as a scaled equivalent.

Certain precautions are necessary, however, due to data distortion, noise, and the rarity of ideal operating conditions.

Sensed current waveforms often have leading-edge spikes or noise caused by reverse recovery of rectifiers, equivalent capacitive loading on the secondary, and inductive circuit effects. Inductive sense resistors must not be used, as they cause large damaging spikes and distort the sensed waveforms. These spikes can confuse the PWM comparator into believing that an overload condition is present. In addition, the Si9114A uses a single pin ($-V_{in}$) for all the return current requirements, including the output driver. As a result, the current pulse from the gate charge transfer into the MOSFET will appear on the sense pin and be filtered out.

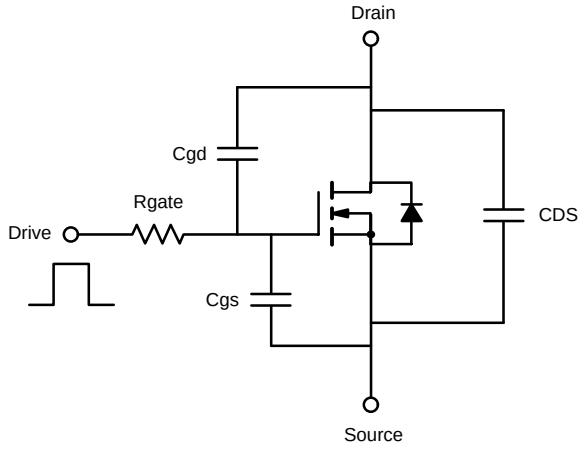


Figure 10

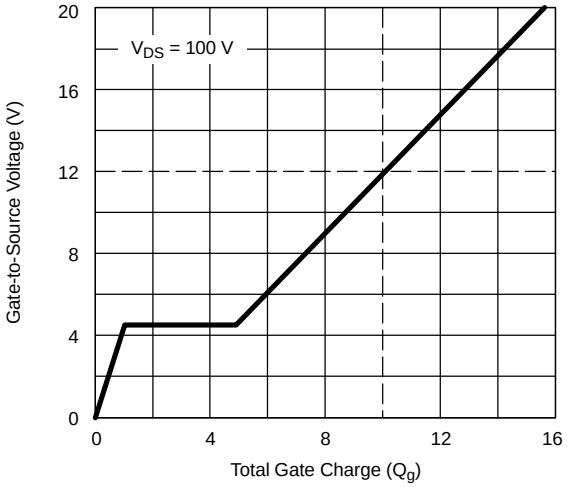


Figure 11 Si9420DY Gate Charge

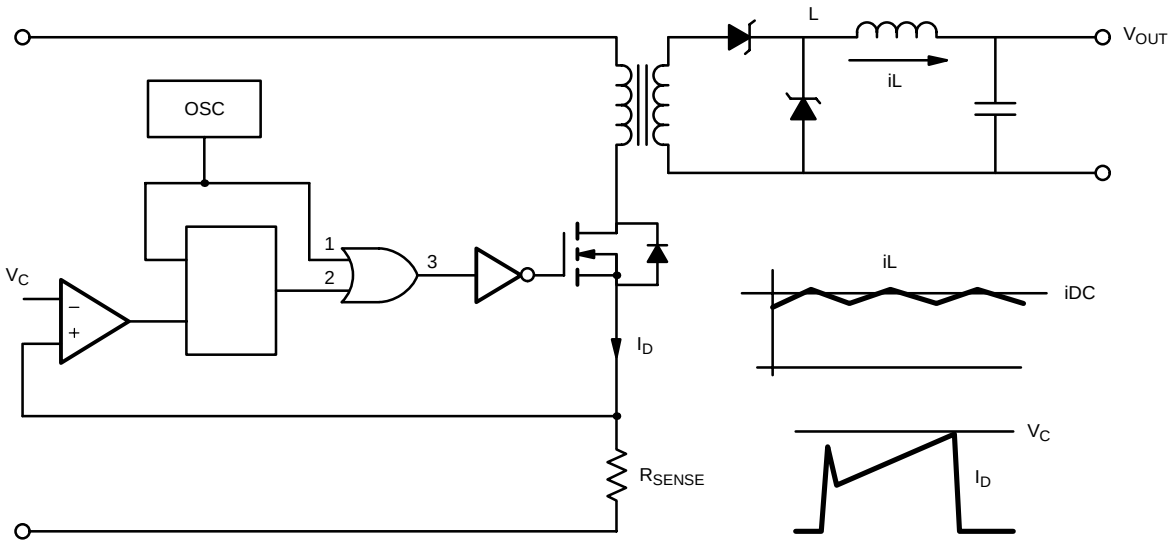


Figure 12. Constant Frequency Current Mode Control

Waveform A has an ideal textbook appearance, but is in fact rarely encountered. Waveforms B and C are typical yet close to the threshold limit, and thus could lead to instability. The addition of a simple RC network on the sensed waveform suppresses this leading-edge spike. The low pass filter should be selected so that only the leading-edge spike is suppressed and the overall waveform is not distorted. The waveform must contain a clean rising slope for the error amplifier to intersect. If the RC time constant is too long, then the waveform will be distorted and lead to falling-edge jitter on the turn-off edge.

Slope compensation can also be used to eliminate noise or jitter. A sample of the oscillator voltage is superimposed on the error amplifier to produce a clean crossing of the thresholds and to avoid any hunting.

The Si9114A has built-in leading-edge blanking/ suppression to eliminate some of the effects of these spikes. The two comparators used to operate the circuit have different delay times as follows:

- The current mode comparator needs more noise immunity, and therefore has a deliberately slower delay time to block out noise and spikes which are present on the leading edge. Typical delay times should be around 100 ns.
- The peak current limiting comparator has the fastest response time, since it is used only to protect the circuit in the event of an overload. The delay times for this comparator should be around 70 ns.

HIGH-FREQUENCY DESIGN REQUIREMENTS

When designing converters for high switching frequency, a certain discipline is required to determine the right choice of components. This process should be an iterative choice and the board layout should be properly planned before CAD layout is undertaken.

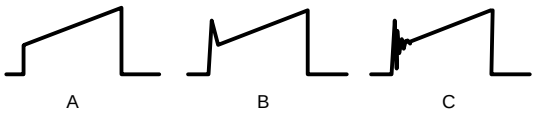


Figure 13 Current Waveforms

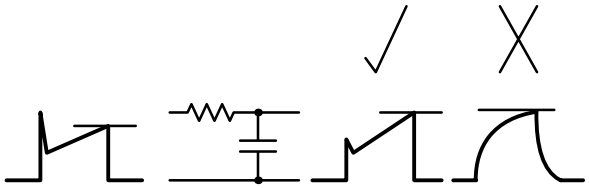


Figure 14 Current Sense Filtering Network

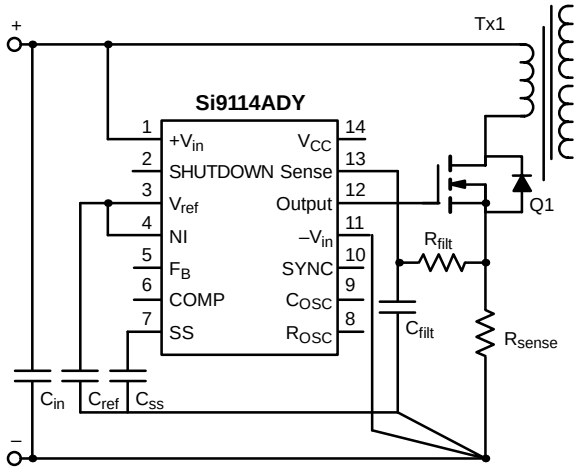


Figure 15

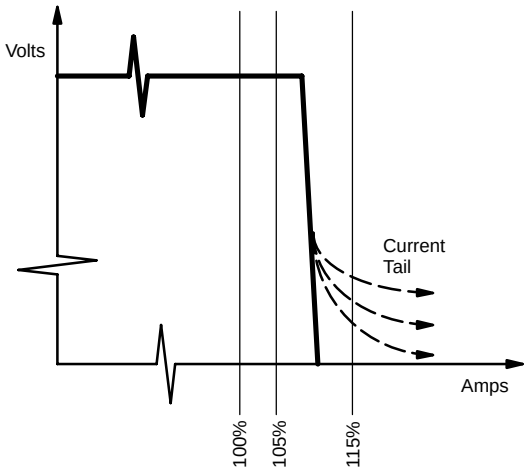


Figure 16

LAYOUT CONSIDERATIONS

The main current loop flows from the input capacitor—through the transformer, MOSFET, and sense resistor—and returns to the capacitor. This current will have high rates of change and associated fast voltage and current edges. It is essential to avoid the injection of noise into the other circuitry.

To prevent this result, a “fishbone” type arrangement is recommended (Figure 15). Designers are encouraged to separate different grounds with “imaginary” dummy resistors. These can be removed at a later stage. Main current loops must be designed to be as short as possible: from C_{IN} to the transformer, through the MOSFET and Sense resistor, and back into C_{IN}. It is obvious that signals switching 50 V or 1 A in 25 ns should not be mixed with signals that are controlling a closed-loop, high-gain feedback system which is capable of regulating the output voltage to less than 1 mV.

CHOOSING THE SWITCHING FREQUENCY

When selecting the switching frequency, it is usually best to choose the lowest possible frequency that the design solution will accept. In PWM control topologies, the maximum switching frequency will be strongly governed by short circuit behavior. When a short circuit is applied to the output, the control circuit is required to reduce the duty cycle to the smallest possible value to maintain constant current operation (Figure 16).

Ideally, the converter should deliver 105% of the output current within regulation and no more than 115% under short circuit. At 500 kHz, the period of conversion is 2 μs and the maximum on time is 1 μs.

High minimum duty ratios will result in current tails and require rectifier oversizing to avoid destructive currents under overload conditions.

The Si9114A has a sync-to-output delay of less than 70 ns, so the minimum duty cycle for operation at 500 kHz would be 70 ns/2 μs = 3.5%. This minimum should be considered when the short circuit current is determined. Designers should note that a shunt placed across the output of the converter is probably not a realistic load in the event of a failure, and the real circuit impedance will probably be substantially lower. In such circumstances, it may be necessary to shift the frequency of the converter to a lower value during overload. Frequency shifting can be accomplished by altering the steady state values of the oscillator programming components (see oscillator section, Figure 8).

SHORT CIRCUIT BEHAVIOR

Short circuit behavior is different for both common topologies, and must be paid special attention.

- In flyback converters, all windings appear in “parallel” with each other. When one winding is shorted, all other flyback windings are also shorted though it. In multiple output converters, therefore, any single winding without a separate secondary current-limiting protection will “drag down” all the other windings. As a result, if a bias winding is used to power the control circuit, it will stop delivering power. When this occurs, the Si9114A depletion device will turn on and regulate the supply rail to 9.2 V, as in its normal starting mode. In this event, designers should calculate the worst-case power dissipation caused by the voltage drop across the depletion transistor at the highest applied voltage across it and with the current flowing through it.

- In forward converters, traditionally the bias winding is also taken in forward conduction mode, but without any series inductance. In the event of a short circuit, the pulse width is reduced to minimum, but it is sufficient to supply enough power to the control circuit. This is an advantage, and avoids the problems encountered with flyback converters. Power may also be taken in flyback mode, however, when the duty cycle is low. There will be very little flyback voltage present, since the applied volt/microseconds is low and the core need not, therefore, fly back very far to reset.

CHOOSING THE TOPOLOGY

The choice of topology is usually based on the designer's previous experience. The two best candidates for the Si9114A are the forward and flyback types, although other types, such as Cuk, are also possible.

In general, forward converters are best for higher-power applications, and flyback converters are best for lower-power applications. Both topologies have their merits, and the designer will have to select the one most suited to his or her own application. See appendices A and B for brief descriptions of topologies and magnetic design equations.

SELECTING THE SEMICONDUCTORS

For power switching, the recommended device is the Si9420DY. The Si9420DY is a 200-V, 1-Ω MOSFET housed in an industry-standard SO-8 package. Since the die is mounted on a copper header, cooling can be accomplished using the PCB area directly below the Drain pins. The combined performance of the Si9420DY's features makes it the best low-profile device available on the market. It is suitable for designing power supplies ranging from 10 to 25 W. Other such single and dual LITTLE FOOT devices are available in both n- and p-channel versions with voltages starting from 12 V.

Rectification for low-voltage outputs (< 5 V) is accomplished using Schottky diodes. In this case, the rectifier selected exhibited forward voltage drops of 0.4 V at 4 A. A 5-V output will require a rectifier with a 40-V reverse voltage rating. Where lower voltages, such as 3 V, are required, devices with lower reverse blocking should be used, since these will have lower forward voltage drops. Designers should avoid using an oversized Schottky diode, since all such devices have parasitic capacitances that need to be charged and discharged to the applied voltages. Driving and commutating oversize devices will not necessarily yield better efficiency, especially at higher frequencies.

Rectification for voltages above 12 V is generally accomplished using fast or ultra-fast rectifiers. Look for devices that have recovery times below 50 ns. An excellent example is Telefunken Semiconductors' BYG22B rated for 100 V and 2 A with 25 ns recovery, and Forward voltage of 0.7 V for 0.5 A current. This device is available in a DO-214 surface-mount package.

Opto-isolators are now available in SO-8 packages with 3000 Vrms isolation rating. These are by far the least expensive and simplest isolated feedback devices now available. Their reliability, once considered questionable, has been greatly improved, and manufacturers now have quality data demonstrating their suitability under the correct operating conditions. A typical device would be the Telefunken Semiconductors' TCMT1020.

CHOOSING FERRITE MATERIALS

Ferrites suitable for operation at high frequencies have recently been introduced to the market. Two such offerings are the Philips 3F3 and 3F4, designed for operation up to 500 kHz and 2 MHz respectively. Many different geometries and good supporting data are now available. Appropriate choices for low-profile and surface-mount capability include devices in the EFD series, which have been extended down to 10 mm. It is better to choose core geometries with shallow and wide bobbins, since these permit good coupling from winding to winding when using high frequencies.

CHOOSING CERAMIC CAPACITORS

High-frequency operation allows the use of very low-value capacitances not generally associated with switchmode power supply output stages. As substantially lower energy storage is required, multilayer ceramic capacitors can be used, and suppliers have made good advances in quality and manufacturing to supply low-cost, high-performance designs. In the sub-25-μF area, a number of good dielectric devices are now available, such as X7R, Z5U, and Y5T.

From manufacturers' data sheets, the following observations were made:

- Z5U has the lowest cost, highest unit capacity, and worst dynamic variations
- X7R has the highest cost, lowest unit capacity, and best dynamic stability
- Y5T has an average of each of the above.

The recently introduced Marcon TCCR series uses the Y5T dielectric, which offers good all-around volumetric, cost, and high-frequency impedance performance, and is available in a surface-mount package with values such as 10 μF at 25 V and 3.3 μF at 100 V. For input and output energy storage, two of each of these devices were selected with the following considerations:

- Realistic market price.
- Voltage variation with applied dc voltage and temperature. Most ceramic capacitors suffer from a drop of capacitance with applied voltage and with temperature. The device needs to be selected so that at the extremes of operation the minimum energy storage is present.
- Equivalent Series Resistance (ESR). ESR will determine the output ripple voltage, and the heating of the device. This should be selected on the basis of the value of output choke, insofar as its design sets the ripple current present in the output capacitor.

The following data was obtained from commercially obtained samples:

At 70°C, the 10-μF device has dropped to 75% of its nominal value. With 5 V applied, the same device has retained 110% of its nominal value.

Care should be taken in selecting these devices to consider worst case requirements and minimum/ maximum operating conditions.

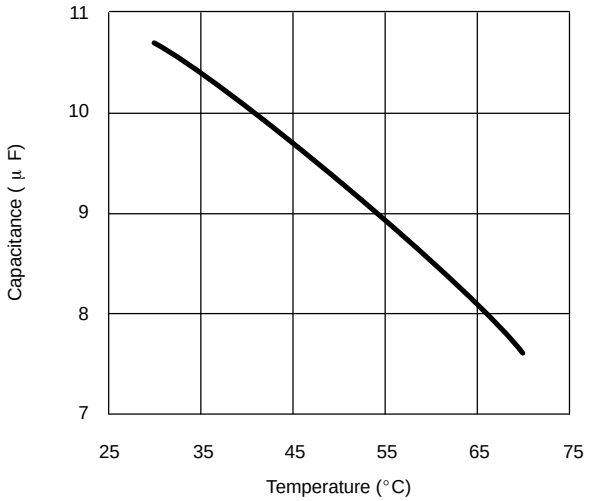


Figure 17. Marcon 10 μF 25 V, Capacitance Versus Temperature

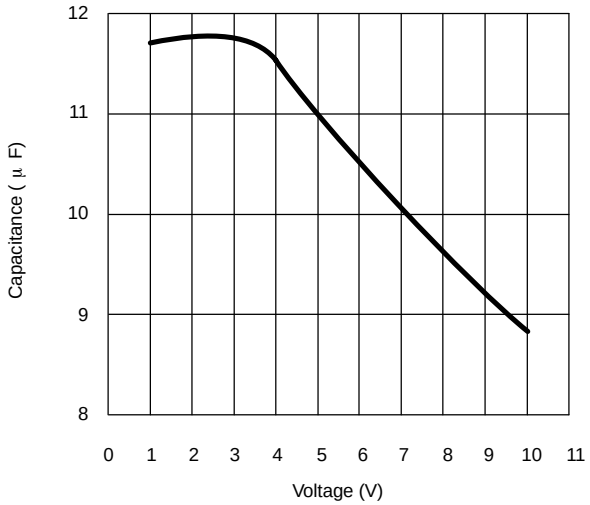


Figure 18. Marcon 10 μF 25 V, Capacitance Change with Voltage

DESIGN EXAMPLE: A 15-W, 500-KHZ, 48-V/5-V DC-TO-DC CONVERTER

Resonant Reset Forward Converter

Most forward converters are designed using a clamp circuit. While at low frequencies this technique may be acceptable, at high frequencies it becomes unnecessary: the parasitic elements of the circuit will reset the transformer flux automatically, provided a few precautions are taken.

It has been shown that [1] the resonant reset concept is dominated by the parasitic capacitance of the MOSFET and the magnetizing inductance of the transformer. Yet the capacitance of the output diode should also be considered. The correct equivalent circuit of the converter the approximates to Figure 19.

During the off time, D_2 is conducting and C_{D1} appears connected across the primary of the transformer, in parallel with L_{MAG}. The leakage inductance has a small and insignificant effect on the waveform—as the primary current has ceased flowing—and the only remaining current is the current that is charging C_{OUT}.

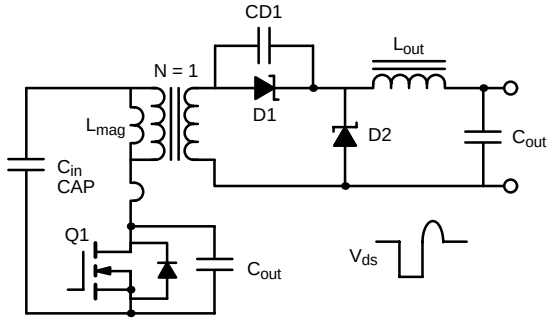


Figure 19 Resonant Reset Forward Converter

In effect, the magnetizing inductance of the transformer forms a parallel tuned circuit across the transformer and resonates at a frequency determined by the parasitic elements. The reset period needs to be short enough to allow full reset of the core, before the next switching interval occurs. This will be governed by the selection of the MOSFET and the Schottky diode.

Component Selection

The following information is supplied in order to help designer select correct components for use with the Si9114A. Vishay Siliconix does not necessarily recommend or approve these components for specific applications. Designers should contact manufacturers directly to obtain correct and current data sheets.

Capacitor Selection

As stated previously, ceramic capacitors are a good choice when operating at high frequency, due to the extremely low ESR, and high reliability, and long operating lifetimes.

In the design example, the required size of capacitors was defined as follows:

Input capacitor:

A 15-W output converter with 85% efficiency will require 15/0·85 = 17.65 W of input power. Assuming that operation at nominal conditions is 48 V, with duty cycle of δ=0.376 (measured), the switching current will be governed by the size of the output inductor (Figure 20).

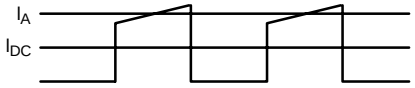


Figure 20

The average input current will be determined by:

$$I_{DC} = \frac{P_{in}}{V_{in}} = \frac{17.65}{48} = 0.358\ A$$

$$I_A = \frac{P_{in}}{V_{in} \times \delta} = \frac{17.65}{48 \times 0.376} = 0.98\ A$$

From this equation the RMS value can also be calculated to be approximately 0.475 A.

The Marcon TCCR70E2A335 3.3-μF, 100-Vdc capacitor has an ESR rating of 20 mΩ at 500 kHz. This type will therefore dissipate $P = 0.475^2 \times 0.020 = 4.5$ mW due to the switching current. The ripple produced across this device will be governed by the discharging current of the capacitor less the input dc voltage in accordance with:

$$Q = i \times t = C \times V$$

$$\therefore V_{ripple} = \frac{I_C \times t}{C} \text{ where } t = t_{sw} \times \delta \text{ and } I_C = I_A - I_{DC}$$

$$\therefore V_{ripple} = \frac{0.612\ A \times 2\ \mu s \times 0.376}{3.3\ \mu F} = 0.14\ V$$

140 mV of ripple is probably acceptable as a first stage of filtering. If lower ripple is required at the input, then a two stage filter will yield better results.

Output capacitor:

$$C_{out} = \frac{\Delta I_{out}}{8 f \Delta V_{out}} \text{ where } \Delta I_{out} = 0.1 \times I_{out}$$

ΔV_{out} = maximum output ripple voltage
f = operating frequency

$$C_{out} = \frac{0.3\ A}{8 \times 500\ kHz \times 50\ mV} = 1.5\ \mu F$$

The required ESR for obtaining 50 mV of ripple would be defined by:

$$ESR_{max} = \frac{\Delta V_{out}}{\Delta I_{out}}$$

$$ESR_{max} = \frac{50\ mV}{0.3\ A} = 167\ m\Omega$$

In practice, it is impossible to precisely match the value of a capacitor with the required ESR, and the values of the capacitors must often be selected to cover all operating conditions including voltage and temperature.

The above equations and calculations are meant to help the designer select the approximate size of the components required, with the final selection based on practical values that meet the minimum required. In designs operating below 500 kHz, the choice of the capacitor is dictated by the ESR, and the best high-frequency electrolytics often require large-size and micro-farad values to meet these requirements. When operating at 500 kHz, the choice becomes more based on the practical value closest to the size and voltage rating required. For example, with electrolytics, in order to guarantee the ESR over temperature or age, it might have been necessary to use a radial 1000-μF, 6.3-V Aluminum Electrolytic in a 10x16 mm case (1257 mm2) to get an ESR value below 100 mΩ. It would also be necessary to check the ESR with frequency at 500 kHz, as this data is seldom offered for electrolytics. By comparison, the Marcon TCCR70E1E106 10-μF, 25-Vdc is available in 7.5 x 6.3 x 2.75 (130 mm2) and has an ESR of less than 15 mΩ at 500 kHz. This will be ideal for low output ripple an noise. Recently introduced organic semiconductor electrolytics offer substantial improvements and could also be considered. In this example, it was decided to use 2 x 10-μF capacitors in order to obtain low output ripple.

OUTPUT INDUCTOR DESIGN

The output inductor limits the rate at which the current flows into the output capacitor when the voltage is applied from the primary through the transformer (Figure 21).

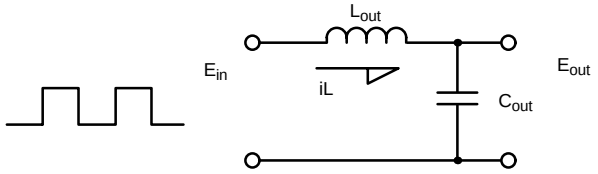


Figure 21

From simple circuit theory, the voltage applied across an inductor is:

$$V_L = L\frac{di}{dt} \qquad \text{where} \qquad V_L = E_{in} - E_{out}$$

$$\text{and } di = \Delta I_L \text{ then } L = \frac{(E_{in} - E_{out}) x \Delta t}{\Delta I_L}$$

In forward converters, at maximum duty cycle, Ein = 2xEout, and:

$$t_{off} = \frac{1}{2 \times F_{SW}}$$

In this case, substituting gives:

$$t_{off} = 1\mu S \text{ and } L = \frac{E_{out} \times t_{off}}{\Delta I_L}$$

Therefore

$$L = \frac{5\ V \times 1\ \mu S}{0.3\ A} = 16.7\ \mu H$$

In practice, an inductor between 5 and 10 μH would be an acceptable choice, allowing for manufacturing tolerances and variations.

The core selected is the EF12.6, which is identical to the core selected for the transformer design. The EF12.6 is a cheap, low-profile design available from many suppliers in all parts of the world. A surface-mounted version of this bobbin was selected for a design that could be entirely machine wound and terminated. This implies that larger wire sizes are not possible, due to automated winding restrictions.

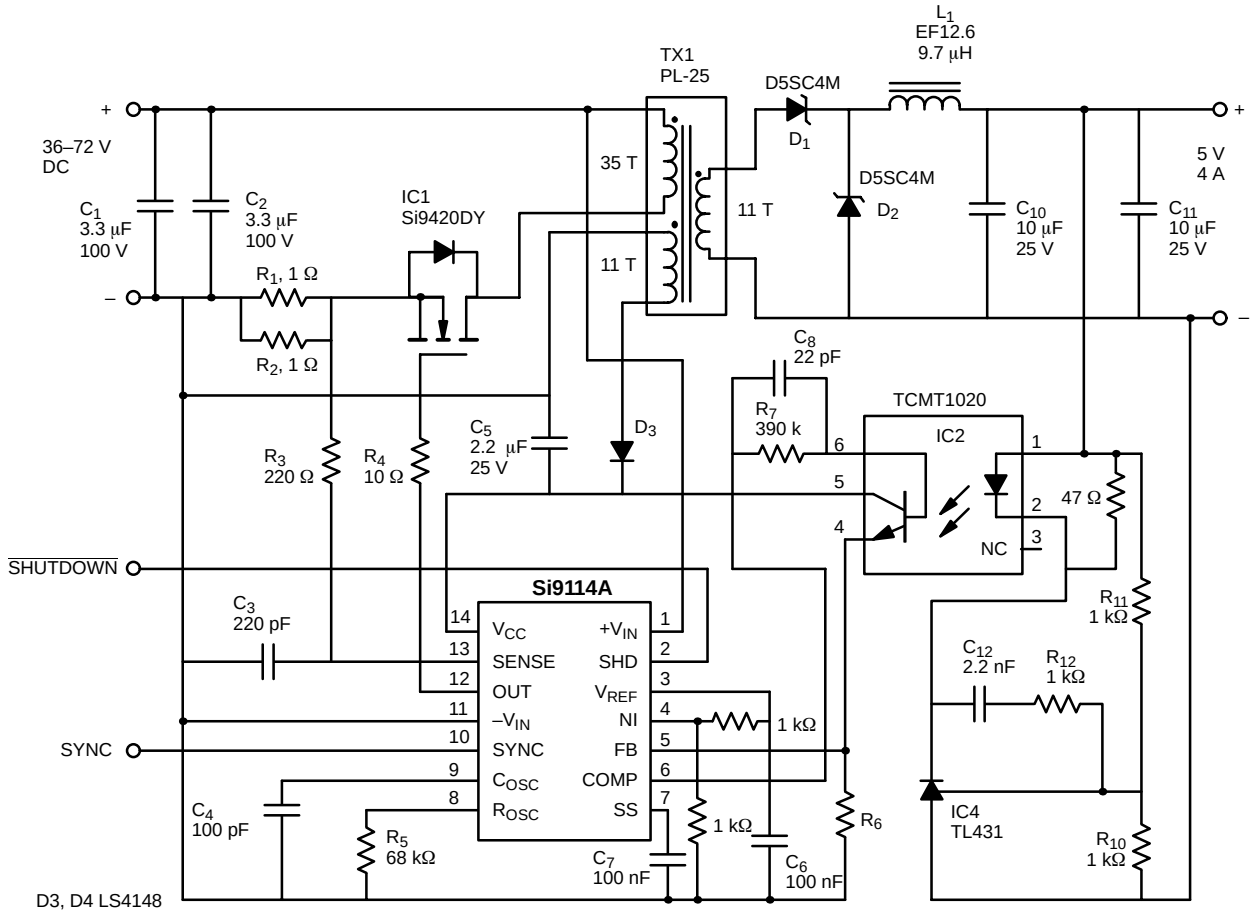


Figure 22 DC-to-DC Converter Block Diagram

Since this choke must carry the full output current, the minimum number of turns required on this core is given by:

$$N_{min} = \frac{L_{choke} \times I_{Choke}}{B_{max} \times A_{min}}$$

where B_{max} is the maximum flux density used, and A_{min} is the minimum core area. In this case B_{max} = 200 mT and A_{min} = 13 mm^2. Substituting in this equation yields:

$$N_{min} = \frac{8\ \mu H \times 3\ A}{200\ mT \times 13\ mm^2} = 9.2\ T$$

In this case it was decided to wind 3 layers of 12 turns of 0.315 mm in one layer each across the bobbin. This allowed the best fill factor of the bobbin, maximizing copper area.

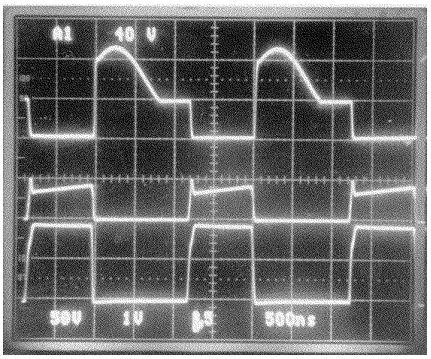
The result yields a choke having a dc resistance of 22 mΩ and therefore a dc copper loss of $P = I^2R_{DC} = 9 \times 0.022 = 200$ mW with 3 A dc. Using a core set with an A_L value of 45, a transformer of $L = N_{min}^2 \times A_L = 12^2 \times 45 \times 10^{-9} = 6.48\mu H$ was calculated. Measured value was 9.73 µH: slightly higher, but acceptable.

TRANSFORMER DESIGN

See appendix A for a design using these specifications.

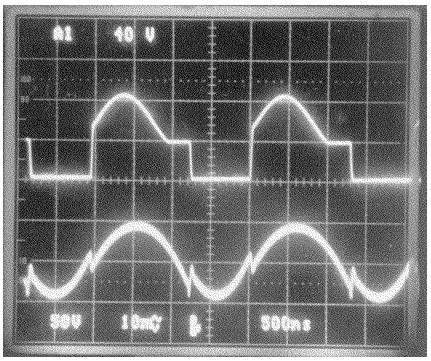
PERFORMANCE RESULTS

The switching waveforms in Figure 23 show that the resonant reset is limiting the peak voltage to 120 V, well below the maximum rating of 200 V. Note the leading edge spike caused mainly by the peak gate current.



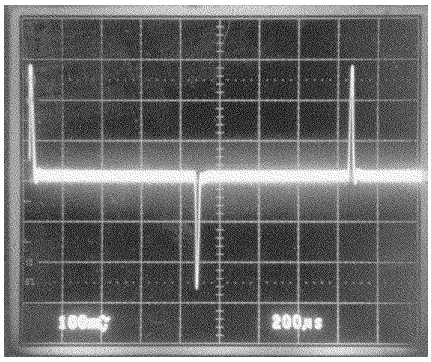
① V_{DS} of MOSFET 50 V/div
② Voltage across sense resistor 1 V/div
③ Voltage across gate 5 V/div

Figure 23 Time Base 500 ns/div.



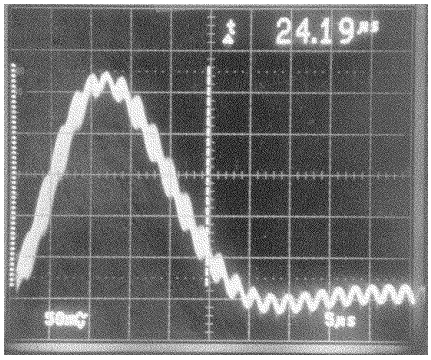
① V_{DS} of MOSFET 50 V/div
② Output ripple 10 mV/div

Figure 24 Time Base 500 ns/div.



① Output transient response for 1.5 to 3 A.

Figure 25 Time Base 200 ms/div.



① Output transient response for 1.5 to 3 A.

Figure 26 Time Base 5 µs/div.

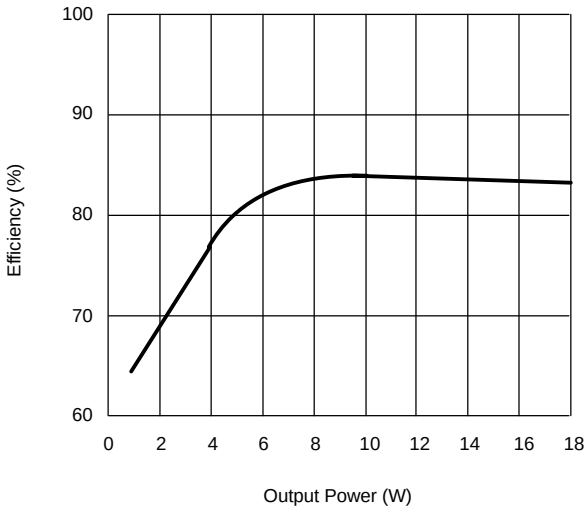


Figure 27 Si9114A 15-W, 500-kHz Converter Efficiency

In Figure 24, the low output ripple (<20 mV) is obtained with two 10-µF capacitors.[1] In Figure 26, note the excellent recovery time of <25 µs to within 1% of output for a 50% load step with total excursion of <300 mV. The efficiency of the converter is measured in Figure 27.

BENEFITS OF USING SI9114A

Low power consumption

at 500 kHz, the Si9114A consumes only 8 mA from the 12-V supply. This amounts to a total of 96 mW or 5.6% of the losses. It is important to remember that this figure represents both the power MOSFET losses as well as the control circuit. The control circuit was measured to consume only 3.2 mA or 2% of the total losses. In comparison, typical bipolar circuits would consume 35 mA, or 21% of the losses.

Short delay times:

with typical delay time approaching 65 ns, short circuit current can be lowered, and operation at higher frequencies is possible.

Integrated high-voltage start circuit:
the depletion transistor circuit allows fast turn-on and eliminates the need for extra components. At lower frequencies and power levels, it is possible to omit the bias winding completely, since circuit consumption is low, and the depletion circuit behaves as a linear regulator.

Synchronization in phase and frequency:
is a necessary benefit for distributed power systems where multiple converters are operated.

CONCLUSIONS

Operation at 500 kHz is possible using BiC/DMOS PWM control circuits. Significant power savings are possible, yielding high efficiencies and lower parts count due to the integrated high-voltage start circuitry. Operation at high frequencies allows the use of small, efficient, low-profile energy storage components, with higher reliability and calculated MTBFs. Surface mounted power MOSFETs are easily assembled using conventional assembly techniques.

REFERENCES

1. Murakami, Noaki and Yamasaki, Mikio. “Analysis of a Resonant Rest Condition for a Single Ended Forward Converter.” *PESC88 Record* (April 1988) CH 2523-9/88/0000-1018 $1.00 ©1988 IEEE.

2. Chryssis, George C. *High Frequency Switching Power Supplies: Theory and Design*. 2nd. ed. New York: McGraw Hill.

3. “Designing DC/DC converters with the Si9110 Switched Controller.” AN703. Vishay Siliconix Power Integrated Circuits Data Book, 1999.

4. “Efficient ISDN Power Converters Using the Si9100.” AN702. Vishay Siliconix Power Integrated Circuits Data Book, 1999.

[1] The strange shape of the ripple needs to be further analyzed but could be explained as follows:

- The step voltage that appears at the same time as the voltage switching edges is caused entirely by the ESR, as it is the only possible cause for a rapid step voltage across a capacitor. In this case, the measured value is on the order of 8 mV, thus predicting an ESR value of 6/0.3 = 20 mΩ for both devices. This is slightly higher than predicted, but of the same order of magnitude.
- The sinusoidal waveform must be caused by the equivalent capacitance that appears across the inductor, causing a capacitive coupling directly into the output.

Appendix A

FORWARD CONVERTER TRANSFORMER DESIGN

The forward converter transformer is operated as a voltage transformer. An ac source applies voltage across the primary, which is then transformed (up or down) by the turns ratio. For correct operation, the transformer must be correctly sized (in order to avoid core saturation) and large enough to accept the number of turns required. Since these two requirements may often compete with one another, compromise may be necessary to complete a design.

In operation, the transformer is driven through the magnetic B/H loop. In a forward converter, the core is only driven in quadrant 1. Care must be taken not to saturate it, since only a “minor loop” is used. The core is driven in the +H direction, and when the MOSFET turns off, the core is allowed to “float back” to the H = 0 position. As there is no negative drive, the core cannot be driven into quadrant 3 (as in the case of a push-pull converter), and so the core always returns to the B_{REM} (remnant) position.

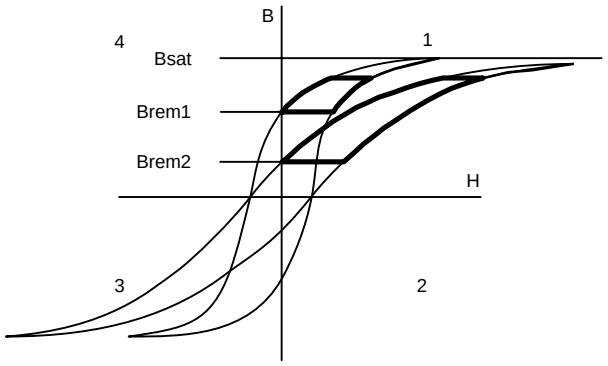


Figure 28

In some cases, a small air gap is placed in the core, which causes the B/H curve to be skewed out. The remnant position can thus be lowered from the Brem1 to the Brem2 position, allowing a larger area of operation. In all joined cores (such as RM or EE), this small gap actually exists in the form of the interface between the two cores and causes the BH curve to skew over. In high-frequency applications, this gap has a significant beneficial effect on the operation of the transformer. The number of turns is already low, and the gap prevents core saturation.

Other converters (such as half-bridge and push-pull) use all four quadrants and make better use of the whole core. These, however, require additional power switching devices and windings and are therefore not used. At high frequencies, the core losses of ferrite materials are high, so the used flux must be reduced. once this is done, the problem becomes insignificant, very small core excursions are used.

In selecting the core type and size, the transformer losses need to be divided more or less evenly between core and copper losses. Most manufacturers will now supply formulas extracted from core loss tables that allow precise core loss calculations to be made. It is important to remember that most ferrite manufacturers use peak-to-peak flux for their calculations, while for single quadrant converters, the core losses will be halved compared to the data published. Most ferrite manufacturers will likewise recommend levels no higher than 200 mT for the highest flux swing, to cover the complete temperature and operating conditions. Most ferrites have the lowest core losses at between 75 and 95°C. As the temperature in the transformer gradually rises, the efficiency of the transformer will increase.

To design a forward converter transformer, the following data is necessary:

F_{SW}	Operating Switching Frequency, usually 20 to 500 kHz
d_{max}	Maximum duty cycle, usually 50% in Vishay Siliconix products
h	Target efficiency, usually 0.75 to 0.85
V_{inmin}	Minimum input voltage used
P_{out}	Total output power
V_{out}	Output Voltage(s) required

In this case, a design for a 48-V (38- to 60-V), 5-V, 4-A (20-W) device operating at 50% duty cycle with 500-kHz switching frequency will be demonstrated. The period of conversion will be 2 μs, and the maximum on-time thus Tonmax = 1 μs.

The EF12.6, or the EPC13, which have similar characteristics, will be used as the core. The core operating flux has been selected to 85 mT as a first pass design. The loss in Philips 3F4 material is calculated from (source Philips Components):

$$P_v = 12x10^{-2} \cdot f^{1.75} \cdot B^{29} \cdot (0.95x10^{-4} \cdot T^2 - 1.1x10^{-2} \cdot T + 1.15)$$

Where:

P_V = power loss in W/m^3

B = operating flux density in Tesla

f = operating frequency in Hertz

T = core temperature in °C

With 500 kHz, 85 mT, and 50°C, the core loss can be calculated as:

$$P_v = 742.5 \times 10^3 \text{ W/m}^3 \text{ or } 0.742 \text{ W/cm}^3$$

The volume of the EF12.6 core is specified as 384 mm^3 or 0.384 cm^3.

Therefore the core loss will be:

$P = 0.742 \times 0.384$
$P = 0.285\ W \approx 1/4\ W$

which represents less than 2% of the total converter losses.

The converter transformer can be calculated by using the following adapted version of Faraday's equation:

$$N = \frac{V_{in\ min} \times t_{on\ max}}{B_{max} \times A_{eff}}$$

Where:

Vinmax = minimum input voltage (V)

N = number of turns (Integer)

B_{max} = maximum peak flux (Tesla)

A_{ef} = effective area of core (m^2)

In the case of the EF12.6, the minimum number of turns will be:

$$N = \frac{36\ V \times 1\ \mu s}{85\ mT \times 12.2\ mm^2}$$

N = 36.64 Turns [37 Turns

This is the calculated minimum number of turns that should be applied. To determine the turns for a given output voltage, first determine the output voltage (5 V). Then determine all the other losses that will exist in series with the output: including the choke, transformer dc losses, and rectifier forward drop. Assuming these add up to 0.5 V, with a duty cycle of 50%, the transformer will be required to supply a peak voltage of

Vsec = (Vout+Vloss)/Dmax

Vsec = (5 V + 0.5 V)/0.5 = 11 V

The transformer turns ratio is thus determined: for 36-V input, 11-V output is required. The turns ratio is therefore TR=36/11 = 3.27.

For the 5-V output, the number of turns required is:

NS=Np/TR = 11.01

Therefore, the number of turns selected is 11. The Si9114A will require a few miliamps of current to power itself and drive the power MOSFET. This power can be taken from a winding which peak charges a capacitor through a diode and does not require an inductor. In this case, 11 turns can also be taken (as this was calculated to be sufficient for 11 V).

SKIN DEPTH

Conductors carrying high-frequency ac current are subject to a "skin effect" in which the current has a tendency to flow predominantly on the surface of the conductor instead through the whole cross section. The value at which the current falls to 1/e (37%) is called the "skin depth." Below this depth, very little usage of copper is made, and multiple strands are required for applications where higher current is required. In some instances, it may be necessary to use larger wire than indicated, due to mechanical assembly constraints and ease of manufacture. The skin depth can be calculated from:

$$X_D = \frac{66}{\sqrt{f}}\ mm$$

Operation at 500 kHz means that the skin depth will be 0.093 mm (or approximately 0.1 mm). Ideally, a conductor with a diameter just over twice the skin depth is recommended. In this case, therefore, 0.2 mm or thereabouts will suffice.

LEAKAGE INDUCTANCE

In PWM converters, the coupling factor between windings should be optimized to minimize the leakage inductance. Leakage inductance is a parasitic element, storing energy that will need to be dissipated. This leakage is a measure of the quality of the coupling; the lower it is, the better the transformer and its performance. The leakage inductance can be measured by shorting out the 5-V winding and measuring the primary inductance. Ideally, this should be zero, but in reality values of less than 10% of the primary inductance are typical. This value can be minimized by splitting the primary winding in two halves, and by sandwiching all secondaries in between the two primary halves.

In this case, the transformer was wound as follows:

Winding Order	Winding Name	# Turns	Wire Size	Start Pin	End Pin
1	Half Primary	17	1x0.3 mm	1	10
2	Bias Winding	11	3x0.3 mm	3	9
3	Secondary	11	3x0 3 mm	4,5	7 6
4	Half Primary	18	1x0.3 mm	10	2

Copper wire of 0.3 mm was used to obtain single layer fill across the surface of the bobbin.

The wound transformer had the following characteristics:

Winding	Inductance	DC Resistance
Primary	883 µH	151 mΩ
Secondary	87 µH	25 mΩ

The leakage inductance was measured at 2.25 µH, which represents less than 1/4% of the primary inductance.

The configuration of the forward converter transformer is as follows (note the polarity/phasing of the windings):

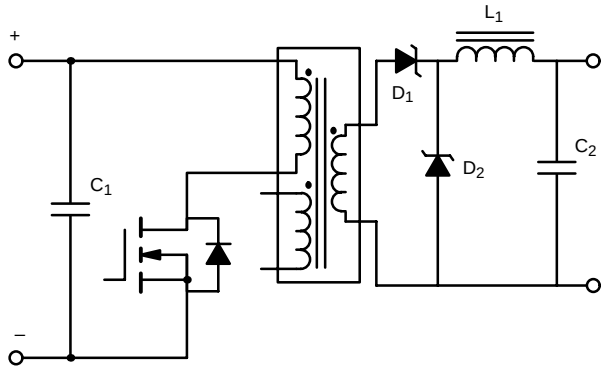


Figure 29

The above equations and calculations are supplied only as a guide for the designer. In practical terms other factors will must be considered, including the following:

- Effective required voltage adjustment range of output
- Losses in the primary side of the circuit, including the sense resistor and the MOSFET voltage drops
- Losses in the secondary side of the circuit, including dc losses in the output choke
- Forward voltage of the rectifier over load and temperature
- Interconnection losses, including remote sense drops
- OR-ing diode losses, if used in multiple converters.

Appendix B

FLYBACK CONVERTER TRANSFORMER DESIGN

The flyback magnetic component is often referred to as a transformer, but should in fact be viewed as an inductor with energy storage capability.

Two modes of operation are possible. In d*iscontinuous mode*, all the energy is transferred to the output(s). In c*ontinuous mode*, some energy remains in the inductor. Discontinuous mode provides the advantages of a smaller inductor and the absence of unexpected or difficult transfer modes in the control mechanism. As energy transfer is complete, furthermore, rectifier currents always fall to zero before reverse voltages are applied. The result is lower rectifier switching losses.

For the sake of simplicity, it is recommended that only highly experienced designers use continuous mode, further information on which can be reviewed in some of the publications listed in the reference section of this application note. In this appendix, only the discontinuous mode is explained.

Due to the discontinuous nature of the energy transfer mechanism, flyback inductors are usually larger than the transformers encountered in forward and other Buck topologies, where only voltage transformation—and no energy storage—is performed.

To design a Flyback *Inductor*, the following information must be known:

F_{sw}	operating switching frequency (usually 20 to 500 kHz)
D_{max}	maximum duty cycle (usually 50% in Vishay Siliconix products)
n	target efficiency (usually 0.75 to 0.85)
V_{MIN}	minimum input voltage used
P_{OUT}	total output power
V_{OUT}	output voltage(s) required.

In this case, a design for a 24-V (16- to 30-V), 5-V, 2-A (10 W) inductor will be demonstrated.

The first step is to determine the minimum primary inductance from:

$$L_{pmin} = \frac{\left(V_{in\ min} \times t_{on\ max}\right)^2 \times f_{sw} \times \eta}{2 \times P_{out}}$$

$$L_{pmin} = \frac{(18\ \text{IV} \times 2\ \mu\text{s})^2 \times 250\ \text{kHz} \times 0.75}{2 \times 10\ \text{W}}$$

$$L_{pmin} = 12.2\ \mu\text{H} \approx 12\ \mu\text{H}$$

The next step is to determine the peak primary current. For a given inductor, the applied voltage will be:

$$V = L\frac{di}{dt}$$

Re-arranging yields:

$$i_{pk} = \frac{V_{in\ min} \times t_{on\ max}}{L_{pmax}}$$

$$i_{pk} = \frac{18\ \text{V} \times 2\ \mu\text{s}}{12\ \mu\text{H}} = 3\ \text{A}$$

The R.M.S. value for a triangular waveform can be used to calculate the power that will be dissipated in the MOSFET:

$$i_{ms} = i_{pk} \times \sqrt{\frac{\delta_{max}}{3}}$$

$$i_{ms} = 3\ \text{A} \times \sqrt{\frac{0.5}{3}} = 1.22\ \text{A} \approx 1.2\ \text{A}$$

To calculate the number of turns required for the 5-V output the following quotation can be used:

$$N_S = N_p \frac{\left(V_O + V_F\right)(1 - D_{max})}{V_{inmin}\, D_{max}}$$

in this case, for D_{max} = 0.5 and V_F = 0.6 V for a 5 V output, the secondary turns will be:

$$N_S = N_p \frac{(5\ \text{V} + 0.6\ \text{V})(1 - 0.5)}{16\ \text{V} \times 0.5}$$

Therefore

$$\therefore \frac{N_P}{N_S} = \frac{1}{0.35} = 2.86$$

The primary turns can be derived from the same equation used for the forward converter output indicator:

$$N_{min} = \frac{L_P \times I_{pK}}{B_{max} \times A_{min}} = \frac{12\ \mu H \times 3\ A}{200\ mT \times 13\ mm^2} = 13.85\ \text{Turns.}$$

$$\therefore N_{min} = 14\ \text{Turns.}$$

For 5 V, the number of turns will then be:

$$N_S = N_p \times 0.35 = 14 \times 0.35 = 4.9\ T \simeq 5\ T$$

In the flyback converter, all windings appear in parallel with each other, and will track the voltage of the controlled output. Small variations will be present due to the differences between Schottky and bipolar rectifiers. It must also be remembered that this will also cause the bias winding to collapse under short circuit conditions with possible overpower dissipation.