AVERLOGIC

AL4CE205/215/225/235/245

256, 512, 1K, 2K, 4K x 18 Advanced Synchronous FIFOs

Applications

- Multimedia System
- ATM Switches
- Routers
- Cable Modems
- Wireless Base Stations
- SONET(Synchronous Optical Network) Multiplexers
- TBC(Time Base Corrector)
- Hard Disk cache memory

Description

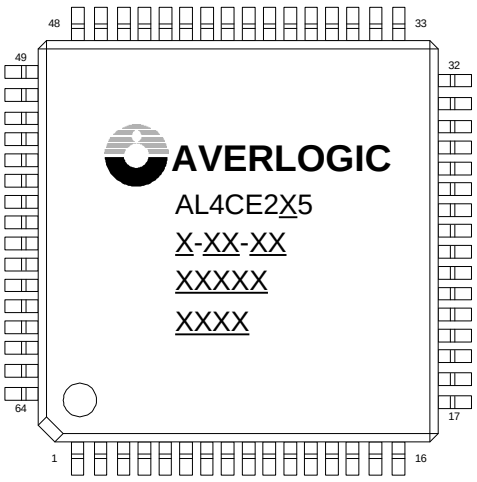
The AL4CE2x5 series memory products are high-performance, low-power 18bit read/write FIFO (First-In-First-Out) memory chip designed to buffer high speed streaming data for a wide range of applications. The AL4CE2x5 FIFO memories are the advanced version of AL4CS2x5. This product series support additional functions, such as Bus-matching, Endian select and Retransmit, can benefit designing efforts.

Features

- High performance, low-power, FIFO(First-In First-Out) memory
- 256 x 18 bit I/O port (AL4CE205)
- 512 x 18 bit I/O port (AL4CE215)
- 1K x18 bit 1/O port (AL4CE225)
- 2K x18 bit I/O port (AL4CE235)
- 4K x18 bit I/O port (AL4CE245)
- High clock speed (133MHz)
- Fully independent read/write access
- Retransmit the data (reread the data)
- Empty, Full, Half Full and programmable Almost Empty, Almost Full flags
- Output enable control (data skipping)
- User selectable input and output bus width
- Big/Little-Endian word format selectable
- 3.3V±10% power supply with 5V signal tolerant input
- Standard 64-pin TQFP and STQFP

Ordering Information

Part number	AL4CE205, AL4CE215, AL4CE225, AL4CE235, AL4CE245
Package	64-pin plastic TQFP and STQFP
Power Supply	+3.3V±10%



TQFP, STQFP PACKAGE TOP VIEW

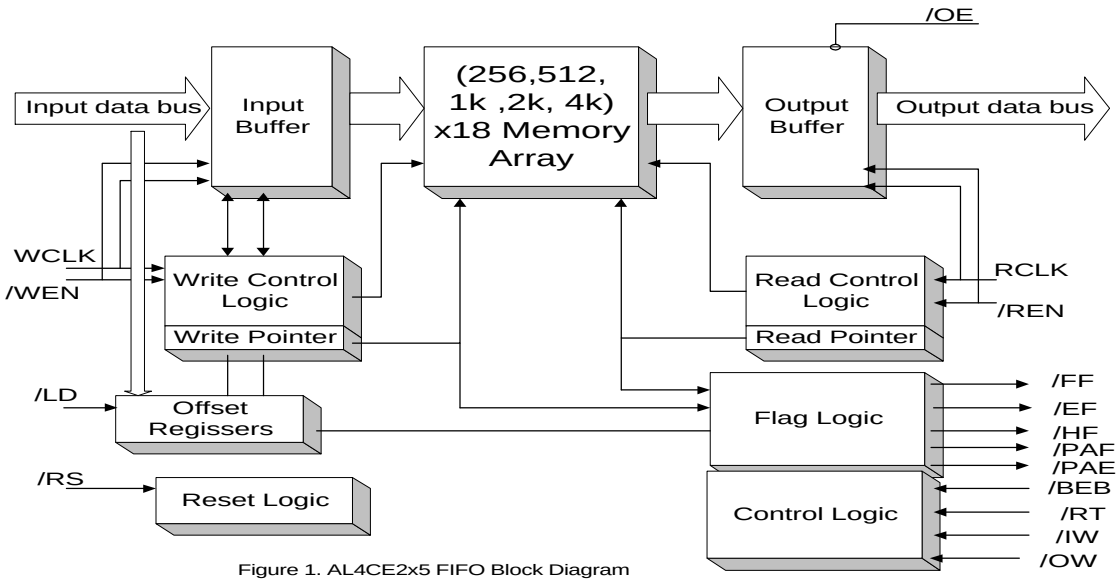


Figure 1. AL4CE2x5 FIFO Block Diagram

The 18bit input and output ports operate independently at a maximum speed of 133 MHz. The built-in address decoder and pointer managing circuits provide a straightforward bus interface to serially read/write memory that reduces inter-chip design efforts. The AL4CE2x5 embedded memory array and high performance process technologies with extended controller functions (read skip, fixed and programmable status flags.. etc.) offer flexible memory management.

These FIFOs support up to 18bit input and output data bus-width that is controlled by separate clock and enable signals respectively. The input data is acquired at each rising edge of a free running write clock while a write enable control pin is asserted. The output data is available after each rising edge of a free running read clock while a read enable and output enable control pins are asserted. When output enable (/OE) is LOW, the data output bus is active. If /OE is HIGH, the output data bus will be in a high-impedance. This signal can control whether the data is going to be skipped during the read operation.

The FIFO Full/Empty, Half-Full and programmable Almost Full/Almost Empty flags are powerful functions that can help controlling software to manipulate the FIFO more easily or to do retransmit operation.

Bus-Matching feature can flexibly configure input and output bus width. The chip can automatically convert the input data bus width to match up output data bus width by packing or unpacking the data. A Big-Endian/Little-Endian data word format is provided to invert the read-in bytes sequence for output. And the Retransmit function allows data to be reread from the FIFO more than once.

These chips are available as a 64pin TQFP and STQFP Package

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