Dual Channel Synchronous Buck DC/DC Converter

Description

The SD8911 is a high efficiency synchronous, dual channel PWM step-down DC/DC converter working under an input voltage range of 2.5V to 5.5V. It integrates two PWM synchronous step-down DC-DC converters. 100% duty cycle capability extends battery life in portable devices, while the quiescent current (one channel) is 200μA with no load, and drops to <1μA in shutdown.

Each DC-DC converter has independent enable input and short-circuit protection allowing versatile power sequence combination.

The SD8911 converters are available in the industry standard DFN3*3-10L packages (or upon request).

Features

- Up to 94% Efficiency
- Current Mode Operation for Excellent Line and Load Transient Response
- Output Voltage: 0.6V ～ 5.5V
- Low Quiescent Current (one Channel): 200μA
- Up to 800mA Load Current
- Soft-start
- Automatic PWM/PFM Mode Switching
- No Schottky Diode Required
- 1MHz Constant Frequency Operation
- Short-Circuit Protection
- Shutdown Quiescent Current: < 1μA
- DFN3*3-10L Package

Applications

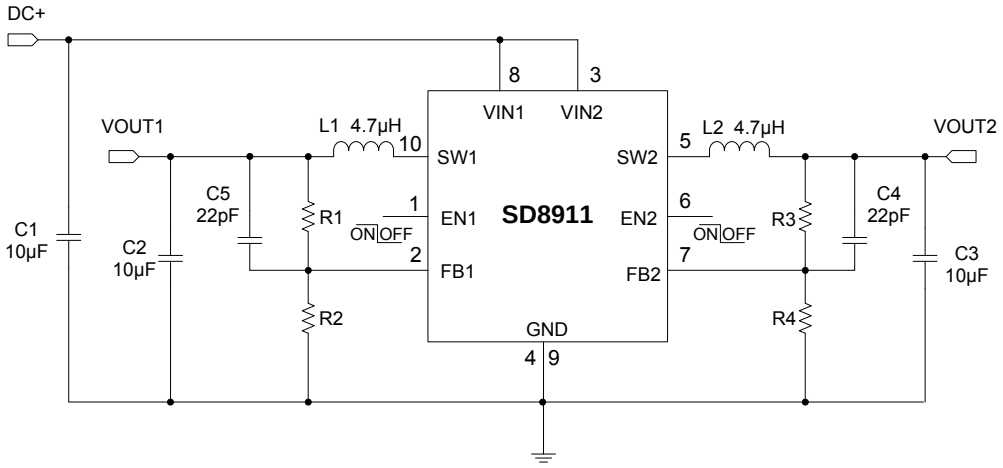
- Digital cameras and MP3
- Palmtop computers / PDAs
- Cellular phones
- Wireless handsets and DSL modems
- Portable media players
- PC cards

Order Information

SD8911-① ②:

Symbol	Description
①	Denotes Output Voltage: A : Adjustable Output
②	Denotes Package Types: J: DFN3*3-10L

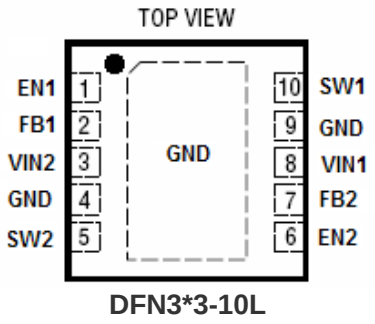
Typical Application Circuit



*Adjustable Output Voltage: V_{OUT1} = 0.6V • [1 + (R1/R2)]; V_{OUT2} = 0.6V • [1+ (R3/R4)].

Model	VOUT (V)	VIN(V)	Package
SD8911-AJ	0.6 ～ 5.5	2.5 ～ 5.5	DFN3*3-10L

Pin Assignment and Description



DFN3*3-10L

PIN	NAME	DESCRIPTION
1	EN1	ON/OFF Control 1 (High Enable)
2	FB1	Output feedback 1
3	VIN2	Input 2
4	GND	Ground
5	SW2	Switch Output 2
6	EN2	ON/OFF Control 2 (High Enable)
7	FB2	Output feedback 2
8	VIN1	Input 1
9	GND	Ground
10	SW1	Switch Output 1

Absolute Maximum Ratings (Note 1)

- Power Dissipation……Internally limited
- V_{IN} ……..-0.3V ～ +6V
- V_{EN} ……..……-0.3V ～ (V_{IN}+0.3)V
- V_{SW} ……..……-0.3V ～ (V_{IN}+0.3)V
- V_{OUT}……...-0.3V ～ +6V
- I_{SW} ……..1.5A
- Operating Temperature Range (Note 2)……..……...-40℃ ～ + 85℃
- Storage Temperature Range ……..……-65℃ ～ +150℃
- Junction Temperature ……..……-40℃ ～ +125℃
- Lead Temperature (Soldering 10 sec.) ……..+265℃

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

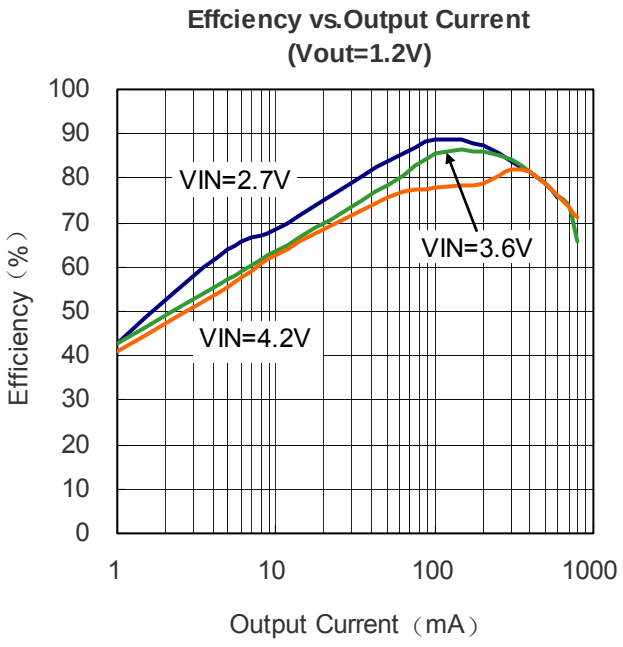
Note 2: The SD8911 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

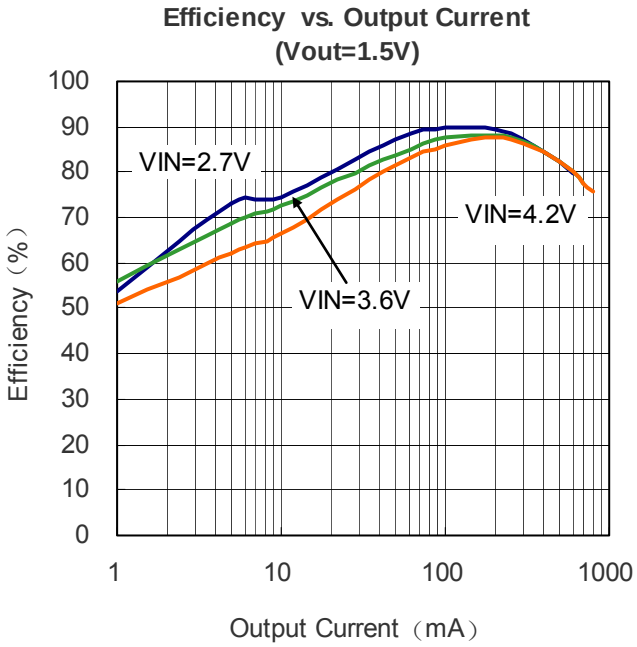
Electrical Characteristics (VOUT1 or VOUT2)

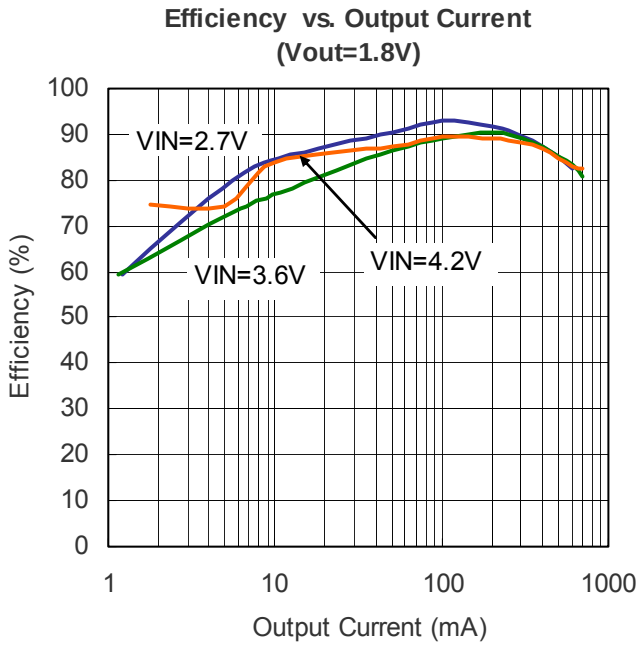
Operating Conditions: TA=25℃, V_{IN}=3.6V, unless otherwise specified.

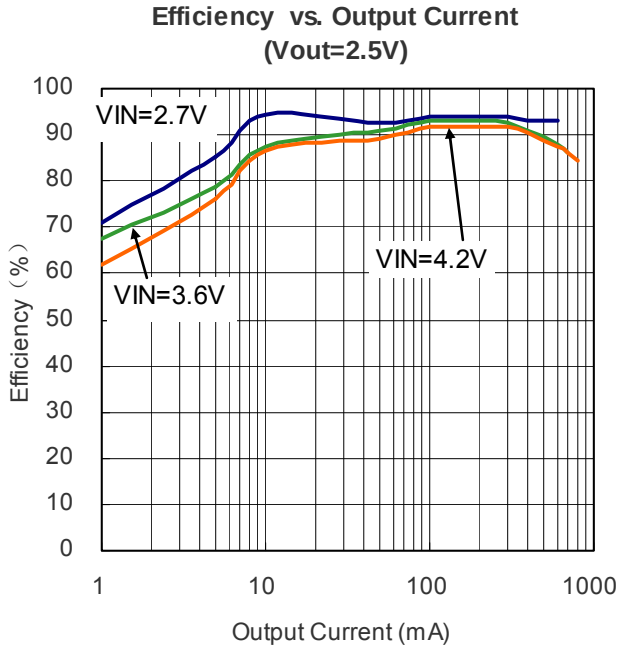
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OUT1,2}$	Output Voltage		0.6		5.5	V
V_{IN}	Operating Voltage Range		2.5		5.5	V
I_Q	Quiescent Current	V_{FB} = 0.5V or V_{OUT} = 90%, I_{LOAD} = 0A		200		μA
I_{SHDN}	Shutdown Current	V_{EN} = 0V, V_{IN} = 4.2V		0.1	1	μA
V_{FB}	Regulated Voltage	TA = 25℃	0.588	0.6	0.612	V
ΔV_{FB}	V_{REF}	V_{IN}=2.5V ～ 5.5V		0.03	0.4	%/V
I_{FB}	Feedback Current				±30	nA
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V or V_{OUT} = 100%		1		MHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 100mA		0.3		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = -100mA		0.39		Ω
ΔV_{LINE}	V_{OUT} Line Regulation	V_{IN}=2.5V ～ 5.5V		0.03	0.3	%/V
ΔV_{LOAD}	V_{OUT} Load Regulation			0.33		%
EFFI	Efficiency	When connected to ext. components, V_{IN} = V_{EN} = 2.7V, V_{OUT} = 2.5V, I_{OUT} = 100mA		94		%

Typical Performance Characteristics (VOUT1 or VOUT2)

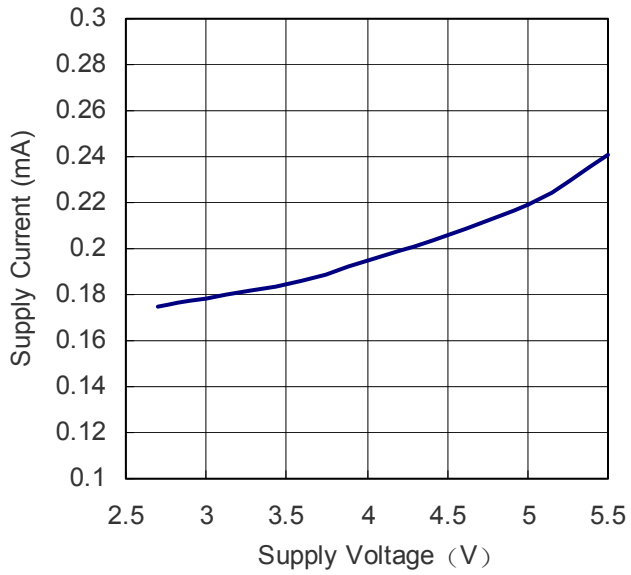




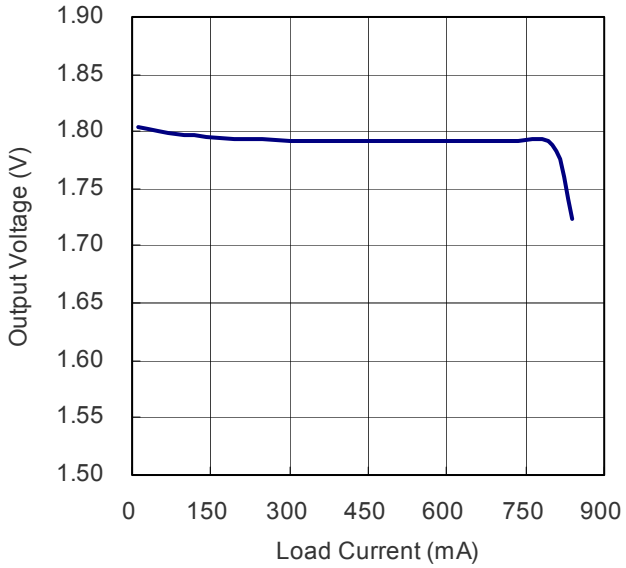




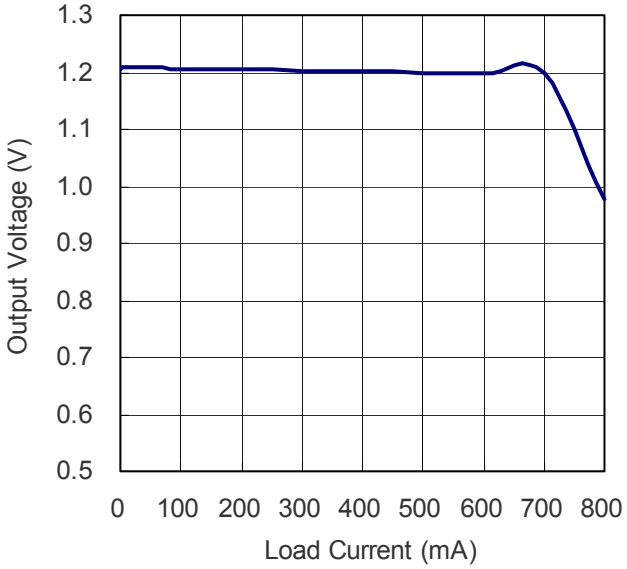
Supply Current vs Supply Voltage
(Vout=1.8V Io=0A)



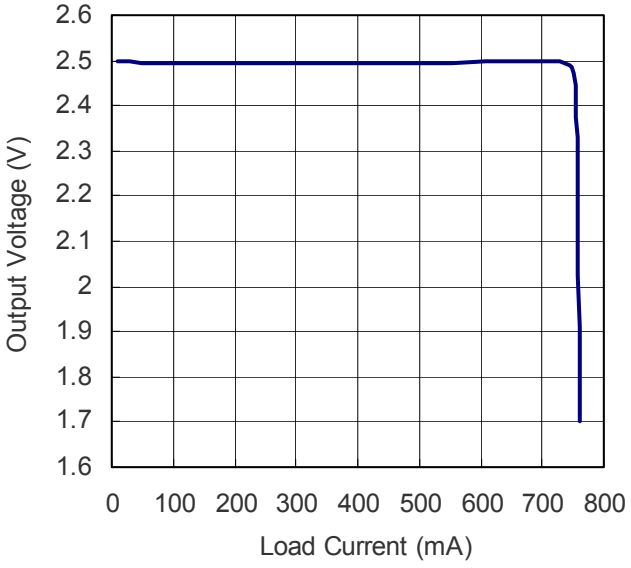
Output Voltage vs. Load Current
(Vin=4.2V,Vout=1.8V)



Output Voltage vs. Load Current
(Vin=3.6V,Vout=1.2V)

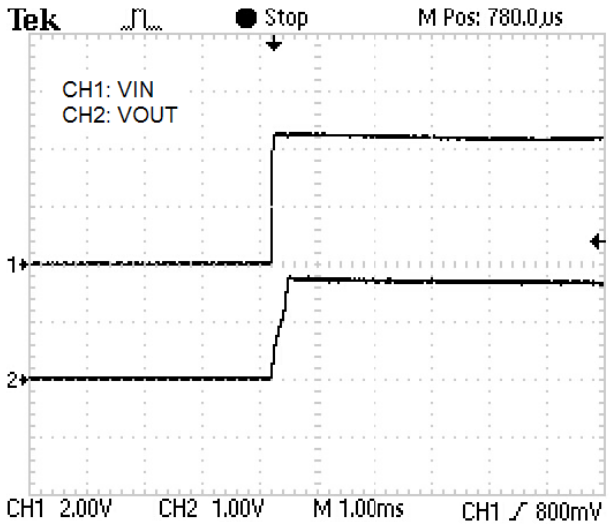


Output Voltage vs. Load Current
(Vin=3.6V,Vout=2.5V)



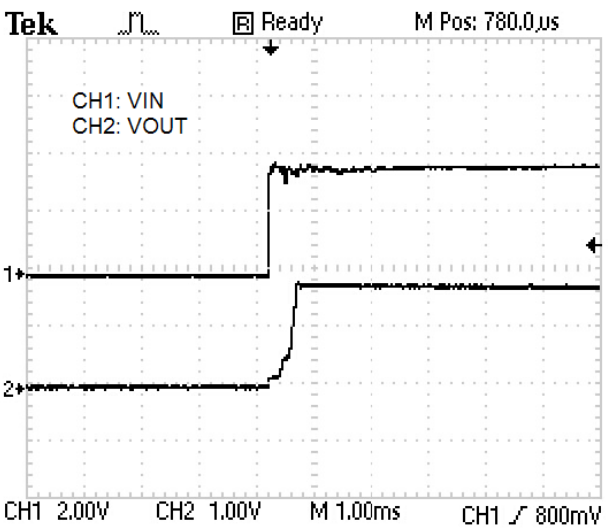
Start –up from Shutdown

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0mA)

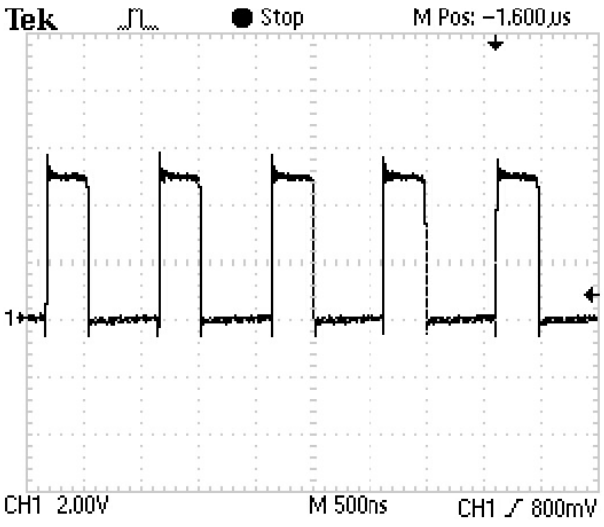


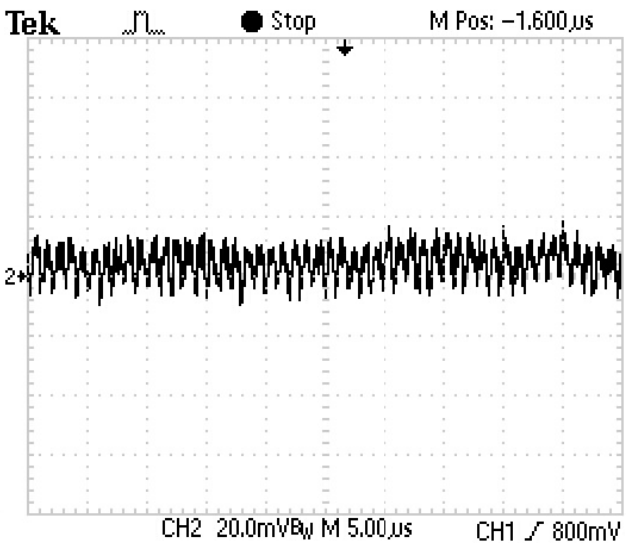
Start –up

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=200mA)

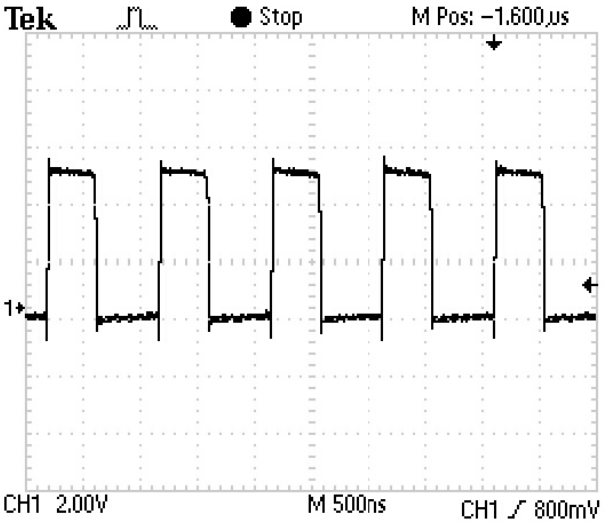


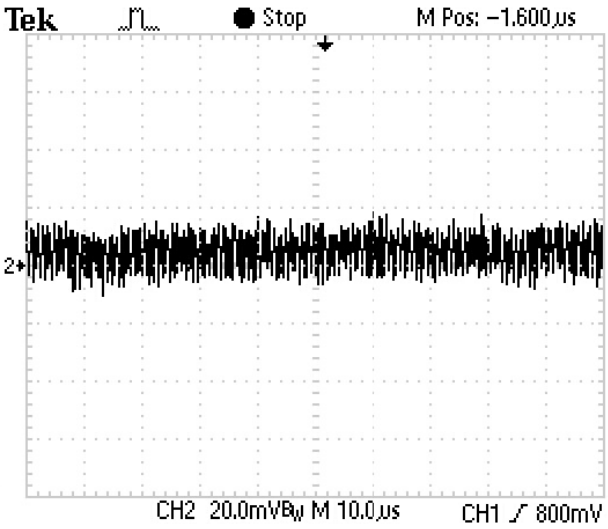
Switching node & output wave (V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=200mA)





Switching node & output wave (V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=800mA)





Pin Functions

EN1 (Pin 1): En Control Input. Forcing this pin above 1.3V enables the VOUT1. Forcing this pin below 0.7V can shuts down the VOUT1. In shutdown, all functions are disabled drawing <1μA supply current. Do not leave EN1 floating.

FB1 (Pin 2): Output Feedback 1. Receive the feedback voltage from an external resistive divider across the output 1. The output voltage is set by a resistive divider according to the following formula: V_{OUT1} = 0.6V • [1 + (R1/R2)].

VIN2 (Pin 3): Supply Pin for VOUT2. It must be closely decoupled to GND, or with a 10μF or greater ceramic capacitor.

GND (Pin 4, 9): Ground Pin.

SW2 (Pin 5): Switch Node for VOUT2 Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

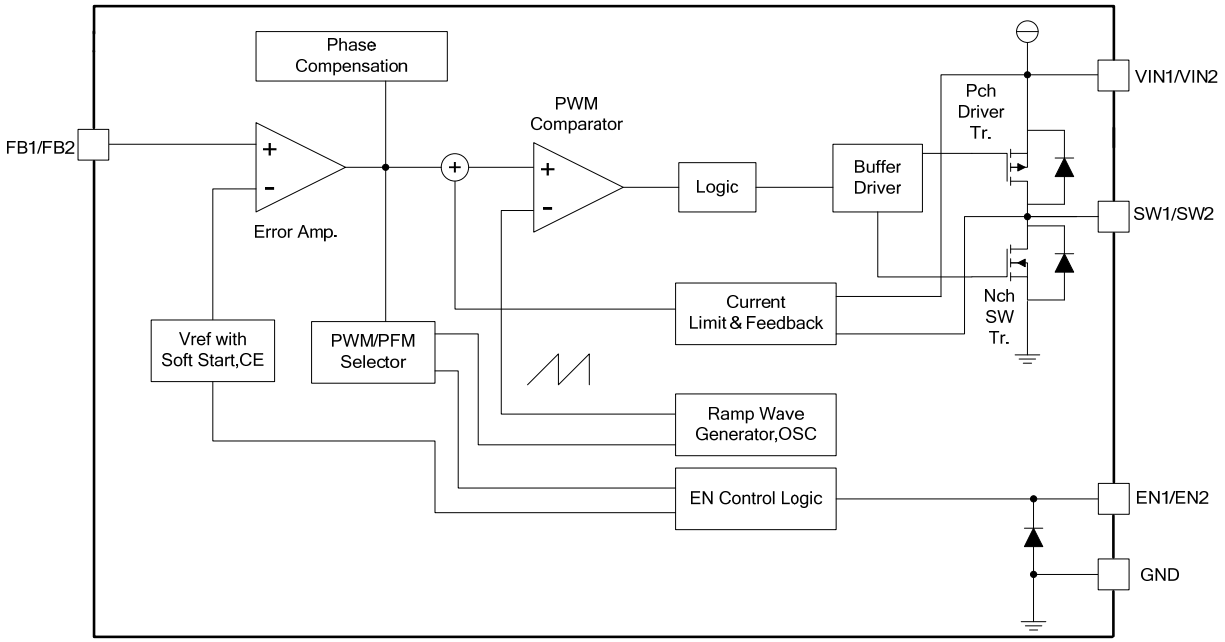
EN2 (Pin 6): En Control Input. Forcing this pin above 1.3V enables the VOUT2. Forcing this pin below 0.7V can shuts down the VOUT2. In shutdown, all functions are disabled drawing <1μA supply current. Do not leave EN2 floating.

FB2 (Pin 7): Output Feedback 2. Receive the feedback voltage from the external resistive divider across the output. The output voltage is set by a resistive divider according to the following formula: V_{OUT2} = 0.6V • [1 + (R3/R4)].

VIN1 (Pin 8): Supply Pin for VOUT1. It must be closely decoupled to GND, or with a 10μF or greater ceramic capacitor.

SW1 (Pin 10): Switch Node for VOUT1 Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

Block Diagram



Application Information

The basic SD8911 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1μH to 4.7μH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is $\triangle I_L$ = 320mA (40% of 800mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 960mA rated inductor should be enough for most applications (800mA + 160mA). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the SD8911 requires to operate.

Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR).Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

Where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% - (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: VIN quiescent current and I^2R losses. The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge △Q moves from VIN to ground. The resulting △Q/△t is the current out of VIN that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f (Q_T+Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows: $R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$ The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

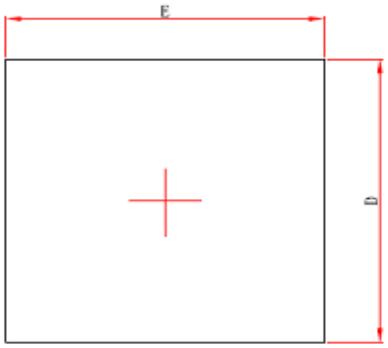
PCB Layout Guidelines

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the SD8911. Check the following in your layout:

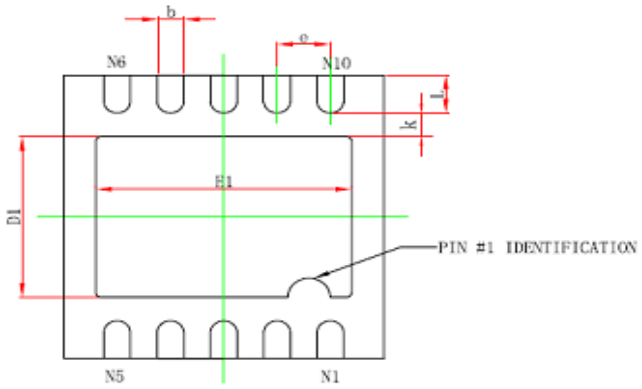
1. The power traces, consisting of the GND trace, the SW1,SW2 trace and the VIN1,VIN2 trace should be kept short, direct and wide.
2. Put the input capacitor as close as possible to the device pins (VIN and GND).
3. SW1, SW2 node is with high frequency voltage swing and should be kept small area. Keep analog components away from SW1, SW2 node to prevent stray capacitive noise pick-up.
4. Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.
5. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

Packaging Information

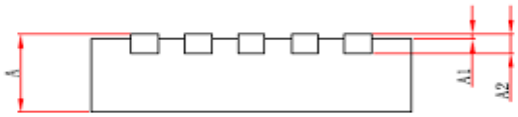
DFN3*3-10L Package Outline Dimension



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A2	0.153	0.253	0.006	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	2.300	2.500	0.091	0.098
k	0.200MIN		0.008MIN	
b	0.200	0.300	0.008	0.012
e	0.500TYP		0.020TYP	
L	0.300	0.500	0.012	0.020