Description

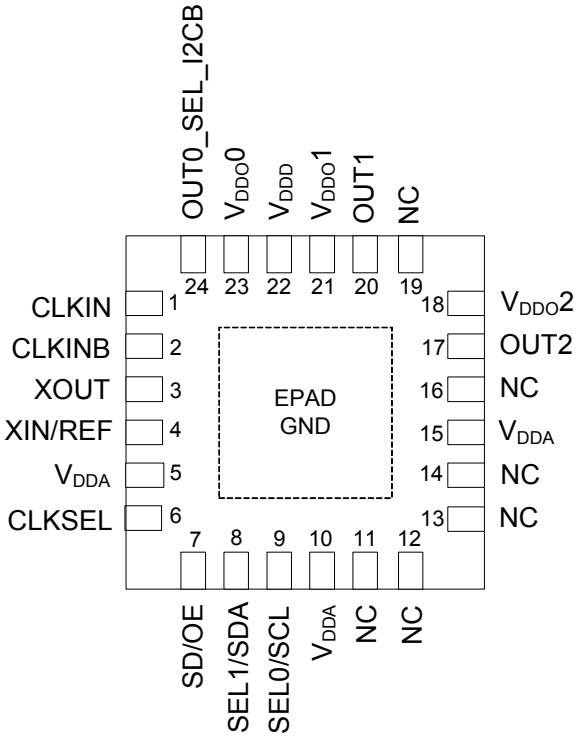
The 5P49V5923 is a programmable clock generator intended for high performance consumer, networking, industrial, computing, and data-communications applications. Configurations may be stored in on-chip One-Time Programmable (OTP) memory or changed using I^2C interface. This is IDT's fifth generation of programmable clock technology (VersaClock® 5).

The frequencies are generated from a single reference clock. The reference clock can come from one of the two redundant clock inputs. A glitchless manual switchover function allows one of the redundant clocks to be selected during normal operation.

Two select pins allow up to 4 different configurations to be programmed and accessible using processor GPIOs or bootstrapping. The different selections may be used for different operating modes (full function, partial function, partial power-down), regional standards (US, Japan, Europe) or system production margin testing.

The device may be configured to use one of two I^2C addresses to allow multiple devices to be used in a system.

Pin Assignment



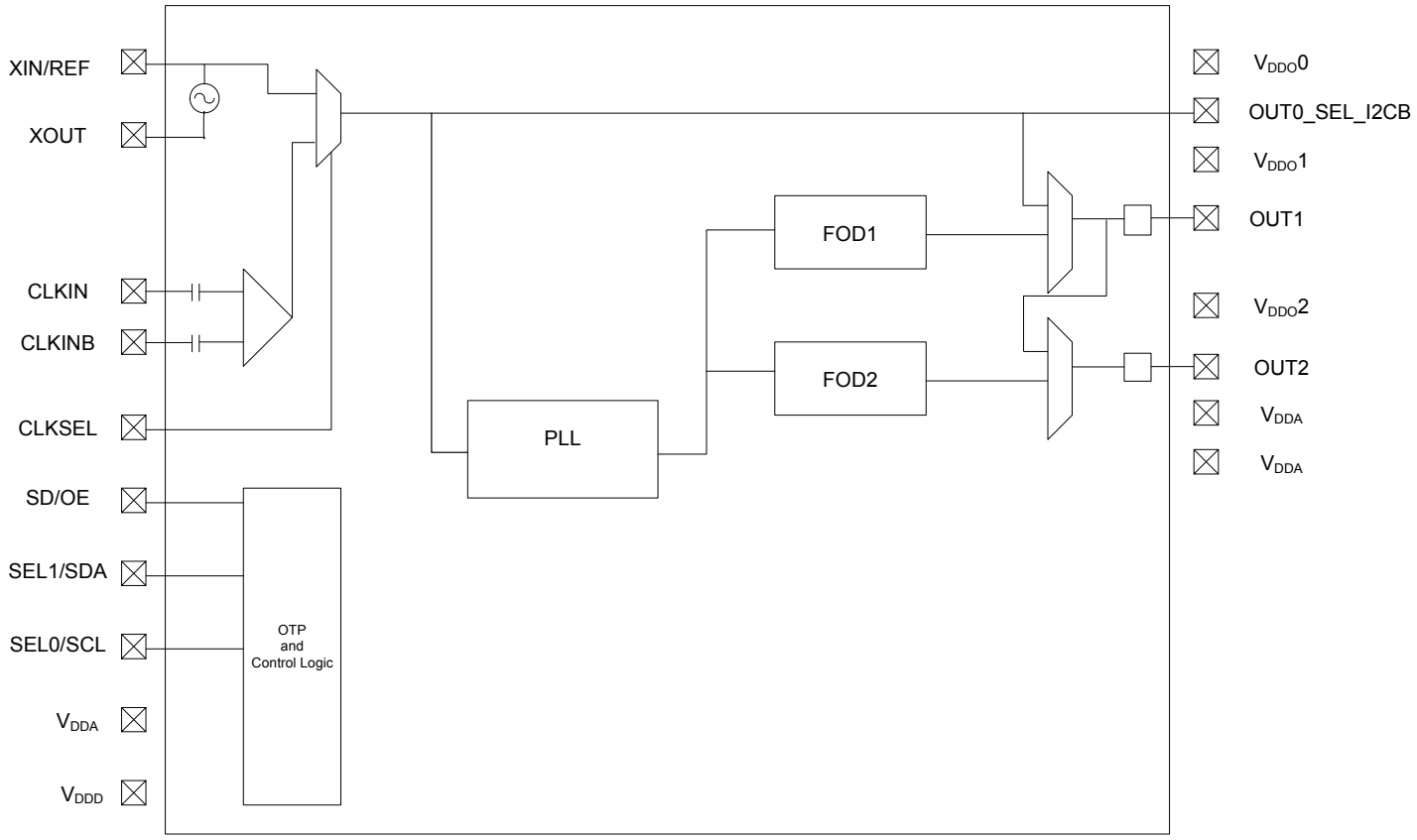
24-pin VFQFPN

Features

- Generates up to two independent output frequencies
- High performance, low phase noise PLL, <0.7 ps RMS typical phase jitter on outputs
- Two fractional output dividers (FODs)
- Independent Spread Spectrum capability on each output
- Four banks of internal non-volatile in-system programmable or factory programmable OTP memory
- I^2C serial programming interface
- Three LVCMOS outputs, including one reference output
- I/O Standards:
  - Single-ended I/Os: 1.8V to 3.3V LVCMOS
- Input frequency ranges:
  - LVCMOS Reference Clock Input (XIN/REF) – 1MHz to 200MHz
  - LVDS, LVPECL, HCSL Differential Clock Input (CLKIN, CLKINB) – 1MHz to 200MHz
  - Crystal frequency range: 8MHz to 40MHz
- Output frequency ranges:
  - LVCMOS Clock Outputs – 1MHz to 200MHz
- Individually selectable output voltage (1.8V, 2.5V, 3.3V) for each output
- Redundant clock inputs with manual switchover
- Programmable loop bandwidth
- Programmable slew rate control
- Programmable crystal load capacitance
- Individual output enable/disable
- Power-down mode
- 1.8V, 2.5V or 3.3V core V_{DDD}, V_{DDA}
- Available in 24-pin VFQFPN 4mm x 4mm package
- -40° to +85°C industrial temperature operation

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Functional Block Diagram



Applications

- Ethernet switch/router
- PCI Express 1.0/2.0/3.0
- Broadcast video/audio timing
- Multi-function printer
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fiber Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

Table 1: Pin Descriptions

Number	Name	Type		Description
1	CLKIN	Input	Internal Pull-down	Differential clock input. Weak 100kohms internal pull-down.
2	CLKINB	Input	Internal Pull-down	Complementary differential clock input. Weak 100kohms internal pull-down.
3	XOUT	Input		Crystal Oscillator interface output.
4	XIN/REF	Input		Crystal Oscillator interface input, or single-ended LVCMOS clock input. Ensure that the input voltage is 1.2V max. Refer to the section “Overdriving the XIN/REF Interface”.
5	V_{DDA}	Power		Analog functions power supply pin. Connect to 1.8V to 3.3V. V_{DDA} and V_{DDD} should have the same voltage applied.
6	CLKSEL	Input	Internal Pull-down	Input clock select. Selects the active input reference source in manual switchover mode. 0 = XIN/REF, XOUT (default) 1 = CLKIN, CLKINB CLKSEL Polarity can be changed by I2C programming as shown in Table 4.
7	SD/OE	Input	Internal Pull-down	Enables/disables the outputs (OE) or powers down the chip (SD). The SH bit controls the configuration of the SD/OE pin. The SH bit needs to be high for SD/OE pin to be configured as SD. The SP bit (0x02) controls the polarity of the signal to be either active HIGH or LOW only when pin is configured as OE (Default is active LOW.) Weak internal pull down resistor. When configured as SD, device is shut down and the single-ended LVCMOS outputs are driven low. When configured as OE, and outputs are disabled, the outputs can be selected to be tri-stated or driven high/low, depending on the programming bits as shown in the SD/OE Pin Function Truth table.
8	SEL1/SDA	Input	Internal Pull-down	Configuration select pin, or I^2C SDA input as selected by OUT0_SEL_I2CB. Weak internal pull down resistor.
9	SEL0/SCL	Input	Internal Pull-down	Configuration select pin, or I^2C SCL input as selected by OUT0_SEL_I2CB. Weak internal pull down resistor.
10	V_{DDA}	Power		Analog functions power supply pin.Connect to 1.8V to 3.3V. V_{DDA} and V_{DDD} should have the same voltage applied.
11	NC	–		No connect.
12	NC	–		No connect.
13	NC	–		No connect.
14	NC	–		No connect.
15	V_{DDA}	Power		Analog functions power supply pin.Connect to 1.8V to 3.3V. V_{DDA} and V_{DDD} should have the same voltage applied.
16	NC	–		No connect.
17	OUT2	Output		Output Clock 2. Please refer to the Output Drivers section for more details.
18	$V_{DDO}2$	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT2.
19	NC	–		No connect.
20	OUT1	Output		Output Clock 1. Please refer to the Output Drivers section for more details.
21	$V_{DDO}1$	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT1.
22	V_{DDD}	Power		Digital functions power supply pin. Connect to 1.8 to 3.3V. V_{DDA} and V_{DDD} should have the same voltage applied.

Number	Name	Type		Description
23	$V_{DDO}0$	Power		Power supply pin for OUT0_SEL_I2CB. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT0.
24	OUT0_SEL_I2CB	Input/ Output	Internal Pull-down	Latched input/LVCMOS Output. At power up, the voltage at the pin OUT0_SEL_I2CB is latched by the part and used to select the state of pins 8 and 9. If a weak pull up (10kohms) is placed on OUT0_SEL_I2CB, pins 8 and 9 will be configured as hardware select pins, SEL1 and SEL0. If a weak pull down (10Kohms) is placed on OUT0_SEL_I2CB or it is left floating, pins 8 and 9 will act as the SDA and SCL pins of an I^2C interface. After power up, the pin acts as a LVCMOS reference output.
ePAD	GND	GND		Connect to ground pad.

PLL Features and Descriptions

Spread Spectrum

To help reduce electromagnetic interference (EMI), the 5P49V5923 supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The 5P49V5923 implements spread spectrum using the Fractional-N output divide, to achieve controllable modulation rate and spreading magnitude. The Spread spectrum can be applied to any output clock, any clock frequency, and any spread amount from ±0.25% to ±2.5% center spread and -0.5% to -5% down spread.

Table 2: Loop Filter

PLL loop bandwidth range depends on the input reference frequency (Fref) and can be set between the loop bandwidth range as shown in the table below.

Input Reference Frequency–Fref (MHz)	Loop Bandwidth Min (kHz)	Loop Bandwidth Max (kHz)
5	40	126
200	300	1000

Table 3: Configuration Table

This table shows the SEL1, SEL0 settings to select the configuration stored in OTP. Four configurations can be stored in OTP. These can be factory programmed or user programmed.

OUT0_SEL_I2CB @ POR	SEL1	SEL0	I^2C Access	REG0:7	Config
1	0	0	No	0	0
1	0	1	No	0	1
1	1	0	No	0	2
1	1	1	No	0	3
0	X	X	Yes	1	I2C defaults
0	X	X	Yes	0	0

At power up time, the SEL0 and SEL1 pins must be tied to either the VDDD/VDDA power supply so that they ramp with that supply or are tied low (this is the same as floating the pins). This will cause the register configuration to be loaded that is selected according to Table 3 above. Providing that OUT0_SEL_I2CB was 1 at POR and OTP register 0:7=0, after the first 10mS of operation the levels of the SELx pins can be changed, either to low or to the same level as VDDD/VDDA. The SELx pins must be driven with a digital signal of < 300ns Rise/Fall time and only a single pin can be changed at a time. After a pin level change, the device must not be interrupted for at least 1ms so that the new values have time to load and take effect.

If OUT0_SEL_I2CB was 0 at POR, alternate configurations can only be loaded via the I2C interface.

Table 4: Input Clock Select

Input clock select. Selects the active input reference source in manual switchover mode.
0 = XIN/REF, XOUT (default)
1 = CLKIN, CLKINB
CLKSEL Polarity can be changed by I^2C programming as shown in Table 4.

PRIMSRC	CLKSEL	Source
0	0	XIN/REF
0	1	CLKIN, CLKINB
1	0	CLKIN, CLKINB
1	1	XIN/REF

PRIMSRC is bit 1 of Register 0x13.

Reference Clock Input Pins and Selection

The 5P49V5923 supports up to two clock inputs. One input supports a crystal between XIN and XOUT. XIN can also be driven from a single ended reference clock. XIN can accept small amplitude signals like from TCXO or one channel of a differential clock.

The second clock input (CLKIN, CLKINB) is a fully differential input that only accepts a reference clock. The differential input accepts differential clocks from all the differential logic types and can also be driven from a single ended clock on one of the input pins.

The CLKSEL pin selects the input clock between either XTAL/REF or (CLKIN, CLKINB).

Either clock input can be set as the primary clock. The primary clock designation is to establish which is the main reference clock to the PLL. The non-primary clock is designated as the secondary clock in case the primary clock goes absent and a backup is needed. See the previous page for more details about primary versus secondary clock operation.

The two external reference clocks can be manually selected using the CLKSEL pin. The SM bits must be set to “0x” for manual switchover which is detailed in Manual Switchover Mode section.

Crystal Input (XIN/REF)

The crystal used should be a fundamental mode quartz crystal; overtone crystals should not be used.

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal and vice versa so for an accurate oscillation frequency you need to make sure to match the oscillator load capacitance with the crystal load capacitance.

To set the oscillator load capacitance there are two tuning capacitors in the IC, one at XIN and one at XOUT. They can be adjusted independently but commonly the same value is used for both capacitors. The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[5:0] register. Adjustment of the crystal tuning capacitors allows for maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table.

XTAL[5:0] Tuning Capacitor Characteristics

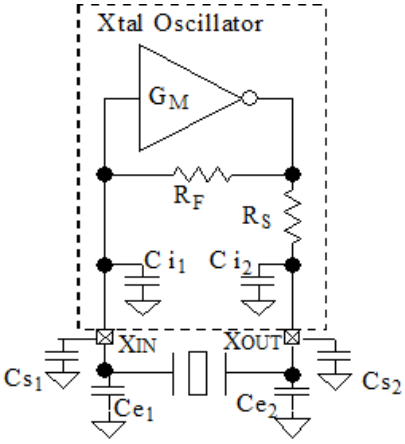
Parameter	Bits	Step (pF)	Min (pF)	Max (pF)
XTAL	6	0.5	9	25

The capacitance at each crystal pin inside the chip starts at 9pF with setting 000000b and can be increased up to 25pF with setting 111111b. The step per bit is 0.5pF.

You can write the following equation for this capacitance:

$Ci = 9pF + 0.5pF \times XTAL[5:0]$

The PCB where the IC and the crystal will be assembled adds some stray capacitance to each crystal pin and more capacitance can be added to each crystal pin with additional external capacitors.



You can write the following equations for the total capacitance at each crystal pin:

$C_{XIN} = Ci_1 + Cs_1 + Ce_1$
$C_{XOUT} = Ci_2 + Cs_2 + Ce_2$

Ci_1 and Ci_2 are the internal, tunable capacitors. Cs_1 and Cs_2 are stray capacitances at each crystal pin and typical values are between 1pF and 3pF.

Ce_1 and Ce_2 are additional external capacitors that can be added to increase the crystal load capacitance beyond the tuning range of the internal capacitors. However, increasing the load capacitance reduces the oscillator gain so please consult the factory when adding Ce_1 and/or Ce_2 to avoid crystal startup issues. Ce_1 and Ce_2 can also be used to adjust for unpredictable stray capacitance in the PCB.

The final load capacitance of the crystal:

$CL = C_{XIN} \times C_{XOUT} / (C_{XIN} + C_{XOUT})$

For most cases it is recommended to set the value for capacitors the same at each crystal pin:

$C_{XIN} = C_{XOUT} = Cx \longrightarrow CL = Cx / 2$

The complete formula when the capacitance at both crystal pins is the same:

$CL = (9pF + 0.5pF \times XTAL[5:0] + Cs + Ce) / 2$

Example 1: The crystal load capacitance is specified as 8pF and the stray capacitance at each crystal pin is Cs=1.5pF. Assuming equal capacitance value at XIN and XOUT, the equation is as follows:

8pF = (9pF + 0.5pF × XTAL[5:0] + 1.5pF) / 2 ⟶
0.5pF × XTAL[5:0] = 5.5pF ⟶ XTAL[5:0] = 11 (decimal)

Example 2: The crystal load capacitance is specified as 12pF and the stray capacitance Cs is unknown. Footprints for external capacitors Ce are added and a worst case Cs of 5pF is used. For now we use Cs + Ce = 5pF and the right value for Ce can be determined later to make 5pF together with Cs.

12pF = (9pF + 0.5pF × XTAL[5:0] + 5pF) / 2 ⟶
XTAL[5:0] = 20 (decimal)

Manual Switchover Mode

When SM[1:0] is “0x”, the redundant inputs are in manual switchover mode. In this mode, CLKSEL pin is used to switch between the primary and secondary clock sources. The primary and secondary clock source setting is determined by the PRIMSRC bit. During the switchover, no glitches will occur at the output of the device, although there may be frequency and phase drift, depending on the exact phase and frequency relationship between the primary and secondary clocks.

OTP Interface

The 5P49V5923 can also store its configuration in an internal OTP. The contents of the device's internal programming registers can be saved to the OTP by setting burn_start (W114[3]) to high and can be loaded back to the internal programming registers by setting usr_rd_start(W114[0]) to high.

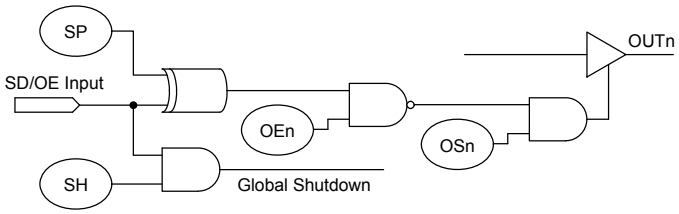
To initiate a save or restore using I^2C, only two bytes are transferred. The Device Address is issued with the read/write bit set to “0”, followed by the appropriate command code. The save or restore instruction executes after the STOP condition is issued by the Master, during which time the 5P49V5923 will not generate Acknowledge bits. The 5P49V5923 will acknowledge the instructions after it has completed execution of them. During that time, the I^2C bus should be interpreted as busy by all other users of the bus.

On power-up of the 5P49V5923, an automatic restore is performed to load the OTP contents into the internal programming registers. The 5P49V5923 will be ready to accept a programming instruction once it acknowledges its 7-bit I^2C address.

Availability of Primary and Secondary I^2C addresses to allow programming for multiple devices in a system. The I^2C slave address can be changed from the default 0xD4 to 0xD0 by programming the I2C_ADDR bit D0. *VersaClock 5 Programming Guide* provides detailed I^2C programming guidelines and register map.

SD/OE Pin Function

The polarity of the SD/OE signal pin can be programmed to be either active HIGH or LOW with the SP bit (W16[1]). When SP is “0” (default), the pin becomes active LOW and when SP is “1”, the pin becomes active HIGH. The SD/OE pin can be configured as either to shutdown the PLL or to enable/disable the outputs. The SH bit controls the configuration of the SD/OE pin The SH bit needs to be high for SD/OE pin to be configured as SD.



When configured as SD, device is shut down, and the single-ended LVCMOS outputs are driven low. When configured as OE, and outputs are disabled, the outputs are driven high/low.

Table 5: SD/OE Pin Function Truth Table

SH bit	SP bit	OSn bit	OEn bit	SD/OE	OUTn
0	0	0	x	x	Tri-state[2]
0	0	1	0	x	Output active
0	0	1	1	0	Output active
0	0	1	1	1	Output driven High Low
0	1	0	x	x	Tri-state[2]
0	1	1	0	x	Output active
0	1	1	1	0	Output driven High Low
0	1	1	1	1	Output active
1	0	0	x	0	Tri-state[2]
1	0	1	0	0	Output active
1	0	1	1	0	Output active
1	1	0	x	0	Tri-state[2]
1	1	1	0	0	Output active
1	1	1	1	0	Output driven High Low
1	x	x	x	1	Output driven High Low [1]

Note 1 : Global Shutdown
Note 2 : Tri-state regardless of OEn bits

Output Alignment

Each output divider block has a synchronizing POR pulse to provide startup alignment between outputs. This allows alignment of outputs for low skew performance. The phase alignment works both for integer output divider values and for fractional output divider values.

Besides the POR at power up, the same synchronization reset is also triggered when switching between configurations with the SEL0/1 pins. This ensures that the outputs remain aligned in every configuration. This reset causes the outputs to suspend for a few hundred microseconds so the switchover is not glitch-less. The reset can be disabled for applications where glitch-less switch over is required and alignment is not critical.

When using I^2C to reprogram an output divider during operation, alignment can be lost. Alignment can be restored by manually triggering the reset through I^2C.

When alignment is required for outputs with different frequencies, the outputs are actually aligned on the falling edges of each output by default. Rising edge alignment can also be achieved by utilizing the programmable skew feature to delay the faster clock by 180 degrees. The programmable skew feature also allows for fine tuning of the alignment.

For details of register programming, please see VersaClock 5 Family Register Descriptions and Programming Guide for details.

Output Divides

Each of the four output divides are comprised of a 12-bit integer counter, and a 24-bit fractional counter. The output divide can operate in integer divide only mode for improved performance, or utilize the fractional counters to generate any frequency with a synthesis accuracy better than 50ppb.

The Output Divide also has the capability to apply a spread modulation to the output frequency. Independent of output frequency, a triangle wave modulation between 30 and 63kHz may be generated.

Output Skew

For outputs that share a common output divide value, there will be the ability to skew outputs by quadrature values to minimize interaction on the PCB. The skew on each output can be adjusted from 0 to 360 degrees. Skew is adjusted in units equal to 1/32 of the VCO period. So, for 100 MHz output and a 2800 MHz VCO, you can select how many 11.161pS units you want added to your skew (resulting in units of 0.402 degrees). For example, 0, 0.402, 0.804, 1.206, 1.408, and so on. The granularity of the skew adjustment is always dependent on the VCO period and the output period.

Output Drivers

The operating voltage ranges of each output is determined by its independent output power pin (V_{DDO}) and thus each can have different output voltage levels. Output voltage levels of 1.8V, 2.5V, or 3.3V are supported for LVCMOS.

Each output may be enabled or disabled by register bits. When disabled an output will be in a logic 0 state as determined by the programming bit table shown on page 6.

LVCMOS Operation

Outputs OUT1 & OUT2 each operate the frequency as determined by corresponding programmed Fractional Output Dividers. All the previously described configuration and control apply equally to all outputs. Frequency, phase alignment, voltage levels and enable / disable status apply to all the OUTx pins. The outputs can be selected to be phase-aligned with each other or inverted relative to one another by register programming bits. Selection of phase-alignment may have negative effects on the phase noise performance of any part of the device due to increased simultaneous switching noise within the device.

Device Hardware Configuration

The 5P49V5923 supports an internal One-Time Programmable (OTP) memory that can be pre-programmed at the factory with up to 4 complete device configuration.

These configurations can be over-written using the serial interface once reset is complete. Any configuration written via the programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is desired.

Device Start-up & Reset Behavior

The 5P49V5923 has an internal power-up reset (POR) circuit. The POR circuit will remain active for a maximum of 10ms after device power-up.

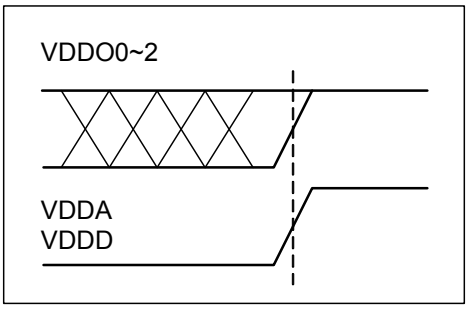
Upon internal POR circuit expiring, the device will exit reset and begin self-configuration.

The device will load internal registers according to Table 3.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock the PLL to the selected source and begin operation.

Power Up Ramp Sequence

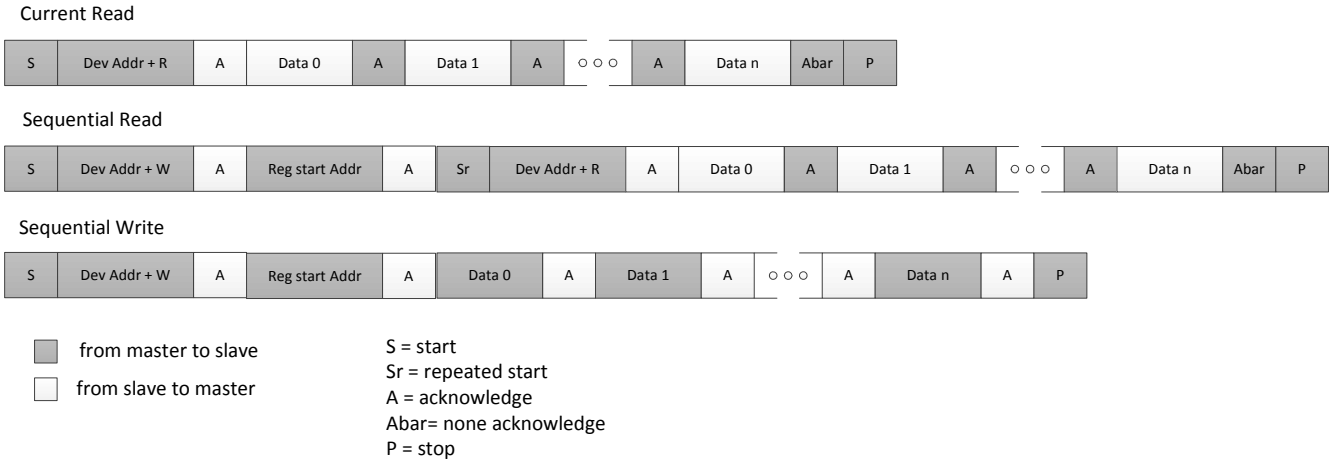
VDDA and VDDD must ramp up together. VDDO0~2 must ramp up before, or concurrently with, VDDA and VDDD. All power supply pins must be connected to a power rail even if the output is unused. All power supplies must ramp in a linear fashion and ramp monotonically.



I²C Mode Operation

The device acts as a slave device on the I²C bus using one of the two I²C addresses (0xD0 or 0xD4) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-down resistors have a size of 100kΩ typical.



I²C Slave Read and Write Cycle Sequencing

Table 6: I^2C Bus DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Level	For SEL1/SDA pin and SEL0/SCL pin.	$0.7xV_{DDD}$		5.5 [2]	V
V_{IL}	Input LOW Level	For SEL1/SDA pin and SEL0/SCL pin.	GND-0.3		$0.3xV_{DDD}$	V
V_{HYS}	Hysteresis of Inputs		$0.05xV_{DDD}$			V
I_{IN}	Input Leakage Current		-1		30	µA
V_{OL}	Output LOW Voltage	I_{OL} = 3 mA			0.4	V

Table 7: I^2C Bus AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Serial Clock Frequency (SCL)	10		400	kHz
t_{BUF}	Bus free time between STOP and START	1.3			µs
$t_{SU:START}$	Setup Time, START	0.6			µs
$t_{HD:START}$	Hold Time, START	0.6			µs
$t_{SU:DATA}$	Setup Time, data input (SDA)	0.1			µs
$t_{HD:DATA}$	Hold Time, data input (SDA) [1]	0			µs
t_{OVD}	Output data valid from clock			0.9	µs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, data and clock (SDA, SCL)	$20 + 0.1xC_B$		300	ns
t_F	Fall Time, data and clock (SDA, SCL)	$20 + 0.1xC_B$		300	ns
t_{HIGH}	HIGH Time, clock (SCL)	0.6			µs
t_{LOW}	LOW Time, clock (SCL)	1.3			µs
$t_{SU:STOP}$	Setup Time, STOP	0.6			µs

Note 1: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(MIN) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 2: I^2C inputs are 5V tolerant.

Table 8: Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5P49V5923. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, V_{DDA}, V_{DDD}, V_{DDO}	3.465V
Inputs XIN/REF CLKIN, CLKINB Other inputs	 0V to 1.2V voltage swing 0V to 1.2V voltage swing single-ended -0.5V to V_{DDD}
Outputs, V_{DDO} (LVCMOS)	-0.5V to V_{DDO}+ 0.5V
Outputs, I_O (SDA)	10mA
Package Thermal Impedance, θ_{JA}	42°C/W (0 mps)
Package Thermal Impedance, θ_{JC}	41.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	2000V
Junction Temperature	125°C

Table 9: Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDOX}	Power supply voltage for supporting 1.8V outputs	1.71	1.8	1.89	V
V_{DDOX}	Power supply voltage for supporting 2.5V outputs	2.375	2.5	2.625	V
V_{DDOX}	Power supply voltage for supporting 3.3V outputs	3.135	3.3	3.465	V
V_{DDD}	Power supply voltage for core logic functions	1.71		3.465	V
V_{DDA}	Analog power supply voltage. Use filtered analog power supply.	1.71		3.465	V
T_A	Operating temperature, ambient	-40		+85	°C
C_{LOAD_OUT}	Maximum load capacitance (3.3V LVCMOS only)			15	pF
F_{IN}	External reference crystal	1		40	MHz
	External reference clock CLKIN, CLKINB	1		200	
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05		5	ms

Note: $V_{DDO}1$ and $V_{DDO}2$ must be powered on either before or simultaneously with V_{DDD}, V_{DDA} and $V_{DDO}0$.

Table 10:Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance (T_A = +25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Input Capacitance (CLKIN, CLKINB, CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL)		3	7	pF
Pull-down Resistor	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL, CLKIN, CLKINB, OUT0_SEL_I2CB	100		300	kΩ
R_{OUT}	LVCMOS Output Driver Impedance (V_{DDO} = 1.8V, 2.5V, 3.3V)		17		Ω
XIN/REF	Programmable input capacitance at XIN/REF	0		8	pF
XOUT	Programmable input capacitance at XOUT	0		8	pF

Table 11:Crystal Characteristics

Parameter	Test Conditions	Min	Typ	Max	Units
Mode of Oscillation		Fundamental			
Frequency		8	25	40	MHz
Equivalent Series Resistance (ESR)			10	100	Ω
Shunt Capacitance				7	pF
Load Capacitance (C_L) @ <=25MHz		6	8	12	pF
Load Capacitance (C_L) > 25M to 40M		6		8	pF
Maximum Crystal Drive Level				100	µW

Note: Typical crystal used is FOX 603-25-150. For different reference crystal options please go to www.foxonline.com.

Table 12:DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Iddcore[3]	Core Supply Current	100 MHz on all outputs, 25 MHz REFCLK		30	34	mA
Iddox	Output Buffer Supply Current	LVCMOS, 50 MHz, 3.3V V_{DDOX}, [1,2]		16	18	mA
		LVCMOS, 50 MHz, 2.5V V_{DDOX}, [1,2]		14	16	mA
		LVCMOS, 50 MHz, 1.8V V_{DDOX}, [1,2]		12	14	mA
		LVCMOS, 200 MHz, 3.3V V_{DDOX}, [1,2]		36	42	mA
		LVCMOS, 200 MHz, 2.5V V_{DDOX}, [1,2]		27	32	mA
		LVCMOS, 200 MHz, 1.8V V_{DDOX}, [1,2]		16	19	mA
Iddpd	Core Power Down Current	SD asserted, I^2C Programming		10	14	mA

1.Single CMOS driver active.
2.Measured into a 5” 50 Ohm trace with 2 pF load.
3. Iddcore = IddA + IddD, no loads.

Table 13:Electrical Characteristics – Differential Clock Input Parameters [1,2] (Supply Voltage V_{DDA}, V_{DDD}, $V_{DDO}0$ = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage–CLKIN, CLKINB	Single-ended input	0.55		1.7	V
V_{IL}	Input LOW Voltage–CLKIN, CLKINB	Single-ended input	GND - 0.3		0.4	V
V_{SWING}	Input Amplitude - CLKIN, CLKINB	Peak to Peak value, single-ended	200		1200	mV
dv/dt	Input Slew Rate - CLKIN, CLKINB	Measured differentially	0.4		8	V/ns
I_{IL}	Input Leakage Low Current	V_{IN} = GND	-5		5	µA
I_{IH}	Input Leakage High Current	V_{IN} = 1.7V			20	µA
d_{TIN}	Input Duty Cycle	Measurement from differential waveform	45		55	%

1. Guaranteed by design and characterization, not 100% tested in production.
2. Slew rate measured through ±75mV window centered around differential zero.

Table 14:DC Electrical Characteristics for 3.3V LVCMOS (V_{DDO} = 3.3V±5%, TA = -40°C to +85°C) [1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -15mA	2.4		V_{DDO}	V
V_{OL}	Output LOW Voltage	I_{OL} = 15mA			0.4	V
I_{OZDD}	Output Leakage Current (OUT1~2)	Tri-state outputs, V_{DDO} = 3.465V			5	µA
I_{OZDD}	Output Leakage Current (OUT0)	Tri-state outputs, V_{DDO} = 3.465V			30	µA
V_{IH}	Input HIGH Voltage	Single-ended inputs - CLKSEL, SD/OE	0.7xVDDD		V_{DDD} + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended inputs, CLKSEL, SD/OE	GND - 0.3		0.3xVDDD	V
V_{IH}	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	2		$V_{DDO}0$ + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
V_{IH}	Input HIGH Voltage	Single-ended input - XIN/REF	0.8		1.2	V
V_{IL}	Input LOW Voltage	Single-ended input - XIN/REF	GND - 0.3		0.4	V
T_R/T_F	Input Rise/Fall Time	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL			300	ns

1. See “Recommended Operating Conditions” table.

Table 15:DC Electrical Characteristics for 2.5V LVCMOS (V_{DDO} = 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -12mA	0.7xV_{DDO}			V
V_{OL}	Output LOW Voltage	I_{OL} = 12mA			0.4	V
I_{OZDD}	Output Leakage Current (OUT1~2)	Tri-state outputs, V_{DDO} = 3.465V			5	µA
I_{OZDD}	Output Leakage Current (OUT0)	Tri-state outputs, V_{DDO} = 3.465V			30	µA
V_{IH}	Input HIGH Voltage	Single-ended inputs - CLKSEL, SD/OE	0.7xVDDD		V_{DDD} + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended inputs, CLKSEL, SD/OE	GND - 0.3		0.3xVDDD	V
V_{IH}	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	1.7		V_{DDO}0 + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
V_{IH}	Input HIGH Voltage	Single-ended input - XIN/REF	0.8		1.2	V
V_{IL}	Input LOW Voltage	Single-ended input - XIN/REF	GND - 0.3		0.4	V
TR/TF	Input Rise/Fall Time	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL			300	ns

Table 16:DC Electrical Characteristics for 1.8V LVCMOS (V_{DDO} = 1.8V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	IOH = -8mA	0.7 xV_{DDO}		V_{DDO}	V
V_{OL}	Output LOW Voltage	IOL = 8mA			0.25 x V_{DDO}	V
I_{OZDD}	Output Leakage Current (OUT1~2)	Tri-state outputs, V_{DDO} = 3.465V			5	µA
I_{OZDD}	Output Leakage Current (OUT0)	Tri-state outputs, V_{DDO} = 3.465V			30	µA
V_{IH}	Input HIGH Voltage	Single-ended inputs - CLKSEL, SD/O	0.7 * V_{DDD}		V_{DDD} + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended inputs, CLKSEL, SD/OL	GND - 0.3		0.3 * V_{DDD}	V
V_{IH}	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	0.65 * V_{DDO}0		V_{DDO}0 + 0.3	V
V_{IL}	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
V_{IH}	Input HIGH Voltage	Single-ended input - XIN/REF	0.8		1.2	V
V_{IL}	Input LOW Voltage	Single-ended input - XIN/REF	GND - 0.3		0.4	V
TR/TF	Input Rise/Fall Time	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL			300	ns

Table 17:AC Timing Electrical Characteristics

(V_{DDO} = 3.3V+5% or 2.5V+5% or 1.8V ±5%, TA = -40°C to +85°C)

(Spread Spectrum Generation = OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{IN} [1]	Input Frequency	Input frequency limit (XIN)	8		40	MHz
		Input frequency limit (REF)	1		200	MHz
		Input frequency limit (CLKIN, CLKINB)	1		200	MHz
f_{OUT}	Output Frequency	Single ended clock output limit (LVCMOS)	1		200	MHz
f_{VCO}	VCO Frequency	VCO operating frequency range	2600		2900	MHz
f_{PFD}	PFD Frequency	PFD operating frequency range	1[1]		150	MHz
f_{BW}	Loop Bandwidth	Input frequency = 25MHz	0.06		0.9	MHz
t2	Input Duty Cycle	Duty Cycle	45	50	55	%
t3 [5]	Output Duty Cycle	Measured at VDD/2, all outputs except Reference output OUT0, VDDOX= 2.5V or 3.3V	45	50	55	%
		Measured at VDD/2, all outputs except Reference output OUT0, VDDOX=1.8V	40	50	60	%
		Measured at VDD/2, Reference output OUT0 (5MHz - 120MHz) with 50% duty cycle input	40	50	60	%
		Measured at VDD/2, Reference output OUT0 (150.1MHz - 200MHz) with 50% duty cycle input	30	50	70	%
t4 [2]	Slew Rate, SLEW[1:0] = 00	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (Output Load = 5 pF) VDDOX=3.3V	1.0	2.2		V/ns
	Slew Rate, SLEW[1:0] = 01		1.2	2.3		V/ns
	Slew Rate, SLEW[1:0] = 10		1.3	2.4		V/ns
	Slew Rate, SLEW[1:0] = 11		1.7	2.7		V/ns
	Slew Rate, SLEW[1:0] = 00	Single-ended 2.5V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (Output Load = 5 pF) VDDOX=2.5V	0.6	0.3		V/ns
	Slew Rate, SLEW[1:0] = 01		0.7	1.4		V/ns
	Slew Rate, SLEW[1:0] = 10		0.6	1.4		V/ns
	Slew Rate, SLEW[1:0] = 11		1.0	1.7		V/ns
	Slew Rate, SLEW[1:0] = 00	Single-ended 1.8V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (Output Load = 5 pF) VDDOX=1.8V	0.3	0.7		V/ns
	Slew Rate, SLEW[1:0] = 01		0.4	0.8		V/ns
	Slew Rate, SLEW[1:0] = 10		0.4	0.9		V/ns
	Slew Rate, SLEW[1:0] = 11		0.7	1.2		V/ns

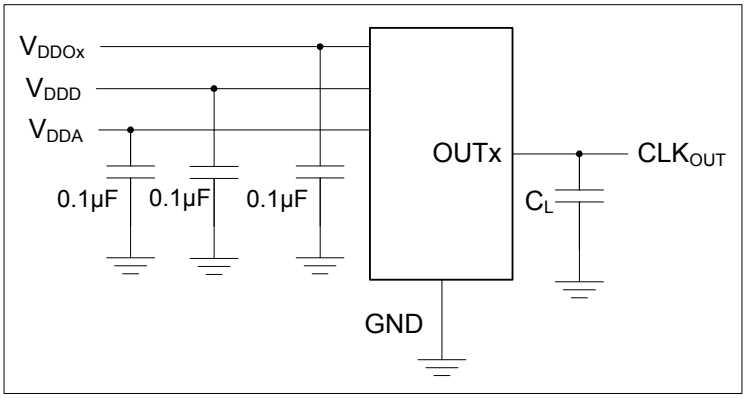
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t6	Clock Jitter	Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, LVCMOS outputs (1.8 to 3.3V nominal output voltage) OUT0=25MHz OUT1=100MHz OUT2=125MHz		74		ps
		RMS Phase Jitter (12kHz to 5MHz integration range) reference clock (OUT0), 25 MHz LVCMOS outputs (1.8 to 3.3V nominal output voltage). OUT0=25MHz OUT1=100MHz OUT2=125MHz		0.5		ps
		RMS Phase Jitter (12kHz to 20MHz integration range) LVCMOS output, VDDO = 3.465V, 25MHz crystal, 125MHz output frequency OUT0=25MHz OUT1=100MHz OUT2=125MHz		0.75	1.5	ps
t7	Output Skew	Skew between the same frequencies, with outputs using the same driver format and phase delay set to 0ns.		75		ps
t8 [3]	Startup Time	PLL lock time from power-up, measured after all VDD's have raised above 90% of their target value.			10	ms
t9 [4]	Startup Time	PLL lock time from shutdown mode		3	4	ms

1. Practical lower frequency is determined by loop filter settings.
2. A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.
3. Includes loading the configuration bits from memory to PLL registers. It does not include memory programming/write time.
4. Actual PLL lock time depends on the loop configuration.
5. Duty Cycle is only guaranteed at max slew rate settings.

Table 18:Spread Spectrum Generation Specifications

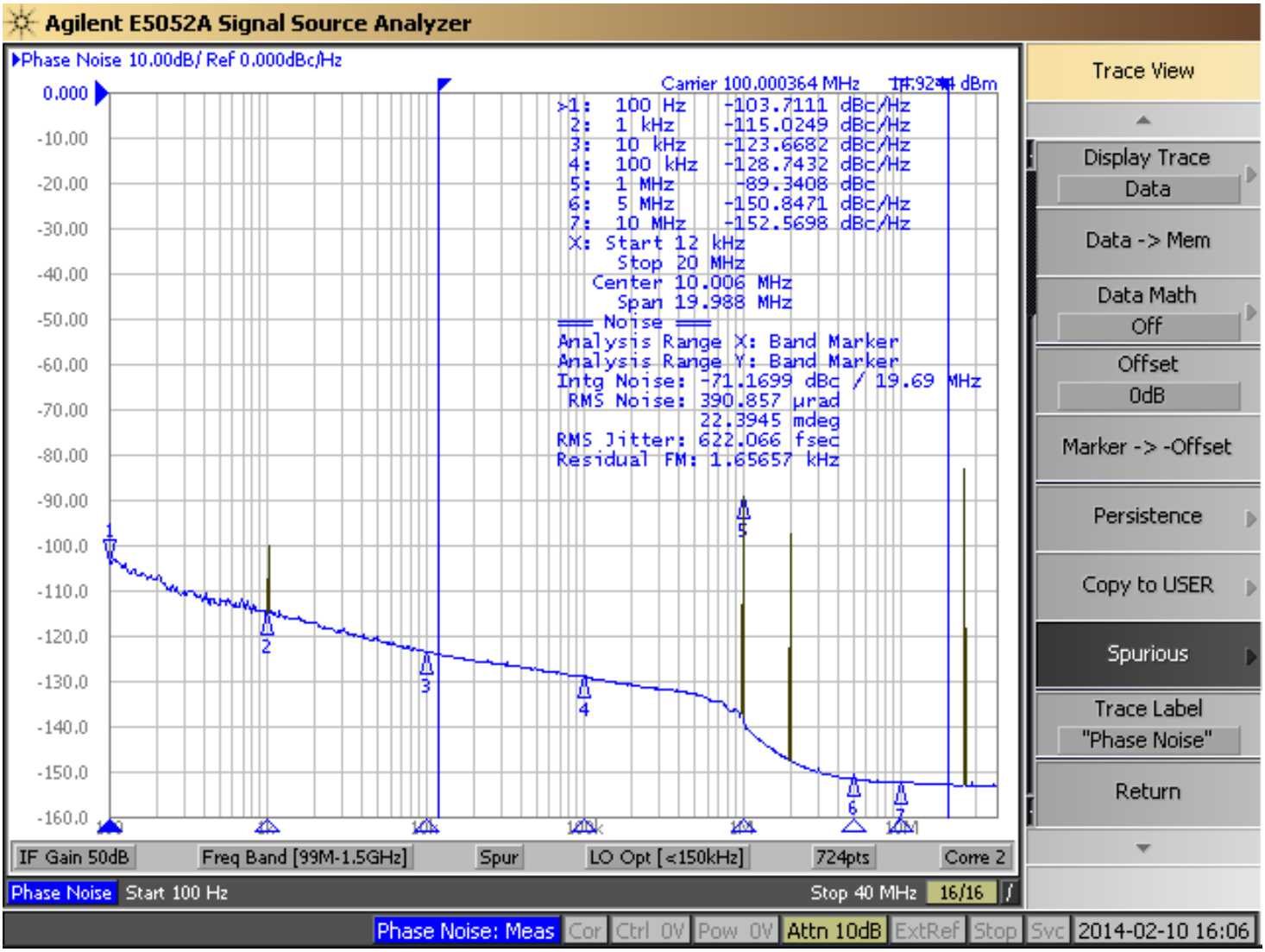
Symbol	Parameter	Description	Min	Typ	Max	Unit
f_{OUT}	Output Frequency	Output Frequency Range	5		300	MHz
f_{MOD}	Mod Frequency	Modulation Frequency	30 to 63			kHz
f_{SPREAD}	Spread Value	Amount of Spread Value (programmable) - Center Spread	±0.25% to ±2.5%			$\%f_{OUT}$
		Amount of Spread Value (programmable) - Down Spread	-0.5% to -5%			

Test Circuits and Loads

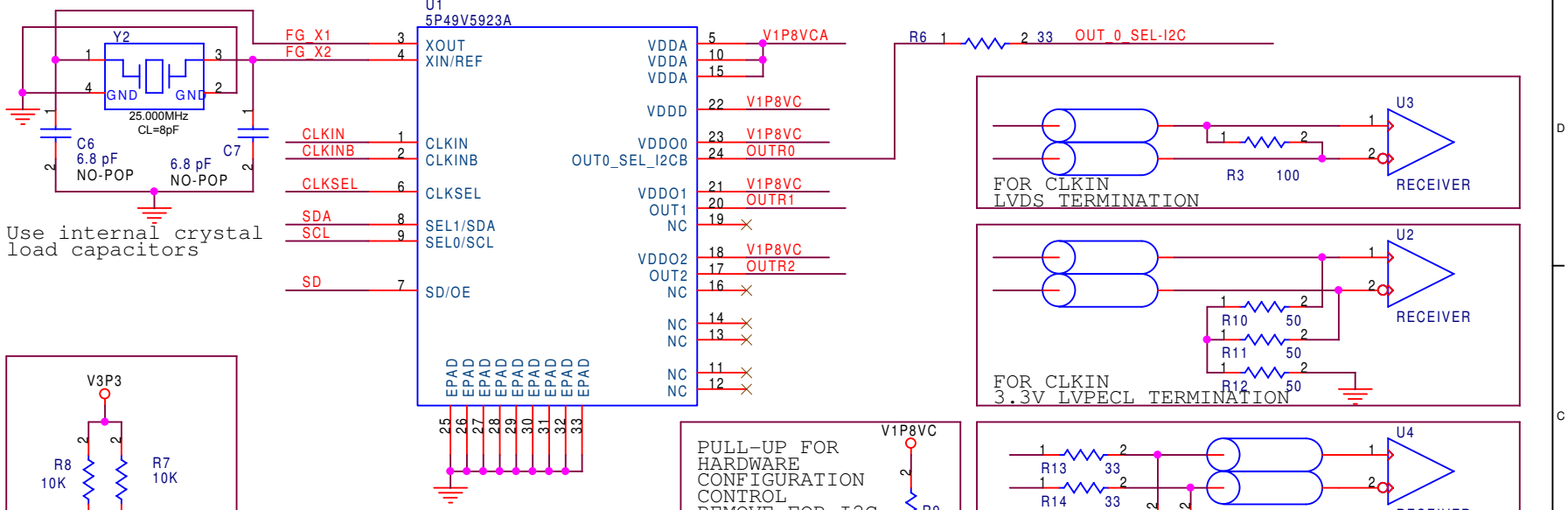


Test Circuits and Loads for Outputs

Typical Phase Noise at 100MHz (3.3V, 25°C)



NOTE: All outputs operational at 100MHz, Phase Noise Plot with Spurs On.



Layout notes.
1. Separate Xout and Xin traces by 3 x the trace width.
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4. Do not share ground vias. One ground pin one ground via.

NOTE:FERRITE BEAD FB1 =

Manufacture	Part Number	Z@100MHz	PkgSz	DC res.	Current(Ma)
Fair-Rite	2504021217Y0	120	0402	0.5	200
muRata	BLM15AG221SN1	220	0402	0.35	300
muRata	BLM15BB121SN1	120	0402	0.35	300
TDK	MMZ1005S241A	240	0402	0.18	200
TECSTAR	TB4532153121	120	0402	0.3	300

Revision history
0.1 9/19/2014 first publication

Integrated Device Technology
San Jose, CA

Size	Document Number	Rev
A	5P49V5923A_SCH	0.1

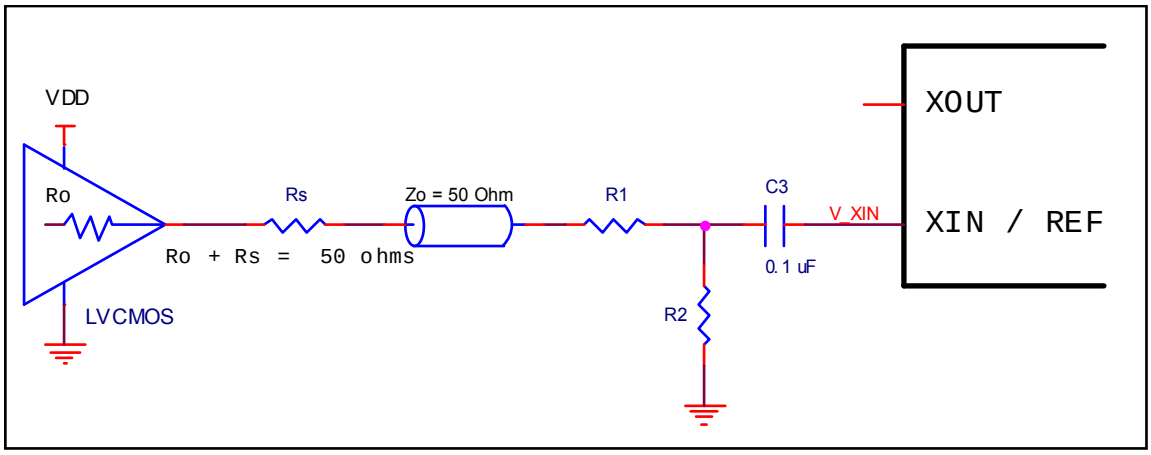
Date: Friday, September 19, 2014 Sheet 1 of 1

Overdriving the XIN/REF Interface

LVCMOS Driver

The XIN/REF input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.2V and the slew rate should not be less than 0.2V/ns. Figure General Diagram for LVCMOS Driver to XTAL Input Interface shows an example of the interface diagram for a LVCMOS driver.

This configuration has three properties; the total output impedance of Ro and Rs matches the 50 ohm transmission line impedance, the Vrx voltage is generated at the CLKIN inputs which maintains the LVCMOS driver voltage level across the transmission line for best S/N and the R1-R2 voltage divider values ensure that the clock level at XIN is less than the maximum value of 1.2V.



General Diagram for LVCMOS Driver to XTAL Input Interface

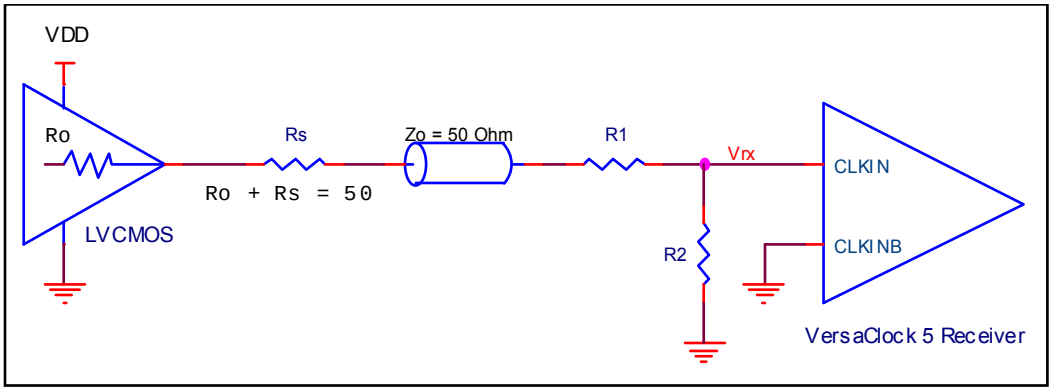
Table 19 *Nominal Voltage Divider Values vs LVCMOS VDD for XIN* shows resistor values that ensure the maximum drive level for the XIN/REF port is not exceeded for all combinations of 5% tolerance on the driver VDD, the VersaClock VDDA and 5% resistor tolerances. The values of the resistors can be adjusted to reduce the loading for slower and weaker LVCMOS driver by increasing the voltage divider attenuation as long as the minimum drive level is maintained over all tolerances. To assist this assessment, the total load on the driver is included in the table.

Table 19: Nominal Voltage Divider Values vs LVCMOS VDD for XIN

LVCMOS Driver VDD	Ro+Rs	R1	R2	V_XIN (peak)	Ro+Rs+R1+R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

Wiring the Differential Input to Accept Single-Ended Levels

Figure *Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels* shows how a differential input can be wired to accept single ended levels. This configuration has three properties; the total output impedance of Ro and Rs matches the 50 ohm transmission line impedance, the Vrx voltage is generated at the CLKIN inputs which maintains the LVCMOS driver voltage level across the transmission line for best S/N and the R1-R2 voltage divider values ensure that Vrx p-p at CLKIN is less than the maximum value of 1.2V.



Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

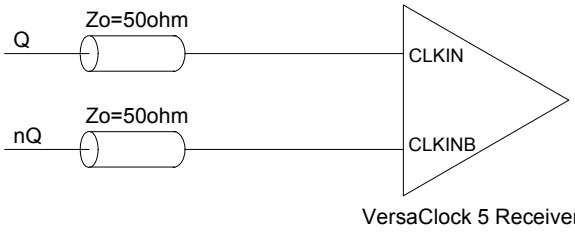
Table 20 *Nominal Voltage Divider Values vs Driver VDD* shows resistor values that ensure the maximum drive level for the CLKIN port is not exceeded for all combinations of 5% tolerance on the driver VDD, the VersaClock Vddo_0 and 5% resistor tolerances. The values of the resistors can be adjusted to reduce the loading for slower and weaker LVCMOS driver by increasing the impedance of the R1-R2 divider. To assist this assessment, the total load on the driver is included in the table.

Table 20: Nominal Voltage Divider Values vs Driver VDD

LVCMOS Driver VDD	Ro+Rs	R1	R2	Vrx (peak)	Ro+Rs+R1+R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

HCSL Differential Clock Input Interface

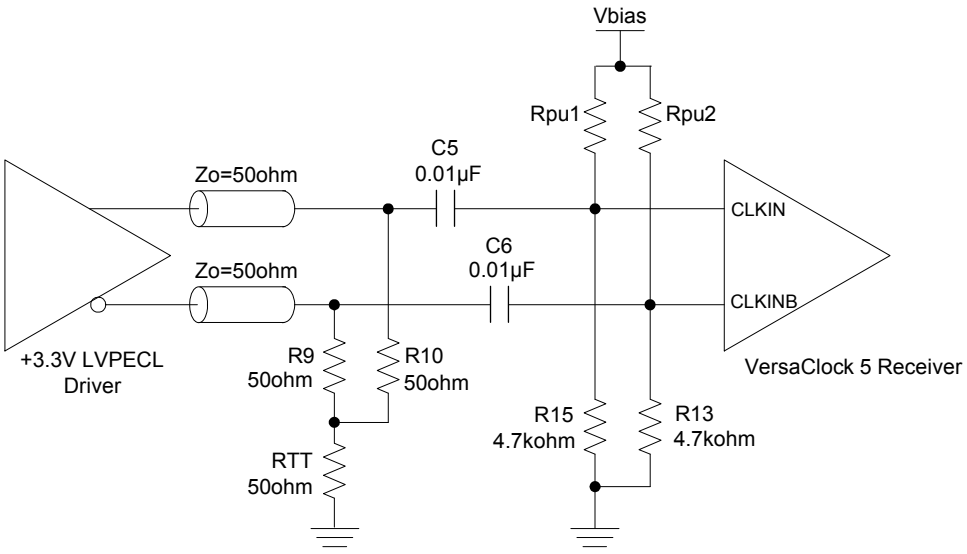
CLKIN/CLKINB will accept DC coupled HCSL signals.



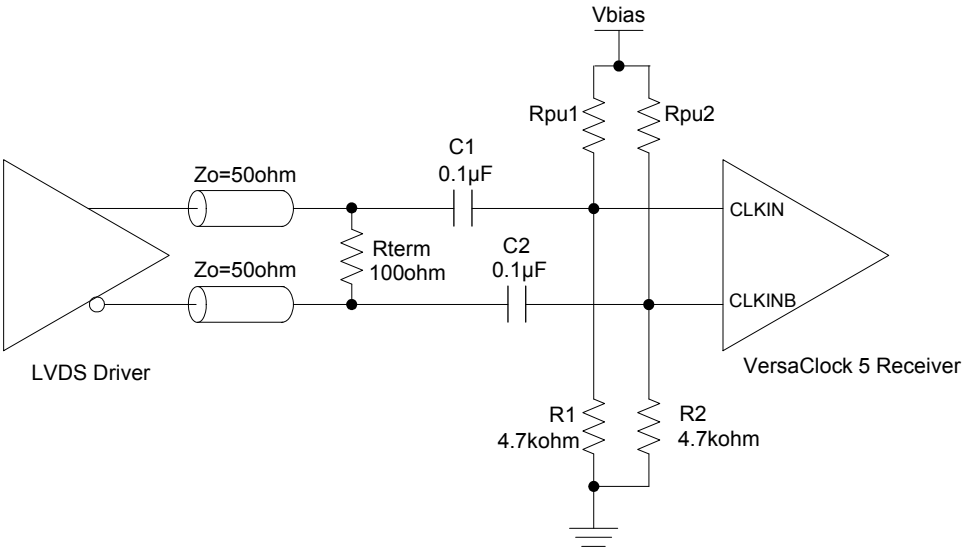
CLKIN, CLKINB Input Driven by an HCSL Driver

3.3V Differential LVPECL Clock Input Interface

The logic levels of 3.3V LVPECL and LVDS can exceed VIH max for the CLKIN/B pins. Therefore the LVPECL levels must be AC coupled to the VersaClock differential input and the DC bias restored with external voltage dividers. A single table of bias resistor values is provided below for both for 3.3V LVPECL and LVDS. Vbias can be VDDD, V_{DDOX} or any other available voltage at the VersaClock receiver that is most conveniently accessible in layout.



CLKIN, CLKINB Input Driven by a 3.3V LVPECL Driver



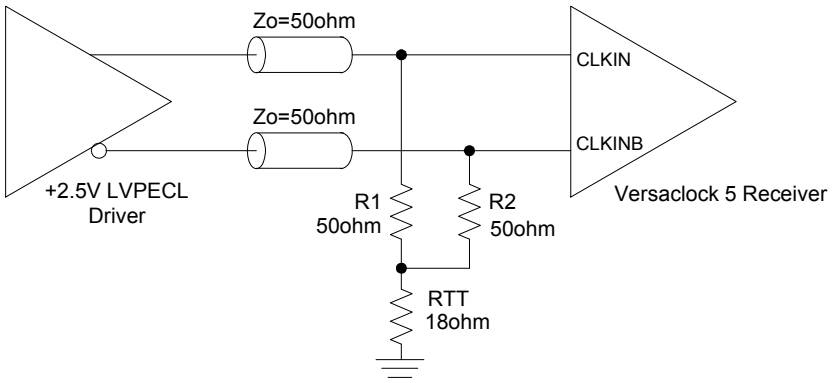
CLKIN, CLKINB Input Driven by an LVDS Driver

Table 21: Bias Resistors for 3.3V LVPECL and LVDS Drive to CLKIN/B

Vbias (V)	Rpu1/2 (kohm)	CLKIN/B Bias Voltage (V)
3.3	22	0.58
2.5	15	0.60
1.8	10	0.58

2.5V Differential LVPECL Clock Input Interface

The maximum DC 2.5V LVPECL voltage meets the VIH max CLKIN requirement. Therefore, 2.5V LVPECL can be connected directly to the CLKIN terminals without AC coupling



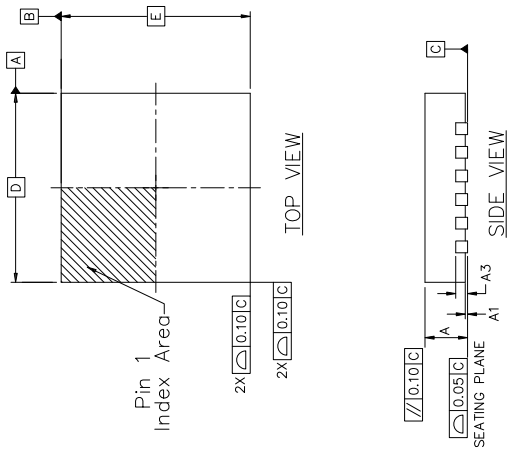
CLKIN, CLKINB Input Driven by a 2.5V LVPECL Driver

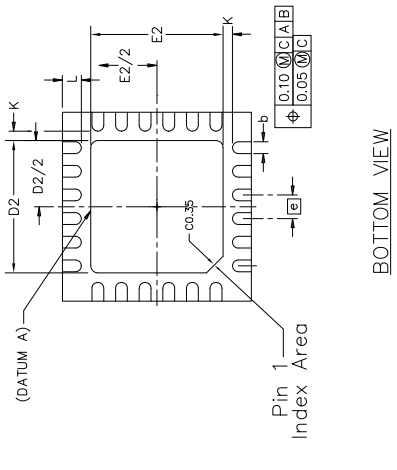
Package Outline and Dimensions (24-pin 4 x 4 mm VFQFPN)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/17/15	J.H
01	ADD CHAMFER	10/12/16	J.H

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20	
D		4.00 BSC	
E		4.00 BSC	
D2	2.70	2.80	2.90
E2	2.70	2.80	2.90
e		0.50 BSC	
L	0.30	0.40	0.50
b	0.18	0.25	0.30

NOTES :
1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.





TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
XX±	±
XXX±	
XXXX±	

APPROVALS	DATE
DRAWN GAC	11/17/15
CHECKED	

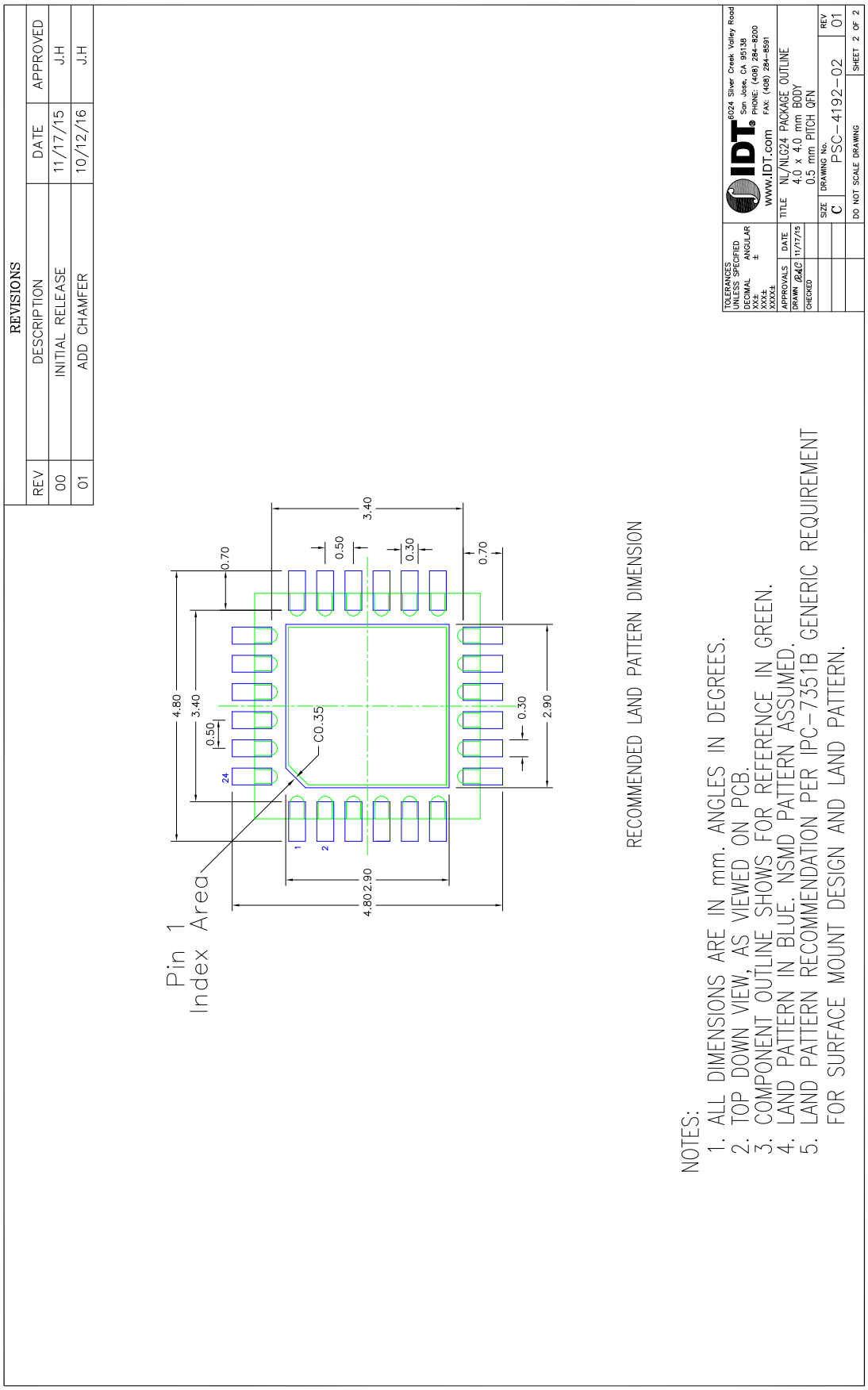
IDT® 6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 www.IDT.com FAX: (408) 284-8591

TITLE NL/NLG24 PACKAGE OUTLINE 4.0 x 4.0 mm BODY 0.5 mm PITCH QFN

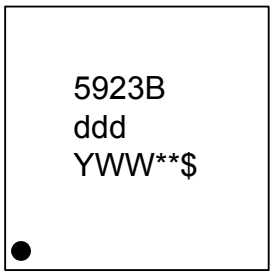
SIZE	DRAWING No.	REV
C	PSC-4192-02	01

DO NOT SCALE DRAWING SHEET 1 OF 2

Package Outline and Dimensions, cont. (24-pin 4 x 4 mm VFQFPN)



Marking Diagram



1. Line 1 is the truncated part number.
2. “ddd” denotes dash code.
3. “YWW” is the last digit of the year and week that the part was assembled.
4. “**” denotes lot number.
5. “$” denotes mark code.

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
5P49V5923BdddNLGI	Tubes	24-pin VFQFPN	-40° to +85°C
5P49V5923BdddNLGI8	Tape and Reel	24-pin VFQFPN	-40° to +85°C

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Date	Description of Change
March 3, 2017	Updated POD drawings and legal disclaimer.
February 24, 2017	1. Added “Output Alignment” section. 2. Update “Output Divides” section.



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

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