MB91F465KA
MB91F465KB

FR60, MB91460K Series, 32-bit Microcontroller Datasheet

MB91460K series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family of CPUs.

This series contains the LIN-USART and CAN controllers.

Features

FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
  Signed 32-bit multiplication: 5 cycles
  Signed 16-bit multiplication: 3 cycles
- Interrupts (save PC/PS): 6 cycles (16 priority levels)
- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

Internal peripheral resources

- General-purpose ports: Maximum 73 ports
- DMAC (DMA Controller)
- Maximum of 5 channels able to operate simultaneously.
- 2 transfer sources (internal peripheral/software)
- Activation source can be selected using software.
- Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
- Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
- Transfer data size selectable from 8/16/32-bit
- Multi-byte transfer enabled (by software)
- DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
- A/D converter (successive approximation type)
- 10-bit resolution: 26 channels
- Conversion time: minimum 1 μs
- External interrupt inputs: 10 channels
- Shares the CAN RX pin and the I^2C SDA pin
- Bit search module (for REALOS)
- Function to search from the MSB (most significant bit) for the position of the first “0”, “1”, or changed bit in a word
- LIN-USART (full duplex double buffer): 5 channels
- Clock synchronous/asynchronous selectable
- Sync-break detection
- Internal dedicated baud rate generator
- I^2C bus interface (supports 400 kbps): 1 channel
- Master/slave transmission and reception
- Arbitration function, clock synchronisation function
- CAN controller (C-CAN): 1 channel
- Maximum transfer speed: 1 Mbps
- 32 transmission/reception message buffers
- 16-bit PPG timer: 12 channels
- 16-bit reload timer: 8 channels
- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
- Input capture: 8 channels (operates in conjunction with the free-run timer)
- Output compare: 8 channels (operates in conjunction with the free-run timer)
- Watchdog timer
- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Supply Supervisor: Low voltage detection circuit for external $V_{DD}5$ and internal 1.8V core voltage
- Clock supervisor
  Monitors the sub-clock (32 kHz) and the main clock (4 MHz) ,

and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.

- Clock modulator
- Clock monitor
- Sub-clock calibration
  Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
- Main oscillator stabilisation timer
  Generates an interrupt in sub-clock mode after the stabilisation wait time has elapsed on the 23-bit stabilisation wait time counter
- Sub-oscillator stabilisation timer
  Generates an interrupt in main clock mode after the stabilisation wait time has elapsed on the 15-bit stabilisation wait time counter

Package and technology

- Package: 120-pin plastic LQFP (LQFP-120)
- CMOS 0.18 μm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between − 40°C and + 105°C

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1. Product Lineup

Feature	MB91V460A (Evaluation device)	MB91F465KA MB91F465KB
Max. core frequency (CLKB)	80MHz	80MHz
Max. resource frequency (CLKP)	40MHz	40MHz
Max. external bus freq. (CLKT)	40MHz	40MHz
Max. CAN frequency (CLKCAN)	20MHz	40MHz
Technology	0.35 μm	0.18 μm
Watchdog timer	yes	yes
Watchdog timer (RC osc. based)	yes (disengageable)	yes
Bit Search	yes	yes
Reset input (INITX)	yes	yes
Hardware Standby input (HSTX)	yes	-
Clock Modulator	yes	yes
Low Power Mode	yes	yes
DMA	5 ch	5 ch
MMU/MPU	MPU (16 ch) [1]	MPU (2 ch) [1]
Flash memory	Emulation SRAM 32bit read data	544 KByte
Satellite Flash memory	n.a.	-
Flash Protection	n.a.	yes
D-RAM	64 KByte	8 KByte
ID-RAM	64 KByte	8 KByte
Flash-cache (F-cache)	16 KByte	4 KByte
Boot-ROM / BI-ROM	4 KByte fixed	4 KByte
RTC	1 ch	1 ch
Free Running Timer	8 ch	8 ch
ICU	8 ch	8 ch
OCU	8 ch	8 ch
Reload Timer	8 ch	8 ch
PPG 16-bit	16 ch	12 ch
PFM 16-bit	1 ch	-
Sound Generator	1 ch	-
Up/Down Counter (8/16-bit)	4 ch (8-bit) / 2 ch (16-bit)	-
C_CAN	6 ch (128msg)	1 ch (32msg)
LIN-USART	4 ch + 4 ch FIFO + 8 ch	4 ch + 1 ch FIFO
I2C (400k)	4 ch	1 ch

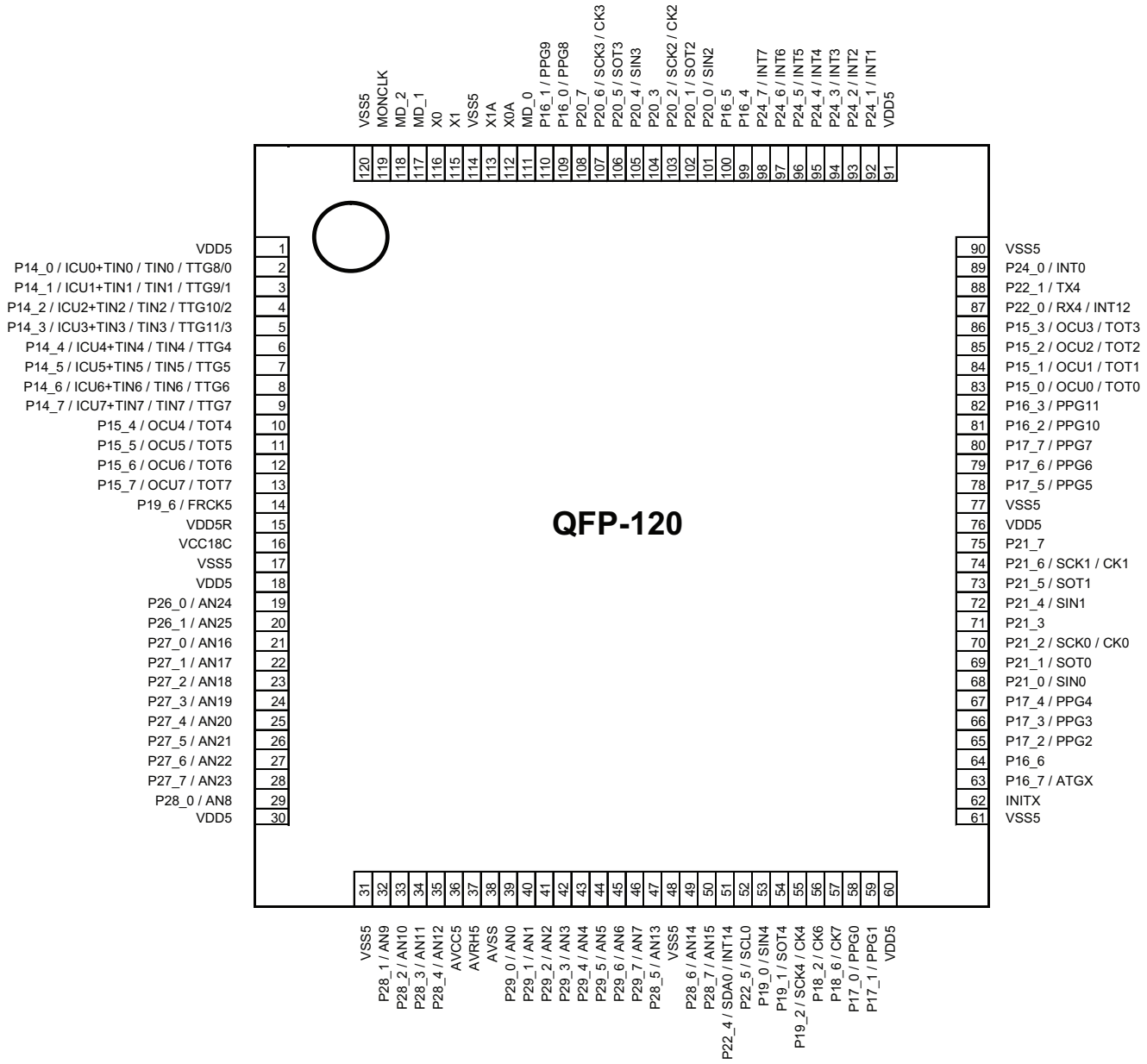
Feature	MB91V460A (Evaluation device)	MB91F465KA MB91F465KB
FR external bus	yes (32bit addr, 32bit data)	-
External Interrupts	16 ch	10 ch
NMI Interrupts	1 ch	-
SMC	6 ch	-
LCD controller (40x4)	1 ch	-
ADC (10 bit)	32 ch	26 ch
Alarm Comparator	2 ch	-
Supply Supervisor (low voltage detection)	yes	yes
Clock Supervisor	yes	yes
Main clock oscillator	4MHz	4MHz
Sub clock oscillator	32kHz	32kHz
RC Oscillator	100kHz	100kHz / 2MHz
PLL	x 20	x 20
DSU4	yes	-
EDSU	yes (32 BP) [1]	yes (4 BP) [1]
Supply Voltage	3V / 5V	3V / 5V
Regulator	yes	yes
Power Consumption	n.a.	< 900 mW
Temperature Range (T_A)	0..70 °C	-40..105°C
Package	BGA660	LQFP120
Power on to PLL run	< 20 ms	< 20 ms
Flash Download Time	n.a.	< 5 sec typical

1. MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

2. Pin Assignment

2.1 MB91F465Kx

(TOP VIEW)



FPT-120P-M21

3. Pin Description

3.1 MB91F465Kx

Pin no.	Pin name	I/O	I/O circuit type[1]	Description
2 to 9	P14_0 to P14_7	I/O	A	General-purpose input/output ports
	ICU0 to ICU7			Input capture input pins
	TIN0 to TIN7			External trigger input pins for reload timer
	TTG0/8 to TTG3/11, TTG4 to TTG7			External trigger input pins for PPG timer
10 to 13	P15_4 to P15_7	I/O	A	General-purpose input/output ports
	OCU4 to OCU7			Output compare output pins
	TOT4 to TOT7			Reload timer output pins
14	P19_6	I/O	A	General-purpose input/output port
	CK5			External clock input pin for free-run timer 5
19, 20	P26_0, P26_1	I/O	B	General-purpose input/output ports
	AN24, AN25			Analog input pins for A/D converter
21 to 28	P27_0 to P27_7	I/O	B	General-purpose input/output ports
	AN16 to AN23			Analog input pins for A/D converter
29, 32 to 35	P28_0 to P28_4	I/O	B	General-purpose input/output ports
	AN8 to AN12			Analog input pins for A/D converter
39 to 46	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins for A/D converter
47, 49, 50	P28_5 to P28_7	I/O	B	General-purpose input/output ports
	AN13 to AN15			Analog input pins for A/D converter
51	P22_4	I/O	C	General-purpose input/output port
	SDA0			I^2C bus data input/output pin
	INT14			External interrupt input pin
52	P22_5	I/O	C	General-purpose input/output port
	SCL0			I^2C bus CLK input/output pin
53	P19_0	I/O	A	General-purpose input/output port
	SIN4			Data input pin for USART4
54	P19_1	I/O	A	General-purpose input/output port
	SOT4			Data output pin for USART4
55	P19_2	I/O	A	General-purpose input/output port
	SCK4			Clock input/output pin for USART4
	CK4			External clock input pin for free-run timer 4
56, 57	P18_2, P18_6	I/O	A	General-purpose input/output port
	CK6, CK7			External clock input pin for free-run timers 6,7

Pin no.	Pin name	I/O	I/O circuit type[1]	Description
58, 59	P17_0, P17_1	I/O	A	General-purpose input/output ports
	PPG0, PPG1			PPG timer output pins
62	INITX	I	H	External reset input pin
63	P16_7	I/O	A	General-purpose input/output port
	ATGX			A/D converter external trigger input pin
64	P16_6	I/O	A	General-purpose input/output port
65 to 67	P17_2 to P17_4	I/O	A	General-purpose input/output ports
	PPG2 to PPG4			PPG timer output pins
68	P21_0	I/O	A	General-purpose input/output port
	SIN0			Data input pin for USART0
69	P21_1	I/O	A	General-purpose input/output port
	SOT0			Data output pin for USART0
70	P21_2	I/O	A	General-purpose input/output port
	SCK0			Clock input/output pin for USART0
	CK0			External clock input pin for free-run timer 0
71	P21_3	I/O	A	General-purpose input/output port
72	P21_4	I/O	A	General-purpose input/output port
	SIN1			Data input pin for USART1
73	P21_5	I/O	A	General-purpose input/output port
	SOT1			Data output pin for USART1
74	P21_6	I/O	A	General-purpose input/output port
	SCK1			Clock input/output pin for USART1
	CK1			External clock input pin for free-run timer 1
75	P21_7	I/O	A	General-purpose input/output port
78 to 80	P17_5 to P17_7	I/O	A	General-purpose input/output ports
	PPG5 to PPG7			PPG timer output pins
81, 82	P16_2, P16_3	I/O	A	General-purpose input/output ports
	PPG10, PPG11			PPG timer output pins
83 to 86	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
87	P22_0	I/O	A	General-purpose input/output port
	RX4			RX input pin for CAN4
	INT12			External interrupt input pin
88	P22_1	I/O	A	General-purpose input/output port
	TX4			TX output pin for CAN4
89, 92 to 98	P24_0 to P24_7	I/O	A	General-purpose input/output ports
	INT0 to INT7			External interrupt input pins
99, 100	P16_4, P16_5	I/O	A	General-purpose input/output ports

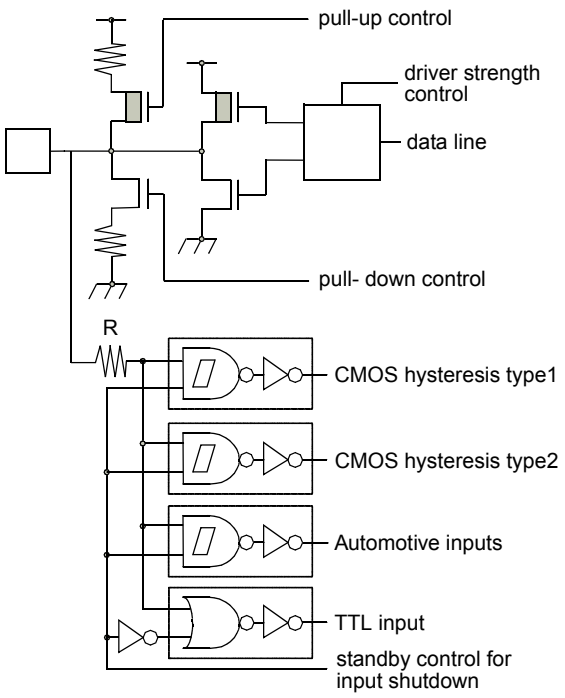
Pin no.	Pin name	I/O	I/O circuit type[1]	Description
101	P20_0	I/O	A	General-purpose input/output port
	SIN2			Data input pin for USART2
102	P20_1	I/O	A	General-purpose input/output port
	SOT2			Data output pin for USART2
103	P20_2	I/O	A	General-purpose input/output port
	SCK2			Clock input/output pin for USART2
	CK2			External clock input pin for free-run timer 2
104	P20_3	I/O	A	General-purpose input/output port
105	P20_4	I/O	A	General-purpose input/output port
	SIN3			Data input pin for USART3
106	P20_5	I/O	A	General-purpose input/output port
	SOT3			Data output pin for USART3
107	P20_6	I/O	A	General-purpose input/output port
	SCK3			Clock input/output pin for USART3
	CK3			External clock input pin for free-run timer 3
108	P20_7	I/O	A	General-purpose input/output port
109, 110	P16_0, P16_1	I/O	A	General-purpose input/output ports
	PPG8, PPG9			PPG timer output pins
111	MD_0	I	G	Mode setting pin
112	X0A	-	J2	Sub clock (oscillation) input
113	X1A	-	J2	Sub clock (oscillation) output
115	X1	-	J1	Clock (oscillation) output
116	X0	-	J1	Clock (oscillation) input
117	MD_1	I	G	Mode setting pins
118	MD_2	I	G	
119	MONCLK	O	M	Clock monitor pin

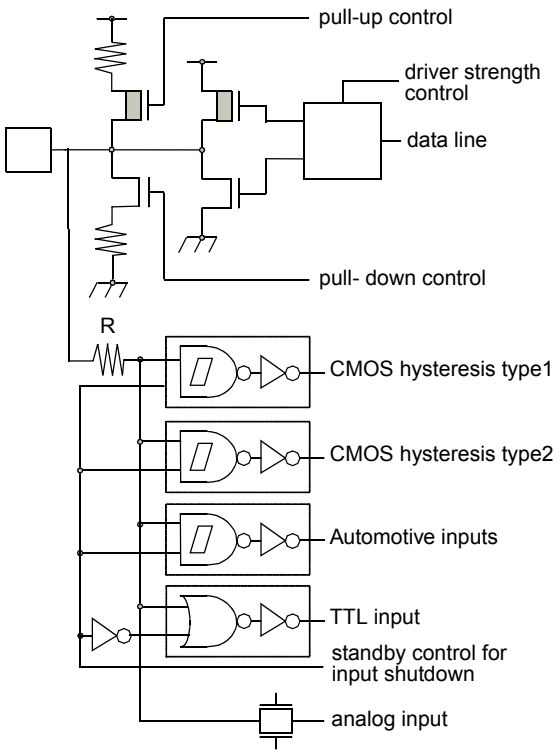
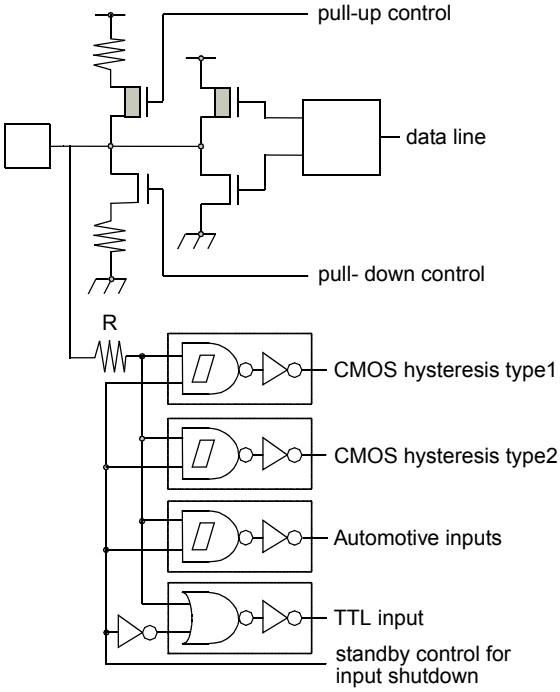
1. For information about the I/O circuit type, refer to "I/O Circuit Types".

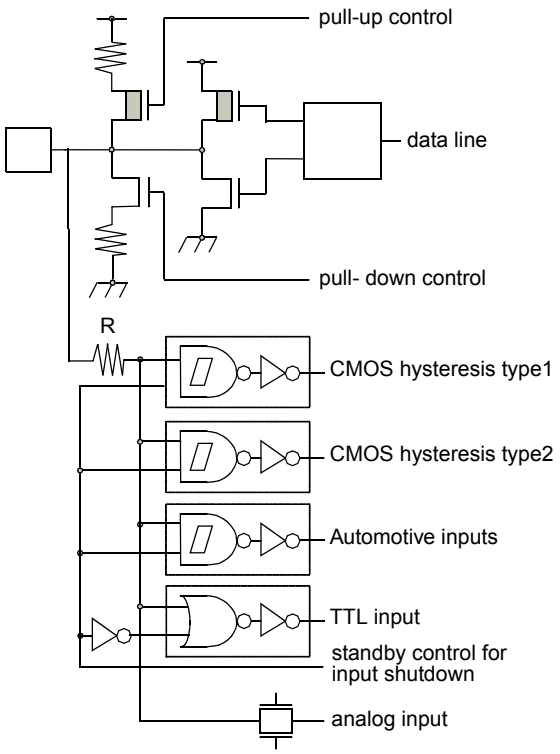
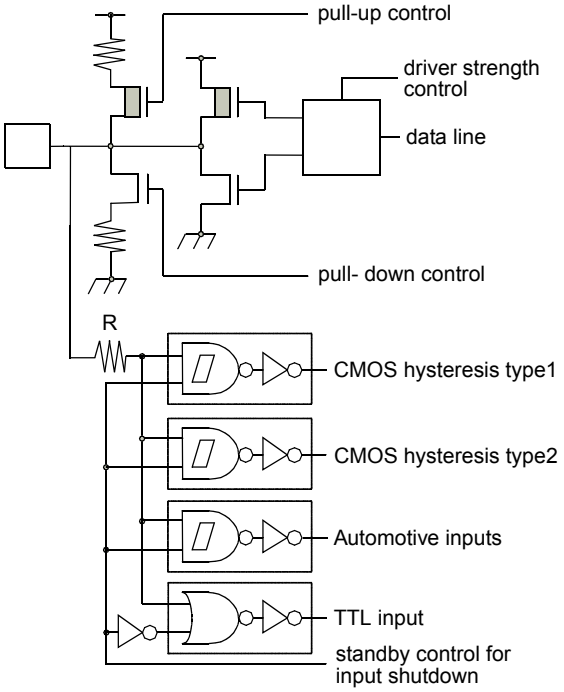
3.2 Power Supply/Ground Pins

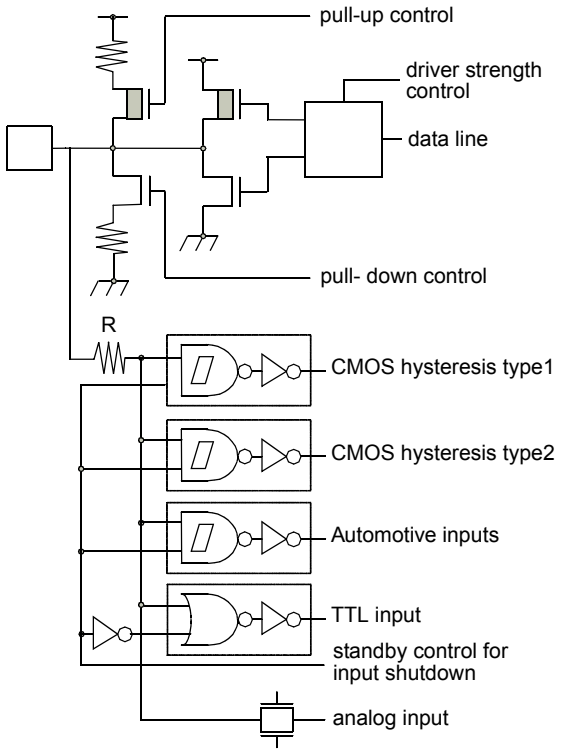
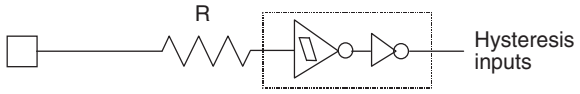
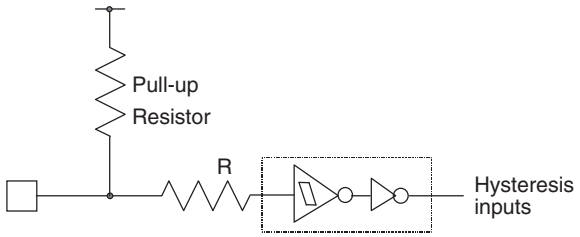
Pin no.	Pin name	Description
17, 31, 46, 61, 77, 90, 114, 120	VSS5	Ground pins
1, 18, 30, 60, 76, 91	VDD5	Power supply pins
15	VDD5R	Power supply pin for internal regulator
38	AVSS5	Analog ground pin for A/D converter
36	AVCC5	Power supply pin for A/D converter
37	AVRH5	Reference power supply pin for A/D converter
16	VCC18C	Capacitor connection pin for internal regulator

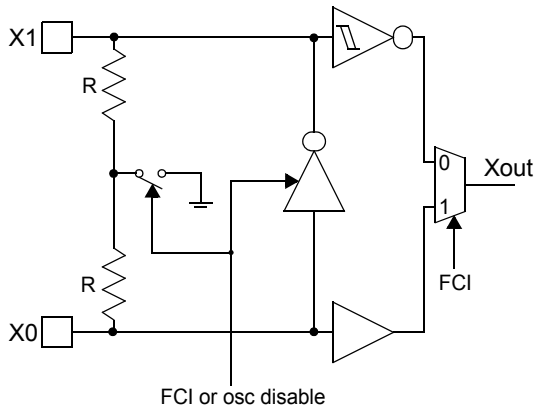
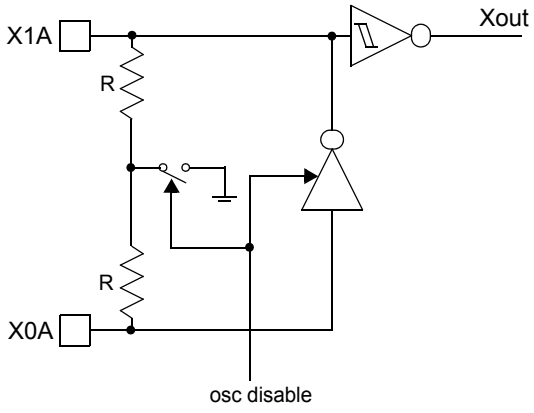
4. I/O Circuit Types

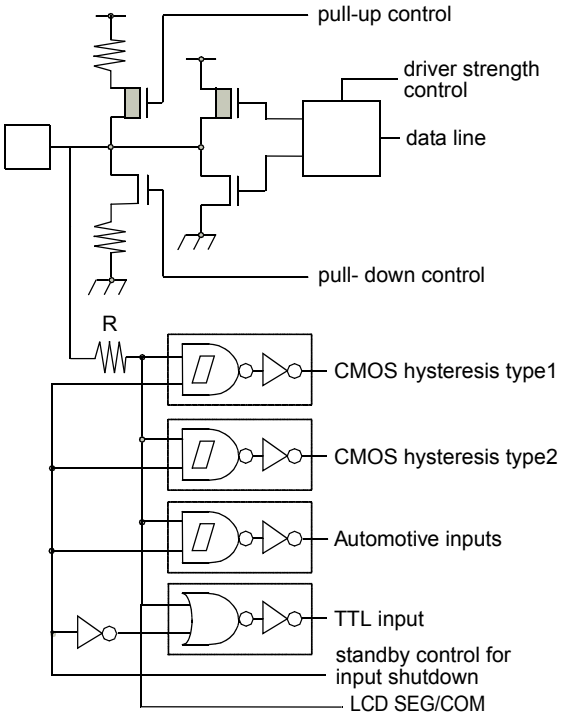
Type	Circuit	Remarks
A		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.

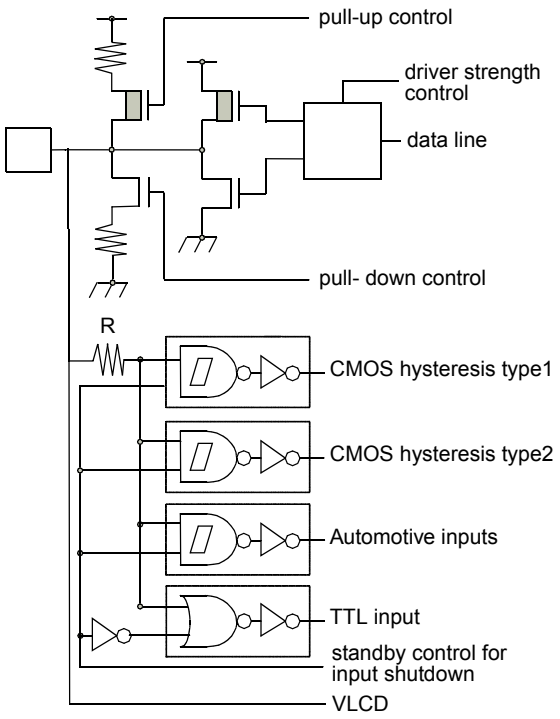
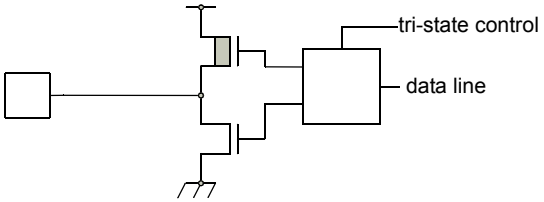
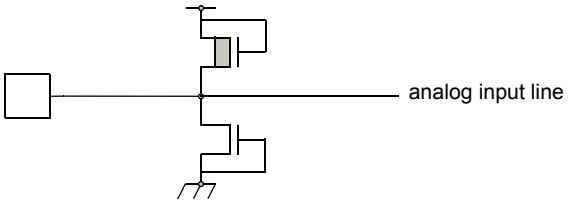
Type	Circuit	Remarks
B		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input
C		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.

Type	Circuit	Remarks
D		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input
E		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.

Type	Circuit	Remarks
F		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.

Type	Circuit	Remarks
J1		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.
J2		Low-speed oscillation circuit: ■ Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled.

Type	Circuit	Remarks
K		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. LCD SEG/COM output

Type	Circuit	Remarks
L		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input LCD Voltage input
M		CMOS level tri-state output(I_{OL} = 5mA, I_{OH} = -5mA)
N		Analog input pin with protection

5. Handling Devices

5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$) or less than ($V_{SS}5$) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

5.2 Handling of Unused Input Pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2KΩ to 10KΩ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to $AV_{SS}5$ directly.

5.3 Power Supply Pins

In MB91460K series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460K series must be connected to the current supply source via a low impedance.It is also recommended to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between power supply pin and ground pin near this device.This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 μF (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

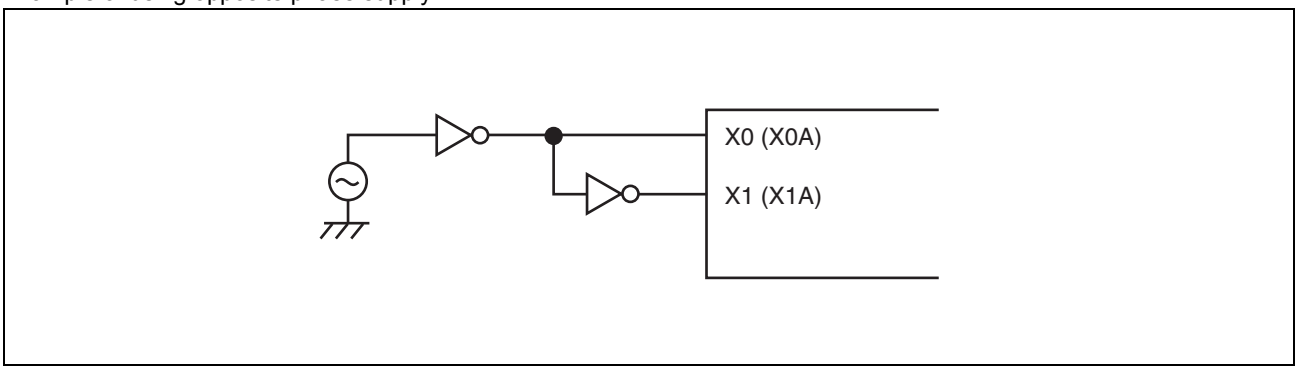
5.4 Crystal Oscillator Circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

5.5 Notes on using External Clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

Example of using opposite phase supply



5.6 Mode Pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

5.7 Notes on Operating in PLL Clock Mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

5.8 Pull-Up Control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

5.9 Notes on PS Register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated. As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event,the operation before and after the EIT always proceeds according to specification.

- **The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:**
  (a) a user interrupt or NMI is accepted;
  (b) single-step execution is performed;
  (c) execution breaks due to a data event or from the emulator menu.
  1. D0 and D1 flags are updated in advance.
  2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
  3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

- **The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.**
  1. The PS register is updated in advance.
  2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
  3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

6. Notes on Debugger

6.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

6.2 Break Function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

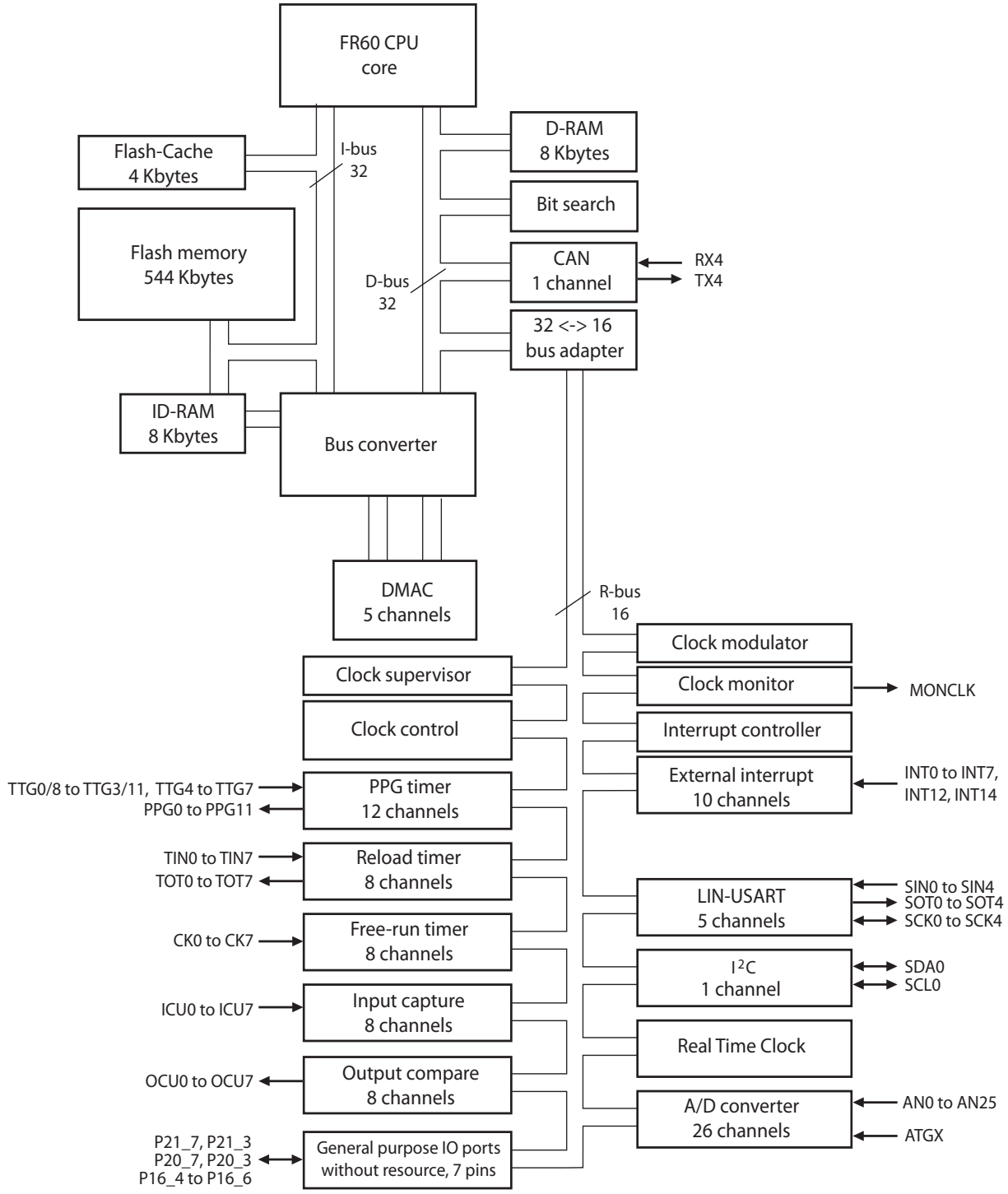
To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

6.3 Operand Break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

7. Block Diagram

7.1 MB91F465Kx



8. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

8.1 Features

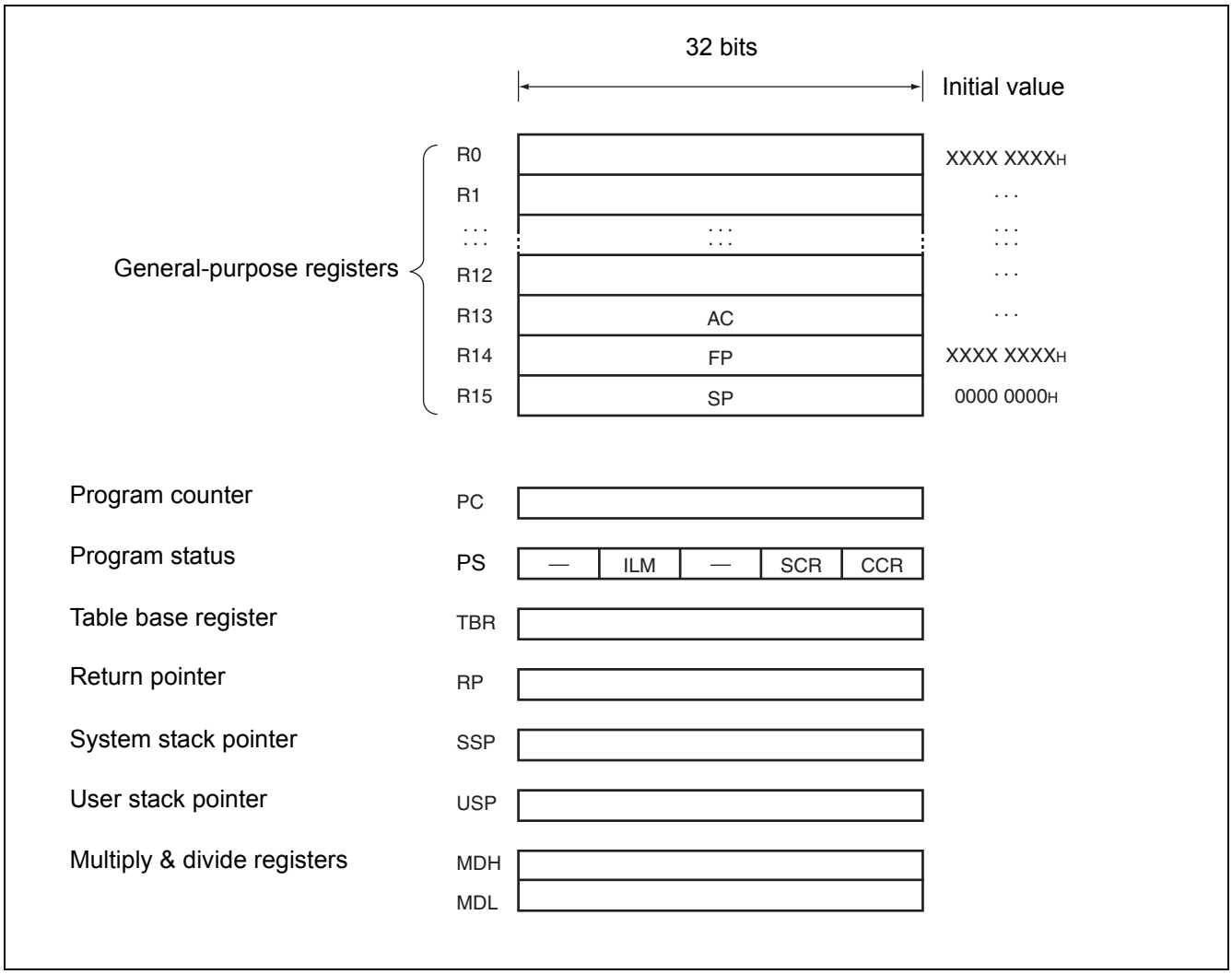
- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

8.2 Internal Architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

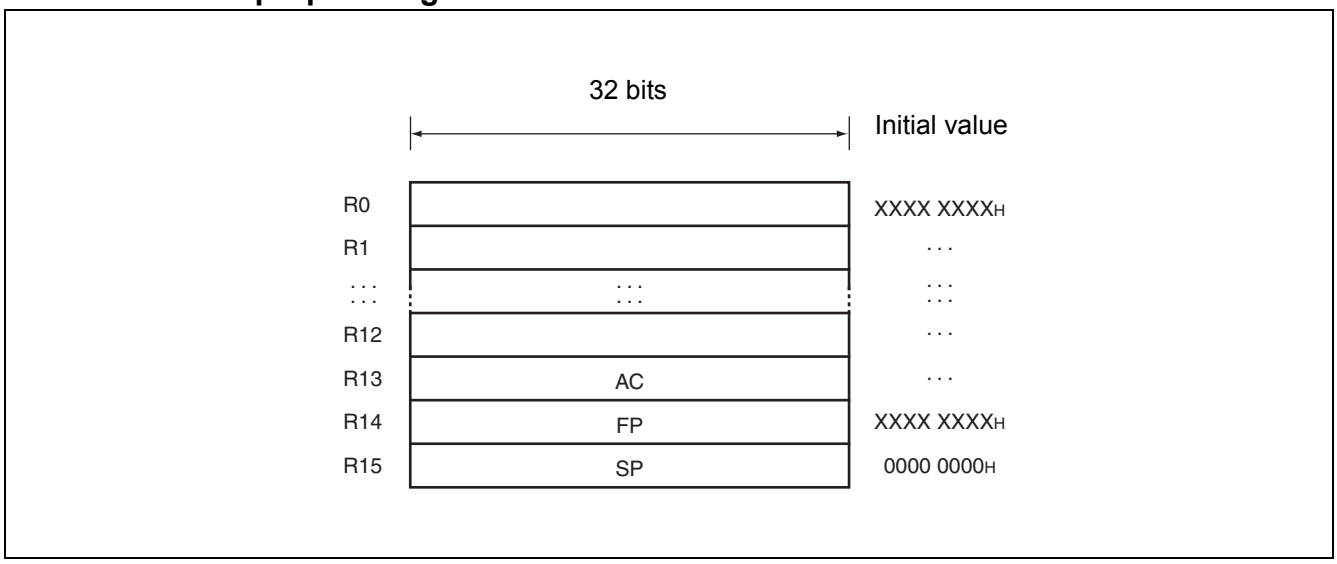
8.3 Programming Model

8.3.1 Basic Programming Model



8.4 Registers

8.4.1 General-purpose register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

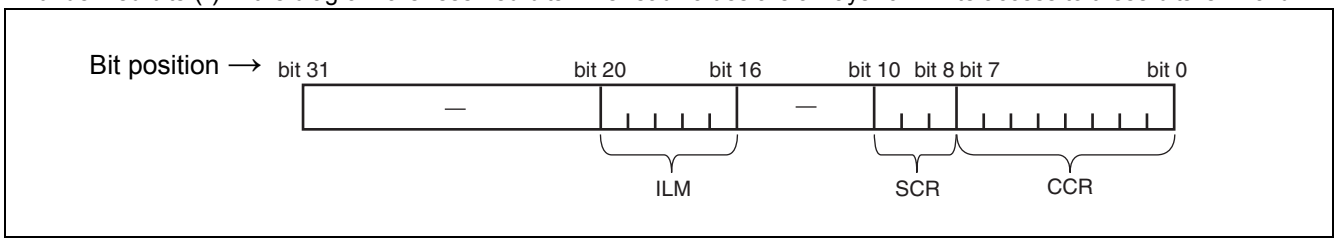
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

8.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.



8.4.3 CCR (Condition Code Register)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
—	SV	S	I	N	Z	V	C	- 000XXXX$_B$

SV: Supervisor flag

S: Stack flag

I: Interrupt enable flag

N: Negative enable flag

Z: Zero flag

V: Overflow flag

C: Carry flag

8.4.4 SCR (System Condition Register)

bit 10	bit 9	bit 8	Initial value
D1	D0	T	XX0$_B$

Flag for step division (D1, D0) This flag stores interim data during execution of step division.

Step trace trap flag (T) This flag indicates whether the step trace trap is enabled or disabled.The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

8.4.5 ILM (Interrupt Level Mask Register)

bit 20	bit 19	bit 18	bit 17	bit 16	Initial value
ILM4	ILM3	ILM2	ILM1	ILM0	01111$_B$

This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value “01111_B” at reset.

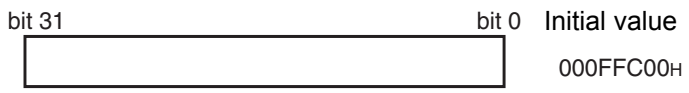
8.4.6 PC (Program Counter)

bit 31	bit 0	Initial value
		XXXXXXXX$_H$

The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

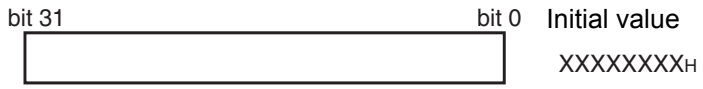
8.4.7 TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is $000FFC00_H$.

8.4.8 RP (Return Pointer)



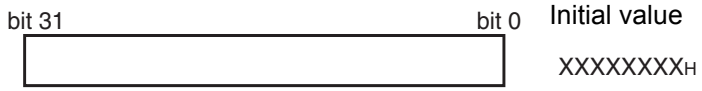
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

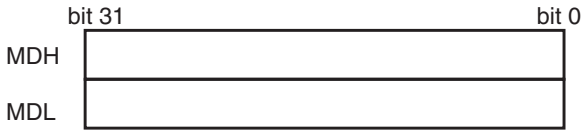
8.4.9 USP (User Stack Pointer)



The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.
The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

8.4.10 Multiply & Divide Registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

9. Embedded Program/Data Memory (Flash)

9.1 Flash Features

- MB91F465Kx: 544 Kbytes (8 × 64 Kbytes + 4 × 8 Kbytes) = 4.25 Mbits
- Programmable wait state for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

9.2 Operation Modes

9.2.1 32-bit CPU mode :

- CPU reads and executes programs in word (32-bit) length units.
- Actual Flash Memory access is performed in word (32-bit) length units.

9.2.2 16-bit CPU mode :

- CPU reads and writes in half-word (16-bit) length units.
- Program execution from the Flash is not possible.
- Actual Flash Memory access is performed in half-word (16-bit) length units.

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 "Flash Access Mode Switching".

9.3 Flash Access in CPU mode

9.3.1 Flash Configuration

9.3.1.1 Flash Memory Map MB91F465Kx

Addr									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				
Legend	Memory not available in this area				Memory available in this area				

9.3.2 Flash Access Timing Settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

9.3.2.1 Flash Read Timing Settings (Synchronous Read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 80 MHz	1	1	3	-	4	
to 100 MHz	1	1	3	-	4	not available on MB91F465Kx

9.3.2.2 Flash Write Timing Settings (Synchronous Write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 32 MHz	1	-	-	0	4	
to 48 MHz	1	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 80 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	0	7	not available on MB91F465Kx

9.3.3 Address Mapping from CPU to Parallel Programming Mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

9.3.3.1 Address Mapping MB91F465Kx

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h + 00:2000h
08:0000h to 0F:FFFFh	addr[2]==0	SA12, SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 00:0000h
08:0000h to 0F:FFFFh	addr[2]==1	SA13, SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 - 00:0000h + 01:0000h

Note: FA result is without 10:0000h offset for parallel Flash programming . Set offset by keeping FA[20] = 1 as described in section “Parallel Flash programming mode”.

9.4 Parallel Flash Programming Mode

9.4.1 Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):

MB91F465Kx

FA[20:0]		
001F:FFFFh 001F:0000h	SA19 (64KB)	
001E:FFFFh 001E:0000h	SA18 (64KB)	
001D:FFFFh 001D:0000h	SA17 (64KB)	
001C:FFFFh 001C:0000h	SA16 (64KB)	
001B:FFFFh 001B:0000h	SA15 (64KB)	
001A:FFFFh 001A:0000h	SA14 (64KB)	
0019:FFFFh 0019:0000h	SA13 (64KB)	
0018:FFFFh 0018:0000h	SA12 (64KB)	
	SA11 (64KB)	
	SA10 (64KB)	
	SA9 (64KB)	
	SA8 (64KB)	
0017:FFFFh 0017:E000h	SA7 (8KB)	
0017:DFFFh 0017:C000h	SA6 (8KB)	
0017:BFFFh 0017:A000h	SA5 (8KB)	
0017:9FFFh 0017:8000h	SA4 (8KB)	
	SA3 (8KB)	
	SA2 (8KB)	
	SA1 (8KB)	
	SA0 (8KB)	
	FA[1:0]=00	FA[1:0]=10
16bit write mode	DQ[15:0]	DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[20] = 1

Legend	
	Memory available in this area
	Memory not available in this area

9.4.2 Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to General Purpose Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Table 1. Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	MB91F465Kx external pins			Comment
		Flash memory mode	Normal function	Pin number	
-	INITX	-	INITX	62	
RESET	-	FRSTX	P16_7	63	
-	-	MD_2	MD_2	118	Set to '1'
-	-	MD_1	MD_1	117	Set to '1'
-	-	MD_0	MD_0	111	Set to '1'
RY/BY	FMCS:RDY bit	RY/BYX	P24_0	89	
BYTE	Internally fixed to 'H'	BYTEX	P24_2	93	
WE	Internal control signal + control via interface circuit	WEX	P28_3	34	
OE		OEX	P28_2	33	
CE		CEX	P28_1	32	
-		ATDIN	P22_1	88	Set to '0'
-		EQIN	P22_0	87	Set to '0'
-		TESTX	P24_3	94	Set to '1'
-		RDYI	P24_1	92	Set to '0'
A-1	Internal address bus	FA0	P19_2	55	Set to '0'
A0 to A7		FA1 to FA8	P27_0 to P27_7	21 to 28	
A8 to A15		FA9 to FA16	P15_0 to P15_3, P15_4, P15_5 P21_0, P21_1	83 to 86, 10, 11, 68, 69	
A16 to A18		FA17 to FA19	P21_2, P21_4, P21_5	70, 72, 73	
-		FA20,FA21	P21_6, P28_0	74, 29	Set to '1'
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	P17_0 to P17_7	58, 59, 65, 66, 67, 78, 79, 80	
DQ8 to DQ15		DQ8 to DQ15	P14_0 to P14_7	2 to 9	

9.5 Power on Sequence in Parallel Programming Mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

9.6 Flash Security

9.6.1 Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
FSV2: 0x14:8008 BSV2: 0x14:800C

9.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

9.6.2.1 FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Table 2: Explanation of the bits in the Flash Security Vector FSV1 [31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to “0”	set to “0”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “0”	set to “1”	set to “0”	Write Protection (all device modes, without exception)
set all to “0”	set to “0”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes)
set all to “0”	set to “1”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “0”	Write Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes except INTVEC mode MD[2:0] = “000”)

9.6.2.2 FSV1 (bit15 to bit0)

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 Kbytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 3: Explanation of the bits in the Flash Security Vector FSV1 [15:0]:
MB91F465Kx:

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	-	set to “0”	set to “1”	not available
FSV1[1]	-	set to “0”	set to “1”	not available
FSV1[2]	-	set to “0”	set to “1”	not available
FSV1[3]	-	set to “0”	set to “1”	not available
FSV1[4]	SA4	set to “0”	-	write protection is mandatory!
FSV1[5]	SA5	set to “0”	set to “1”	
FSV1[6]	SA6	set to “0”	set to “1”	
FSV1[7]	SA7	set to “0”	set to “1”	
FSV1[8]	-	set to “0”	set to “1”	not available
FSV1[9]	-	set to “0”	set to “1”	not available
FSV1[10]	-	set to “0”	set to “1”	not available
FSV1[11]	-	set to “0”	set to “1”	not available
FSV1[12]	-	set to “0”	set to “1”	not available
FSV1[13]	-	set to “0”	set to “1”	not available
FSV1[14]	-	set to “0”	set to “1”	not available
FSV1[15]	-	set to “0”	set to “1”	not available

Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

9.6.3 Security Vector FSV2

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 Kbytes sectors. It is only evaluated if write protection bit FSV1 [17] is set.

Table 4: Explanation of the bits in the Flash Security Vector FSV2[31:0]
MB91F465Kx:

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[3:0]	-	set to “0”	set to “1”	not available
FSV2[4]	SA12	set to “0”	set to “1”	
FSV2[5]	SA13	set to “0”	set to “1”	
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[31:12]	-	set to “0”	set to “1”	not available

Note: See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

10. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

■ Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access: 000_H to $0FF_H$

Half word access: 000_H to $1FF_H$

Word data access: 000_H to $3FF_H$

11. Memory Maps

11.1 MB91F465Kx

MB91F465Kx

00000000H	I/O (direct addressing area)
00000400H	I/O
00001000H	DMA
00002000H	
00005000H	Flash-Cache (4 KBytes)
00006000H	
00007000H	Flash memory control
00008000H	
0000B000H	Boot ROM (4 Kbytes)
0000C000H	CAN
0000D000H	
0002E000H	D-RAM (0 wait, 8 Kbytes)
00030000H	ID-RAM (8 Kbytes)
00032000H	
00040000H	External bus area
00080000H	Flash memory (512 Kbytes)
00100000H	External bus area
00148000H	Flash memory (32 Kbytes)
00150000H	
00180000H	External bus area
00500000H	External data bus
FFFFFFFFH	

Note:	Access prohibited areas

12. I/O Map

12.1 MB91F465Kx

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register

Read/write attribute

Register initial value after reset

Register name (column 1 register at address 4n, column 2 register at address 4n + 1...)

Leftmost register address (for word access, the register in column 1 becomes the MSB side of the data.)

Note: Initial values of register bits are represented as follows:
" 1 ": Initial value " 1 "
" 0 ": Initial value " 0 "
" X ": Initial value " undefined "
" - ": No physical register at this location
Access is barred with an undefined data access attribute.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H to 000008_H	Reserved				R-bus Port Data Register
$00000C_H$	Reserved		PDR14 [R/W] XXXXXXXX	PDR15 [R/W] XXXXXXXX	
000010_H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - X - - - X -	PDR19 [R/W] - X - - - XXX	
000014_H	PDR20 [R/W] XXXX XXXX	PDR21 [R/W] XXXX XXXX	PDR22 [R/W] - - XX - - XX	Reserved	
000018_H	PDR24 [R/W] XXXXXXXX	Reserved	PDR26 [R/W] - - - - - - XX	PDR27 [R/W] XXXXXXXX	
$00001C_H$	PDR28 [R/W] XXXXXXXX	PDR29 [R/W] XXXXXXXX	Reserved		
000020_H to $00002C_H$	Reserved				Reserved
000030_H	EIRR0 [R/W] XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External Interrupt (INT0 to INT7)
000034_H	EIRR1 [R/W] XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External Interrupt (INT8 to INT15)
000038_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	Reserved		Delay Interrupt
$00003C_H$	Reserved				Reserved
000040_H	SCR00 [R/W, W] 00000000	SMR00 [R/W, W] 00000000	SSR00 [R/W, R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044_H	ESCR00 [R/W] 00000X00	ECCR00 [R/W, R, W] -00000XX	Reserved		
000048_H	SCR01 [R/W, W] 00000000	SMR01 [R/W, W] 00000000	SSR01 [R/W, R] 00001000	RDR01/TDR01 [R/W] 00000000	LIN-USART 1
$00004C_H$	ESCR01 [R/W] 00000X00	ECCR01 [R/W, R, W] -00000XX	Reserved		
000050_H	SCR02 [R/W, W] 00000000	SMR02 [R/W, W] 00000000	SSR02 [R/W, R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W, R, W] -00000XX	Reserved		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000058_H	SCR03 [R/W, W] 00000000	SMR03 [R/W, W] 00000000	SSR03 [R/W, R] 00001000	RDR03/TDR03 [R/W] 00000000	LIN-USART 3
$00005C_H$	ESCR03 [R/W] 00000X00	ECCR03 [R/W, R, W] -00000XX	Reserved		
000060_H	SCR04 [R/W, W] 00000000	SMR04 [R/W, W] 00000000	SSR04 [R/W, R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064_H	ESCR04 [R/W] 00000X00	ECCR04 [R/W, R, W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068_H to $00007C_H$	Reserved				Reserved
000080_H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	BGR101 [R/W] 00000000	BGR001 [R/W] 00000000	Baudrate Generator LIN-USART 0 to 4
000084_H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088_H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	Reserved		
$00008C_H$ to $0000CC_H$	Reserved				Reserved
$0000D0_H$	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I^2C 0
$0000D4_H$	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
$0000D8_H$	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] 00011111	Reserved	
$0000DC_H$ to $0000FC_H$	Reserved				Reserved
000100_H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] - - - - 0000	PPG Control 0 to 3
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108_H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8 to 11
$00010C_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	

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(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000160_H to $00017C_H$	Reserved				Reserved
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H, $00019C_H$	Reserved				Reserved
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
$0001A4_H$	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	Reserved				Reserved
$0001B0_H$	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0, PPG 1)
$0001B4_H$	Reserved		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
$0001B8_H$	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2, PPG 3)
$0001BC_H$	Reserved		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	
$0001C0_H$	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
$0001C4_H$	Reserved		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$0001C8_H$	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
$0001CC_H$	Reserved		TMCSRH3 [R/W] - - - 00000	TMCSRL3 [R/W] 0 - 000000	
$0001D0_H$	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8, PPG 9)
$0001D4_H$	Reserved		TMCSRH4 [R/W] - - - 00000	TMCSRL4 [R/W] 0 - 000000	
$0001D8_H$	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10, PPG 11)
$0001DC_H$	Reserved		TMCSRH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
$0001E0_H$	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12, PPG 13)
$0001E4_H$	Reserved		TMCSRH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
$0001E8_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (ADC)
$0001EC_H$	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
$0001F0_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
$0001F4_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
$0001F8_H$	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU1)
$0001FC_H$	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU3)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H to $00023C_H$	Reserved				
000240_H	DMACR [R/W] 00 - - 0000	Reserved			
000244_H to $0002CC_H$	Reserved				Reserved
$0002D0_H$	Reserved	ICS045 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7
$0002D4_H$	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
$0002D8_H$	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
$0002DC_H$	OCS45 [R/W] - - - 0 - - 00 0000 - - 00		OCS67 [R/W] - - -0 - -00 0000 - -00		Output Compare 4 to 7
$0002E0_H$	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
$0002E4_H$	OCCP6 [R/W] XXXXXXXX XXXXXXXX		OCCP7 [R/W] XXXXXXXX XXXXXXXX		
$0002E8_H$ to $0002EC_H$	Reserved				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$0002F0_H$	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU4, ICU5)
$0002F4_H$	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU6, ICU7)
$0002F8_H$	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6 (OCU4, OCU5)
$0002FC_H$	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7 (OCU6, OCU7)
000300_H to $00038C_H$	Reserved				Reserved
000390_H	ROMS [R] 11111111 01000011		Reserved		ROM Select Register
000394_H to $0003EC_H$	Reserved				Reserved
$0003F0_H$	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
$0003F4_H$	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400_H to $00043C_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
$00044C_H$	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450_H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454_H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
$00045C_H$	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460_H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464_H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468_H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
$00046C_H$	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470_H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474_H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478_H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
$00047C_H$	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] X0000X00	CTBR [W] XXXXXXXX	Clock Control
000484_H	CLKR [R/W] 00000000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00048C_H$	PLLDIVM [R/W] - - - 00000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [W] 00000000	PLL Interface
000490_H	PLLCTRL [R/W] - - - - 0000	Reserved			
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control
000498_H	PORTEN [R/W] - - - - - - 00	Reserved			Port Input Enable Control
$0004A0_H$	Reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
$0004A4_H$	Reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
$0004A8_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	Reserved	
$0004AC_H$	CSVTR [R/W] - - - 00010	CSVCR [R/W] 00011100	CSCFG [R/W] 0X000000	Reserved	Clock Supervisor / Selector
$0004B0_H$	CUCR [R/W] - - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration of Sub Clock
$0004B4_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
$0004B8_H$	CMPR [R/W] - - 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulator
$0004BC_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
$0004C0_H$	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - - 0 - - - -	Reserved		CAN Clock Control
$0004C4_H$	LVSEL [R/W] 00000111	LVDET [R/W] 0000 0 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W, W] 00011000	Low Voltage Detection / Hardware Watchdog
$0004C8_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 00 - - - 000	WPCRL [R/W] - - - - - - 00	Main/Sub Oscillation Stabilisation Timer
$0004CC_H$	OSCCR [R/W] - - - - - - - 0	Reserved	REGSEL [R/W] - - 000110	REGCTR [R/W] - - - 0 - - 00	Main Oscillation Standby Control / Main/Sub Regulator Control
$0004D0_H$ to $000D08_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000D0C_H$	Reserved		PDRD14 [R] XXXXXXXX	PDRD15 [R] XXXXXXXX	R-bus Port Data Direct Read Register
$000D10_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] - X - - - X -	PDRD19 [R] - X - - - XXX	
$000D14_H$	PDRD20 [R] XXXX XXXX	PDRD21 [R] XXXX XXXX	PDRD22 [R] - - XX - - XX	Reserved	
$000D18_H$	PDRD24 [R] XXXXXXXX	Reserved	PDRD26 [R] - - - - - - XX	PDRD27 [R] XXXXXXXX	
$000D1C_H$	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	Reserved		
$000D20_H$ to $000D48_H$	Reserved				Reserved
$000D4C_H$	Reserved		DDR14 [R/W] 00000000	DDR15 [R/W] 00000000	R-bus Port Direction Register
$000D50_H$	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] - 0 - - - 0 -	DDR19 [R/W] - 0 - - - 000	
$000D54_H$	DDR20 [R/W] 0000 0000	DDR21 [R/W] 0000 0000	DDR22 [R/W] - - 00 - - 00	Reserved	
$000D58_H$	DDR24 [R/W] 00000000	Reserved	DDR26 [R/W] - - - - - - 00	DDR27 [R/W] 00000000	
$000D5C_H$	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	Reserved		
$000D60_H$ to $000D88_H$	Reserved				Reserved
$000D8C_H$	Reserved		PFR14 [R/W] 00000000	PFR15 [R/W] 00000000	R-bus Port Function Register
$000D90_H$	PFR16 [R/W] 0 - - - 0000	PFR17 [R/W] 00000000	PFR18 [R/W] - 0 - - - 0 -	PFR19 [R/W] - 0 - - - 000	
$000D94_H$	PFR20 [R/W] - 000 - 000	PFR21 [R/W] - 000 - 000	PFR22 [R/W] - - 00 - - 00	Reserved	
$000D98_H$	PFR24 [R/W] 00000000	Reserved	PFR26 [R/W] - - - - - - 00	PFR27 [R/W] 00000000	
$000D9C_H$	PFR28 [R/W] 00000000	PFR29 [R/W] 00000000	Reserved		
$000DA0_H$ to $000DC8_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000DCC_H$	Reserved		EPFR14 [R/W] 00000000	EPFR15 [R/W] 00000000	R-bus Expansion Port Function Register
$000DD0_H$	EPFR16 [R/W] 0 - - - - - - -	EPFR17 [R/W] - - - - - - - -	EPFR18 [R/W] - 0 - - - - 0 -	EPFR19 [R/W] - 0 - - - 0 - -	
$000DD4_H$	EPFR20 [R/W] - 0 - - - 0 - -	EPFR21 [R/W] - 0 - - - 0 - -	EPFR22 [R/W] - - - - - - - -	Reserved	
$000DD8_H$	EPFR24 [R/W] - - - - - - - -	Reserved	EPFR26 [R/W] - - - - - - 00	EPFR27 [R/W] 00000000	
$000DDC_H$	EPFR28 [R/W] - - - - - - - -	EPFR29 [R/W] - - - - - - - -	Reserved		
$000DE0_H$ to $000E08_H$	Reserved				Reserved
$000E0C_H$	Reserved		PODR14 [R/W] 00000000	PODR15 [R/W] 00000000	R-bus Port Output Drive Select Register
$000E10_H$	PODR16 [R/W] 00000000	PODR17 [R/W] 00000000	PODR18 [R/W] - 0 - - - 0 -	PODR19 [R/W] - 0 - - - 000	
$000E14_H$	PODR20 [R/W] 0000 0000	PODR21 [R/W] 0000 0000	PODR22 [R/W] - - 00 - - 00	Reserved	
$000E18_H$	PODR24 [R/W] 00000000	Reserved	PODR26 [R/W] - - - - - - 00	PODR27 [R/W] 00000000	
$000E1C_H$	PODR28 [R/W] 00000000	PODR29 [R/W] 00000000	Reserved		
$000E20_H$ to $000E48_H$	Reserved				Reserved
$000E4C_H$	Reserved		PILR14 [R/W] 00000000	PILR15 [R/W] 00000000	R-bus Pin Input Level Select Register
$000E50_H$	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] - 0 - - - 0 -	PILR19 [R/W] - 0 - - - 000	
$000E54_H$	PILR20 [R/W] 0000 0000	PILR21 [R/W] 0000 0000	PILR22 [R/W] - - 00 - - 00	Reserved	
$000E58_H$	PILR24 [R/W] 00000000	Reserved	PILR26 [R/W] - - - - - - 00	PILR27 [R/W] 00000000	
$000E5C_H$	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	Reserved		
$000E60_H$ to $000E88_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000E8C_H$	Reserved		EPILR14 [R/W] 00000000	EPILR15 [R/W] 00000000	R-bus Expansion Port Input Level Select Register
$000E90_H$	EPILR16 [R/W] 00000000	EPILR17 [R/W] 00000000	EPILR18 [R/W] - 0 - - - 0 -	EPILR19 [R/W] - 0 - - - 000	
$000E94_H$	EPILR20 [R/W] 0000 0000	EPILR21 [R/W] 0000 0000	EPILR22 [R/W] - - 00 - - 00	Reserved	
$000E98_H$	EPILR24 [R/W] 00000000	Reserved	EPILR26 [R/W] - - - - - - 00	EPILR27 [R/W] 00000000	
$000E9C_H$	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	Reserved		
$000EA0_H$ to $000EC8_H$	Reserved				Reserved
$000ECC_H$	Reserved		PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	R-bus Port Pull-Up/Down Enable Register
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] - 0 - - - 0 -	PPER19 [R/W] - 0 - - - 000	
$000ED4_H$	PPER20 [R/W] 0000 0000	PPER21 [R/W] 0000 0000	PPER22 [R/W] - - 00 - - 00	Reserved	
$000ED8_H$	PPER24 [R/W] 00000000	Reserved	PPER26 [R/W] - - - - - - 00	PPER27 [R/W] 00000000	
$000EDC_H$	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	Reserved		
$000EE0_H$ to $000F08_H$	Reserved				Reserved
$000F0C_H$	Reserved		PPCR14 [R/W] 00000000	PPCR15 [R/W] 00000000	R-bus Port Pull-Up/Down Control Register
$000F10_H$	PPCR16 [R/W] 00000000	PPCR17 [R/W] 00000000	PPCR18 [R/W] - 0 - - - 0 -	PPCR19 [R/W] - 0 - - - 000	
$000F14_H$	PPCR20 [R/W] 0000 0000	PPCR21 [R/W] 0000 0000	PPCR22 [R/W] - - 00 - - 00	Reserved	
$000F18_H$	PPCR24 [R/W] 00000000	Reserved	PPCR26 [R/W] - - - - - - 00	PPCR27 [R/W] 00000000	
$000F1C_H$	PPCR28 [R/W] 00000000	PPCR29 [R/W] 00000000	Reserved		
$000F20_H$ to $000F3C_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H to $004FFC_H$	Reserved				Reserved
005000_H to $005FFC_H$	MB91F465Kx Instruction RAM/Flash Cache size is 4KB				Instruction RAM / Flash Cache
006000_H to $006FFC_H$	reserved				reserved
007000_H	FMCS [R/W] 01101000	FMCR [R] - - - 00000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/F-Cache/ I-RAM Control Register
007004_H	FMWT [R/W] 11111111 11111111		FMWT2 [R] - 001 - - - -	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] - - - - - - - - - - - - 00000 00000000 00000000				Flash-cache Non- cacheable area setting Register
007010_H	FCHA1 [R/W] - - - - - - - - - - - - 00000 00000000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
007014_H to $007FFC_H$	Reserved				Reserved
008000_H to $00BFFC_H$	MB91F465Kx Boot-ROM size is 4 Kbytes : $00B000_H$ to $00BFFC_H$ (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
$00C000_H$ to $00C3FC_H$	Reserved				Reserved
$00C400_H$	CTRLR4 [R/W] 00000000 00000001		STATR4 [R/W] 00000000 00000000		CAN 4 Control Register
$00C404_H$	ERRCNT4 [R] 00000000 00000000		BTR4 [R/W] 00100011 00000001		
$00C408_H$	INTR4 [R] 00000000 00000000		TESTR4 [R/W] 00000000 X0000000		
$00C40C_H$	BRPE4 [R/W] 00000000 00000000		Reserved		
$00C410_H$	IF1CREQ4 [R/W] 00000000 00000001		IF1CMSK4 [R/W] 00000000 00000000		CAN 4 IF 1 Register
$00C414_H$	IF1MSK24 [R/W] 11111111 11111111		IF1MSK14 [R/W] 11111111 11111111		
$00C418_H$	IF1ARB24 [R/W] 00000000 00000000		IF1ARB14 [R/W] 00000000 00000000		
$00C41C_H$	IF1MCTR4 [R/W] 00000000 00000000		Reserved		
$00C420_H$	IF1DTA14 [R/W] 00000000 00000000		IF1DTA24 [R/W] 00000000 00000000		
$00C424_H$	IF1DTB14 [R/W] 00000000 00000000		IF1DTB24 [R/W] 00000000 00000000		
$00C428_H$ to $00C42C_H$	Reserved				
$00C430_H$	IF1DTA24 [R/W] 00000000 00000000		IF1DTA14 [R/W] 00000000 00000000		
$00C434_H$	IF1DTB24 [R/W] 00000000 00000000		IF1DTB14 [R/W] 00000000 00000000		
$00C438_H$, $00C43C_H$	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00C440_H$	IF2CREQ4 [R/W] 00000000 00000001		IF2CMSK4 [R/W] 00000000 00000000		CAN 4 IF 2 Register
$00C444_H$	IF2MSK24 [R/W] 11111111 11111111		IF2MSK14 [R/W] 11111111 11111111		
$00C448_H$	IF2ARB24 [R/W] 00000000 00000000		IF2ARB14 [R/W] 00000000 00000000		
$00C44C_H$	IF2MCTR4 [R/W] 00000000 00000000		Reserved		
$00C450_H$	IF2DTA14 [R/W] 00000000 00000000		IF2DTA24 [R/W] 00000000 00000000		
$00C454_H$	IF2DTB14 [R/W] 00000000 00000000		IF2DTB24 [R/W] 00000000 00000000		
$00C458_H$, $00C45C_H$	Reserved				
$00C460_H$	IF2DTA24 [R/W] 00000000 00000000		IF2DTA14 [R/W] 00000000 00000000		
$00C464_H$	IF2DTB24 [R/W] 00000000 00000000		IF2DTB14 [R/W] 00000000 00000000		
$00C468_H$ to $00C47C_H$	Reserved				
$00C480_H$	TREQR24 [R] 00000000 00000000		TREQR14 [R] 00000000 00000000		CAN 4 Status Flags
$00C484_H$ to $00C48C_H$	Reserved				
$00C490_H$	NEWDT24 [R] 00000000 00000000		NEWDT14 [R] 00000000 00000000		
$00C494_H$ to $00C49C_H$	Reserved				
$00C4A0_H$	INTPND24 [R] 00000000 00000000		INTPND14 [R] 00000000 00000000		
$00C4A4_H$ to $00C4AC_H$	Reserved				
$00C4B0_H$	MSGVAL24 [R] 00000000 00000000		MSGVAL14 [R] 00000000 00000000		
$00C4B4_H$ to $00EFFC_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
020000_H to $02FFFC_H$	MB91F465Kx D-RAM size is 8 Kbytes : $02E000_H$ to $02FFFC_H$ (data access is 0 wait cycles)				D-RAM area
030000_H to $03FFFC_H$	MB91F465Kx ID-RAM size is 8 Kbytes : 030000_H to $031FFC_H$ (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area

1. depends on the number of available CAN channels
2. ACR0 [11 : 10] depends on bus width setting in Mode vector fetch information
3. TCR [3 : 0] INIT value = 0000, keeps value after RST

12.2 Flash Memory and External Bus Area

12.2.1 MB91F465Kx

32bit read mode	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000_H to $05FFF8_H$	reserved				reserved				ROMS0
060000_H to $07FFF8_H$	reserved				reserved				ROMS1
080000_H to $09FFF8_H$	SA12 (64KB)				SA13 (64KB)				ROMS2
$0A0000_H$ to $0BFFF8_H$	SA14 (64KB)				SA15 (64KB)				ROMS3
$0C0000_H$ to $0DFFF8_H$	SA16 (64KB)				SA17 (64KB)				ROMS4
$0E0000_H$ to $0FFFF0_H$	SA18 (64KB) FMV [R] $06\ 00\ 00\ 00_H$				SA19 (64KB) FRV [R] $00\ 00\ BF\ F8_H$				ROMS5
$0FFFF8_H$									
100000_H to $11FFF8_H$	reserved				reserved				ROMS6
120000_H to $13FFF8_H$	reserved				reserved				
140000_H to $143FF8_H$	reserved				reserved				ROMS7
144000_H to $17FF8_H$	reserved				reserved				
148000_H to $14BFF8_H$	SA4 (8KB)				SA5 (8KB)				
$14C000_H$ to $14FFF8_H$	SA6 (8KB)				SA7 (8KB)				
150000_H to $17FFF8_H$	Reserved								

32bit read mode	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000_H to $1BFFF8_H$	Reserved								ROMS8
$1C0000_H$ to $1FFFF8_H$									ROMS9
200000_H to $27FFF8_H$									ROMS10
280000_H to $2FFFF8_H$									ROMS11
300000_H to $37FFF8_H$									ROMS12
380000_H to $3FFFF8_H$									ROMS13
400000_H to $47FFF8_H$									ROMS14
480000_H to $4FFFF8_H$									ROMS15

Note: Write operations to address $0FFFF8_H$ and $0FFFFC_H$ are not possible. When reading these addresses, the values shown above will be read.

13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Deci-mal	Hexa-de cimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	00	-	-	$3FC_H$	$000FFFFC_H$	-
Mode vector	1	01	-	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	02	-	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	03	-	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	04	-	-	$3EC_H$	$000FFFEC_H$	-
CPU supervisor mode (INT #5 instruction) [5]	5	05	-	-	$3E8_H$	$000FFFE8_H$	-
Memory Protection exception [5]	6	06	-	-	$3E4_H$	$000FFFE4_H$	-
System reserved	7	07	-	-	$3E0_H$	$000FFFE0_H$	-
System reserved	8	08	-	-	$3DC_H$	$000FFFDC_H$	-
System reserved	9	09	-	-	$3D8_H$	$000FFFD8_H$	-
System reserved	10	0A	-	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	-	$3C8_H$	$000FFFC8_H$	-
Undefined instruction exception	14	0E	-	-	$3C4_H$	$000FFFC4_H$	-
NMI request	15	0F	F_H fixed		$3C0_H$	$000FFFC0_H$	-
External Interrupt 0	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16
External Interrupt 1	17	11			$3B8_H$	$000FFFB8_H$	1, 17
External Interrupt 2	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18
External Interrupt 3	19	13			$3B0_H$	$000FFFB0_H$	3, 19
External Interrupt 4	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20
External Interrupt 5	21	15			$3A8_H$	$000FFFA8_H$	21
External Interrupt 6	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22
External Interrupt 7	23	17			$3A0_H$	$000FFFA0_H$	23
Reserved	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	-
Reserved	25	19			398_H	$000FFF98_H$	-
Reserved	26	1A	ICR05	445_H	394_H	$000FFF94_H$	-
Reserved	27	1B			390_H	$000FFF90_H$	-
External Interrupt 12	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	-
Reserved	29	1D			388_H	$000FFF88_H$	-
External Interrupt 14	30	1E	ICR07	447_H	384_H	$000FFF84_H$	-
Reserved	31	1F			380_H	$000FFF80_H$	-

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Deci-mal	Hexa-de cimal	Setting Register	Register address	Offset	Default Vector address	
Reload Timer 0	32	20	ICR08	448_H	$37C_H$	$000FFF7C_H$	4, 32
Reload Timer 1	33	21			378_H	$000FFF78_H$	5, 33
Reload Timer 2	34	22	ICR09	449_H	374_H	$000FFF74_H$	34
Reload Timer 3	35	23			370_H	$000FFF70_H$	35
Reload Timer 4	36	24	ICR10	$44A_H$	$36C_H$	$000FFF6C_H$	36
Reload Timer 5	37	25			368_H	$000FFF68_H$	37
Reload Timer 6	38	26	ICR11	$44B_H$	364_H	$000FFF64_H$	38
Reload Timer 7	39	27			360_H	$000FFF60_H$	39
Free Run Timer 0	40	28	ICR12	$44C_H$	$35C_H$	$000FFF5C_H$	40
Free Run Timer 1	41	29			358_H	$000FFF58_H$	41
Free Run Timer 2	42	2A	ICR13	$44D_H$	354_H	$000FFF54_H$	42
Free Run Timer 3	43	2B			350_H	$000FFF50_H$	43
Free Run Timer 4	44	2C	ICR14	$44E_H$	$34C_H$	$000FFF4C_H$	44
Free Run Timer 5	45	2D			348_H	$000FFF48_H$	45
Free Run Timer 6	46	2E	ICR15	$44F_H$	344_H	$000FFF44_H$	46
Free Run Timer 7	47	2F			340_H	$000FFF40_H$	47
Reserved	48	30	ICR16	450_H	$33C_H$	$000FFF3C_H$	-
Reserved	49	31			338_H	$000FFF38_H$	-
Reserved	50	32	ICR17	451_H	334_H	$000FFF34_H$	-
Reserved	51	33			330_H	$000FFF30_H$	-
CAN 4	52	34	ICR18	452_H	$32C_H$	$000FFF2C_H$	-
Reserved	53	35			328_H	$000FFF28_H$	-
LIN-USART 0 RX	54	36	ICR19	453_H	324_H	$000FFF24_H$	6, 48
LIN-USART 0 TX	55	37			320_H	$000FFF20_H$	7, 49
LIN-USART 1 RX	56	38	ICR20	454_H	$31C_H$	$000FFF1C_H$	8, 50
LIN-USART 1 TX	57	39			318_H	$000FFF18_H$	9, 51
LIN-USART 2 RX	58	3A	ICR21	455_H	314_H	$000FFF14_H$	52
LIN-USART 2 TX	59	3B			310_H	$000FFF10_H$	53
LIN-USART 3 RX	60	3C	ICR22	456_H	$30C_H$	$000FFF0C_H$	54
LIN-USART 3 TX	61	3D			308_H	$000FFF08_H$	55
System reserved	62	3E	ICR23 [3]	457_H	304_H	$000FFF04_H$	-
Delayed Interrupt	63	3F			300_H	$000FFF00_H$	-

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Deci-mal	Hexa-de cimal	Setting Register	Register address	Offset	Default Vector address	
System reserved [4]	64	40	(ICR24)	(458_H)	$2FC_H$	$000FFEFC_H$	-
System reserved [4]	65	41			$2F8_H$	$000FFEF8_H$	-
LIN-USART (FIFO) 4 RX	66	42	ICR25	459_H	$2F4_H$	$000FFEF4_H$	10, 56
LIN-USART (FIFO) 4 TX	67	43			$2F0_H$	$000FFEF0_H$	11, 57
Reserved	68	44	ICR26	$45A_H$	$2EC_H$	$000FFEEC_H$	12, 58
Reserved	69	45			$2E8_H$	$000FFEE8_H$	13, 59
Reserved	70	46	ICR27	$45B_H$	$2E4_H$	$000FFEE4_H$	60
Reserved	71	47			$2E0_H$	$000FFEE0_H$	61
Reserved	72	48	ICR28	$45C_H$	$2DC_H$	$000FFEDC_H$	62
Reserved	73	49			$2D8_H$	$000FFED8_H$	63
I^2C 0	74	4A	ICR29	$45D_H$	$2D4_H$	$000FFED4_H$	-
Reserved	75	4B			$2D0_H$	$000FFED0_H$	-
Reserved	76	4C	ICR30	$45E_H$	$2CC_H$	$000FFECC_H$	64
Reserved	77	4D			$2C8_H$	$000FFEC8_H$	65
Reserved	78	4E	ICR31	$45F_H$	$2C4_H$	$000FFEC4_H$	66
Reserved	79	4F			$2C0_H$	$000FFEC0_H$	67
Reserved	80	50	ICR32	460_H	$2BC_H$	$000FFEBC_H$	68
Reserved	81	51			$2B8_H$	$000FFEB8_H$	69
Reserved	82	52	ICR33	461_H	$2B4_H$	$000FFEB4_H$	70
Reserved	83	53			$2B0_H$	$000FFEB0_H$	71
Reserved	84	54	ICR34	462_H	$2AC_H$	$000FFEAC_H$	72
Reserved	85	55			$2A8_H$	$000FFEA8_H$	73
Reserved	86	56	ICR35	463_H	$2A4_H$	$000FFEA4_H$	74
Reserved	87	57			$2A0_H$	$000FFEA0_H$	75
Reserved	88	58	ICR36	464_H	$29C_H$	$000FFE9C_H$	76
Reserved	89	59			298_H	$000FFE98_H$	77
Reserved	90	5A	ICR37	465_H	294_H	$000FFE94_H$	78
Reserved	91	5B			290_H	$000FFE90_H$	79
Input Capture 0	92	5C	ICR38	466_H	$28C_H$	$000FFE8C_H$	80
Input Capture 1	93	5D			288_H	$000FFE88_H$	81
Input Capture 2	94	5E	ICR39	467_H	284_H	$000FFE84_H$	82
Input Capture 3	95	5F			280_H	$000FFE80_H$	83

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Deci-mal	Hexa-de cimal	Setting Register	Register address	Offset	Default Vector address	
Input Capture 4	96	60	ICR40	468_H	$27C_H$	$000FFE7C_H$	84
Input Capture 5	97	61			278_H	$000FFE78_H$	85
Input Capture 6	98	62	ICR41	469_H	274_H	$000FFE74_H$	86
Input Capture 7	99	63			270_H	$000FFE70_H$	87
Output Compare 0	100	64	ICR42	$46A_H$	$26C_H$	$000FFE6C_H$	88
Output Compare 1	101	65			268_H	$000FFE68_H$	89
Output Compare 2	102	66	ICR43	$46B_H$	264_H	$000FFE64_H$	90
Output Compare 3	103	67			260_H	$000FFE60_H$	91
Output Compare 4	104	68	ICR44	$46C_H$	$25C_H$	$000FFE5C_H$	92
Output Compare 5	105	69			258_H	$000FFE58_H$	93
Output Compare 6	106	6A	ICR45	$46D_H$	254_H	$000FFE54_H$	94
Output Compare 7	107	6B			250_H	$000FFE50_H$	95
Reserved	108	6C	ICR46	$46E_H$	$24C_H$	$000FFE4C_H$	-
Reserved	109	6D			248_H	$000FFE48_H$	-
System reserved	110	6E	ICR47 [3]	$46F_H$	244_H	$000FFE44_H$	-
System reserved	111	6F			240_H	$000FFE40_H$	-
PPG0	112	70	ICR48	470_H	$23C_H$	$000FFE3C_H$	15, 96
PPG1	113	71			238_H	$000FFE38_H$	97
PPG2	114	72	ICR49	471_H	234_H	$000FFE34_H$	98
PPG3	115	73			230_H	$000FFE30_H$	99
PPG4	116	74	ICR50	472_H	$22C_H$	$000FFE2C_H$	100
PPG5	117	75			228_H	$000FFE28_H$	101
PPG6	118	76	ICR51	473_H	224_H	$000FFE24_H$	102
PPG7	119	77			220_H	$000FFE20_H$	103
PPG8	120	78	ICR52	474_H	$21C_H$	$000FFE1C_H$	104
PPG9	121	79			218_H	$000FFE18_H$	105
PPG10	122	7A	ICR53	475_H	214_H	$000FFE14_H$	106
PPG11	123	7B			210_H	$000FFE10_H$	107
Reserved	124	7C	ICR54	476_H	$20C_H$	$000FFE0C_H$	108
Reserved	125	7D			208_H	$000FFE08_H$	109
Reserved	126	7E	ICR55	477_H	204_H	$000FFE04_H$	110
Reserved	127	7F			200_H	$000FFE00_H$	111

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-de cimal	Setting Register	Register address	Offset	Default Vector address	
Reserved	128	80	ICR56	478_H	$1FC_H$	$000FFDFC_H$	-
Reserved	129	81			$1F8_H$	$000FFDF8_H$	-
Reserved	130	82	ICR57	479_H	$1F4_H$	$000FFDF4_H$	-
Reserved	131	83			$1F0_H$	$000FFDF0_H$	-
Real Time Clock	132	84	ICR58	$47A_H$	$1EC_H$	$000FFDEC_H$	-
Calibration Unit	133	85			$1E8_H$	$000FFDE8_H$	-
A/D Converter 0	134	86	ICR59	$47B_H$	$1E4_H$	$000FFDE4_H$	14, 112
Reserved	135	87			$1E0_H$	$000FFDE0_H$	-
Reserved	136	88	ICR60	$47C_H$	$1DC_H$	$000FFDDC_H$	-
Reserved	137	89			$1D8_H$	$000FFDD8_H$	-
Low Voltage Detection	138	8A	ICR61	$47D_H$	$1D4_H$	$000FFDD4_H$	-
Reserved	139	8B			$1D0_H$	$000FFDD0_H$	-
Timebase Overflow	140	8C	ICR62	$47E_H$	$1CC_H$	$000FFDCC_H$	-
PLL Clock Gear	141	8D			$1C8_H$	$000FFDC8_H$	-
DMA Controller	142	8E	ICR63	$47F_H$	$1C4_H$	$000FFDC4_H$	-
Main/Sub OSC stability wait	143	8F			$1C0_H$	$000FFDC0_H$	-
Security vector	144	90	-	-	$1BC_H$	$000FFDBC_H$	-
Used by the INT instruction.	145 to 255	91 to FF	-	-	$1B8_H$ to 000_H	$000FFDB8_H$ to $000FFC00_H$	-

1. The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

2. The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value ($000FFC00_H$) . The TBR is initialized to this value by a reset. The TBR is set to $000FFC00_H$ after the internal boot ROM is executed.

3. ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr $0C03_H$: IOS[0])

4. Used by REALOS

5. Memory Protection Unit (MPU) support

14. Recommended Settings

14.1 PLL and Clockgear settings

Please note that for MB91F465Kx, the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash.

Table 5: Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	[1]
4	2	24	16	24	192	96	[1]
4	2	23	16	24	184	92	[1]
4	2	22	16	24	176	88	[1]
4	2	21	16	20	168	84	[1]
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

1. This setting is not possible at MB91F465Kx

14.2 Clock Modulator Settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 48MHz. Base clock frequencies above 48 MHz are not allowed on MB91F465Kx.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Table 6: Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F	48	44.2	52.5	
1	5	02AE	48	41.8	56.4	
1	7	02ED	48	39.6	60.9	
1	9	032C	48	37.7	66.1	
1	11	036B	48	35.9	72.3	
1	13	03AA	48	34.3	79.9	
1	15	03E9	48	32.8	89.1	[1]
2	3	046E	48	41.8	56.4	
2	5	04AC	48	37.7	66.1	
2	7	04EA	48	34.3	79.9	
3	3	066D	48	39.6	60.9	
3	5	06AA	48	34.3	79.9	
4	3	086C	48	37.7	66.1	
5	3	0A6B	48	35.9	72.3	
6	3	0C6A	48	34.3	79.9	
7	3	0E69	48	32.8	89.1	[1]
1	3	026F	44	40.6	48.1	
1	5	02AE	44	38.4	51.6	
1	7	02ED	44	36.4	55.7	
1	9	032C	44	34.6	60.4	
1	11	036B	44	33	66.1	
1	13	03AA	44	31.5	73	
1	15	03E9	44	30.1	81.4	[1]
2	3	046E	44	38.4	51.6	
2	5	04AC	44	34.6	60.4	
2	7	04EA	44	31.5	73	
2	9	0528	44	28.9	92.1	[1]

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
3	3	066D	44	36.4	55.7	
3	5	06AA	44	31.5	73	
4	3	086C	44	34.6	60.4	
4	5	08A8	44	28.9	92.1	[1]
5	3	0A6B	44	33	66.1	
6	3	0C6A	44	31.5	73	
7	3	0E69	44	30.1	81.4	[1]
8	3	1068	44	28.9	92.1	[1]
1	3	026F	40	37	43.6	
1	5	02AE	40	34.9	46.8	
1	7	02ED	40	33.1	50.5	
1	9	032C	40	31.5	54.8	
1	11	036B	40	30	59.9	
1	13	03AA	40	28.7	66.1	
1	15	03E9	40	27.4	73.7	
2	3	046E	40	34.9	46.8	
2	5	04AC	40	31.5	54.8	
2	7	04EA	40	28.7	66.1	
2	9	0528	40	26.3	83.3	[1]
3	3	066D	40	33.1	50.5	
3	5	06AA	40	28.7	66.1	
3	7	06E7	40	25.3	95.8	[1]
4	3	086C	40	31.5	54.8	
4	5	08A8	40	26.3	83.3	[1]
5	3	0A6B	40	30	59.9	
6	3	0C6A	40	28.7	66.1	
7	3	0E69	40	27.4	73.7	
8	3	1068	40	26.3	83.3	[1]
9	3	1267	40	25.3	95.8	[1]
1	3	026F	36	33.3	39.2	
1	5	02AE	36	31.5	42	
1	7	02ED	36	29.9	45.3	
1	9	032C	36	28.4	49.2	
1	11	036B	36	27.1	53.8	
1	13	03AA	36	25.8	59.3	

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	15	03E9	36	24.7	66.1	
2	3	046E	36	31.5	42	
2	5	04AC	36	28.4	49.2	
2	7	04EA	36	25.8	59.3	
2	9	0528	36	23.7	74.7	
3	3	066D	36	29.9	45.3	
3	5	06AA	36	25.8	59.3	
3	7	06E7	36	22.8	85.8	[1]
4	3	086C	36	28.4	49.2	
4	5	08A8	36	23.7	74.7	
5	3	0A6B	36	27.1	53.8	
6	3	0C6A	36	25.8	59.3	
7	3	0E69	36	24.7	66.1	
8	3	1068	36	23.7	74.7	
9	3	1267	36	22.8	85.8	[1]
1	3	026F	32	29.7	34.7	
1	5	02AE	32	28	37.3	
1	7	02ED	32	26.6	40.2	
1	9	032C	32	25.3	43.6	
1	11	036B	32	24.1	47.7	
1	13	03AA	32	23	52.5	
1	15	03E9	32	22	58.6	
2	3	046E	32	28	37.3	
2	5	04AC	32	25.3	43.6	
2	7	04EA	32	23	52.5	
2	9	0528	32	21.1	66.1	
2	11	0566	32	19.5	89.1	[1]
3	3	066D	32	26.6	40.2	
3	5	06AA	32	23	52.5	
3	7	06E7	32	20.3	75.9	
4	3	086C	32	25.3	43.6	
4	5	08A8	32	21.1	66.1	
5	3	0A6B	32	24.1	47.7	
5	5	0AA6	32	19.5	89.1	[1]
6	3	0C6A	32	23	52.5	

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
7	3	0E69	32	22	58.6	
8	3	1068	32	21.1	66.1	
9	3	1267	32	20.3	75.9	
10	3	1466	32	19.5	89.1	[1]

1. These settings are not possible at MB91F465Kx

15. Electrical Characteristics

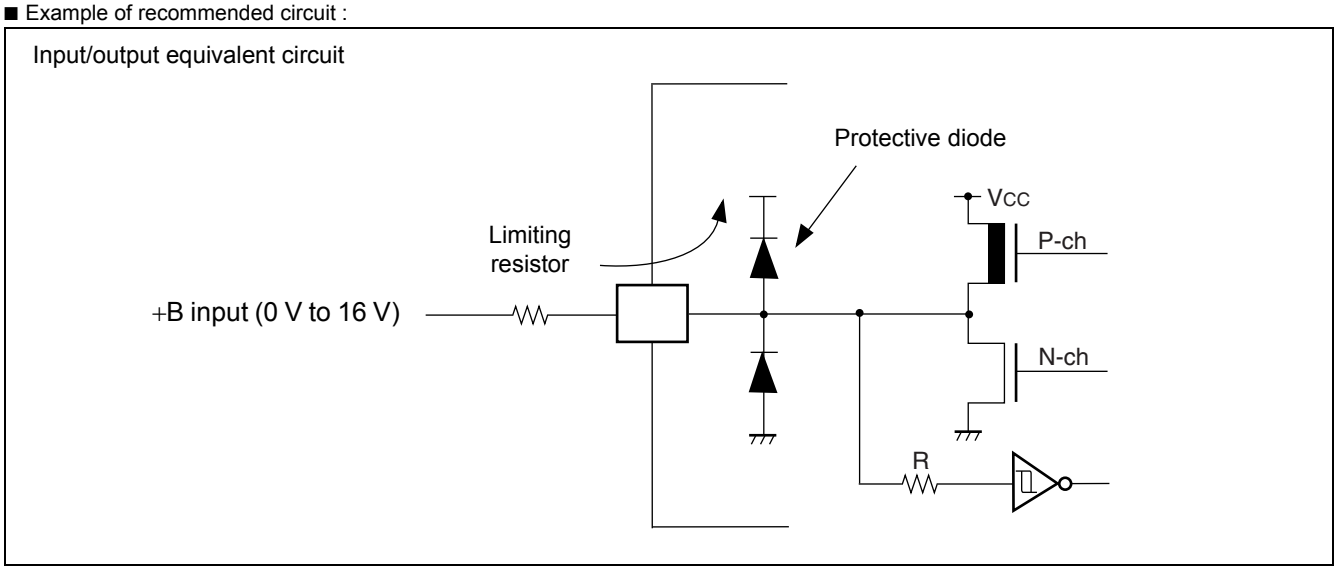
15.1 Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	-	-	50	V/ms	
Power supply voltage 1[1]	$V_{DD}5R$	− 0.3	+ 6.0	V	
Power supply voltage 2[1]	$V_{DD}5$	− 0.3	+ 6.0	V	
Relationship of the supply voltages	$AV_{CC}5$	$V_{DD}5$-0.3	$V_{DD}5$+0.3	V	At least one pin of the Ports 25 to 29 (ANn) is used as digital input or output
		$V_{SS}5$-0.3	$V_{DD}5$+0.3	V	All pins of the Ports 25 to 29 (ANn) follow the condition of V_{IA}
Analog power supply voltage[1]	$AV_{CC}5$	− 0.3	+ 6.0	V	[2]
Analog reference power supply voltage[1]	AVRH5	− 0.3	+ 6.0	V	[2]
Input voltage 1[1]	V_{I1}	Vss5 − 0.3	$V_{DD}5$ + 0.3	V	
Analog pin input voltage[1]	V_{IA}	AVss5 − 0.3	AVcc5 + 0.3	V	
Output voltage 1[1]	V_{O1}	Vss5 − 0.3	$V_{DD}5$ + 0.3	V	
Maximum clamp current	I_{CLAMP}	− 4.0	+ 4.0	mA	[3]
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	-	20	mA	[3]
"L" level maximum output current[4]	I_{OL}	-	10	mA	
"L" level average output current[5]	I_{OLAV}	-	8	mA	
"L" level total maximum output current	ΣI_{OL}	-	100	mA	
"L" level total average output current[6]	ΣI_{OLAV}	-	50	mA	
"H" level maximum output current[4]	I_{OH}	-	− 10	mA	
"H" level average output current[5]	I_{OHAV}	-	− 4	mA	
"H" level total maximum output current	ΣI_{OH}	-	− 100	mA	
"H" level total average output current[6]	ΣI_{OHAV}	-	− 25	mA	
Power consumption	P_D	-	500	mW	at T_A = 105°C
Operating temperature	T_A	− 40	+ 105	°C	
Storage temperature	Tstg	− 55	+ 150	°C	

1. The parameter is based on $V_{SS}5 = AV_{SS}5 = 0.0$ V.
2. $AV_{CC}5$ and AVRH5 must not exceed $V_{DD}5 + 0.3$ V
3.

- Use within recommended operating conditions.
- Use with DC voltage (current).
- B signals are input signals that exceed the $V_{DD}5$ voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.

- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time , either instantaneously or for an extended period, when the +B signal is input
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.
- Example of recommended circuit :



4. Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins

5. Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

6. Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

15.2 Recommended Operating Conditions

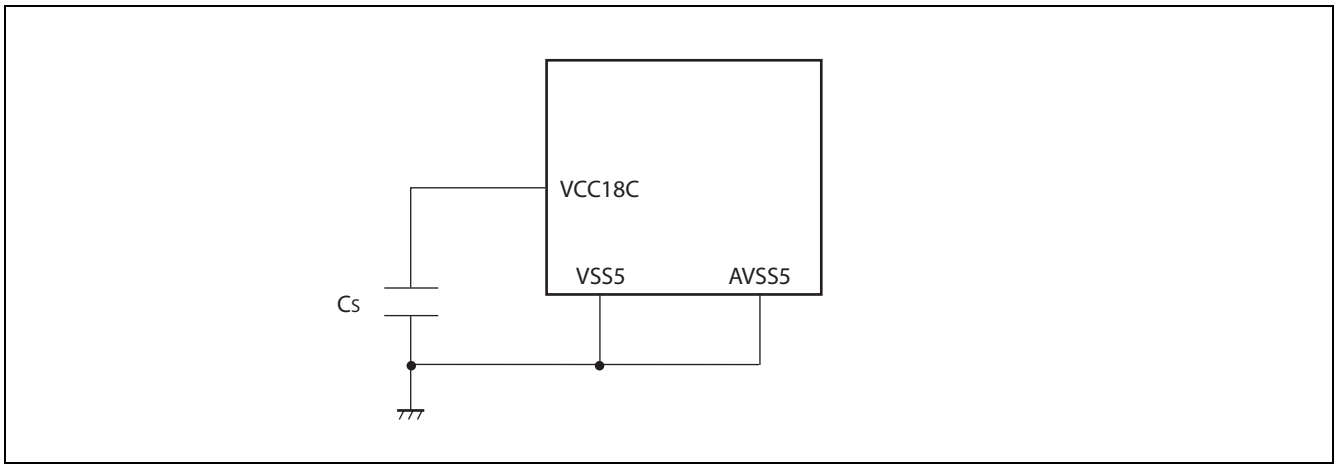
($V_{SS}5 = AV_{SS}5 = 0.0$ V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{DD}5$	3.0	-	5.5	V	
	$V_{DD}5R$	3.0	-	5.5	V	Internal regulator
	$AV_{CC}5$	3.0	-	5.5	V	A/D converter
Smoothing capacitor at VCC18C pin	C_S	-	4.7	-	µF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.
Power supply slew rate		-	-	50	V/ms	
Operating temperature	T_A	− 40	-	+ 105	°C	
Main Oscillation stabilisation time		10			ms	
Lock-up time PLL (4 MHz ->16 ...100MHz)				0.6	ms	
ESD Protection (Human body model)	V_{surge}	2			kV	$R_{discharge}$ = 1.5kΩ $C_{discharge}$ = 100pF
RC Oscillator	$f_{RC100kHz}$	50	100	200	kHz	$VDD_{CORE} \geq 1.65V$
	f_{RC2MHz}	1	2	4	MHz	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



15.3 DC Characteristics

Note: In the following tables, "V_{DD}" means $V_{DD}5$ for all pins.

In the following tables, "V_{SS}" means $V_{SS}5$ for all pins.

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40°C$ to $+105°C$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$0.8 \times V_{DD}$	-	$V_{DD} + 0.3$	V	CMOS hysteresis input
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$0.7 \times V_{DD}$	-	$V_{DD} + 0.3$	V	$4.5\ V \le V_{DD} \le 5.5\ V$
				$0.74 \times V_{DD}$	-	$V_{DD} + 0.3$	V	$3\ V \le V_{DD} < 4.5\ V$
		-	AUTOMOTIVE Hysteresis input is selected	$0.8 \times V_{DD}$	-	$V_{DD} + 0.3$	V	
		-	Port inputs if TTL input is selected	2.0	-	$V_{DD} + 0.3$	V	
	V_{IHR}	INITX	-	$0.8 \times V_{DD}$	-	$V_{DD} + 0.3$	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_2 to MD_0	-	$V_{DD} - 0.3$	-	$V_{DD} + 0.3$	V	Mode input pins
	V_{IHX0S}	X0, X0A	-	2.5	-	$V_{DD} + 0.3$	V	External clock in "Oscillation mode"
	V_{IHX0F}	X0	-	$0.8 \times V_{DD}$	-	$V_{DD} + 0.3$	V	External clock in "Fast Clock Input mode"
Input "L" voltage	V_{IL}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$V_{SS} - 0.3$	-	$0.2 \times V_{DD}$	V	
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$V_{SS} - 0.3$	-	$0.3 \times V_{DD}$	V	
		-	Port inputs if AUTOMOTIVE Hysteresis input is selected	$V_{SS} - 0.3$	-	$0.5 \times V_{DD}$	V	$4.5\ V \le V_{DD} \le 5.5\ V$
				$V_{SS} - 0.3$	-	$0.46 \times V_{DD}$	V	$3\ V \le V_{DD} < 4.5\ V$
		-	Port inputs if TTL input is selected	$V_{SS} - 0.3$	-	0.8	V	
	V_{ILR}	INITX	-	$V_{SS} - 0.3$	-	$0.2 \times V_{DD}$	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_2 to MD_0	-	$V_{SS} - 0.3$	-	$V_{SS} + 0.3$	V	Mode input pins
	V_{ILXDS}	X0, X0A	-	$V_{SS} - 0.3$	-	0.5	V	External clock in "Oscillation mode"

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40°C$ to $+105°C$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "L" voltage	V_{ILXDF}	X0	-	$V_{SS} - 0.3$	-	$0.2 \times V_{DD}$	V	External clock in "Fast Clock Input mode"
Output "H" voltage	V_{OH2}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OH} = -2mA$	$V_{DD} - 0.5$	-	-	V	Driving strength set to 2 mA
			$3.0V \le V_{DD} \le 4.5V$, $I_{OH} = -1.6mA$					
	V_{OH5}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OH} = -5mA$	$V_{DD} - 0.5$	-	-	V	Driving strength set to 5 mA
			$3.0V \le V_{DD} \le 4.5V$, $I_{OH} = -3mA$					
	V_{OH3}	I^2C outputs	$3.0V \le V_{DD} \le 5.5V$, $I_{OH} = -3mA$	$V_{DD} - 0.5$	-	-	V	
Output "L" voltage	V_{OL2}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OL} = +2mA$	-	-	0.4	V	Driving strength set to 2 mA
			$3.0V \le V_{DD} \le 4.5V$, $I_{OL} = +1.6mA$					
	V_{OL5}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, $I_{OL} = +5mA$	-	-	0.4	V	Driving strength set to 5 mA
			$3.0V \le V_{DD} \le 4.5V$, $I_{OL} = +3mA$					
	V_{OL3}	I^2C outputs	$3.0V \le V_{DD} \le 5.5V$, $I_{OL} = +3mA$	-	-	0.4	V	
Input leakage current	I_{IL}	Pnn_m [1]	$3.0V \le V_{DD} \le 5.5V$ T_A=25 ·C	-1	-	$+1$	µA	$V_{SS}5 < V_I < V_{DD}$
			$3.0V \le V_{DD} \le 5.5V$ T_A=105 ·C	-3	-	$+3$	µA	
Analog input leakage current	I_{AIN}	ANn [2]	$3.0V \le V_{DD} \le 5.5V$ T_A=25 ·C	-1	-	$+1$	µA	$AV_{SS}5 < V_I < AV_{CC}5$, AVRH5
			$3.0V \le V_{DD} \le 5.5V$ T_A=105 ·C	-3	-	$+3$	µA	

1. Pnn_m includes all GPIO pins. Analog (AN) channels and Pull-Up/Pull-Down are disabled.
2. ANn includes all pins where AN channels are enabled.

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40°C$ to $+105°C$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-up resistance	R_{UP}	Pnn_m [1] INITX	$3.0V \le V_{DD} \le 3.6V$	40	100	160	kΩ	
			$4.5V \le V_{DD} \le 5.5V$	25	50	100		
Pull-down resistance	R_{DOWN}	Pnn_m[2]	$3.0V \le V_{DD} \le 3.6V$	40	100	180	kΩ	
			$4.5V \le V_{DD} \le 5.5V$	25	50	100		
Input capacitance	C_{IN}	All except $V_{DD}5$, $V_{DD}5R$, $V_{SS}5$, $AV_{CC}5$, $AV_{SS}5$, AVRH5	f = 1 MHz	-	5	15	pF	
Power supply current MB91F-465Kx	I_{CC}	$V_{DD}5R$	CLKB: 80 MHz CLKP: 40 MHz CLKT: 40 MHz CLKCAN: 40 MHz	-	80	90	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$	$T_A = +25°C$	-	30	150	μA	At stop mode [3]
			$T_A = +105°C$	-	400	2000	μA	
			$T_A = +25°C$	-	100	500	μA	RTC : 4 MHz mode [3]
			$T_A = +105°C$	-	500	2400	μA	
			$T_A = +25°C$	-	50	250	μA	RTC : 100 kHz mode [3] 32 kHz mode [4]
			$T_A = +105°C$	-	450	2200	μA	
	I_{LVE}	$V_{DD}5$	-	-	70	150	μA	External low voltage detection
	I_{LVI}	$V_{DD}5R$	-	-	50	100	μA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	-	-	250	500	μA	Main clock (4 MHz)
			-	-	20	40	μA	Sub clock (32 kHz)

1. Pnn_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
2. Pnn_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
3. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled.
4. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled, RC oscillator enabled. Additional current consumption of Sub oscillator IOSC has to be taken into account

15.4 A/D Converter Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40°C$ to $+105°C$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	– 3	-	+ 3	LSB	
Nonlinearity error	-	-	– 2.5	-	+ 2.5	LSB	
Differential nonlinearity error	-	-	– 1.9	-	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL– 1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH– 3.5 LSB	AVRH– 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	T_{comp}	-	0.6	-	16,500	µs	$4.5 V \le AV_{CC}5 \le 5.5 V$
			2.0	-	-	µs	$3.0 V \le AV_{CC}5 \le 4.5 V$
Sampling time	T_{samp}	-	0.4	-	-	µs	$4.5 V \le AV_{CC}5 \le 5.5 V$, $R_{EXT} < 2 k\Omega$
			1.0	-	-	µs	$3.0 V \le AV_{CC}5 \le 4.5 V$, $R_{EXT} < 1 k\Omega$
Conversion time	T_{conv}	-	1.0	-	-	µs	$4.5 V \le AV_{CC}5 \le 5.5 V$
			3.0	-	-	µs	$3.0 V \le AV_{CC}5 \le 4.5 V$
Input capacitance	C_{IN}	ANn	-	-	11	pF	
Input resistance	R_{IN}	ANn	-	-	2.6	kΩ	$4.5 V \le AV_{CC}5 \le 5.5 V$
			-	-	12.1	kΩ	$3.0 V \le AV_{CC}5 \le 4.5 V$
Analog input leakage current	I_{AIN}	ANn	– 1	-	+ 1	µA	$T_A = +25°C$
			– 3	-	+ 3	µA	$T_A = +105°C$
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as AVRH - AVRL becomes smaller

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	$0.75 \times AV_{CC}5$	-	$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$	-	$AV_{CC}5 \times 0.25$	V	
Power supply current	I_A	$AV_{CC}5$	-	2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$	-	-	5	μA	A/D Converter not operated [1]
Reference voltage current	I_R	AVRH5	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5	-	-	5	μA	A/D Converter not operated [2]

1. Supply current at $AV_{CC}5$, if the A/D converter is not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)
2. Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

Sampling Time Calculation

$T_{samp} = (2.6\ kOhm + R_{EXT}) \times 11pF \times 7$; for $4.5V \le AV_{CC}5 \le 5.5V$

$T_{samp} = (12.1\ kOhm + R_{EXT}) \times 11pF \times 7$; for $3.0V \le AV_{CC}5 \le 4.5V$

Conversion Time Calculation

$T_{conv} = T_{samp} + T_{comp}$

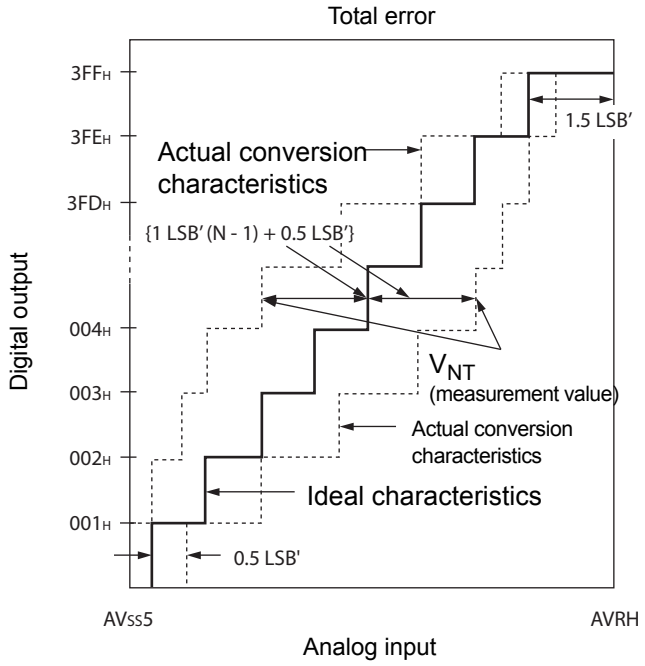
15.4.1 Definition of A/D Converter Terms

■ Resolution
Analog variation that is recognizable by the A/D converter.

■ Nonlinearity error
Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).

■ Differential nonlinearity error
Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.

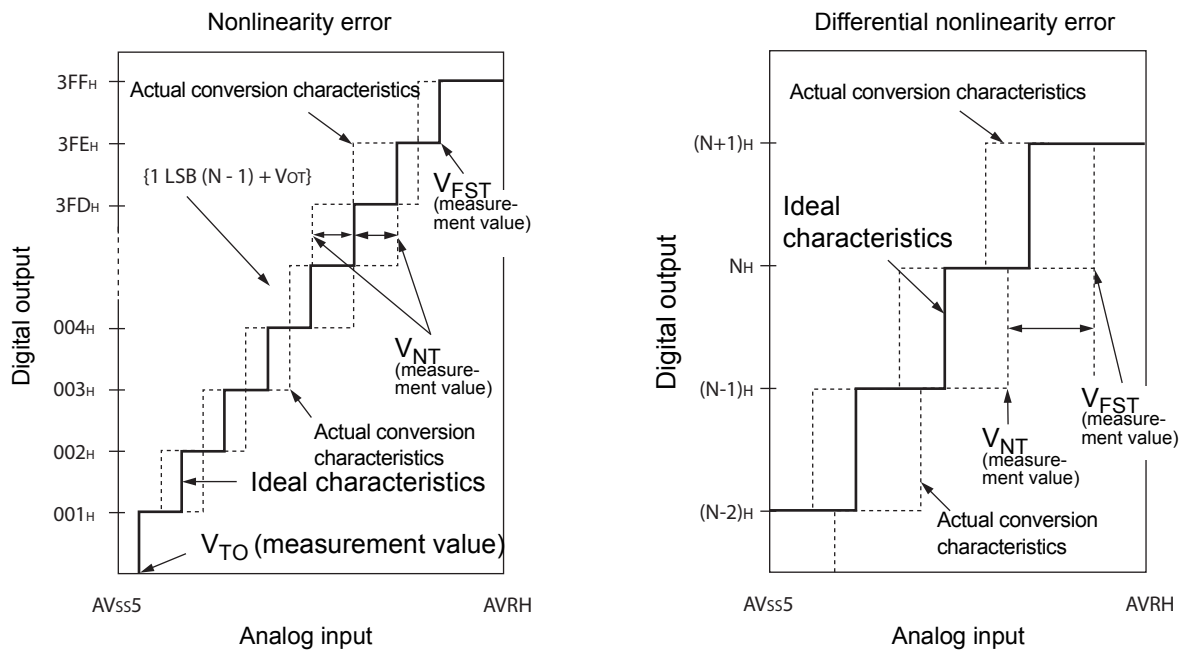
■ Total error
This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.



$$1LSB'\ (\text{ideal value}) = \frac{AVRH - AV_{SS}5}{1024}\ [V]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N: A/D converter digital output value
V_{OT}' (ideal value) = $AV_{SS}5 + 0.5\ LSB'$ [V]
V_{FST}' (ideal value) = $AVRH - 1.5\ LSB'$ [V]
V_{NT}: Voltage at which the digital output changes from $(N + 1)_H$ to N_H



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N-1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N: A/D converter digital output value
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST}: Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

15.5 Flash Memory Program/erase Characteristics

15.5.1 MB91F465Kx

(T_A = 25°C, Vcc = 5.0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erasure programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	-	23	370	μs	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	[1]

1. This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

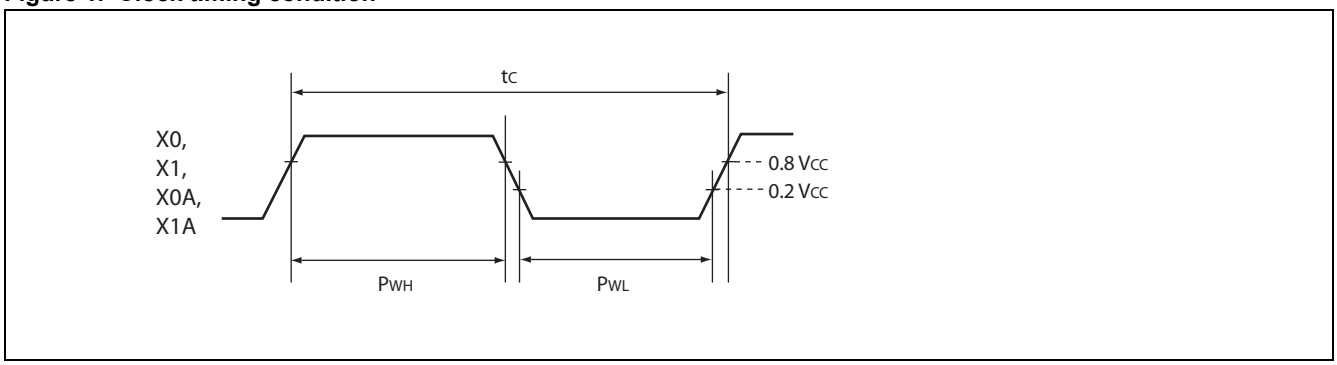
15.6 AC Characteristics

15.6.1 Clock timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

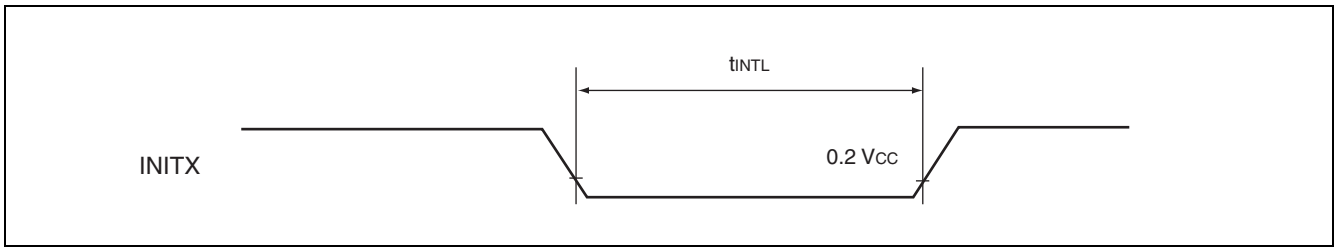
Figure 1. Clock timing condition



15.6.2 Reset Input Ratings

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time(at power-on)	t_{INTL}	INITX	-	10	-	ms
INITX input time(other than the above)				20	-	µs



15.6.3 LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements
- All AC tests were measured under the following conditions:
  - ❒ - IO_{drive} = 5 mA
  - ❒ - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
  - ❒ - $V_{SS}5$ = 0 V
  - ❒ - T_A = -40°C to +105°C
  - ❒ - C_l = 50 pF (load capacity value of pins when testing)
  - ❒ - V_{OL} = 0.2 x $V_{DD}5$
  - ❒ - V_{OH} = 0.8 x $V_{DD}5$
  - ❒ - EPILR = 0, PILR = 1 (Automotive Level == worst case)

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	$V_{DD}5$ = 3.0 V to 4.5 V		$V_{DD}5$ = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	4 t_{CLKP}	-	4 t_{CLKP}	-	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCKn SOTn		– 30	30	– 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn		m × t_{CLKP} – 30[1]	-	m × t_{CLKP} – 20[1]	-	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55	-	t_{CLKP} + 45	-	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCKn SINn		0	-	0	-	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
Serial clock“L” pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
SCK ↓→ SOT delay time	t_{SLOVE}	SCKn SOTn		-	2 t_{CLKP} + 55	-	2 t_{CLKP} + 45	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	-	10	-	ns
SCK ↑→ valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
SCK rising time	t_{FE}	SCKn		-	20	-	20	ns
SCK falling time	t_{RE}	SCKn		-	20	-	20	ns

1. Parameter m depends on t_{SCYCI} and can be calculated as :

- if t_{SCYCI} = 2*k*t_{CLKP}, then m = k, where k is an integer > 2
- if t_{SCYCI} = (2*k + 1)*t_{CLKP}, then m = k + 1, where k is an integer > 1

Notes :

- The above values are AC characteristics for CLK synchronous mode.
- t_{CLKP} is the cycle time of the peripheral clock.

Figure 2. Internal clock mode (master mode)

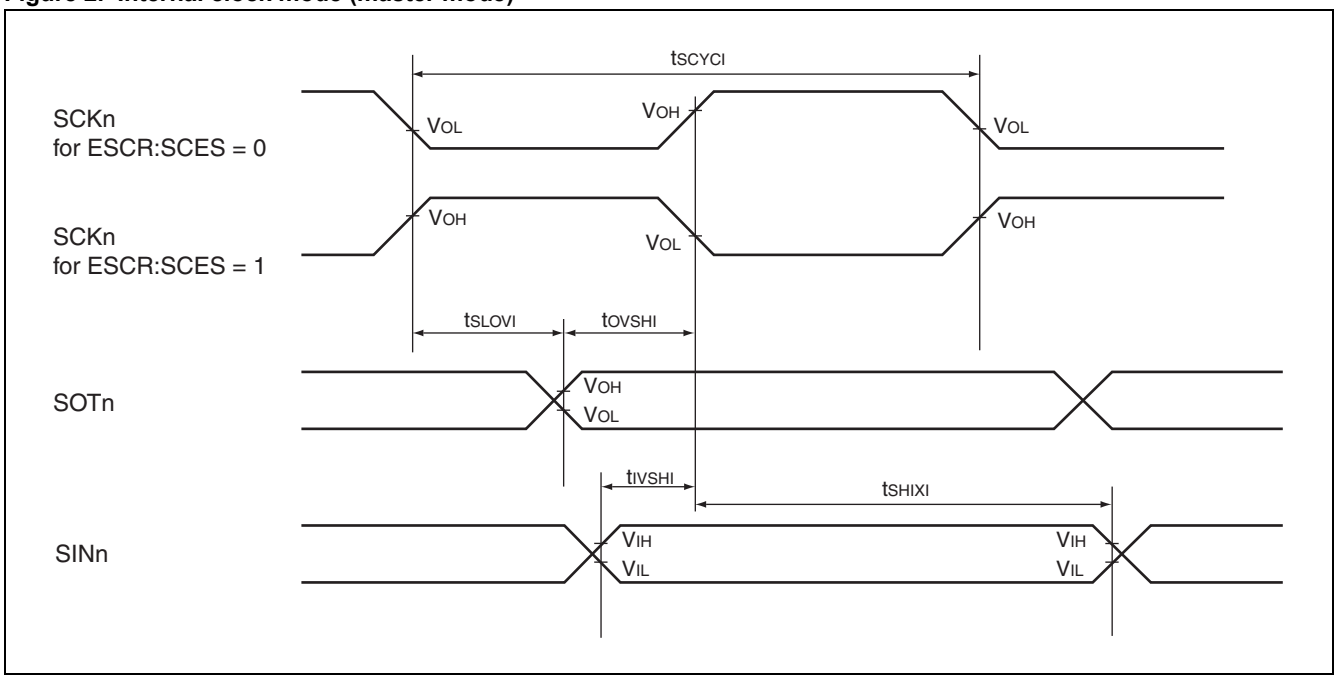
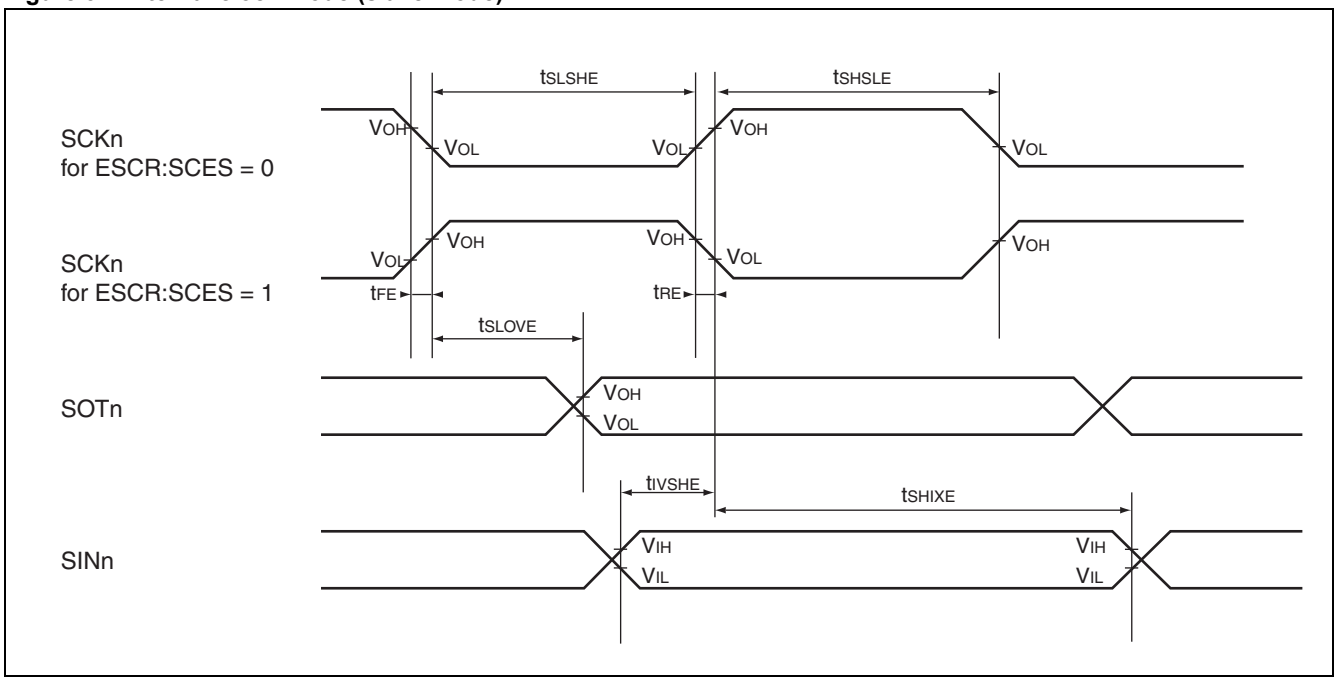


Figure 3. External clock mode (slave mode)



15.6.4 I²C AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

■ Conditions during AC measurements
All AC tests were measured under the following conditions:
- ❒ -IO_{drive} = 3 mA
- ❒ -$V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
- ❒ -$V_{SS}5$ = 0 V
- ❒ -T_A = −40°C to +105°C
- ❒ -C_l = 50 pF
- ❒ -V_{OL} = 0.3 × $V_{DD}5$
- ❒ -V_{OH} = 0.7 × $V_{DD}5$
- ❒ -EPILR = 0, PILR = 0 (CMOS Hysteresis V_{IL}/V_{IH} = 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

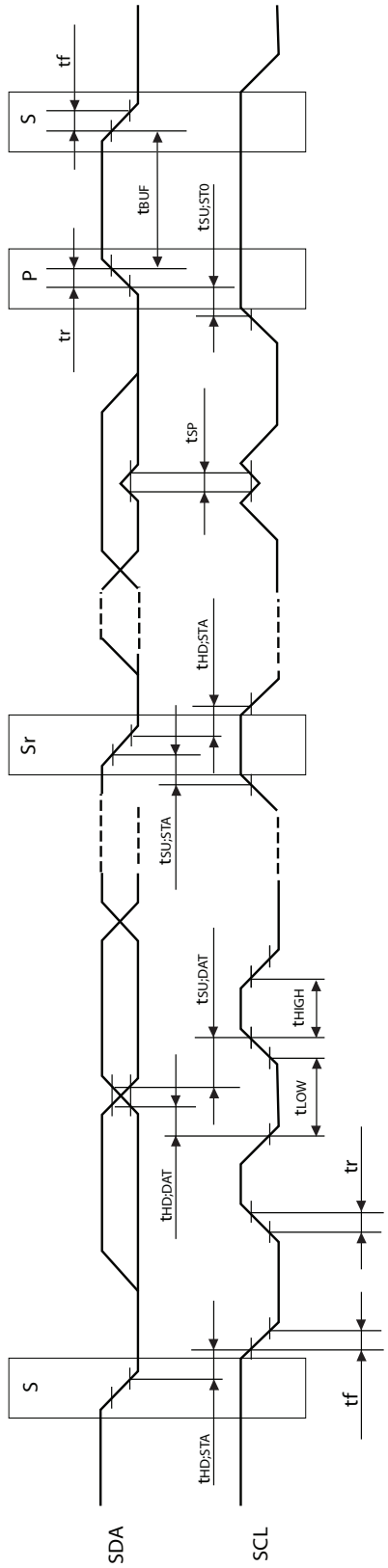
15.6.4.1 Fast Mode:

($V_{DD}5$ = 3.5 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40°C to +105°C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f_{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	SCLn, SDAn	0.6	-	µs	
LOW period of the SCL clock	t_{LOW}	SCLn	1.3	-	µs	
HIGH period of the SCL clock	t_{HIGH}	SCLn	0.6	-	µs	
Setup time for a repeated START condition	$t_{SU;STA}$	SCLn, SDAn	0.6	-	µs	
Data hold time for I²C-bus devices	$t_{HD;DAT}$	SCLn, SDAn	0	0.9	µs	
Data setup time	$t_{SU;DAT}$	SCLn SDAn	100	-	ns	
Rise time of both SDA and SCL signals	t_r	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t_f	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	$t_{SU;STO}$	SCLn, SDAn	0.6	-	µs	
Bus free time between a STOP and START condition	t_{BUF}	SCLn, SDAn	1.3	-	µs	
Capacitive load for each bus line	C_b	SCLn, SDAn	-	400	pF	
Pulse width of spike suppressed by input filter	t_{SP}	SCLn, SDAn	0	(1..1.5) × t_{CLKP}	ns	[1]

1. The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I²C signals (SDA, SCL) and peripheral clock.

Note: t_{CLKP} is the cycle time of the peripheral clock.

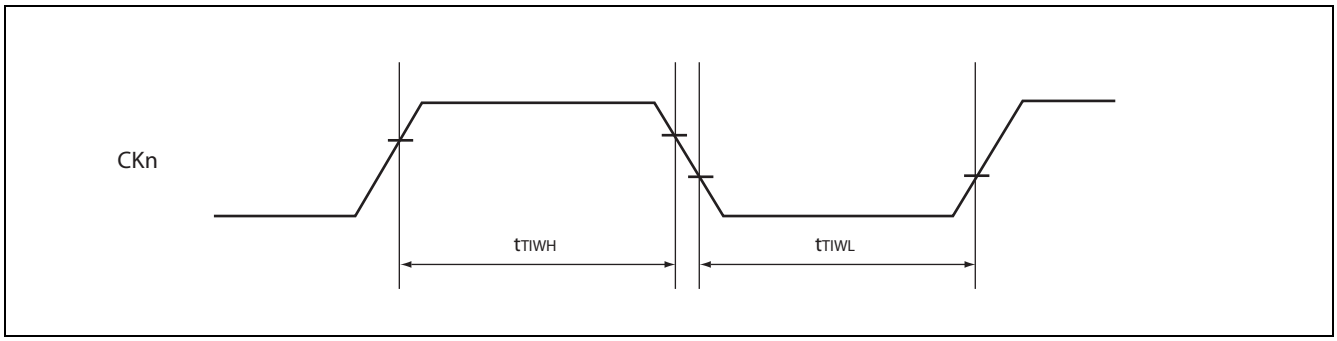

SDA
SCL
S
tHD;STA
tHD;DAT
tSU;DAT
tLOW
tr
tf
tHIGH
Sr
tSU;STA
tHD;STA
tSP
P
tr
tBUF
tSU;STO
S
tf

15.6.5 Free-Run Timer Clock

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5 = AV_{SS}5$ = 0 V, T_A = –40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	CKn	-	$4t_{CLKP}$	-	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.

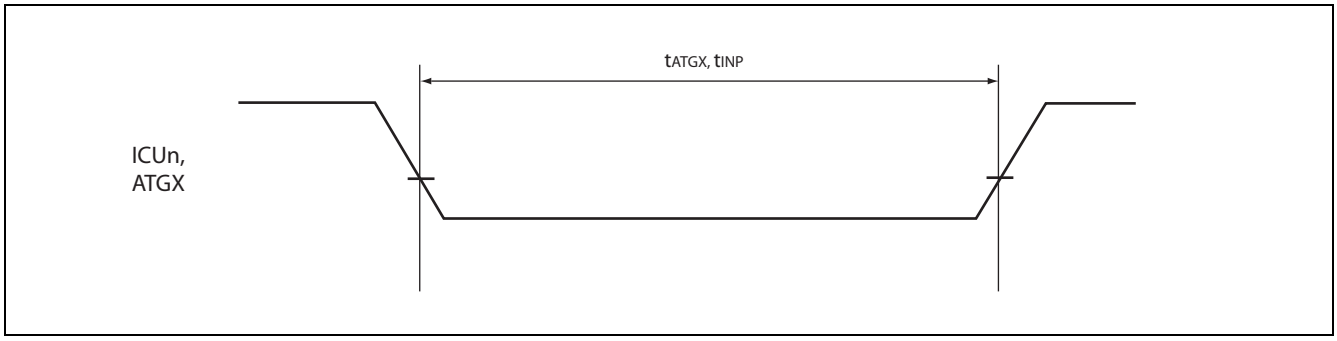


15.6.6 Trigger Input Timing

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5 = AV_{SS}5$ = 0 V, T_A = –40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICUn	-	$5t_{CLKP}$	-	ns
A/D converter trigger	t_{ATGX}	ATGX	-	$5t_{CLKP}$	-	ns

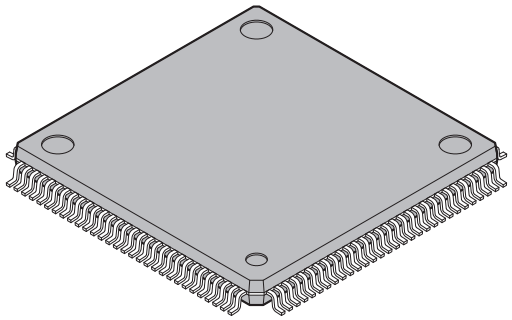
Note: t_{CLKP} is the cycle time of the peripheral clock.



16. Ordering Information

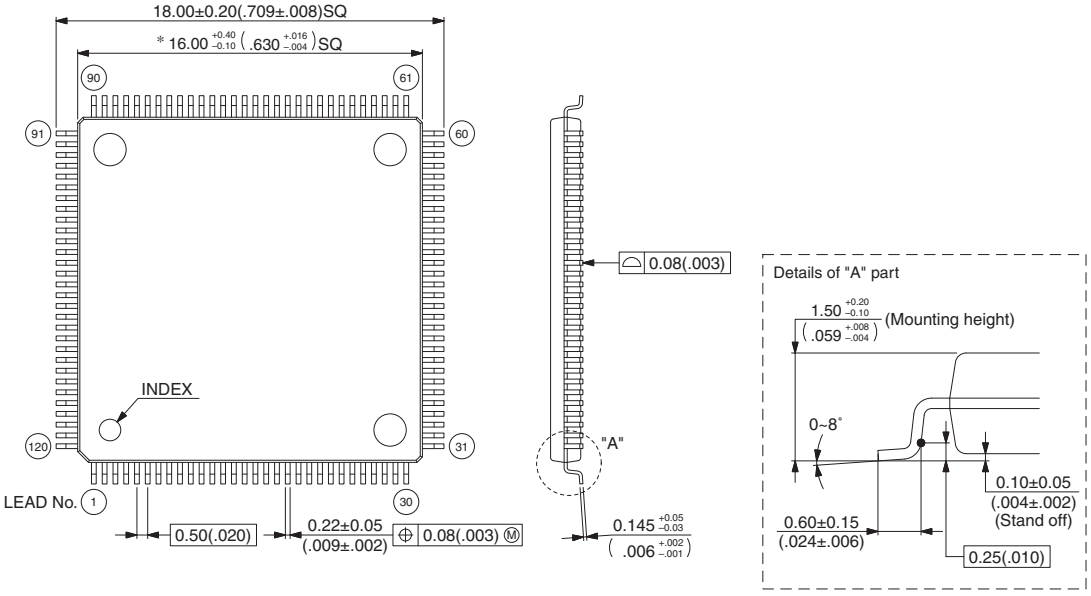
Part number	Package	Remarks
MB91F465KAPMT-GSE2	120-pin plastic LQFP (FPT-120P-M21)	not recommended
MB91F465KBPMT-GSE2		Lead-free package

17. Package Dimension

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

18. Main Changes in this Edition

Spansion Publication Number: **DS07-16606-2E**

Page	Section	Change Results
4	Product lineup	Technology in μm instead of um
4	Product lineup	Temteratur --> Temperature
6	Pin Assignment	Removed the quadratic index mark on upper left corner,Renamed "FRCKn" into "CKn" (n=0 to 7)
10	Pin Description; Power supply/Ground pins	Renamed "GND" into "ground"
18	Handling devices; Power supply pins	Corrected "capacitator" into “capacitor”
21	Block diagram	Renamed "RTC" into "Real Time Clock”,General purpose IO ports: Added "without resource"
23	Programming model	Renamed Program status register into "PS" (instead of RS)
28	Flash memory map MB91F465Kx	Changed unit "kB" into "KB"
38	I/O Map address 00010CH	Added address 00010CH (Reserved)
45	I/O Map address 0004C0H	Changed “CAN (Clock Control)” into “CAN Clock Control”
49	IO Map after address 7010_H	Changed the start address of the Reserved area after 007010_H to 007014H
53	I/O Map; Flash memory and external bus area	Corrected table header (Added "+0 +1 +2 +3")
60	Recommended Settings; Clock Modulator settings	Removed all settings for Baseclk > 48 MHz
67	Recommended operating conditions	Corrected "Look-up time PLL" into "Lock-up time PLL"
69	DC Characteristics; Output "L" voltage	Corrected condition I_{OH} into I_{OL}
70	DC Characteristics; Table foot note	Changed “PullUp/PullDown” into “Pull-Up/Pull-Down”
70	DC Characteristics; IccH	IccH (RTC mode) at 32kHz is similar to 100kHz, footnote added
71	A/D converter characteristics; Zero reading voltage, Full scale reading voltage	Corrected Values into “value +- n LSB “and Unit into “V” (Volt)
76	AC Characteristics; Reset input ratings	INITX at power-on min. 10ms (according to the Main Oscillation Stabilisation Time)
5,76,78	Ambient temperature	Changed the symbol of ambient temperature from Ta into T_A
76,78	AC Characteristics; LIN AC Timings I2C AC Timings	Corrected condition VOL into V_{OL}, VOH into V_{OH}
79	AC Characteristics; I^2C AC Timings	Corrected EPILR,PILR condition into "CMOS Hysteresis VIL/VIH =..."
82	Package Dimension	Corrected the link to package web page,Updated package drawing (latest formatting only)

NOTE: Please see “Document History” for later revised information.

Document History

Document Title: MB91F465KA, MB91F465KB, FR60 MB91460K Series, 32-bit Microcontroller Datasheet Document Number: 002-04602				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	11/11/2009	Migrated to Cypress and assigned document number 002-04602. No change to document contents or format.
*A	5200604	AKIH	04/11/2016	Updated to Cypress template

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