

# MOSFET - Power, Single N-Channel, TOLL

## 40 V, 0.67 mΩ, 240 A



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## FDBL9401-F085T6

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- Small Footprint (TOLL) for Compact Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	40	V	
Gate-to-Source Voltage	$V_{GS}$	+20/-16	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$ 240	A
		$T_C = 100^\circ\text{C}$	240	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$P_D$ 180.7	W
		$T_C = 100^\circ\text{C}$	90.3	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ 58.4	A
		$T_A = 100^\circ\text{C}$	41.3	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 4.3	W
		$T_A = 100^\circ\text{C}$	2.1	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$ 2758	A	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	138	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 45 \text{ A}, L = 1 \text{ mH}$ )	$E_{AS}$	1012	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

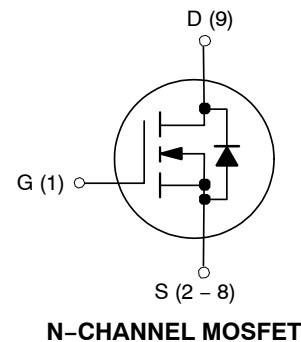
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	0.83	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	35	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Current is limited by bondwire configuration.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
40 V	0.67 mΩ @ 10 V	240 A



N-CHANNEL MOSFET



H-PSOF8L  
CASE 100CU

### ORDERING INFORMATION

Device	Package	Shipping†
FDBL9401-F085T6	H-PSOF8L (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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**Table 1. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			23.4		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\ \text{V}$ , $V_{GS} = 0\ \text{V}$	$T_J = 25^\circ\text{C}$		1	$\mu\text{A}$
			$T_J = 175^\circ\text{C}$		1	$\text{mA}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\ \text{V}$ , $V_{GS} = +20/-16\ \text{V}$			$\pm 100$	$\text{nA}$

**ON CHARACTERISTICS** (Note 4)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$ , $I_D = 290\ \mu\text{A}$	2	2.8	4	V
Threshold Temperature Coefficient	$V_{GS(th)}/T_J$			-6.5		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$ , $I_D = 50\ \text{A}$		0.6	0.67	$\text{m}\Omega$

**CHARGES, CAPACITANCES & GATE RESISTANCE**

Input Capacitance	$C_{iss}$	$V_{GS} = 0\ \text{V}$ , $V_{DS} = 25\ \text{V}$ , $f = 100\ \text{KHz}$		10000		$\text{pF}$
Output Capacitance	$C_{oss}$			5100		$\text{pF}$
Reverse Transfer Capacitance	$C_{rss}$			177		$\text{pF}$
Gate Resistance	$R_g$	$V_{GS} = 0.5\ \text{V}$ , $f = 1\ \text{MHz}$		2.1		$\Omega$
Total Gate Charge	$Q_{G(tot)}$	$V_{GS} = 10\ \text{V}$ , $V_{DS} = 20\ \text{V}$ , $I_D = 50\ \text{A}$		148		$\text{nC}$
Threshold Gate Charge	$Q_{G(th)}$	$V_{GS} = 0\ \text{to}\ 2\ \text{V}$		18		$\text{nC}$
Gate-to-Source Gate Charge	$Q_{gs}$	$V_{DD} = 32\ \text{V}$ , $I_D = 50\ \text{A}$		42		$\text{nC}$
Gate-to-Drain "Miller" Charge	$Q_{gd}$			30		$\text{nC}$
Plateau Voltage	$V_{GP}$			4.5		V

**SWITCHING CHARACTERISTICS** (Note 5)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\ \text{V}$ , $V_{DD} = 20\ \text{V}$ , $I_D = 50\ \text{A}$ , $R_{GEN} = 6\ \Omega$		37		$\text{ns}$
Turn-On Rise Time	$t_r$			76		$\text{ns}$
Turn-Off Delay Time	$t_{d(off)}$			133		$\text{ns}$
Turn-Off Fall Time	$t_f$			65		$\text{ns}$

**DRAIN-SOURCE DIODE CHARACTERISTICS**

Source-to-Drain Diode Voltage	$V_{SD}$	$I_{SD} = 50\ \text{A}$ , $V_{GS} = 0\ \text{V}$		0.77	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_{GS} = 0\ \text{V}$ , $dI_S/dt = 100\ \text{A}/\mu\text{s}$ , $I_S = 50\ \text{A}$		97		$\text{ns}$
Charge Time	$t_a$			37		$\text{ns}$
Discharge Time	$t_b$			60		$\text{ns}$
Reverse Recovery Charge	$Q_{rr}$			218		$\text{nC}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

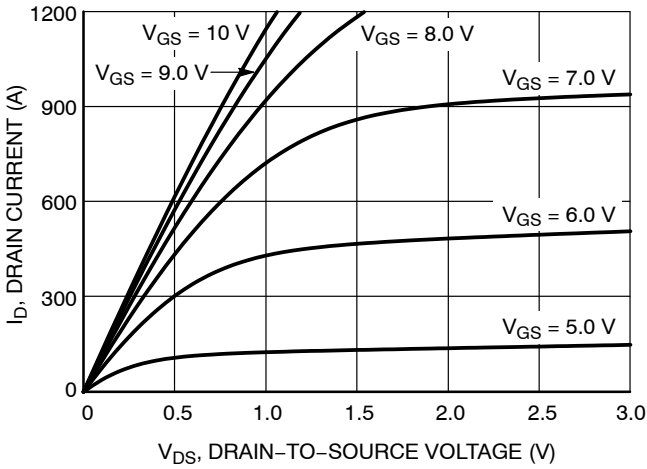


Figure 1. On-Region Characteristics

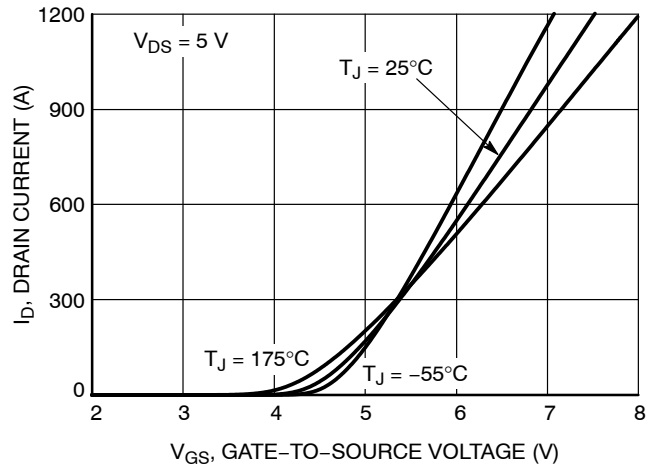


Figure 2. Transfer Characteristics

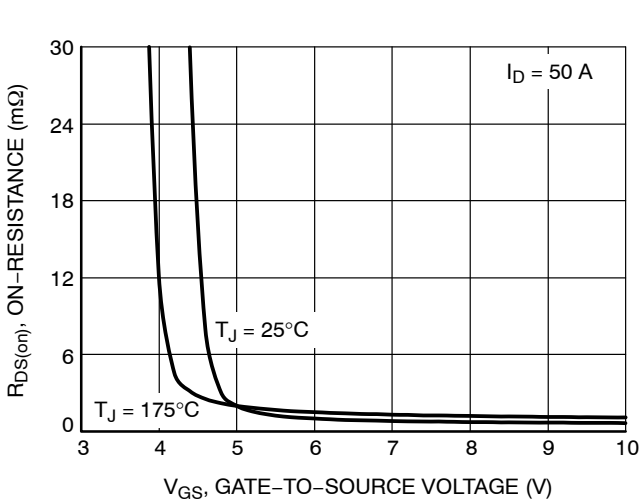


Figure 3. On-Resistance vs. Gate-to-Source Voltage

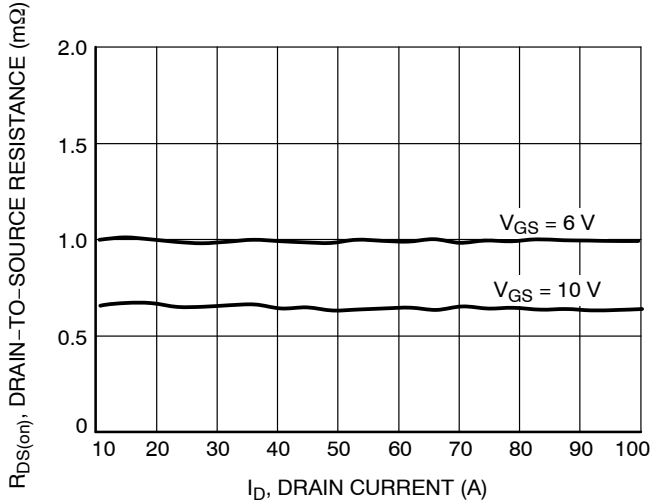


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

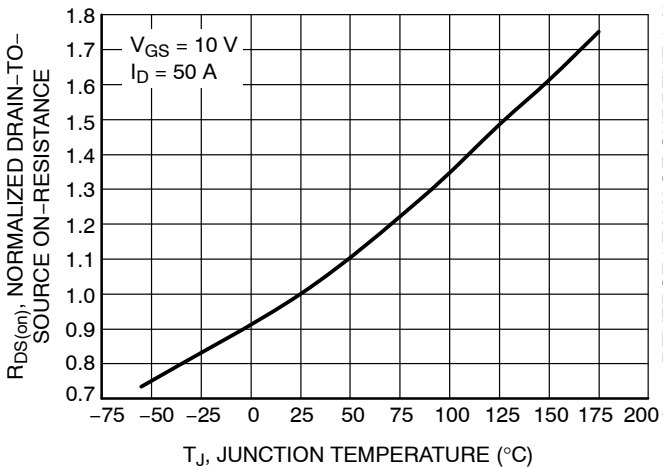


Figure 5. On-Resistance Variation with Temperature

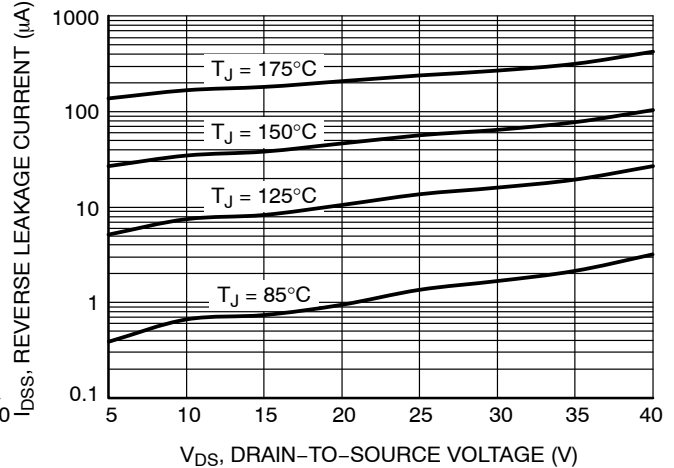


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

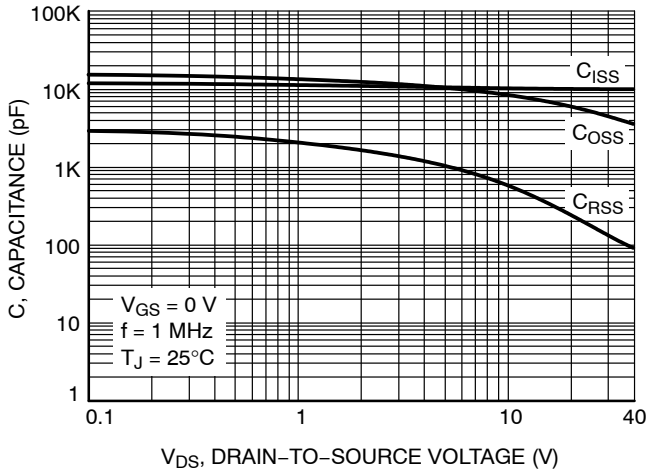


Figure 7. Capacitance Variation

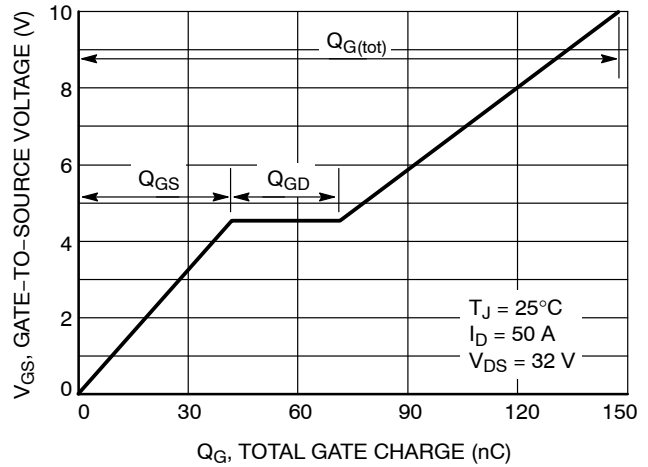


Figure 8. Gate-to-Source Voltage vs. Total Charge

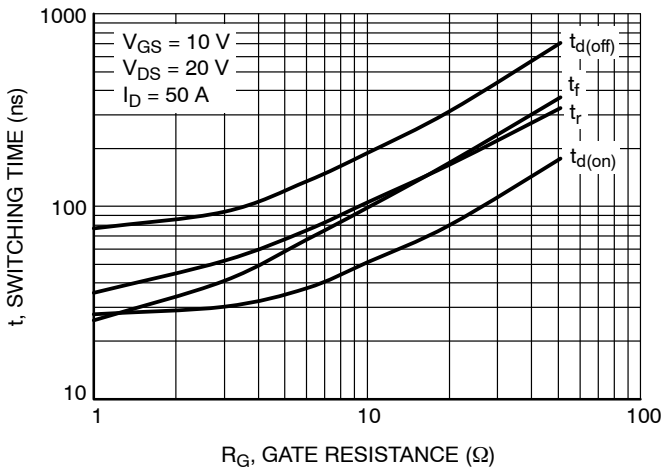


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

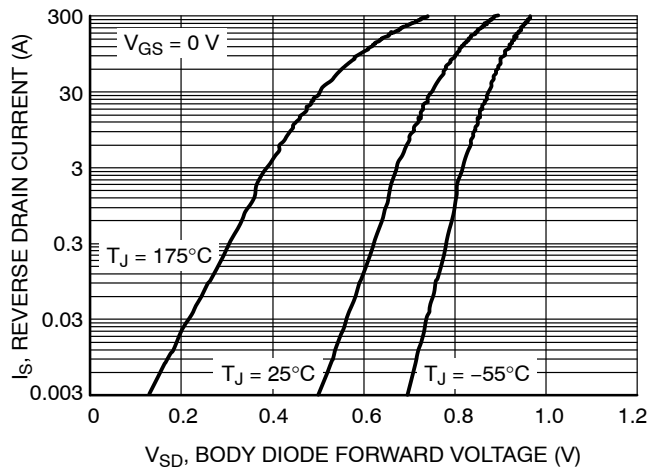


Figure 10. Diode Forward Voltage vs. Current

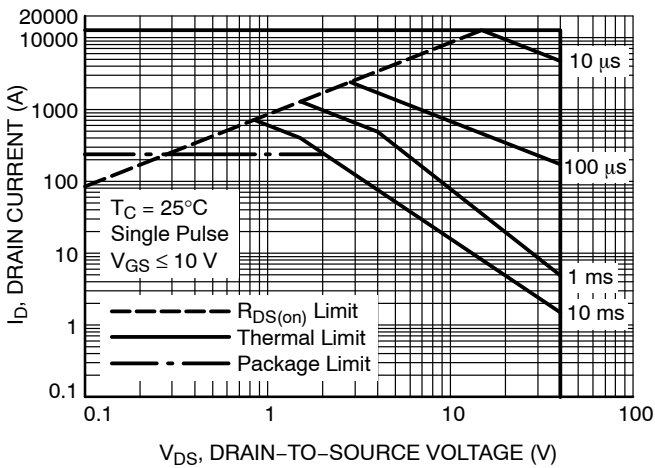


Figure 11. Maximum Rated Forward Biased Safe Operating Area

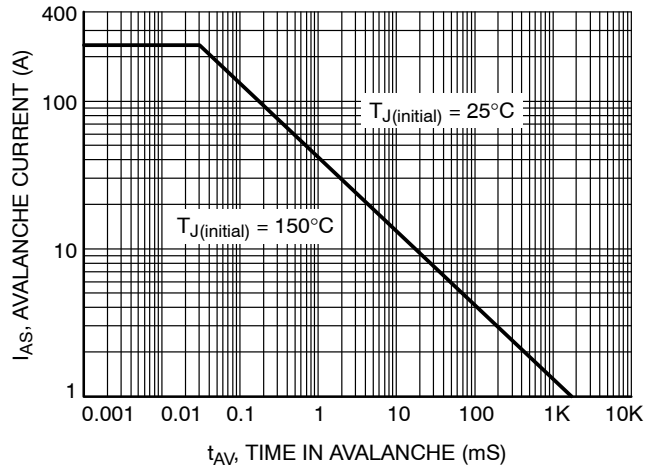


Figure 12. Maximum Drain Current vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS

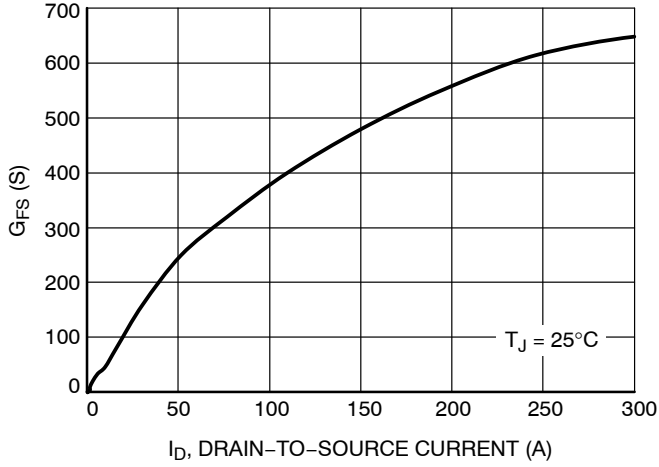


Figure 13.  $G_{FS}$  vs.  $I_D$

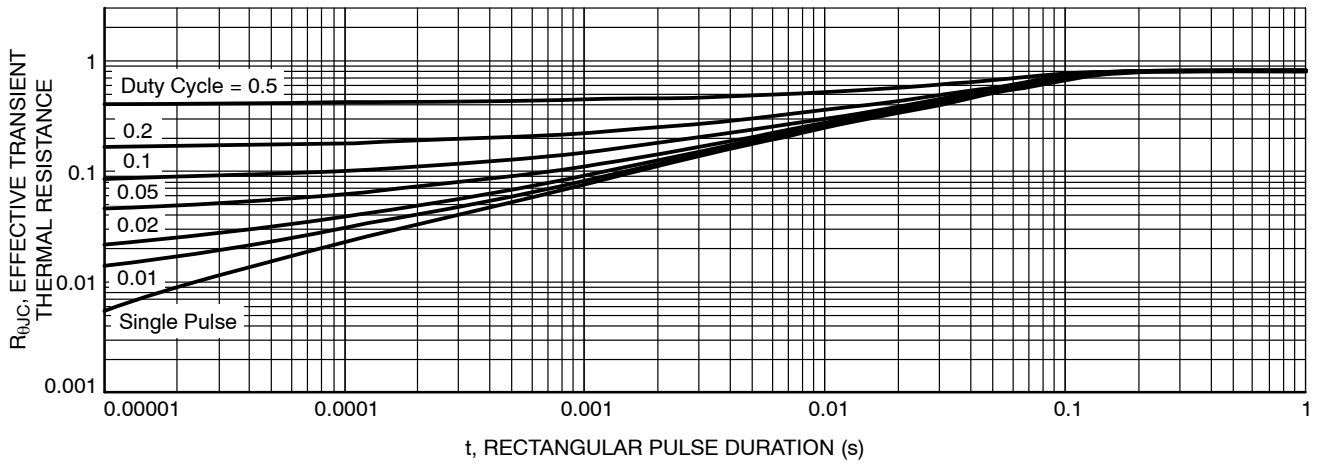
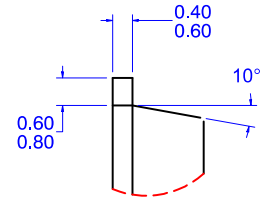
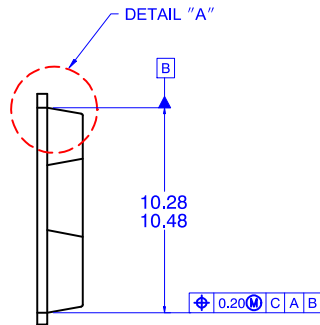
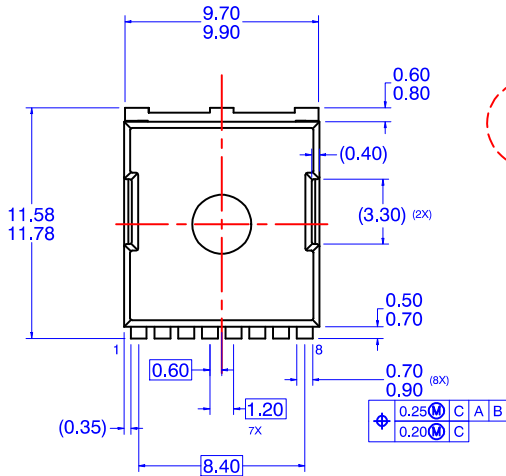


Figure 14. Transient Thermal Impedance

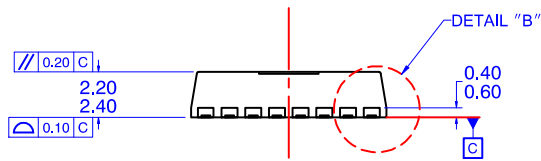
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## PACKAGE DIMENSIONS

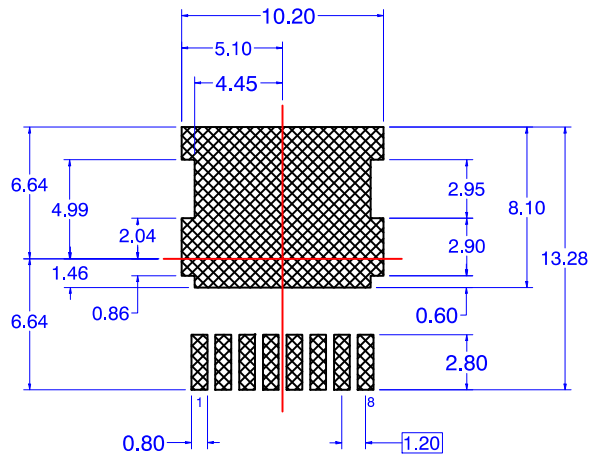
H-PSOF8L 11.68x9.80  
CASE 100CU  
ISSUE O



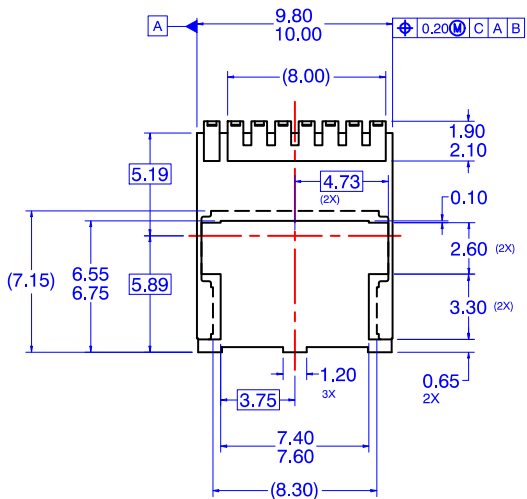
DETAIL "A"



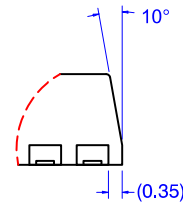
SIDE VIEW



LAND PATTERN RECOMMENDATION



BOTTOM VIEW



DETAIL "B"

- NOTES: UNLESS OTHERWISE SPECIFIED
- PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A, DATED NOVEMBER 2009.
  - ALL DIMENSIONS ARE IN MILLIMETERS.
  - DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

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