FEATURES

- Multi-standard 32-bit High Definition Audio Decoding plus Post Processing
- Supports high-definition audio formats including:
  - Dolby Digital® Plus
  - Dolby® TrueHD
  - DTS-HD™ High Resolution Audio
  - DTS-HD™ Master Audio
  - DSD®
- Additional Applications Library
  - Dolby Digital® EX, Dolby® Pro Logic® IIx, Dolby Headphone®, Dolby® Virtual Speaker®
  - DTS-ES 96/24™, DTS-ES™ Discrete 6.1, DTS-ES™ Matrix 6.1
  - AAC™ Multichannel 5.1
  - SRS® CS2® and TSXT®
  - THX® Ultra2™, THX® ReEQ™
  - Crossbar Mixer, Signal Generator
  - Advanced Post-Processor including: 7.1 Bass Manager, Tone Control, 11- Band Parametric EQ, Delay, 1:2 Upsampler
  - Microsoft® HDCD®
  - Thomson MP3 Surround, DTS:Neo6™, DSD-to-PCM Conversion, Neural Surround, Cirrus Original Multi-Channel Surround 2 (COMS2), and more. Please contact your local FAE for more information on available applications.
- Up to 12 Channels of 32-bit Serial Audio Input

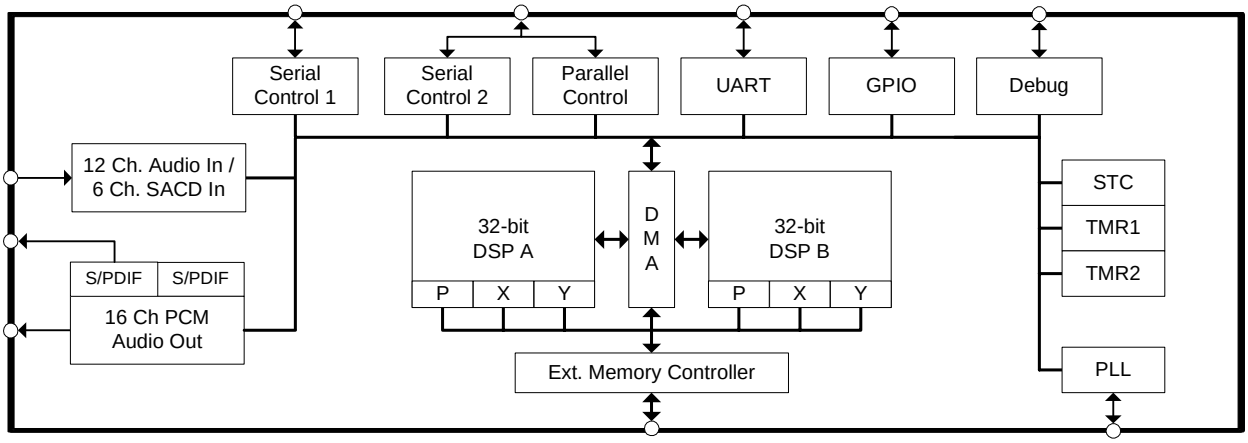
32-bit High Definition Audio Decoder DSP Family with Dual DSP Engine Technology

- Customer Software Security Keys
- 6 Channel DSD® Input
- 16 Ch x 32-bit PCM Out with Dual 192 kHz SPDIF Tx
- Two SPI™/I²C®, One Parallel and One UART Port
- Large On-chip X, Y, and Program RAM & ROM
- SDRAM and Serial Flash Memory Support

The CS4970x4 DSP family is an enhanced version of the CS4953x DSP family with higher overall performance. In addition to all the mainstream audio processing codes in on-chip ROM that the CS4953x DSP offers, the CS4970x4 device family also supports the decoding of major high-definition audio formats. Additionally, the CS4970x4, a dual-core device, performs the high-definition audio decoding on the first core, leaving the second core available for audio post-processing and audio enhancement. The CS4970x4 device will support the most demanding audio post processing requirements. It is also designed as an easy upgrade path to systems currently using the CS495xx or CS4953x device with minor hardware and software changes.

Ordering Information

See page 30 for ordering information.



Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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1. Documentation Strategy

The CS4970x4 data sheet describes the CS4970x4 family of multichannel audio decoders. This document should be used in conjunction with the following documents when evaluating or designing a system around the CS4970x4 family of processors.

Table 1. CS4970x4 Related Documentation

Document Name	Description
CS4970x4 Data Sheet	This document
CS4970x4 System Designer's Guide	A new consolidated documentation set that includes: • Detailed system design information including Typical Connection Diagrams, Boot-Procedures, Pin Descriptions, Etc. Also describes use of DSP Condenser tool. • Detailed firmware design information including signal processing flow diagrams and control API information

The scope of the *CS4970x4 Data Sheet* is primarily the hardware specifications of the CS4970x4 family of devices. This includes hardware functionality, characteristic data, pinout, and packaging information.

The intended audience for the *CS4970x4 Data Sheet* is the system PCB designer, MCU programmer, and the quality control engineer.

2. Overview

The CS4970x4 DSP Family, together with Cirrus Logic's comprehensive library of audio processing algorithms, enables the development of next-generation high-definition audio solutions. Cirrus Logic also provides a broad array of digital interface products, audio converters, and ARM® Processors to meet your audio system-level design requirements.

The CS4970x4 is available in 144-pin and 128-pin LQFP packages. The audio processing features of the CS4970x4 product family are a superset of audio features available in the CS4953xx product family.

Please refer to Table 2 on page 5 for the speed and firmware features of CS4970x4 product family.

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Table 2. Device and Firmware Selection Guide

Device	Pre-Process	Decode Processor A[1]	Mid-processor A[1]	Mid-processor B[1]	Post-processor[1]
CS497004 300 MIPS **CS497024** 300 MIPS	Lip Sync Delay	Stereo PCM Multi-Channel PCM (2:1 Down-sampling Option) Dolby Digital AAC MP3 HDCD Dolby Digital Plus Dolby True-HD DTS-HD DSD to PCM Conversion	Dolby PLIIx SRS® Circle Surround® II (Stereo In) Cirrus Original Multi-Channel Surround (Effects / Reverb Processor) DTS Neo6 Crossbar (Down-mix / Upmix) (Simultaneous Process)	Dolby Headphone Dolby Virtual Speaker	APP (Advanced Post-processing) –Tone Control –Re-EQ –PEQ (up to 11 Bands) –Delay –7.1 Bass Manager –Audio Manager 1:2 Up-sampling

1. Processing may be restricted and dependent on firmware selected. Contact your Cirrus Logic FAE for concurrency matrix.

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2.1 Migrating from the CS495xx(2) to the CS4970x4

The CS4970x4 was designed to provide an easy upgrade path from the CS495xx & CS4953x. Although 144-pin versions of the two devices are virtually identical with respect to external system connection, there are some small differences the hardware designer should be aware of:

- The PLL supply voltage on the CS4970x4 is 3.3V vs. 1.8V on the CS495xx.
- The PLL filter topology is simpler when using the CS4970x4 rather than the CS495xx.
- The CS4970x4 adds support for 6-channel DSD input.
- The CS4970x4 adds support for TDM mode on both audio input and output ports.
- The CS4970x4 does not support external SRAM operation.
- The CS4970x4 external SDRAM bus speed is fixed at 150 MHz vs. the 120 MHz max bus speed for the CS495xx. Some firmware modules also support a 75 MHz CS4970x4 SDRAM bus speed. Please refer to AN304 for details.
- The CS4970x4 CLKOUT pin can output XTALI or XTALI/2. The CS495xx can only output XTALI.

2.2 Licensing

Licenses are required for all of the third party audio decoding/processing algorithms listed below, including the application notes. Please contact your local Cirrus Sales representative for more information.

3. Code Overlays

The suite of software available for the CS4970x4 family consists of operating systems (OS) and a library of overlays. The overlays have been divided into three main groups called Decoders, Mid-processors, and Post-processors. All software components are defined the following list:

- **OS/Kernel** - Encompasses all non-audio processing tasks, including loading data from external memory, processing host messages, calling audio-processing subroutines, auto-detection, error concealment, etc.
- **Decoders** - Any Module that initially writes data into the audio I/O buffers, e.g. AC-3®, DTS, PCM, etc. All the decoding/processing algorithms listed require delivery of PCM or IEC61937-packed, compressed data via I^2S- or LJ-formatted digital audio to the CS4970x4 from A/D converters, SPDIF Rx, HDMI Rx, etc.
- **Mid-processors** - Any module that processes audio I/O buffer PCM data in-place before the Post-processors. Generally speaking, these modules alter the number of valid channels in the audio I/O buffer through processes like Virtualization (n⇨2 channels) or Matrix Decoding (2⇨n channels). Examples are Dolby ProLogic IIx and DTS Neo:6.
- **Post-processors** - Any module that processes audio I/O buffer PCM data in-place after the Mid-Processors. Examples are Bass Management, Audio Manager, Tone Control, EQ, Delay, Customer-specific Effects, Dolby Headphone/Virtual Speaker, etc.

The overlay structure reduces the time required to reconfigure the DSP when a processing change is requested. Each overlay can be reloaded independently without disturbing the other overlays. For example, when a new decoder is selected, the OS, mid-, and post-processors do not need to be reloaded — only the new decoder (the same is true for the other overlays).

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4. Hardware Functional Description

4.1 DSP Core

The CS4970x4 is a dual-core DSP with separate X and Y data and P code memory spaces. Each core is a high-performance, 32-bit, user-programmable, fixed-point DSP that is capable of performing two memory access control (MAC) operations per clock cycle. Each core has eight 72-bit accumulators, four X- and four Y-data registers, and 12 index registers.

Both DSP cores are coupled to a flexible DMA engine. The DMA engine can move data between peripherals such as the digital audio input (DAI) and digital audio output (DAO), external memory, or any DSP core memory, all without the intervention of the DSP. The DMA engine offloads data move instructions from the DSP core, leaving more MIPS available for signal processing instructions.

CS4970x4 functionality is controlled by application codes that are stored in on-board ROM or downloaded to the CS4970x4 from a host MCU or external FLASH/EEPROM. Users can choose to use standard audio decoder and post-processor modules which are available from Cirrus Logic.

The CS4970x4 is suitable for Audio Decoder, Audio Post-processor, Audio Encoder, DVD Audio/Video Player, and Digital Broadcast Decoder applications.

4.1.1 DSP Memory

Each DSP core has its own on-chip data and program RAM and ROM and does not require external memory for any of today's popular audio algorithms including Dolby Digital Surround EX, AAC Multichannel, DTS-ES 96/24, and THX Ultra2. However, if the end-system design requires support of the new high-definition audio formats, external SDRAM will be needed to support Dolby TrueHD and DTS-HD Master Audio.

The memory maps for the DSPs are as follows. All memory sizes are composed of 32-bit words.

Table 3. CS4970x4 DSP Memory Sizes

Memory Type	DSP A	DSP B
X	16k SRAM, 32k ROM	10k SRAM, 8k ROM
Y	24k SRAM, 32k ROM	16k SRAM, 16k ROM
P	8k SRAM, 32k ROM	8k SRAM, 24k ROM

4.1.2 DMA Controller

The powerful 12-channel DMA controller can move data between 8 on-chip resources. Each resource has its own arbiter: X, Y, and P RAM/ROMs on DSP A; X, Y, and P RAM/ROMs on DSP B; external memory; and the peripheral bus. Modulo and linear addressing modes are supported, with flexible start address and increment controls. The service interval for each DMA channel as well as up to 6 interrupt events, is programmable.

4.2 On-chip DSP Peripherals

4.2.1 Digital Audio Input Port (DAI)

The 12-channel (6 line) DAI port supports a wide variety of data input formats. The port is capable of accepting PCM, IEC61937, or DSD. Up to 32-bit word lengths are supported. Up to 6 channels of DSD are supported and internally converted to PCM before processing. Additionally support is provided for audio data input to the DSP via the DAI from an HDMI receiver.

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The port has two independent slave-only clock domains. Each data input can be independently assigned to a clock domain. The sample rate of the input clock domains can be determined automatically by the DSP, which off-loads the task of monitoring the SPDIF receiver from the host. A time-stamping feature allows the input data to be sample-rate converted via software.

4.2.2 Digital Audio Output Port (DAO)

There are two DAO ports. Each port can output 8 channels of up to 32-bit PCM data. The port supports data rates from 32 kHz to 192 kHz. Each port can be configured as an independent clock domain in slave mode, or the ratio of the two clocks can be set to even multiples of each other in master mode. The two ports can also be ganged together into a single clock domain. Each port has one serial audio pin that can be configured as a 192 kHz SPDIF transmitter (data with embedded clock on a single line).

4.2.3 Serial Control Port 1 & 2 ($I^2C^{®}$ or SPI™)

There are two on-chip serial control ports that are capable of operating as master or slave in either I^2C or SPI modes. SCP1 defaults to slave operation. It is dedicated for external host-control and supports an external clock up to 50 MHz in SPI mode. This high clock speed enables very fast code download, control or data delivery. SCP2 defaults to master mode and is dedicated for booting from external serial Flash memory or for audio sub-system control.

4.2.4 Parallel Control Port

The CS4970x4 parallel port supports both Motorola® and Intel® interfaces. It can be used for both control and data delivery. The parallel port pins are multiplexed with serial control port 2 and are available in the 144-pin package.

4.2.5 External Memory Interface

The external memory interface controller supports up to 128 Mbits of SDRAM, using a 16-bit data bus.

4.2.6 GPIO

Many of the CS4970x4 peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.2.7 PLL-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency which are used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS4970x4 defaults to running from the external reference frequency and can be switched to use the PLL output after overlays have been loaded and configured, either through master boot from an external FLASH or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

4.3 DSP I/O Description

4.3.1 Multiplexed Pins

Many of the CS4970x4 pins are multi-functional. For details on pin functionality please refer to the *CS4970x4 System Designer's Guide.*

4.3.2 Termination Requirements

Open-drain pins on the CS4970x4 must be pulled high for proper operation. Please refer to the *CS4970x4 System Designer's Guide* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

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Mode select pins on the CS4970x4 are used to select the boot mode upon the rising edge of reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS4970x4 System Designer's Guide*.

4.3.3 Pads

The CS4970x4 I/O operate from the 3.3 V supply and are 5 V tolerant.

4.4 Application Code Security

The external program code may be encrypted by the programmer to protect any intellectual property it may contain. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device.

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5. Characteristics and Specifications

Note: All data sheet minimum and maximum timing parameters are guaranteed over the rated voltage and temperature. All data sheet typical parameters are measured under the following conditions: T = 25 °C, C_L = 20 pF, VDD = 1.8 V, VDDA = VDDIO = 3.3 V, GNDD = GNDIO = GNDA = 0 V.

5.1 Absolute Maximum Ratings

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter	Symbol	Min	Max	Unit
DC power supplies: Core supply	VDD	–0.3	2.0	V
PLL supply	VDDA	–0.3	3.6	V
I/O supply	VDDIO	–0.3	3.6	V
|VDDA – VDDIO|		-	0.3	V
Input pin current, any pin except supplies	I_{in}	-	+/- 10	mA
Input voltage on PLL_REF_RES	V_{filt}	-0.3	3.6	V
Input voltage on I/O pins	V_{inio}	-0.3	5.0	V
Storage temperature	T_{stg}	–65	150	°C

Caution: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5.2 Recommended Operating Conditions

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
DC power supplies: Core supply	VDD	1.71	1.8	1.89	V
PLL supply	VDDA	3.13	3.3	3.46	V
I/O supply	VDDIO	3.13	3.3	3.46	V
|VDDA – VDDIO|			0		V
Ambient operating temperature Commercial Grade (CQZ/CVZ)	T_A	0	+25	+ 70	°C

Note: It is recommended that the 3.3 V IO supply come up ahead of or simultaneously with the 1.8 V core supply.

5.3 Digital DC Characteristics

(Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.0	-	-	V
Low-level input voltage, except XTI	V_{IL}	-	-	0.8	V
Low-level input voltage, XTI	V_{ILXTI}	-	-	0.6	V
Input Hysteresis	V_{hys}		0.4		V
High-level output voltage (I_O = -4mA), except XTI, SDRAM pins	V_{OH}	VDDIO * 0.9	-	-	V
Low-level output voltage (I_O = 4mA), except XTI, SDRAM pins	V_{OL}	-	-	VDDIO * 0.1	V
SDRAM High-level output voltage (I_O = -8mA)	V_{OH}	VDDIO * 0.9	-	-	V
SDRAM Low-level output voltage (I_O = 8mA)	V_{OL}	-	-	VDDIO * 0.1	V
Input leakage current (all digital pins with internal pull-up resistors disabled)	I_{IN}	-	-	5	µA

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Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current (all digital pins with internal pull-up resistors enabled, and XTI)	I_{IN-PU}	-	-	50	µA

5.4 Power Supply Characteristics

(Measurements performed under operating conditions.)

Parameter	Min	Typ	Max	Unit
Power supply current:				
Core and I/O operating: VDD[1]	-	500	-	mA
PLL operating: VDDA	-	3.5	-	mA
With external memory and most ports operating: VDDIO	-	120	-	mA

1.Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (144-Pin LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C / Watt
Two-layer Board[1]		-	48	-	
Four-layer Board[2]		-	40	-	
Thermal Resistance (Junction to Top of Package)	ψ_{jt}				°C / Watt
Two-layer Board[1]		-	.39	-	
Four-layer Board[2]		-	.33	-	

Notes: 1. Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz copper covering 20% of the top and bottom layers.

2. Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz copper covering 20% of the top and bottom layers and 0.5-oz copper covering 90% of the internal power plane and ground plane layers.

3. To calculate the die temperature for a given power dissipation

T_j = Ambient Temperature + [(Power Dissipation in Watts) * θ_{ja}]

4. To calculate the case temperature for a given power dissipation

$T_c = T_j$ - [(Power Dissipation in Watts) * ψ_{jt}]

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5.6 Switching Characteristics— RESET

Parameter	Symbol	Min	Max	Unit
RESET# minimum pulse width low	T_{rstl}	1	-	µs
All bidirectional pins high-Z after RESET# low	T_{rst2z}	-	100	ns
Configuration pins setup before RESET# high	T_{rstsu}	50	-	ns
Configuration pins hold after RESET# high	T_{rsthld}	20	-	ns

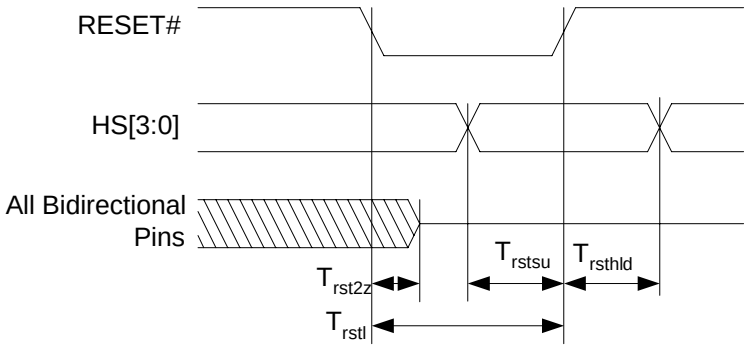


Figure 1. RESET Timing

5.7 Switching Characteristics — XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency[1]	F_{xtal}	11.2896	27	MHz
XTI period	T_{clki}	33.3	100	ns
XTI high time	T_{clkih}	13.3	-	ns
XTI low time	T_{clkil}	13.3	-	ns
External Crystal Load Capacitance (parallel resonant)[2]	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR		50	W

1. Part characterized with the following crystal frequency values: 11.2896, 12.288, 18.432, 24.576, and 27 MHz.
2. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals which require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

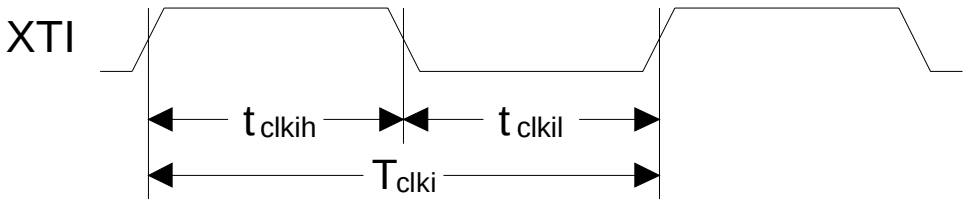


Figure 2. XTI Timing

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5.8 Switching Characteristics — Internal Clock

Parameter	Symbol	Min	Max	Unit
Internal DCLK frequency[1] CS497004-CQZ CS497004-CQZR CS497024-CVZ CS497024-CVZR	F_{dclk}	F_{xtal}	150	MHz
Internal DCLK period[1] CS497004-CQZ CS497004-CQZR CS497024-CVZ CS497024-CVZR	DCLKP	6.7	$1/F_{xtal}$	ns

1.After initial power-on reset, $F_{dclk} = F_{xtal}$. After initial kickstart commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

5.9 Switching Characteristics — Serial Control Port - SPI Slave Mode

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Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		25	MHz
SCP_CS# falling to SCP_CLK rising	t_{spicss}	24		-	ns
SCP_CLK low time	t_{spickl}	20		-	ns
SCP_CLK high time	t_{spickh}	20		-	ns
Setup time SCP_MOSI input	t_{spidsu}	5		-	ns
Hold time SCP_MOSI input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MISO output valid	t_{spidov}	-		11	ns
SCP_CLK falling to SCP_IRQ# rising	$t_{spiirqh}$	-		20	ns
SCP_CS# rising to SCP_IRQ# falling	$t_{spiirql}$	0			ns
SCP_CLK low to SCP_CS# rising	t_{spicsh}	24		-	ns
SCP_CS# rising to SCP_MISO output high-Z	$t_{spicsdz}$	-	20		ns
SCP_CLK rising to SCP_BSY# falling	$t_{spicbsyl}$	-	3∗DCLKP+20		ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_BSY# pin should be implemented to prevent overflow of the input data buffer.At boot the maximum speed is Fxtal/3.

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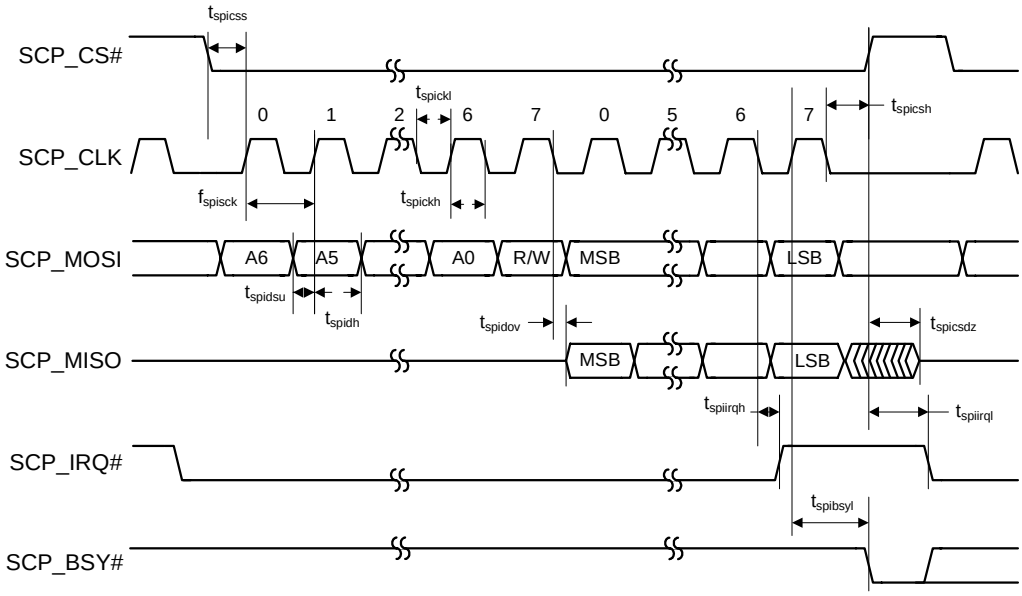


Figure 3. Serial Control Port - SPI Slave Mode Timing

5.10 Switching Characteristics — Serial Control Port - SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		$F_{xtal}/2$ (See Footnote 2)	MHz
SCP_CS# falling to SCP_CLK rising [3]	t_{spicss}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
SCP_CLK low time	t_{spickl}	18		-	ns
SCP_CLK high time	t_{spickh}	18		-	ns
Setup time SCP_MISO input	t_{spidsu}	11		-	ns
Hold time SCP_MISO input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	-		11	ns
SCP_CLK low to SCP_CS# falling	t_{spicsl}	7		-	ns
SCP_CLK low to SCP_CS# rising	t_{spicsh}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
Bus free time between active SCP_CS#	t_{spicsx}		3*DCLKP	-	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	-		20	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. See Section 5.7.
3. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter.

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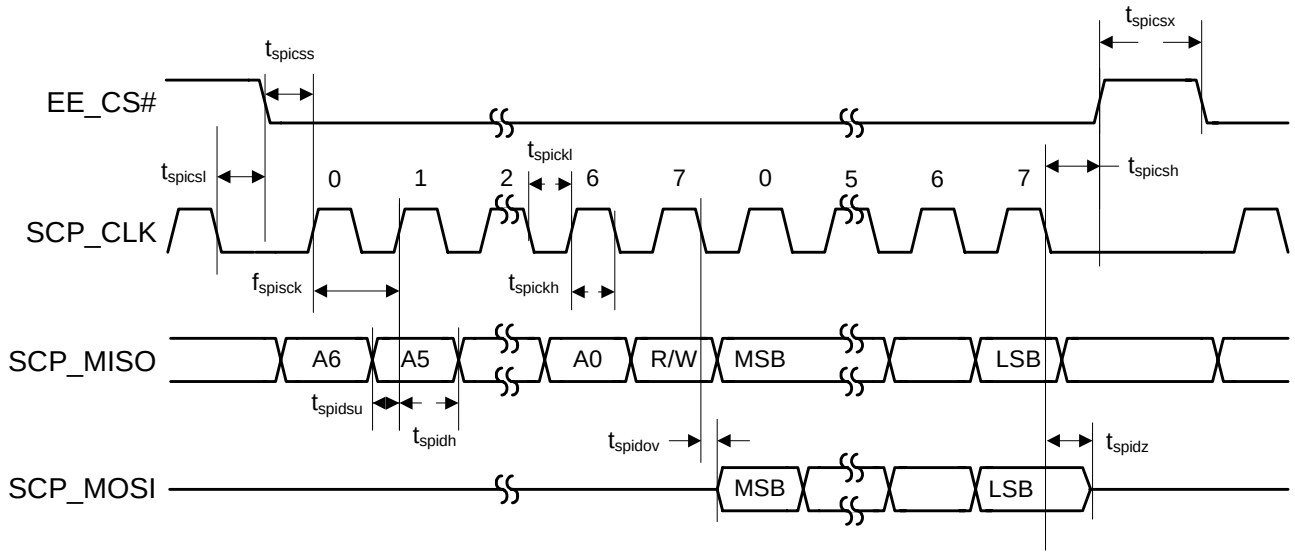


Figure 4. Serial Control Port - SPI Master Mode Timing

5.11 Switching Characteristics — Serial Control Port - I²C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-		400	kHz
SCP_CLK low time	t_{iicckl}	1.25		-	µs
SCP_CLK high time	t_{iicckh}	1.25		-	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25			µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25		-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5		-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3		-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100			ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20		-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-		18	ns
SCP_CLK falling to SCP_IRQ# rising	$t_{iicirqh}$	-		3∗DCLKP + 40	ns
NAK condition to SCP_IRQ# low	$t_{iicirql}$		3∗DCLKP + 20		ns
SCP_CLK rising to SCB_BSY# low	$t_{iicbsyl}$	-	3∗DCLKP + 20		ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_BSY# pin should be implemented to prevent overflow of the input data buffer.

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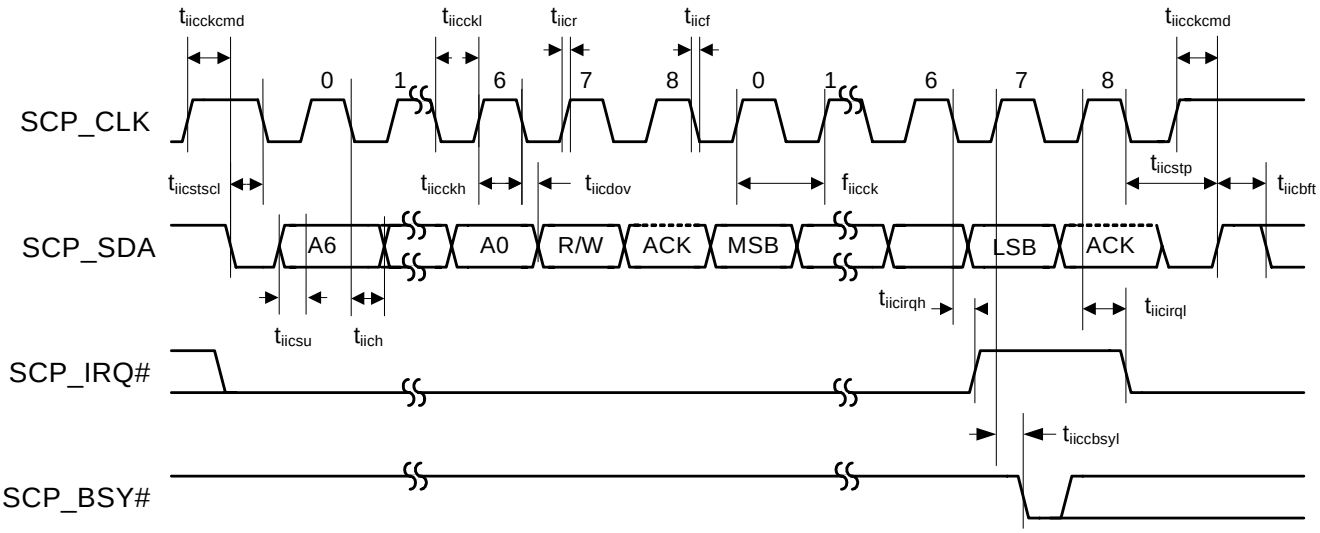


Figure 5. Serial Control Port - I²C Slave Mode Timing

5.12 Switching Characteristics — Serial Control Port - I²C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	-	µs
SCP_CLK high time	t_{iicckh}	1.25	-	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25		µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100		ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20	-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-	18	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.

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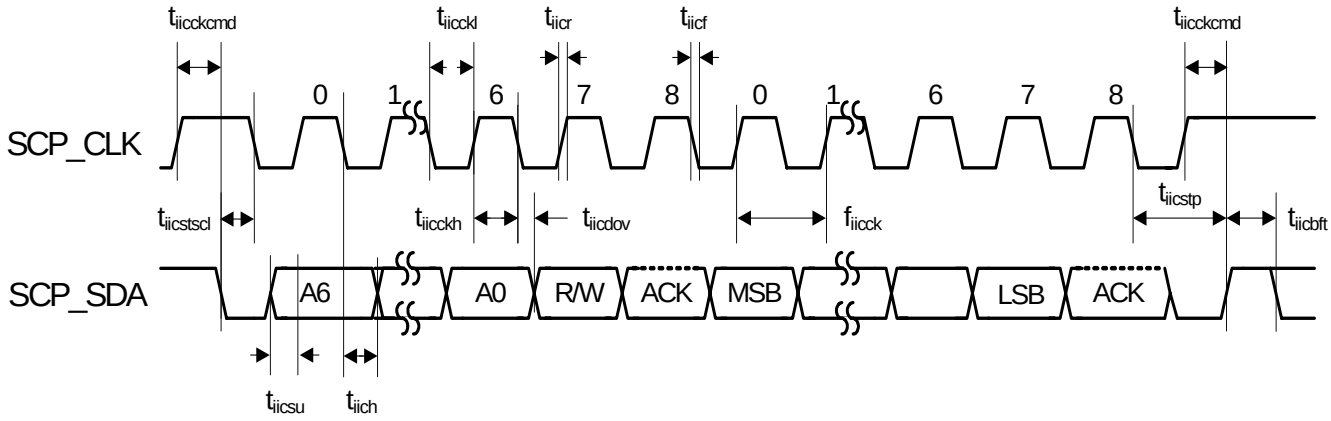


Figure 6. Serial Control Port - I²C Master Mode Timing

5.13 Switching Characteristics — Parallel Control Port - Intel Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
Address setup before PCP_CS# and PCP_RD# low or PCP_CS# and PCP_WR# low	t_{ias}	5		-	ns
Address hold time after PCP_CS# and PCP_RD# low or PCP_CS# and PCP_WR# high	t_{iah}	5		-	ns
Read					
Delay between PCP_RD# then PCP_CS# low or PCP_CS# then PCP_RD# low	t_{icdr}	0		-	ns
Data valid after PCP_CS# and PCP_RD# low	t_{idd}	-		18	ns
PCP_CS# and PCP_RD# low for read	t_{irpw}	24		-	ns
Data hold time after PCP_CS# or PCP_RD# high	t_{idhr}	8		-	ns
Data high-Z after PCP_CS# or PCP_RD# high	t_{idis}	-		18	ns
PCP_CS# or PCP_RD# high to PCP_CS# and PCP_RD# low for next read[1]	t_{ird}	30		-	ns
PCP_CS# or PCP_RD# high to PCP_CS# and PCP_WR# low for next write[1]	t_{irdtw}	30		-	ns
PCP_RD# rising to PCP_IRQ# rising	$t_{irdirqhl}$	-		12	ns
Write					
Delay between PCP_WR# then PCP_CS# low or PCP_CS# then PCP_WR# low	t_{icdw}	0		-	ns
Data setup before PCP_CS# or PCP_WR# high	t_{idsu}	8		-	ns
PCP_CS# and PCP_WR# low for write	t_{iwpw}	24		-	ns
Data hold after PCP_CS# or PCP_WR# high	t_{idhw}	8		-	ns
PCP_CS# or PCP_WR# high to PCP_CS# and PCP_RD# low for next read[1]	t_{iwtrd}	30		-	ns
PCP_CS# or PCP_WR# high to PCP_CS# and PCP_WR# low for next write[1]	t_{iwd}	30		-	ns
PCP_WR# rising to PCP_BSY# falling	$t_{iwrbsyl}$	-	2*DCLKP + 20	-	ns

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1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_BSY# pin/bit should be observed to prevent overflowing the input data buffer. *CS4970x4 System Designer's Guide* should be consulted for the firmware speed limitations.

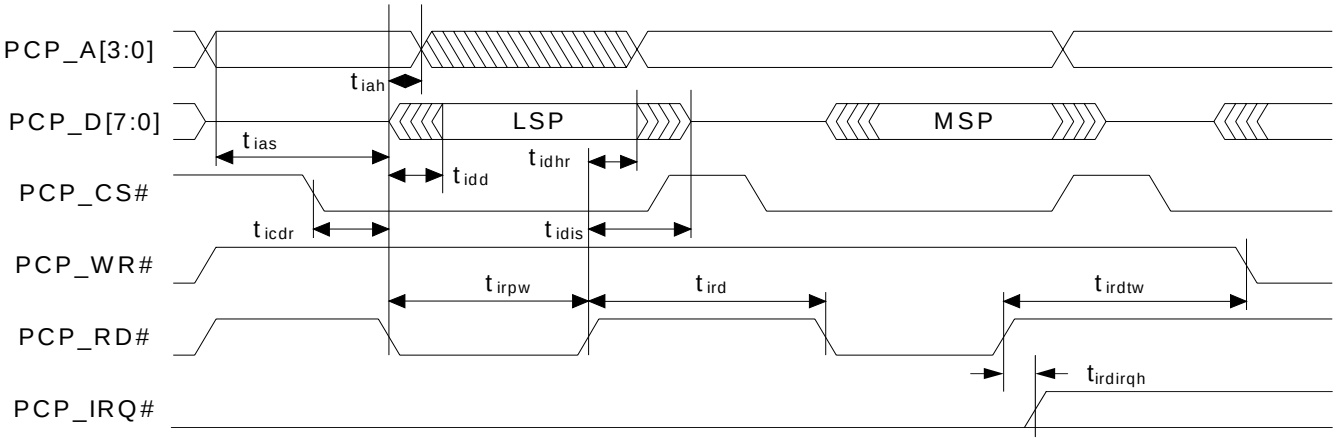


Figure 7. Parallel Control Port - Intel Mode Read Cycle

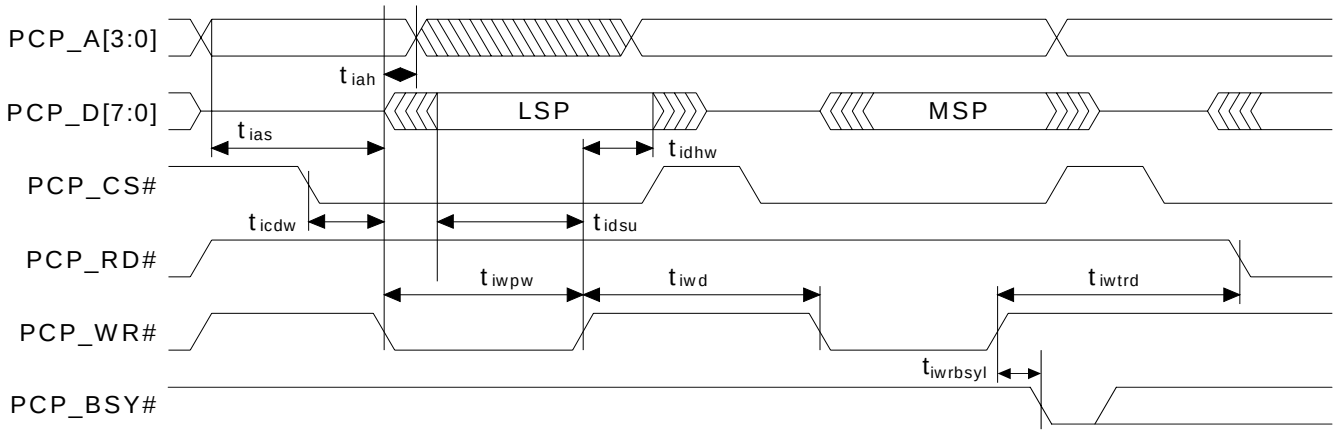


Figure 8. Parallel Control Port - Intel Mode Write Cycle

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5.14 Switching Characteristics — Parallel Control Port - Motorola Slave Mode

Parameter	Symbol	Min		Max	Unit
Address setup before PCP_CS# and PCP_DS# low	t_{mas}	5		-	ns
Address hold time after PCP_CS# and PCP_DS# low	t_{mah}	5		-	ns
Read					
Delay between PCP_DS# then PCP_CS# low or PCP_CS# then PCP_DS# low	t_{mcdr}	0		-	ns
Data valid after PCP_CS# and PCP_DS# low with PCP_R/W# high	t_{mdd}	-		19	ns
PCP_CS# and PCP_DS# low for read	t_{mrpw}	24		-	ns
Data hold time after PCP_CS# or PCP_DS# high after read	t_{mdhr}	8		-	ns
Data high-Z after PCP_CS# or PCP_DS# high after read	t_{mdis}	-		18	ns
PCP_CS# or PCP_DS# high to PCP_CS# and PCP_DS# low for next read[1]	t_{mrd}	30		-	ns
PCP_CS# or PCP_DS# high to PCP_CS# and PCP_DS# low for next write[1]	t_{mrdtw}	30		-	ns
PCP_RW# rising to PCP_IRQ# falling	$t_{mrwirqh}$	-		12	ns
Write					
Delay between PCP_DS# then PCP_CS# low or PCP_CS# then PCP_DS# low	t_{mcdw}	0		-	ns
Data setup before PCP_CS# or PCP_DS# high	t_{mdsu}	8		-	ns
PCP_CS# and PCP_DS# low for write	t_{mwpw}	24		-	ns
PCP_R/W# setup before PCP_CS# AND PCP_DS# low	t_{mrwsu}	24		-	ns
PCP_R/W# hold time after PCP_CS# or PCP_DS# high	t_{mrwhld}	8		-	ns
Data hold after PCP_CS# or PCP_DS# high	t_{mdhw}	8		-	ns
PCP_CS# or PCP_DS# high to PCP_CS# and PCP_DS# low with PCP_R/W# high for next read[1]	t_{mwtrd}	30		-	ns
PCP_CS# or PCP_DS# high to PCP_CS# and PCP_DS# low for next write[1]	t_{mwd}	30		-	ns
PCP_RW# rising to PCP_BSY# falling	$t_{mrwbsyl}$	-	2*DCLKP + 20	-	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_BSY# pin/bit should be observed to prevent overflowing the input data buffer. *CS4970x4 System Designer's Guide* should be consulted for the firmware speed limitations.

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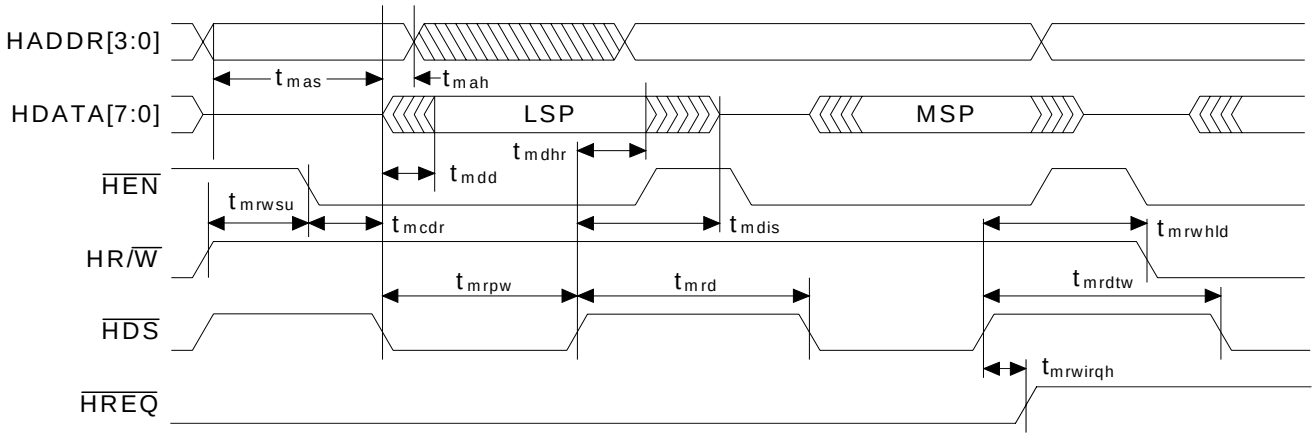


Figure 9. Parallel Control Port - Motorola Mode Read Cycle Timing

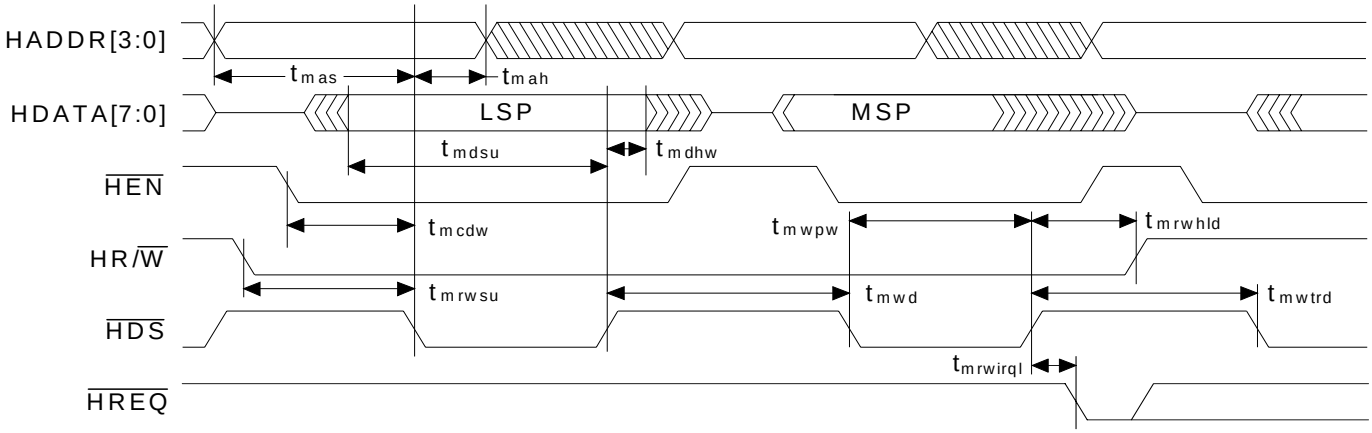


Figure 10. Parallel Control Port - Motorola Mode Write Cycle Timing

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5.15 Switching Characteristics — UART

Parameter	Symbol	Min	Max	Unit
UART_CLK period[1]	t_{uclki}	266	-	ns
UART_CLK duty cycle	-	40	60	%
Setup time for UART_RXD	$t_{uckrxsu}$	5	-	
Hold time for UART_RXD	$t_{uckrxdv}$	5	-	ns
Delay from CLK transition to TXD transition	$t_{ucktxdv}$	-	29	ns
	t_{txen}	TBD	TBD	ns
	t_{txhz}	TBD	TBD	ns

1. The minimum clock period is limited to DCLKP/32 or the minimum value, whichever is larger.

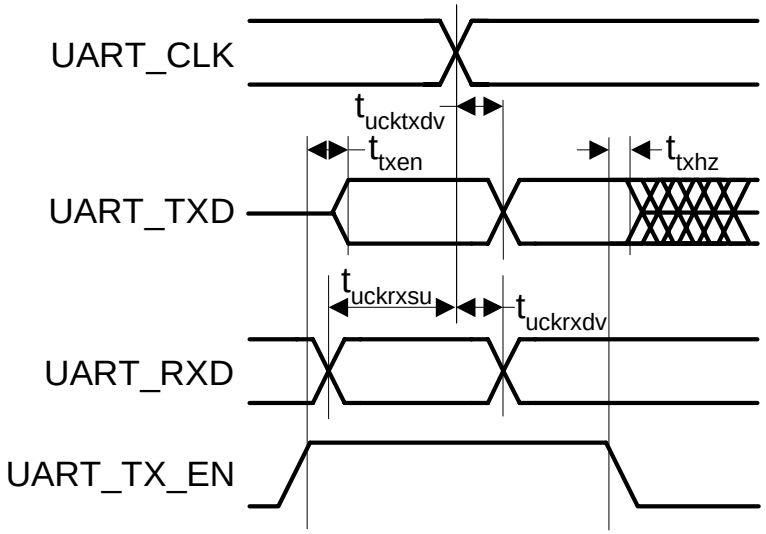


Figure 11. UART Timing

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5.16 Switching Characteristics — Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	40	-	ns
DAI_SCLK duty cycle	-	45	55	%
Setup time DAI_DATAn	t_{daidsu}	10	-	ns
Hold time DAI_DATAn	t_{daidh}	5	-	ns

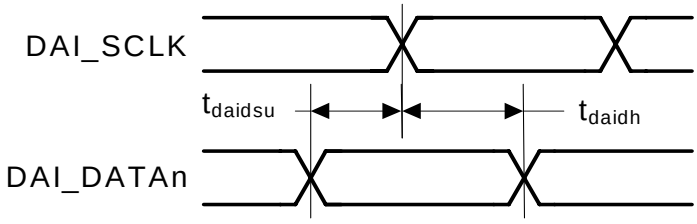


Figure 12. Digital Audio Input (DAI) Port Timing Diagram

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5.17 Switching Characteristics — Direct Stream Digital Slave Input Port

Parameter	Symbol	Min	Typ	Max	Unit
DSD_SCLK Pulse Width Low	t_{sclkl}	78	-	-	ns
DSD_SCLK Pulse Width High	t_{sclkh}	78	-	-	ns
DSD_SCLK Frequency (64x Oversampled)	-	1.024	-	3.2	MHz
(128x Oversampled)	-	2.048	-	6.4	MHz
DSD_A / _B valid to DSD_SCLK rising setup time	t_{sdlrs}	20	-	-	ns
DSD_SCLK rising to DSD_A or DSD_B hold time	t_{sdh}	20	-	-	ns

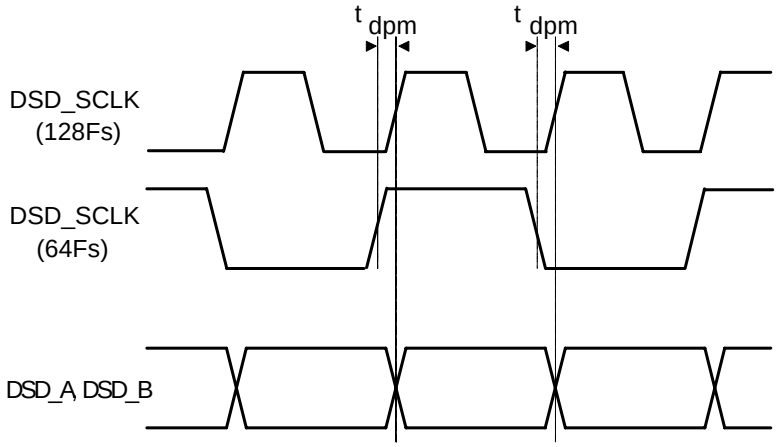


Figure 13. Direct Stream Digital - Serial Audio Input Timing

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5.18 Switching Characteristics — Digital Audio Output Port

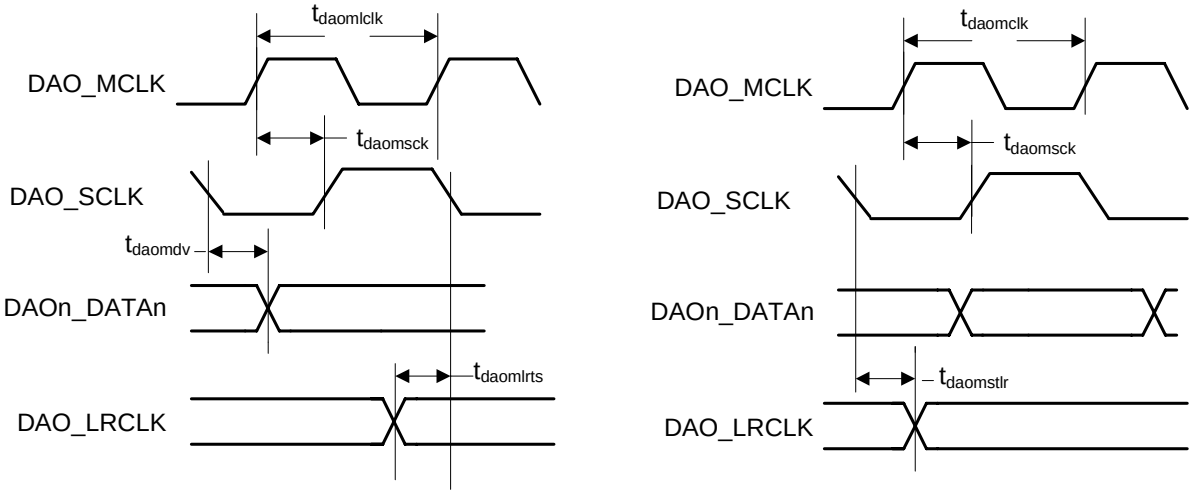
Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	40	-	ns
DAO_MCLK duty cycle	-	45	55	%
DAO_SCLK period for Master or Slave mode[1]	$T_{daosclk}$	40	-	ns
DAO_SCLK duty cycle for Master or Slave mode[1]	-	40	60	%
Master Mode (Output A1 Mode)[1,2]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO_MCLK as an input	$t_{daomsck}$	-	19	ns
DAO_LRCLK delay from DAO_SCLK transition, respectively[3]	$t_{daomstlr}$	-	8	ns
DAO_SCLK delay from DAO_LRCLK transition, respectively[3]	$t_{daomlrts}$	-	8	ns
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition[3]	t_{daomdv}	-	10	ns
Slave Mode (Output A0 Mode)[4]				
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition[3]	t_{daosdv}	-	15	ns
DAO_LRCLK delay from DAO_SCLK transition, respectively[3]	$t_{daosstlr}$	-	30	ns
DAO_SCLK delay from DAO_LRCLK transition, respectively[3]	$t_{daoslrts}$	-	15	ns

1.Master mode timing specifications are characterized, not production tested.

2.Master mode is defined as the CS48DVxx driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.

3.This timing parameter is defined from the non-active edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.

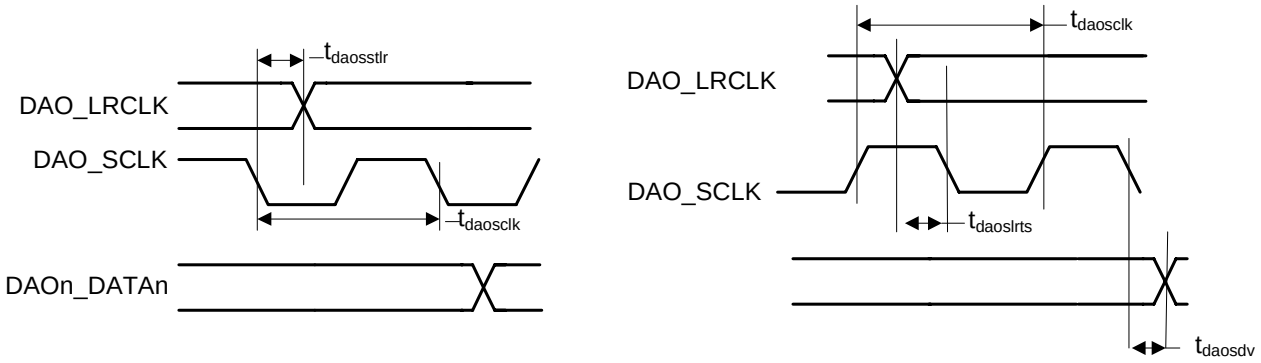
4.Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.



Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 14. Digital Audio Port Timing Master Mode

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Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 15. Digital Audio Output Timing, Slave Mode (Relationship LRCLK to SCLK)

5.19 Switching Characteristics — SDRAM Interface

Refer to Figure 16 through Figure 19.

(SD_CLKOUT = SD_CLKIN)

Parameter	Symbol	Min	Typical	Max	Unit
SD_CLKIN high time	t_{sdclkh}	2.3		-	ns
SD_CLKIN low time	t_{sdclkl}	2.3		-	ns
SD_CLKOUT rise/fall time	$t_{sdclkrf}$	-		1	ns
SD_CLKOUT Frequency			150		MHz
SD_CLKOUT duty cycle	-	45		55	%
SD_CLKOUT rising edge to signal valid	t_{sdcmdv}	-		3.8	ns
Signal hold from SD_CLKOUT rising edge	t_{sdcmdh}		1.1	-	ns
SD_CLKOUT rising edge to SD_DQMn valid	t_{sddqv}	-	3.8	-	ns
SD_DQMn hold from SD_CLKOUT rising edge	t_{sddqh}	1.38		-	ns
SD_DATA valid setup to SD_CLKIN rising edge	t_{sddsu}	1.3		-	ns
SD_DATA valid hold to SD_CLKIN rising edge	t_{sddh}	1.38		-	ns
SD_CLKOUT rising edge to ADDRn valid	t_{sdav}	-	3.8	-	ns

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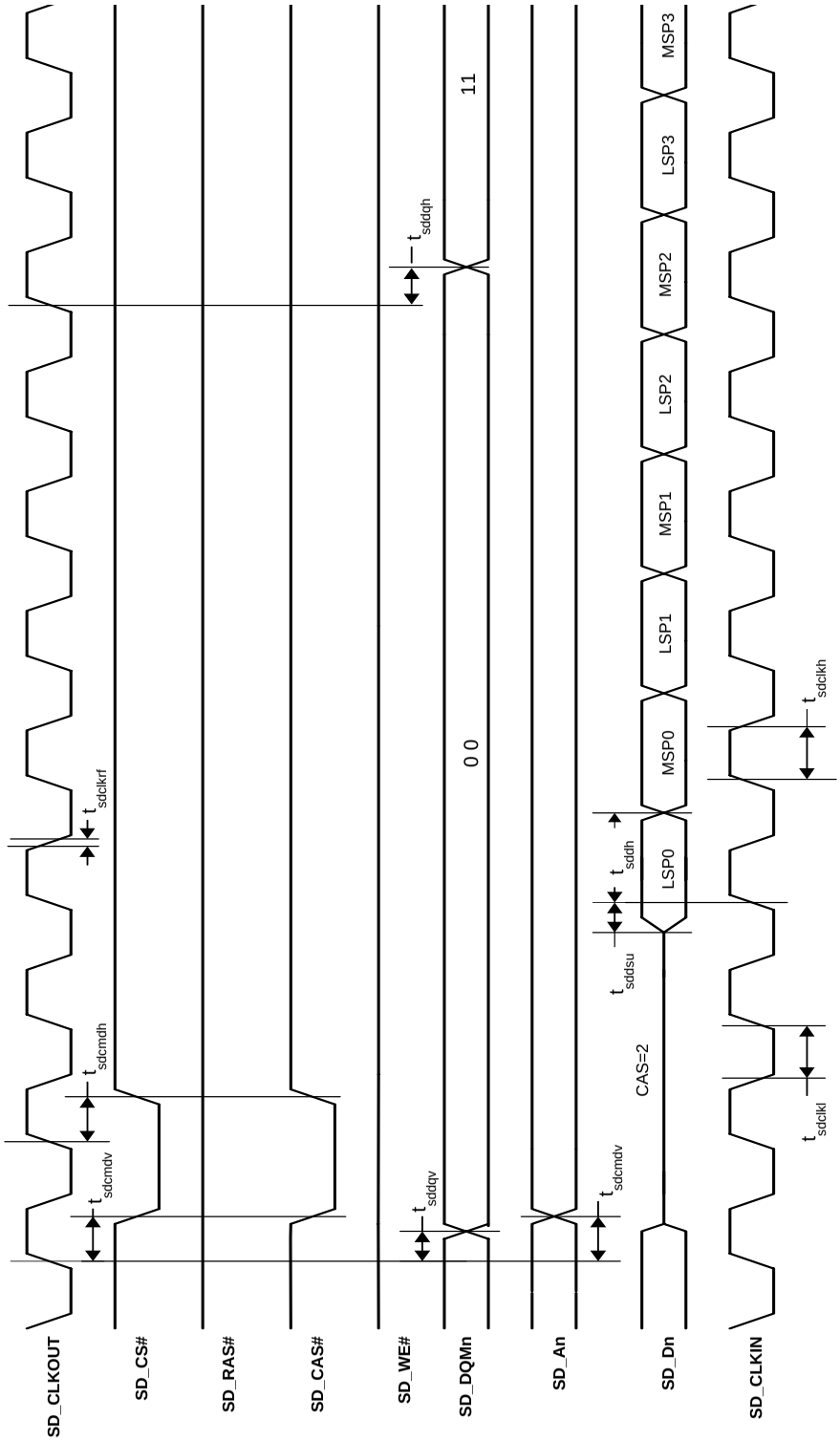


Figure 16. External Memory Interface - SDRAM Burst Read Cycle

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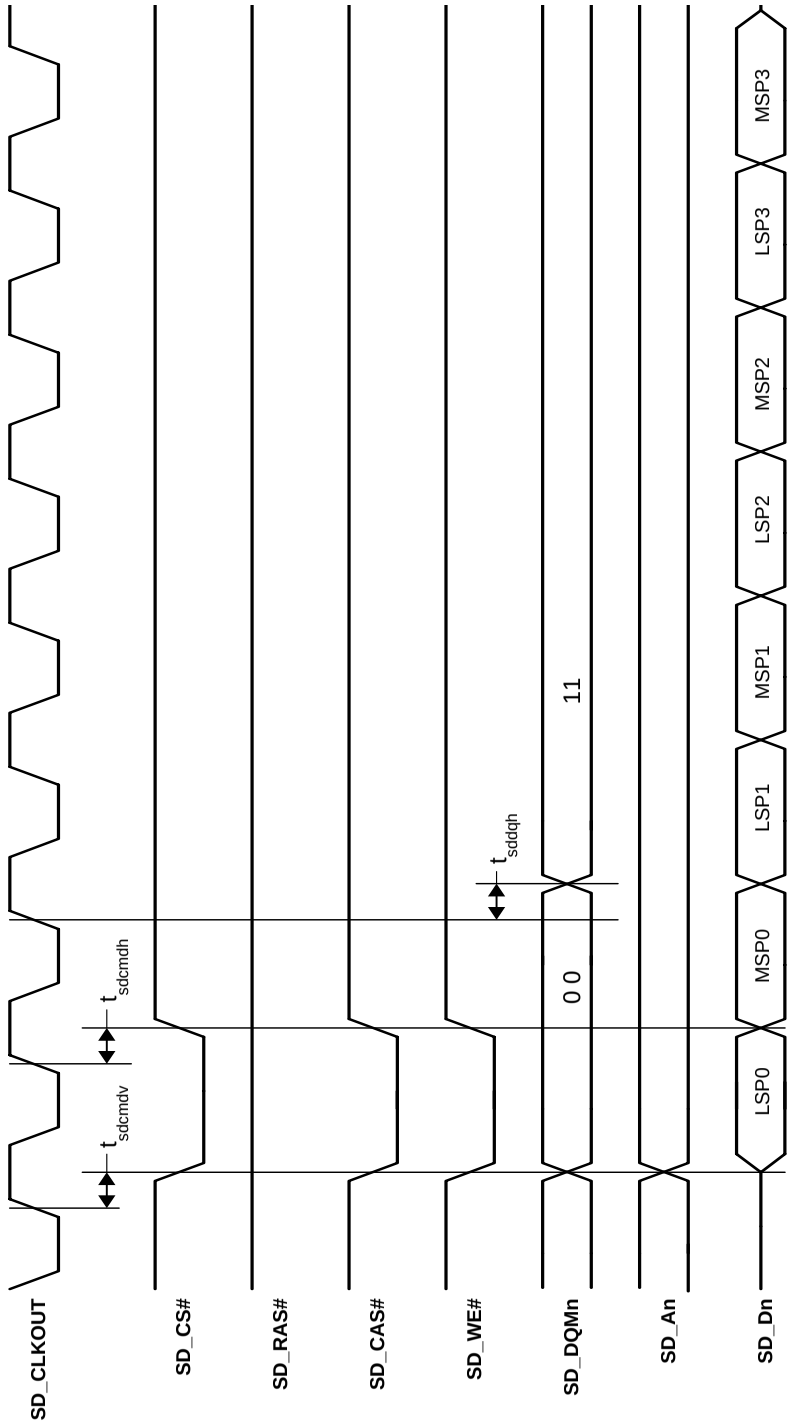


Figure 17. External Memory Interface - SDRAM Burst Write Cycle

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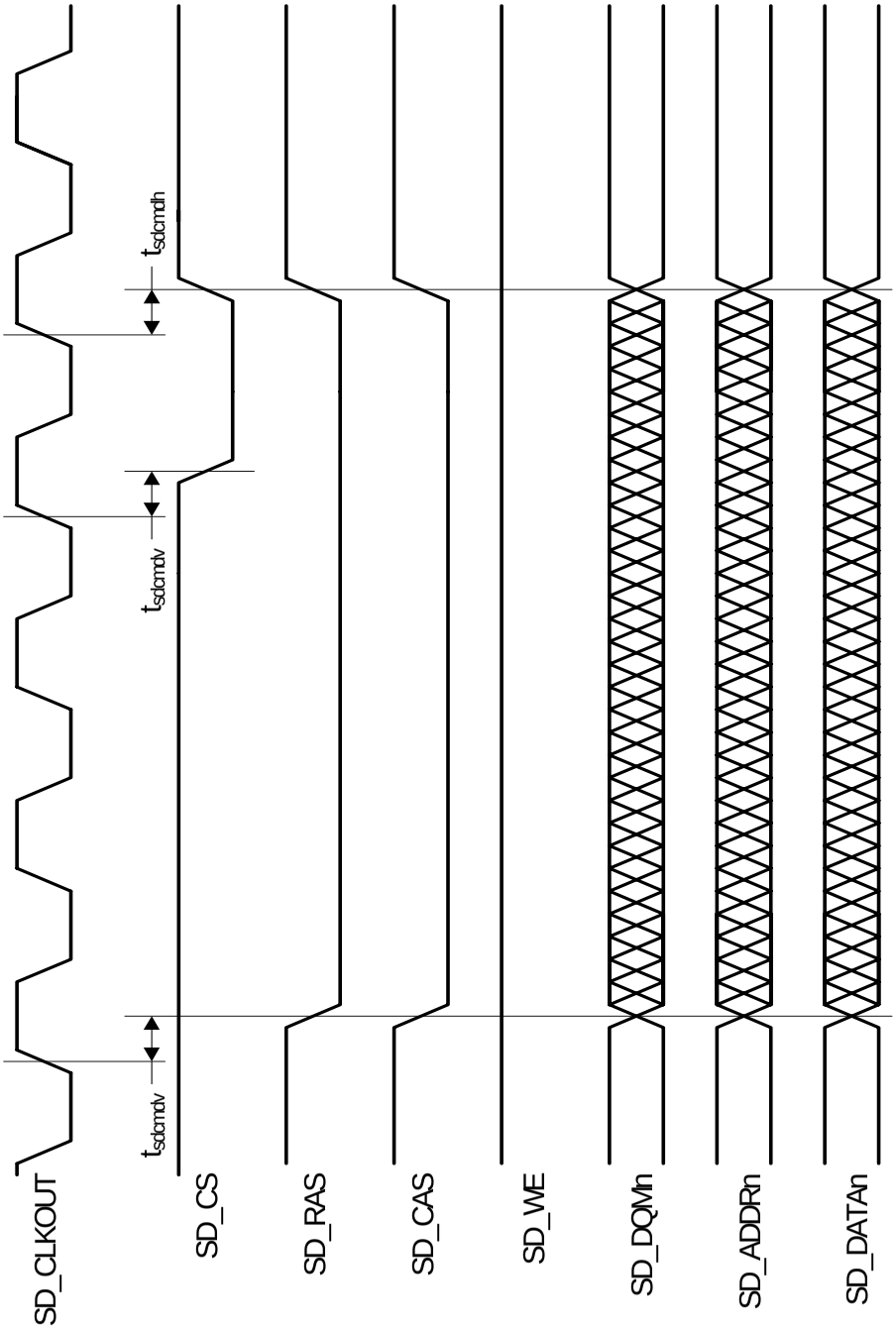


Figure 18. External Memory Interface - SDRAM Auto Refresh Cycle

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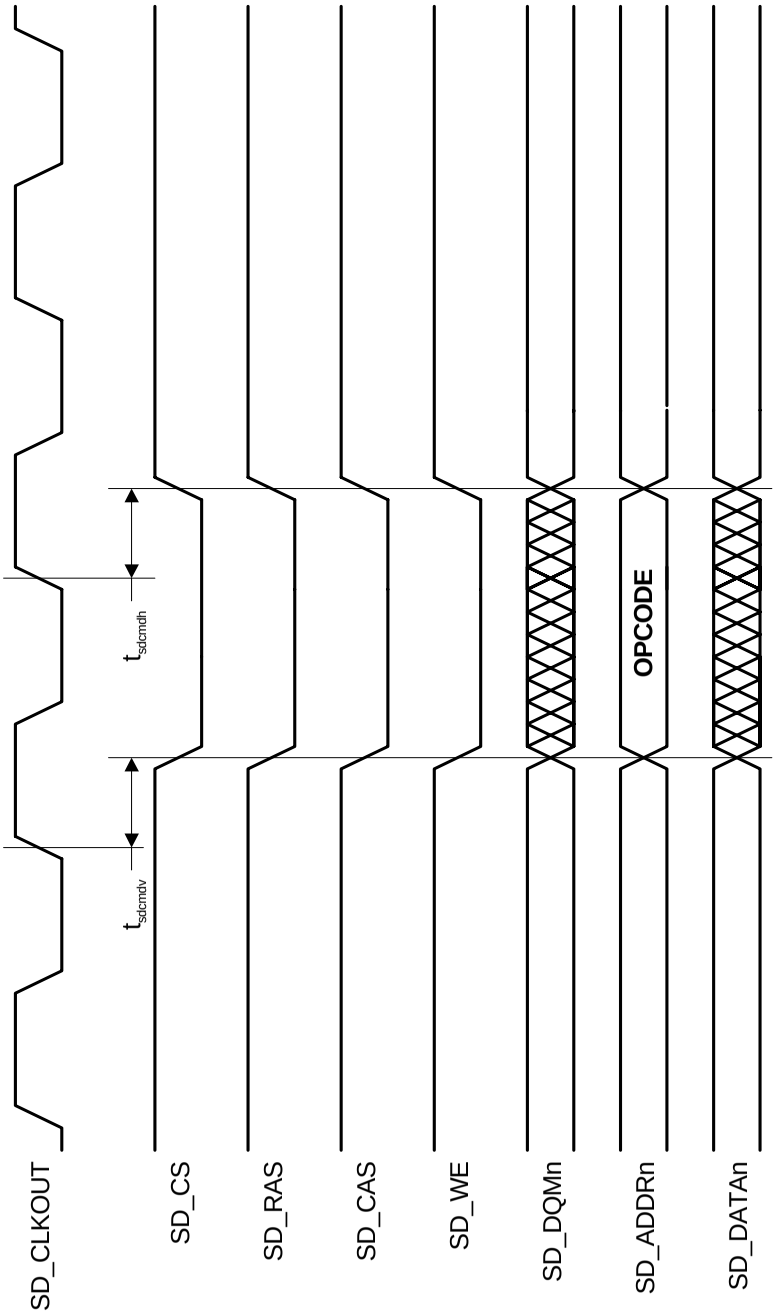


Figure 19. External Memory Interface - SDRAM Load Mode Register Cycle

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6. Ordering Information

The CS4970x4 family part number is described as follows:

CS497NNI-XYZ

where

NN - Product Number Variant

I - ROM ID Number

X - Product Grade

Y - Package Type

Z - Lead (Pb) Free

Table 4. Ordering Information

Part No.	Grade	Temp. Range	Container	Package
CS497004-CQZ	Commercial	0 to +70 °C	Tray	144-pin LQFP
CS497004-CQZR	Commercial	0 to +70 °C	Reel	
CS497024-CVZ	Commercial	0 to +70 °C	Tray	128-pin LQFP
CS497024-CVZR	Commercial	0 to +70 °C	Reel	

Note: Please contact the factory for availability of the -D (automotive grade) package.

7. Environmental, Manufacturing, and Handling Information

Table 5. Environmental, Manufacturing, & Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS497004-CQZ	260 °C	3	7 Days
CS497004-CQZR	260 °C	3	7 Days
CS497024-CVZ	260 °C	3	7 Days
CS497024-CVZR	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

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8. Device Pin-Out Diagram

8.1 128-Pin LQFP Pin-Out Diagram

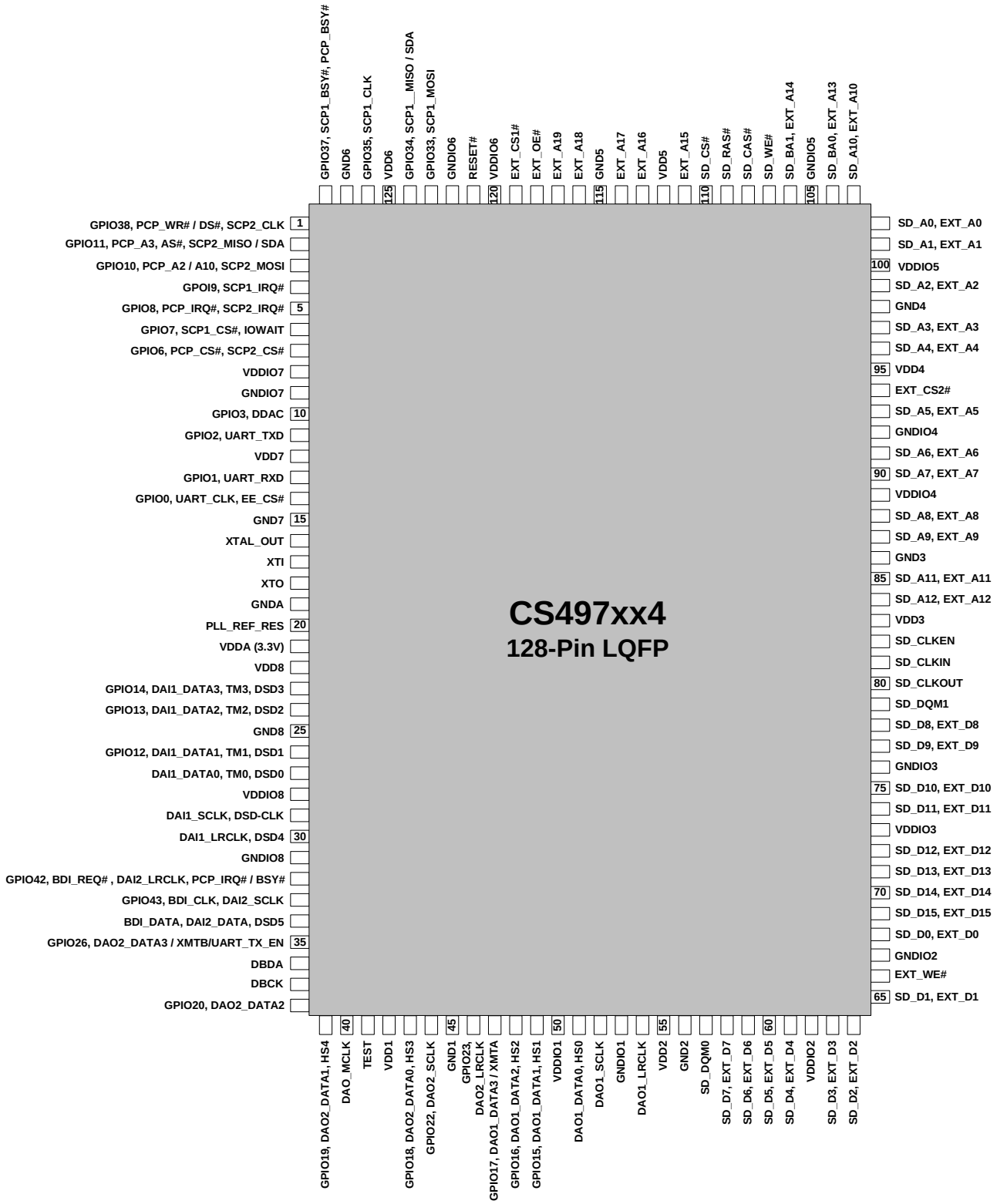


Figure 20. 128-Pin LQFP Pin-Out Diagram

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8.2 144-Pin LQFP Pin-Out Diagram

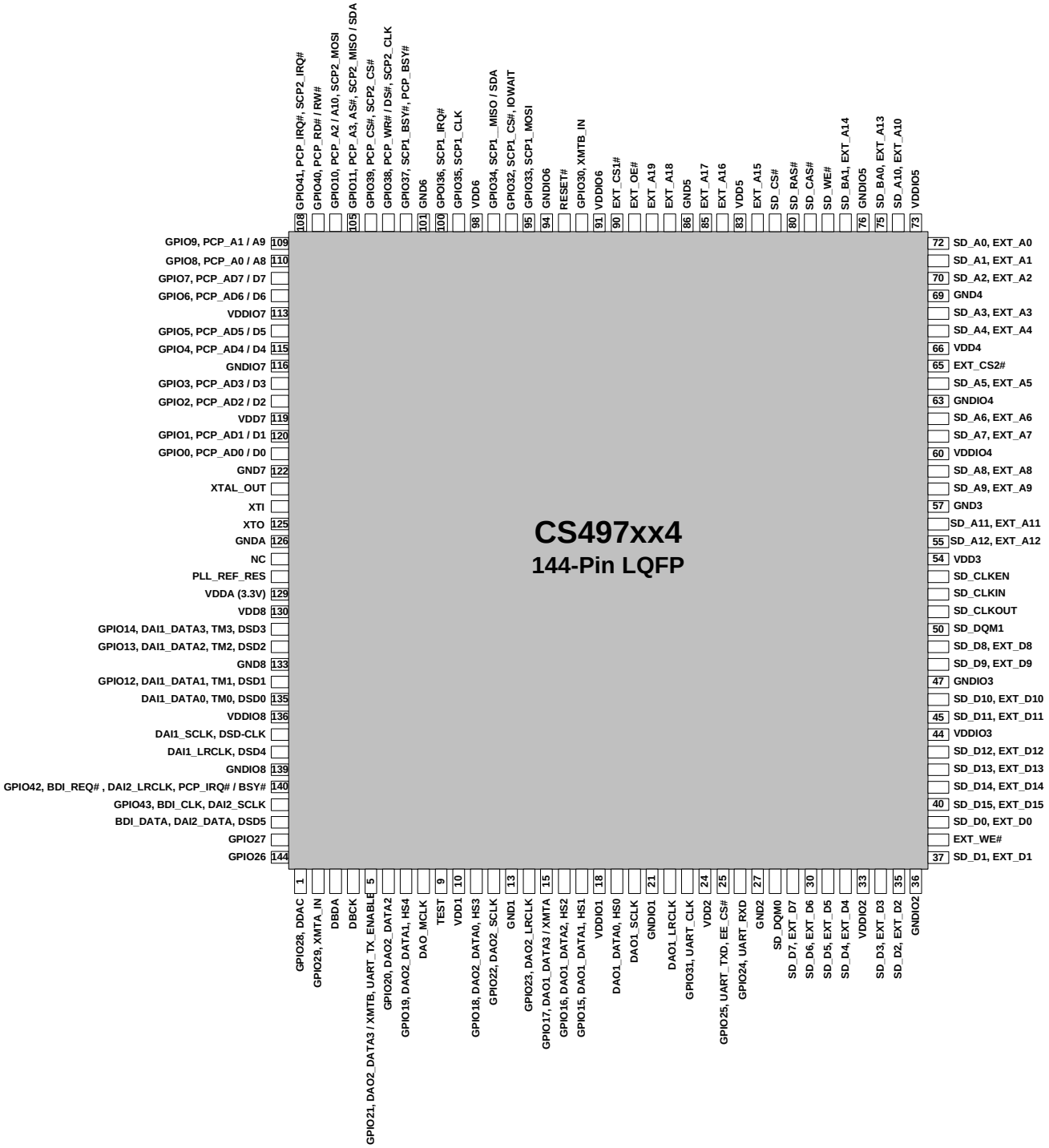


Figure 21. 144-Pin LQFP Pin-Out Diagram

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9. Package Mechanical Drawings

9.1 128-Pin LQFP Package Drawing

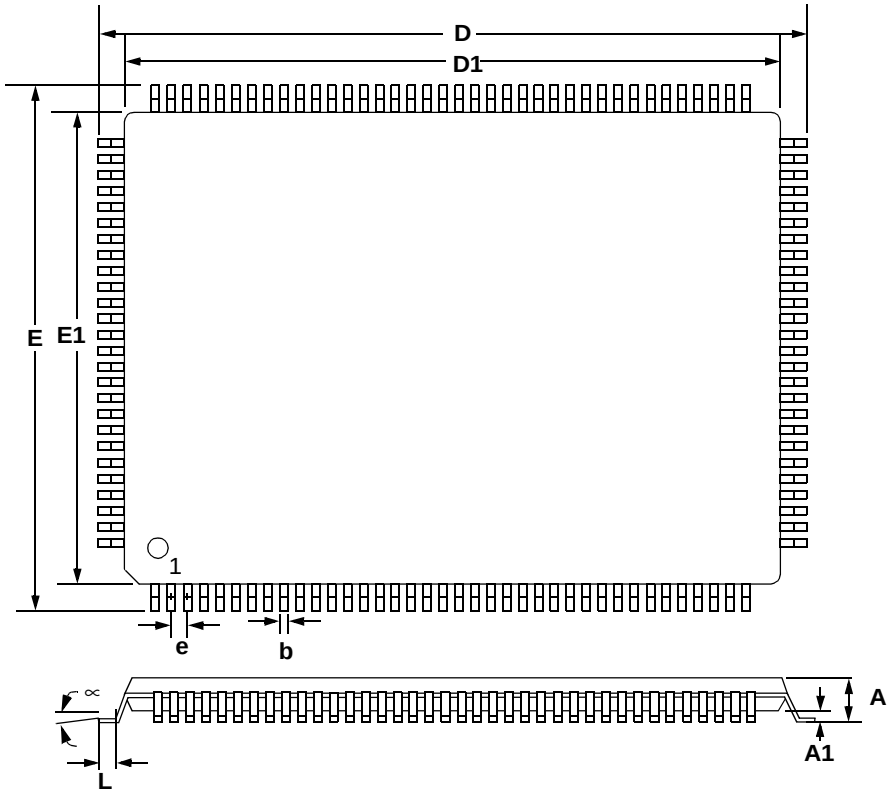


Figure 22. 128-Pin LQFP Package Drawing

Table 6. 128-Pin LQFP Package Characteristics

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.60	---	---	.063”
A1	0.05	---	0.15	.002”	---	.006”
b	0.17	0.22	0.27	.007”	.009”	.011”
D	22.00 BSC			.866”		
D1	20.00 BSC			.787”		
E	16.00 BSC			.630”		
E1	14.00 BSC			.551”		
e	0.50 BSC			.020”		
q	0°	3.5	7°	0°	3.5	7°
L	0.45	0.60	0.75	.018”	.024”	.030”
L1	1.00 REF			.039” REF		
TOLERANCES OF FORM AND POSITION						
ddd	0.08			.003”		

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9.2 144-Pin LQFP Package Drawing

Notes:

Controlling dimension is millimeter.

Dimensioning and tolerancing per ASME Y14.5M-1994.

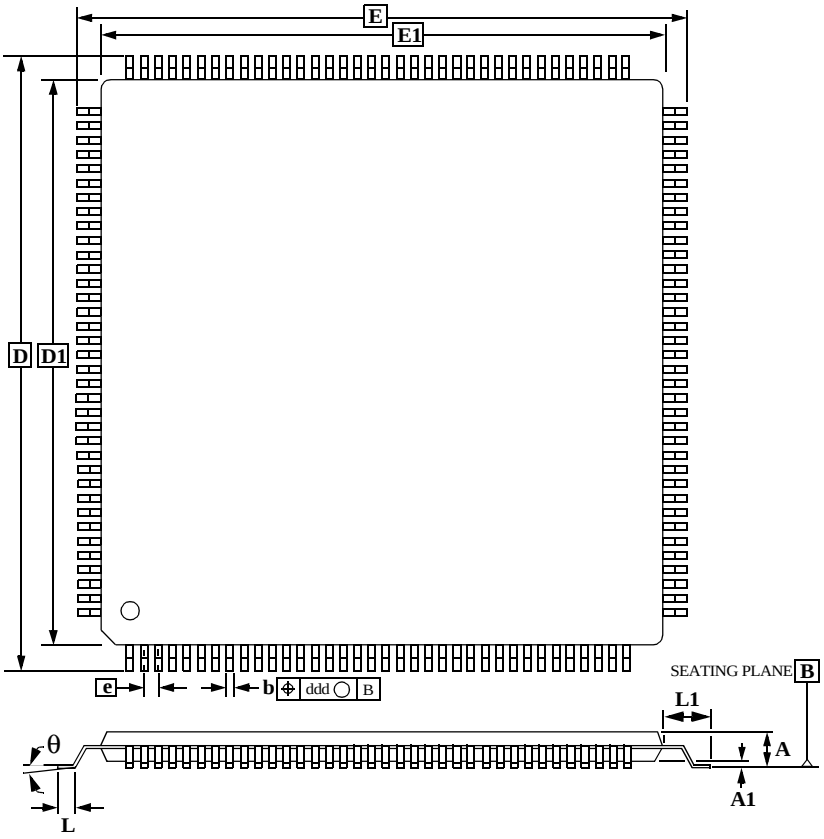


Figure 23. 144-Pin LQFP Package Drawing

Table 7. 144-Pin LQFP Package Characteristics

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.60	---	---	.063”
A1	0.05	---	0.15	.002”	---	.006”
b	0.17	0.22	0.27	.007”	.009”	.011”
D	22.00 BSC			.866”		
D1	20.00 BSC			.787”		
E	22.00 BSC			.866”		
E1	20.00 BSC			.787”		
e	0.50 BSC			.020”		
q	0°	---	7°	0°	---	7°
L	0.45	0.60	0.75	.018”	.024”	.030”
L1	1.00 REF			.039” REF		
TOLERANCES OF FORM AND POSITION						
ddd	0.08			.003”		

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10. Revision History

Revision	Date	Changes
A1	FEB 2007	Advance Release.
PP1	MAY 2007	Removed Advanced Product watermark, corrected logo, and added “Preliminary Product Information” on first page and modified legal information to reflect Preliminary Product status.
PP2	JULY 2007	Added notice about status of DTS-HD license on page 1 and 7.
PP3	OCT 2007	Updated the Tspidsu, Tspickl, and Tspickh timing parameters for master mode SPI. This applies to both SPI ports. Removed DTS-HD license notice inserted in version PP2. The license for the DTS-HD decoder is now in place.Updated Pin Assignments in 144-Pin LQFP Pin-Out Diagram, removing EE_CS from Pin 7 and adding EE_CS to Pin 25.
PP4	December 20, 2007	Updated DAO timing specifications and timing diagrams. Changed product naming conventions in Table 4 and Table 5. Changed references to *CS4970x4 Hardware User’s Manual* to *CS4970x4 System Designer’s Guide.* Changed references to *CS4970x4 Firmware User’s Manual* to *CS4970x4 System Designer’s Guide*
PP5	May 28, 2008	Added 128-Pin LQFP Pin-Out and Package drawings. Changed part numbering in Section 6.and Section 7. Added device and firmware selection guide in Table 2.
PP6	August 4, 2008	Added typical crystal frequency values in Table Footnote 1 and the Max and Min values of F_{xtal} in Section 5.7. Removed DSD Phase Modulation Mode from Section 5.17. Removed reference to MCLK in Section 5.17. Redefined Master mode clock speed for SCP_CLK in Section 5.10.. Redefined DC leakage characterization data in Section 5.3, correcting units of measurement. Modified Footnote 1 under Section 5.9. Changed product family numbering from CS497xx to CS4970x4. Corrected product listings in table under Section 5.8 “Switching Characteristics — Internal Clock” on page 13.
PP7	September 30, 2008	Removed references to External Parallel Flash / SRAM Interface.

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Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
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