LM1771 Low-Voltage Synchronous Buck Controller with Precision Enable and No External Compensation

Check for Samples: LM1771

FEATURES

- **Input Voltage Range of 2.8V to 5.5V**
- **0.8V Reference Voltage**
- **Precision Enable**
- **No Compensation Required**
- **Constant Frequency Across Input Range**
- **Low Quiescent Current of 400 µA**
- **Internal Soft-start**
- **Short Circuit Protection**
- **6-Pin WSON Package and 8-Pin VSSOP Package**

APPLICATIONS

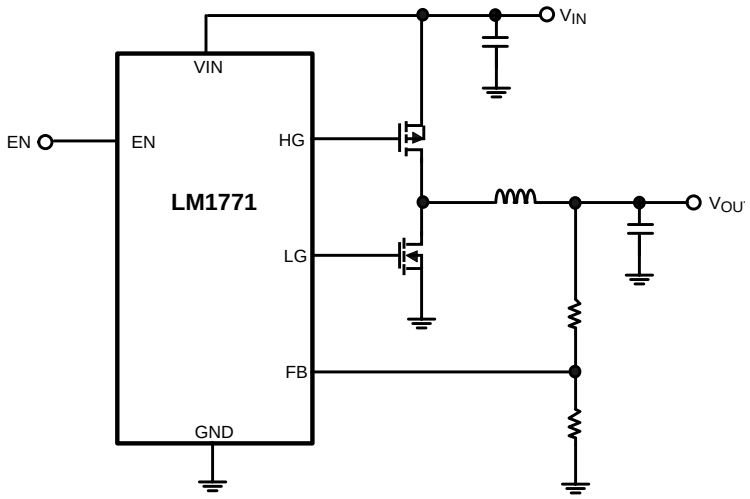
- **Simple To Design, High Efficiency Step Down Switching Regulators**
- **FPGAs, DSPs, and ASIC Power Supplies**
- **Set-Top Boxes**
- **Cable Modems**
- **Printers**
- **Digital Video Recorders**
- **Servers**
- **Graphic Cards**

DESCRIPTION

The LM1771 is an efficient synchronous buck switching controller with a precision enable requiring no external compensation. The constant on-time control scheme provides a simple design free of compensation components, allowing minimal component count and board space. The precision enable pin allows flexibility in sequencing multiple rails and setting UVLO. The LM1771 also incorporates a unique input feed-forward to maintain a constant frequency independent of the input voltage. The LM1771 is optimized for a low voltage input range of 2.8V to 5.5V and can provide an adjustable output as low as 0.8V. Driving an external high side PFET and low side NFET it can provide efficiencies as high as 95%.

Three versions of the LM1771 are available depending on the switching frequency desired for the application. Nominal switching frequencies are in the range of 100kHz to 1000kHz.

Typical Application Circuit



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Connection Diagram

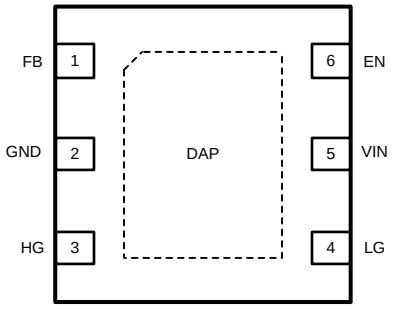

Figure 1. 6-Pin WSON (3mm x 3mm)
Top View
See NGG0006A Package

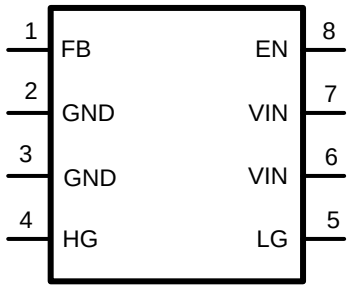

Figure 2. 8-Pin VSSOP
Top View
See DGK Package

PIN DESCRIPTIONS

Pin #		Name	Function
WSON	VSSOP		
1	1	FB	Feedback Pin
2	2, 3	GND	Ground
3	4	HG	PFET Gate Drive
4	5	LG	NFET Gate Drive
5	6, 7	VIN	Input Supply
6	8	EN	Enable Pin
DAP		-	Die Attach Pad is internally connected to GND, but it cannot be used as the primary GND connection

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

V_{IN}		-0.3V to 6V
EN, FB, HG, LG		-0.3V to V_{IN}
Storage Temperature Range		−65°C to 150°C
Junction Temperature		150°C
Lead Temperature	(soldering, 10sec)	260°C
	ESD Rating	2kV

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see ELECTRICAL CHARACTERISTICS.

OPERATING RATINGS

V_{IN} to GND	2.8V to 5.5V
Junction Temperature Range (T_J)	−40°C to +125°C

ELECTRICAL CHARACTERISTICS

Specifications with standard typeface are for T_J = 25°C, and those in **bold face type** apply over the full Junction Temperature Range (−40°C to +125°C). Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only. Unless otherwise specified V_{IN} = 3.3V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{FB}	Feedback pin voltage		**0.782**	0.8	**0.818**	V
I_Q	Quiescent current	V_{FB} = 0.9V		400	**700**	µA
T_{ON}	Switch On-Time	LM1771S - (500ns)	**0.4**	0.5	**0.6**	µs
		LM1771T - (1000ns)	**0.8**	1.0	**1.2**	
		LM1771U - (2000ns)	**1.6**	2.0	**2.4**	
T_{OFF_MIN}	Minimum Off-Time	LM1771S - (500ns)		150	**250**	ns
		LM1771T - (1000ns)		135	**225**	
		LM1771U - (2000ns)		120	**220**	
T_D	Gate Drive Dead-Time			70		ns
V_{IH_EN}	EN Pin Rising Threshold		**1.15**	1.2	**1.25**	V
V_{EN_HYS}	EN Pin Hysteresis			50	**200**	mV
I_{FB}	Feedback pin bias current	V_{FB} = 0.9V		50		nA
V_{UVLO}	Under-voltage lock out	V_{IN} Rising Edge		2.65	**2.8**	V
V_{UVLO_HYS}	Under-voltage lock out hysteresis			50		mV
V_{SC_TH}	Feedback pin Short Circuit Latch Threshold		**0.42**	0.55	**0.65**	V
$R_{DS(ON)\ 1}$	HG FET driver pull-up On resistance	I_{HG} = 20 mA		4		Ω
$R_{DS(ON)\ 2}$	HG FET driver pull-down On resistance	I_{HG} = 20 mA		6		Ω
$R_{DS(ON)\ 3}$	LG FET driver pull-up On resistance	I_{LG} = 20 mA		4		Ω
$R_{DS(ON)\ 4}$	LG FET driver pull-down On resistance	I_{LG} = 20 mA		6		Ω

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TYPICAL PERFORMANCE CHARACTERISTICS

All curves taken at VIN = 3.3V with configuration in typical application circuit shown in APPLICATION INFORMATION section of this datasheet. T_J = 25°C, unless otherwise specified.

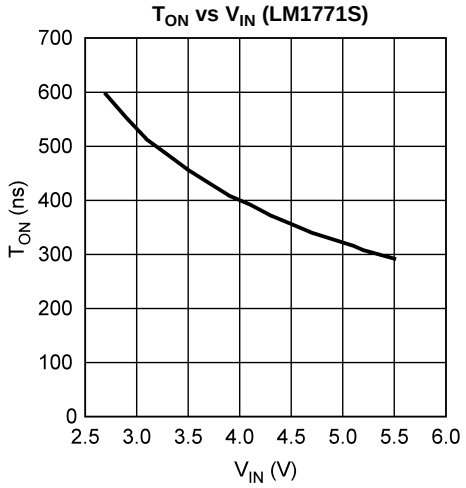


Figure 3.

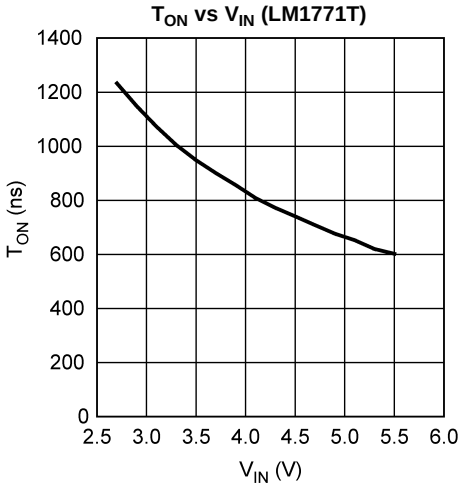
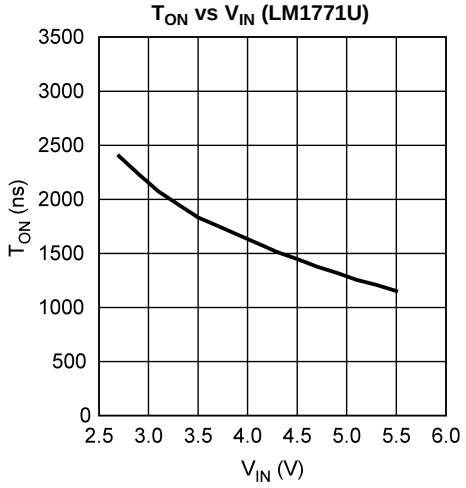


Figure 4.



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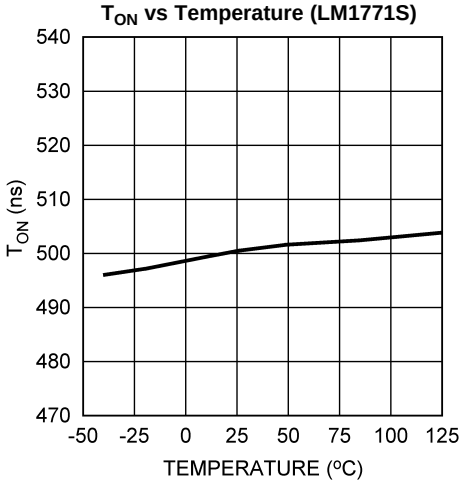

Figure 6.

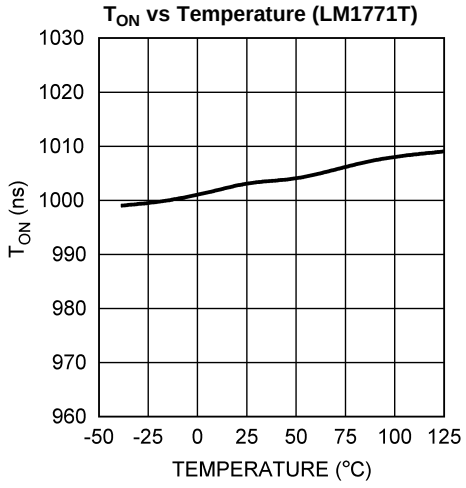

Figure 7.

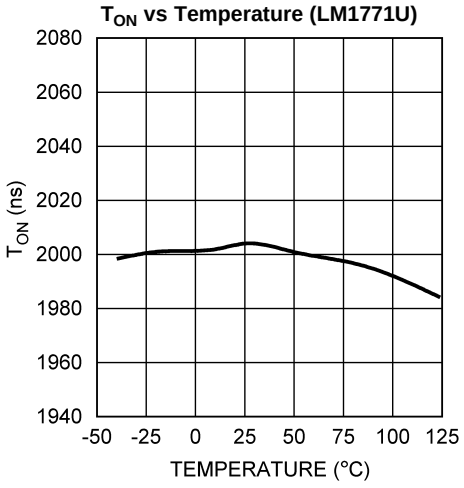

Figure 8.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

All curves taken at VIN = 3.3V with configuration in typical application circuit shown in APPLICATION INFORMATION section of this datasheet. T_J = 25°C, unless otherwise specified.

T_{OFF} vs Temperature (LM1771S)

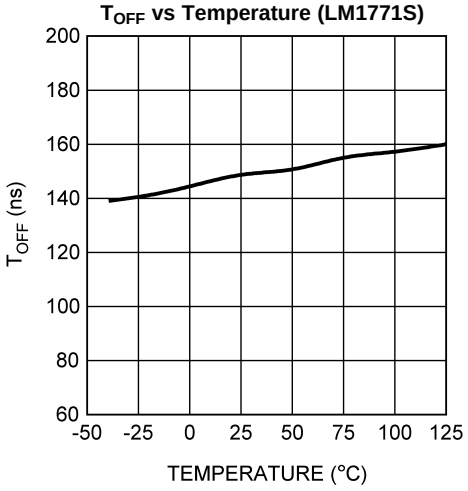

Figure 9.

T_{OFF} vs Temperature (LM1771T)

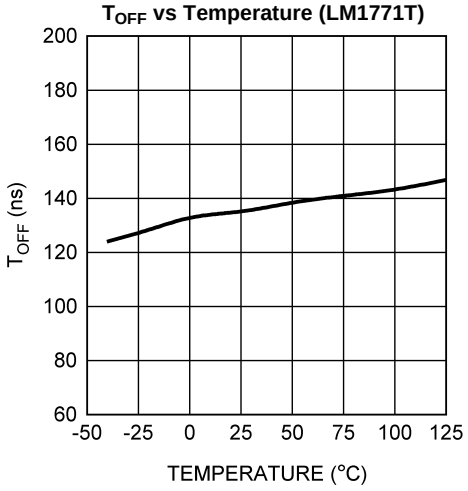

Figure 10.

T_{OFF} vs Temperature (LM1771U)

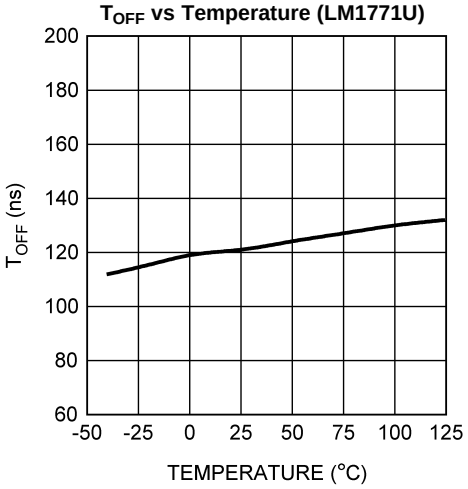

Figure 11.

Feedback Voltage vs Temperature

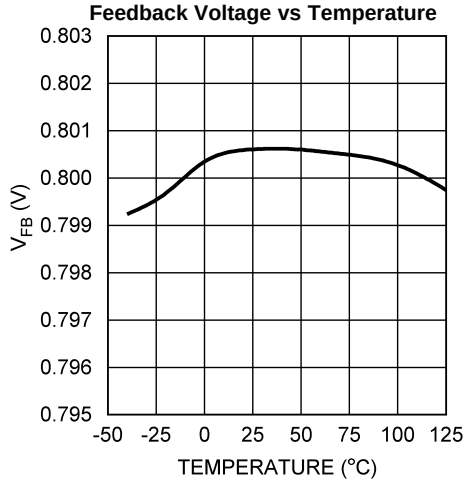

Figure 12.

V_{EN} Threshold vs Temperature

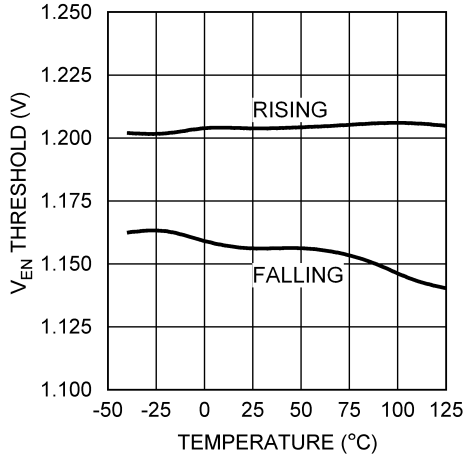

Figure 13.

Short Circuit Threshold vs Temperature

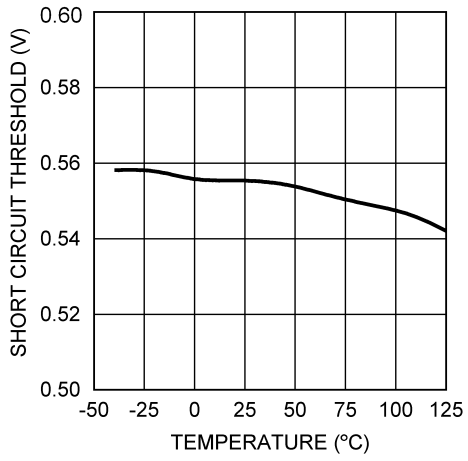

Figure 14.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

All curves taken at VIN = 3.3V with configuration in typical application circuit shown in APPLICATION INFORMATION section of this datasheet. T_J = 25°C, unless otherwise specified.

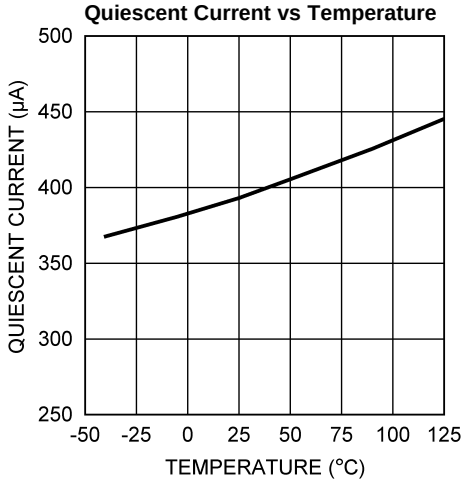

Figure 15.

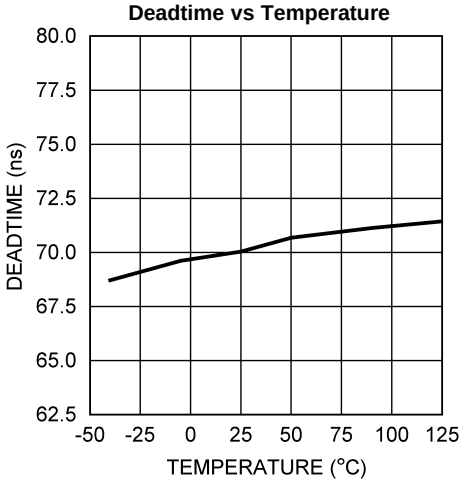

Figure 16.

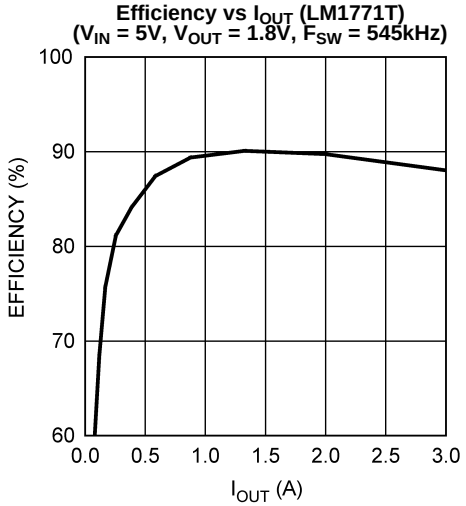

Figure 17.

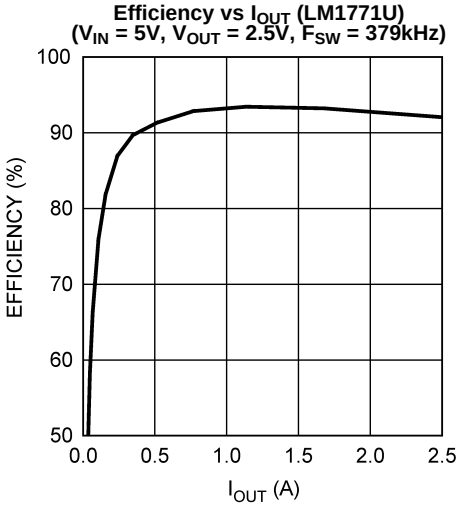

Figure 18.

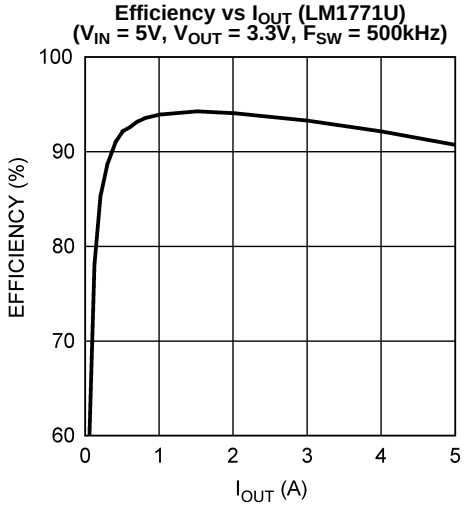

Figure 19.

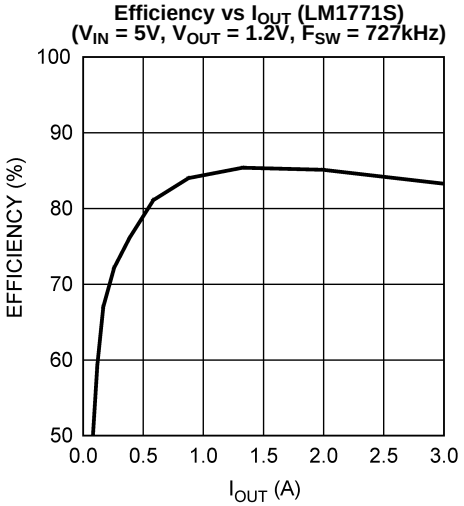

Figure 20.

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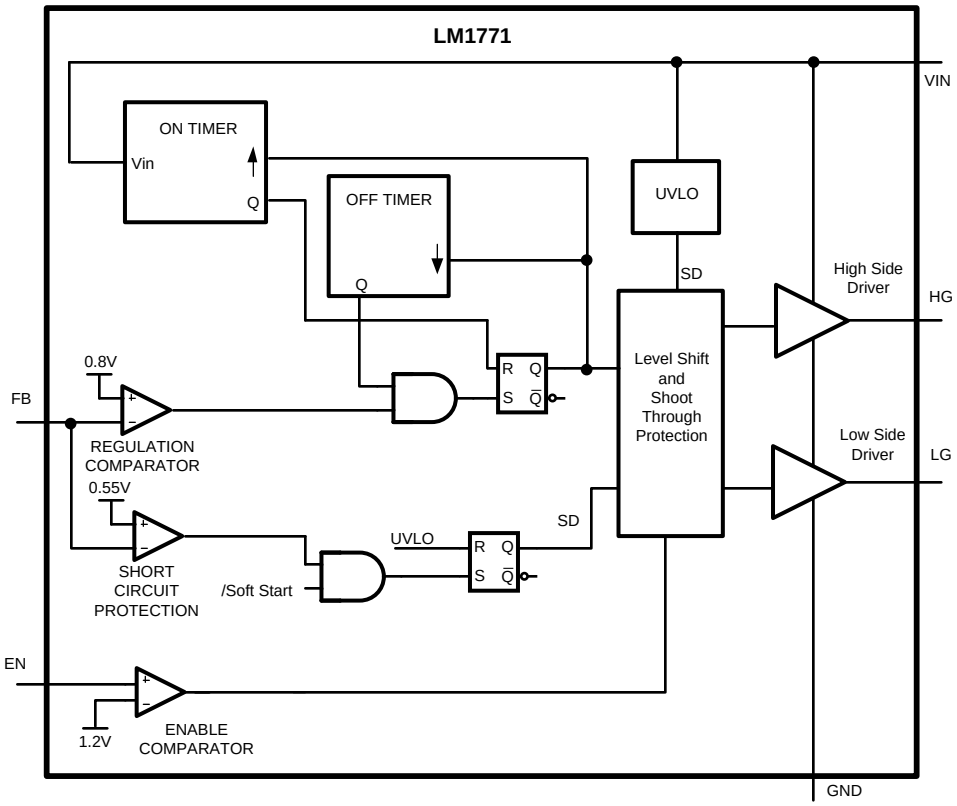
BLOCK DIAGRAM



APPLICATION INFORMATION

Theory of Application

The LM1771 synchronous buck controller has a control scheme that is referred to as adaptive on-time control. This topology relies on a fixed switch on-time to regulate the output voltage. This on-time is internally set by EEPROM and is available with three different set-points to allow for different frequency options. The LM1771 automatically adjusts the on-time during operation inversely with the input voltage (VIN) to maintain a constant frequency. Therefore the switching frequency during continuous conduction mode is independent of the inductor and capacitor size unlike hysteretic switchers.

At the beginning of the cycle the LM1771 turns on the high side PFET for a fixed duration. This on-time is predetermined (internally set by EEPROM and adjusted by V_{IN}) and the switch will not turn off until the timer has completed its period. The PFET will then turn off for a minimum pre-determined time period. This minimum T_{OFF} of 150ns is internally set and cannot be adjusted. This is to prevent false triggering from occurring on the comparator due to noise from the SW node transition. After the minimum T_{OFF} period has expired, the PFET will remain off until the comparator trip-point has been reached. Upon passing this trip-point (set at 0.8V at the feedback pin), the PFET will turn back on and the process will repeat, thus regulating the output.

The NFET control is complementary to the PFET control with the exception of a short dead-time to prevent shoot through from occurring.

Device Operation

Timing Opinion

Three versions of the LM1771 are available each with a predetermined T_{ON} set internally by EEPROM. This T_{ON} setting will determine the switching frequency for the application. Derivation and calculation of the switching frequency's dependence on V_{IN} and T_{ON} can be seen in the following section.

In a PWM buck switcher the following equations can be manipulated to obtain the switching frequency. The first equation shows the standard duty-cycle equation given by the volts-seconds balance on the inductor with the following equations defining standard relationships:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$T_{ON} = D \times T_P \quad (2)$$

$$T_P = \frac{1}{f_{SW}} \quad (3)$$

Using these equations and solving for duty-cycle:

$$D = f_{SW} \times T_{ON} \quad (4)$$

Frequency can now be expressed as:

$$F = \frac{V_{OUT}}{V_{IN} \times T_{ON}} \quad (5)$$

Or simply written as:

$$f_{SW} = \frac{V_{OUT}}{\alpha}$$

where

- $\alpha = V_{IN} \times T_{ON}$ (6)

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To maintain a set frequency in an application, α is always held constant by varying T_{ON} inversely with V_{IN}. The three versions of the LM1771 are identified by the on times at a V_{IN} of 3.3V for consistency. For clarification see the table below:

Product ID	T_{ON} @ 3.3V	α (V µs)
LM1771S	0.5µs	1.65
LM1771T	1.0µs	3.3
LM1771U	2.0µs	6.6

The variation of T_{ON} versus V_{IN} can also be expressed graphically. These graphs can be found in the typical curves section of the datasheet.

With α being a constant regardless of the version of the LM1771 used, Equation 6 shows that the only dependent variable remaining is V_{OUT}. Since V_{OUT} will be a constant in any application, the frequency will also remain constant. The switching frequency at which the application runs depends upon the V_{OUT} desired and the LM1771 version chosen. For any V_{OUT}, three frequency options (LM1771 versions) can be selected. This can be seen in the table below. The recommended frequency range of operation is 100kHz to 1000kHz.

	Timing Options (1)		
VOUT	500ns	1000ns	2000ns
0.8	485	242	121
1	606	303	152
1.2	727	364	182
1.5	909	455	227
1.8	1091	545	273
2.5	1515	758	379
3.3	2000	1000	500

(1) Switching Frequency (kHz) of LM1771 based on output voltage and timing option.

Short-Circuit Protection

The LM1771 has an internal short circuit comparator that constantly monitors the feedback node (except during soft-start). If the feedback voltage drops below 0.55V (equivalent to the output voltage dropping below 68% of nominal), the comparator will trip causing the part to latch off. The LM1771 will not resume switching until the input voltage is taken below the UVLO threshold and then brought back into its normal operating range, or the part is disabled then re-enabled through the enable pin. The purpose of this function is to prevent a severe short circuit from causing damage to the application. Due to the fast transient response of the LM1771 a severe short on the output causing the feedback to drop would only occur if the load applied had an effective resistance that approaches the PMOS $R_{DS(ON)}$.

Precision Enable

The LM1771 features a precision enable circuit. If the voltage on the EN pin is 1.2V or greater, the part is enabled and switching will occur. If the enable voltage falls below 1.2V, the part will be placed into a shutdown state and the drivers will be tri-stated. This allows the LM1771 to be easily sequenced using a resistive divider from the output of another regulator, or the working input voltage range of the LM1771 to be set using a resistive divider on V_{IN}. There is no internal pull-up connected to the EN pin, so an external signal is required to initiate switching. It should be noted that when power is first applied to the LM1771, there is a slight delay before the enable comparator is functional. During this delay, typically on the order of 400 µs, the part will be disabled regardless of the voltage on the EN pin. The falling enable threshold features 50 mV of hysteresis

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Soft-Start

To limit in-rush current and allow for a controlled startup the LM1771 incorporates an internal soft-start scheme. Every time the enable voltage rises rises above 1.2V while V_{IN} is greater than the UVLO threshold, the LM1771 goes through an adaptive soft-start that limits the on-time and expands the minimum off-time. In addition the part will only activate the PMOS allowing a discontinuous mode of operation enabling a pre-biased startup. The time spent in soft-start will depend on the load applied to the output, but is usually close to a set time that is dependent on the timing option. The approximate soft-start time can be seen below for each timing option.

Product ID	Timing	T_{SS}
LM1771S	0.5 µs	1 ms
LM1771T	1.0 µs	1.2 ms
LM1771U	2.0 µs	1.8 ms

It should be noted that as soon as soft-start terminates the short-circuit protection is enabled. This means that if the output voltage does not reach at least 68% of its final value the part will latch off. Therefore, if the input supply is extremely slow rising such that at the end of soft-start the input voltage is still near the UVLO threshold, a timing option should be chosen to ensure that maximum duty-cycle permits the output to meet the minimum condition. As a general recommendation it is advisable to use the 2000 ns option (LM1771U) in conditions where the output voltage is 2.5V or greater to avoid false latch offs when there is concern regarding the input supply slew rate.

In some situations, the internal soft-start routine can create a slight overshoot on the output voltage. If this must be avoided, the use of a feed-forward capacitor as detailed in the Feed-Forward Capacitor section of this datasheet is recommended.

Jitter

The LM1771 utilizes an adaptive on-time control scheme that relies on the output voltage ripple to provide a consistent switching frequency. Under certain conditions, excessive noise can couple onto the feedback pin causing the switch node to appear to have a slight amount of jitter. This is not indicative of an unstable design. The output voltage will still regulate to the exact same value. Careful component selection and layout should minimize any external influence.

In addition to any external noise that can add to the jitter seen on the switch node, the LM1771 will always have a slight amount of switch jitter. This is because the LM1771 makes a small alteration in the reference voltage every 128 cycles to improve its accuracy and long term performance. This has the effect of causing a change in the switching frequency at that instant. When viewed on an oscilloscope this can be seen as a jitter in the switch node. The change in feedback voltage or output voltage, however, is almost indistinguishable.

DESIGN GUIDE

The following section walks the designer through the steps necessary to select the external components to build a fully functional power supply. As with any DC-DC converter numerous trade-offs are possible to optimize the design for efficiency, size or performance. These will be taken into account and highlighted throughout this discussion.

The first equation to calculate for any buck converter is duty-cycle. Ignoring conduction losses associated with the FETs and parasitic resistances it can be approximated by:

$$D = \frac{V_{OUT}}{V_{IN}} \tag{7}$$

A more accurate calculation for duty-cycle can be used that takes into account the voltage drops across the FETs. This equation can be used to determine the slight load dependency on switch frequency if needed. Otherwise the simplified equation works well for component calculation.

$$D = \frac{V_{OUT} + V_{DS_NMOS}}{V_{IN} + V_{DS_NMOS} + V_{DS_PMOS}} \tag{8}$$

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Frequency Selection

The LM1771 is available with three preset timing options that select the on-time and hence determine the switching frequency of the application. Increasing the switching frequency has the effect of reducing the inductor size needed for the application while requiring a slight trade-off in efficiency. The table below shows the same frequency table as shown earlier, with the exception that the recommended timing option for each V_{OUT} is highlighted. It is not recommended to use a high switching frequency with V_{OUT} equal to or greater than 2.5V due to the maximum duty-cycle limitations of the device coupled with the internal startup.

	Timing Options (1)		
V_{OUT}	500 ns	1000 ns	2000 ns
0.8	485	242	-
1	606	303	-
1.2	727	364	-
1.5	909	455	227
1.8	-	545	273
2.5	-	-	379
3.3	-	-	500

(1) Recommended switching frequency (kHz) based on output voltage and timing option.

Inductor Selection

The inductor selection is an iterative process likely requiring several passes before settling on a final value. The reason for this is because it influences the amount of ripple seen at the output, a critical component to ensure general stability of an adaptive on-time circuit. For the first pass at inductor selection the value can be obtained by targeting a maximum peak-to-peak ripple current equal to 30% of the maximum load current. The inductor current ripple (ΔI_L) can be calculated by:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}} \tag{9}$$

Therefore, L can be initially set to the following by applying the 30% rule:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{0.3 \times f_{SW} \times I_{OUT}} \tag{10}$$

The other features of the inductor that can be selected besides inductance value are saturation current and core material. Because the LM1771 does not have a current limit, it is recommended to have a saturation current higher than the maximum output current to handle any ripple or momentary over-current events. The core material also influences the saturation characteristics as ferrite materials have a hard saturation curve and care should be taken such that they never saturate during normal use. A shielded inductor or low profile unshielded inductor is recommended to reduce EMI. This also helps prevent any spurious noise from picking up on the feedback node resulting in unexpected tripping of the feedback comparator.

Output Capacitor

One of the most important components to select with the LM1771 is the output capacitor. This is because its size and ESR have a direct effect on the stability of the loop. A constant on-time control scheme works by sensing the output voltage ripple and switching the FETs appropriately. The output voltage ripple on a buck converter can be approximated by stating that the AC inductor ripple flows entirely into the output capacitor and is created by the ESR of the capacitor. This can be expressed in the following equation:

$$\Delta V_{OUT} = \Delta I_L \times R_{ESR} \tag{11}$$

To ensure stability, two constraints need to be met. The first is that there is sufficient ESR to create enough voltage ripple at the feedback pin. The recommendation is to have at least 10mV of ripple seen at the feedback pin. This can be calculated by multiplying the output voltage ripple by the gain seen through the feedback resistors. This gain, H, can be calculated below:

$$H = \frac{V_{FB}}{V_{OUT}} = \frac{0.8V}{V_{OUT}} \tag{12}$$

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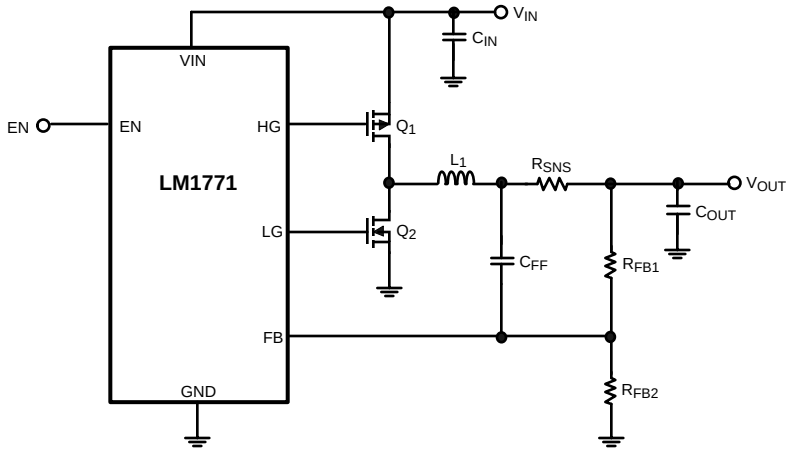
If the output voltage is fairly high, causing significant attenuation through the feedback resistors, a feed-forward capacitor can be used. This is actually recommended for most circuits as it improves performance. See the Feed-Forward Capacitor section for more details.

The second criteria is to ensure that there is sufficient ripple at the output that is in-phase with the switch. The problem exists that there is actually ripple caused by the capacitor charging and discharging, not only the ESR ripple. Since these are effectively out of phase, problems can exist. To avoid this issue it is recommended that the ratio of the two ripples (β) is always greater than 5. To calculate the minimum ESR value needed, the following equation can be used.

$$R_{ESR} \geq \frac{\beta \times t_P}{8 \times C} \tag{13}$$

In general the best capacitors to use are chemistries that have a known and consistent ESR across the entire operating temperature range. Tantalum capacitors or similar chemistries such as Niobium Oxide perform well along with certain families of Aluminum Electrolytics. Small value POSCAPs and SP CAPs also work as they have sufficient ESR. When used in conjunction with a low value inductor it is possible to have an extremely stable design. The only capacitors that require modification to the circuit are ceramic capacitors. Ceramic capacitors cause problems meeting both criteria because they have low ESR and low capacitance. Therefore, if they are to be used, an external ESR resistor (R_{SNS}) should be added. This can be seen below in the following circuit.



This circuit uses an additional resistor in series with the inductor to add ripple at the output. It is placed in this location and used in combination with the feed-forward capacitor (C_{FF}) to provide ripple to the feedback pin, without adding ripple or a DC offset to the output. The benefit of using a ceramic capacitor is still obtained with this technique. Because the addition of the resistor results in power loss, this circuit implementation is only recommended for low currents (2A and below). The power loss and rating of the resistor should be taken into account when selecting this component.

This circuit implementation utilizing the feed-forward capacitor begins to experience limitations when the output voltage is small. Previously the circuit relied on the C_{FF} for all the ripple at the feedback node by assuming that the resistor divider was negligible. As V_{OUT} decreases this can not be assumed. The resistor divider contributes a larger amount of ripple which is problematic as it is also out of phase. Therefore the resistor location should be changed to be in series with the output capacitor. This can be viewed as adding an effective ESR to the output capacitor.

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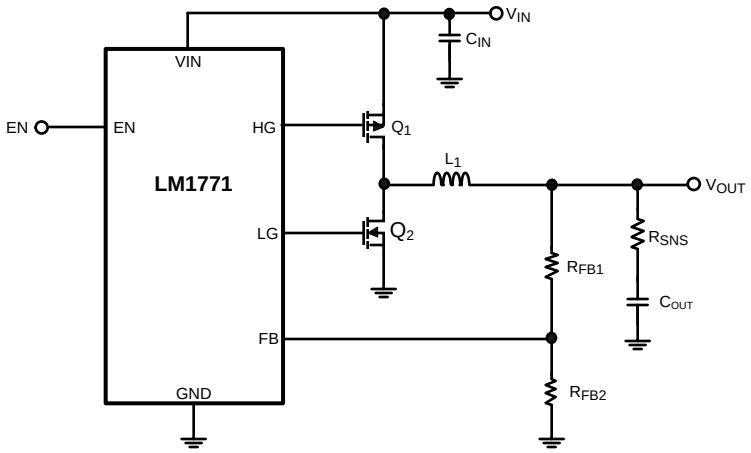

Feed-Forward Capacitor

The feed-forward capacitor is used across the top feedback resistor to provide a lower impedance path for the high frequency ripple without degrading the DC accuracy. Typically the value for this capacitor should be small enough to prevent load transient errors because of the discharging time, but large enough to prevent attenuation of the ripple voltage. In general a small ceramic capacitor in the range of 1nF to 10nF is sufficient.

If C_{FF} is used then it can be assumed that the ripple voltage seen at the feedback pin is the same as the ripple voltage at the output. The attenuation factor H no longer needs to be used. However, in these conditions, it is recommended to have a minimum of 20mV ripple at the feedback pin. The use of a C_{FF} capacitor is recommended as it improves the regulation and stability of the design. However, its benefit is diminished as V_{OUT} starts approaching V_{REF} , therefore it is not needed in this situation.

Input Capacitor

The dominating factor that usually sets an input capacitors' size is the current handling ability. This is usually determined by the package size and ESR of the capacitor. If these two criteria are met then there usually should be enough capacitance to prevent impedance interactions with the source. In general it is recommended to use a ceramic capacitor for the input as they provide a low impedance and small footprint. One important note is to use a good dielectric for the ceramic capacitor such as X5R or X7R. These provide better over temperature performance and also minimize the DC voltage derating that occurs on Y5V capacitors. To calculate the input capacitor RMS current, the equation below can be used:

$$I_{CIN_RMS} = I_{OUT} \sqrt{D\left(1 - D + \frac{\Delta I_L^2}{12 \times I_{OUT}^2}\right)} \quad (14)$$

which can be approximated by,

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D(1 - D)} \quad (15)$$

MOSFET Selection

The two FETs used in the LM1771 requires attention to selection of parameters to ensure optimal performance of the power supply. The high side FET should be a PFET and the low side an NFET. These can be integrated in one package or as two separate packages. The criteria that matter in selection are listed below:

VDS Voltage Rating

The first selection criteria is to select FETs that have sufficient V_{DS} voltage ratings to handle the maximum voltage seen at the input plus any transient spikes that can occur from parasitic ringing. In general most FETs available for this application will have ratings from 8V to 20V. If a larger voltage rating is used then the performance will most likely be degraded because of higher gate capacitance.

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RDSON

The $R_{DS(ON)}$ specification is important as it determines several attributes of the FET and the overall power supply. The first is that it sets the maximum current of the FET for a given package. A lower $R_{DS(ON)}$ will permit a higher allowable current and reduce conduction losses, however, it will increase the gate capacitance and the switching losses.

Gate Drive

The next step is to ensure that the FETs are capable of switching at the low Vin supplies used by the LM1771. The FET should have the Rdson specified at either 1.8V or 2.5V to ensure that it can switch effectively as soon as the LM1771 starts up.

Gate Charge

Because the LM1771 utilizes a fixed dead-time scheme to prevent cross conduction, the FET transitions must occur in this time. The rise and fall time of the FETs gate can be influenced by several factors including the gate capacitance. Therefore the total gate charge of both FETs should be limited to less than 20nC at 4.5V V_{GS}. The lower the number the faster the FETs should switch and the better the efficiency.

Rise / Fall Times

A better indication of the actual switching times of the FETs can be found in their ELECTRICAL CHARACTERISTICS table. The rise and fall time should be specified and selected to be at a minimum. This helps improve efficiency and ensuring that shoot through does not occur.

Gate Charge Ratio

Another consideration in selecting the FETs is to pay attention to the Qgd / Qgs ratio. The reason for this is that proper selection can prevent spurious turn on. If we look at the NFET for example, when the FET is turning off, the gate signal will pull to ground. Conversely the PFET will be turning on, causing the SW node to rise towards V_{IN}. The gate to drain capacitance of the NFET couples the SW node to the gate and will cause it to rise. If this voltage is excessive, then it could weakly turn on the low side FET causing an efficiency loss. However, this coupling is mitigated by having a large gate to source capacitance of the FET, which helps to hold the gate voltage down. Ideally, a very low Qgd / Qgs would be ideal, but in practice it is common to find the number around 1. As a general rule, the lower the ratio, the better.

If the above selection criteria have been met it is useful to generate a figure of merit to allow comparison between the FETs. One such method is to multiply the $R_{DS(ON)}$ of the FET by the total gate charge. This allows an easy comparison of the different FETs available. Once again, the lower the product, the better.

Feedback Resistors

The feedback resistors are used to scale the output voltage to the internal reference value such that the loop can be regulated. The feedback resistors should not be made arbitrarily large as this creates a high impedance node at the feedback pin that is more susceptible to noise. A combined value of 50kΩ for the two resistors is adequate. To calculate the resistor values use the equation below. Typically the low side resistor is initially set to a pre-determined value such as 10 kΩ.

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{V_{FB}} - 1\right) \quad (16)$$

where

- V_{FB} is the internal reference voltage that can be found in the ELECTRICAL CHARACTERISTICS table or approximated by 0.8V

The output voltage value can be set in a precise manner by taking into account the fact that the reference voltage is regulating the bottom of the output ripple as opposed to the average value. This relationship is shown in the figure below.

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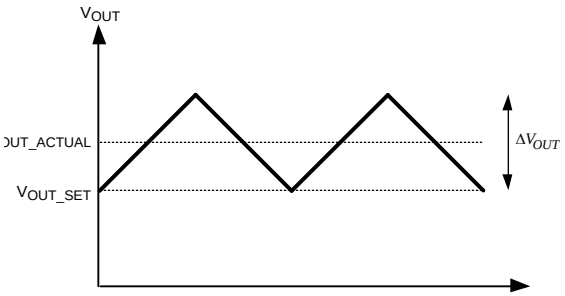

It can be seen that the average output voltage (V_{OUT_ACTUAL}) is higher than the output voltage (V_{OUT_SET}) that was calculated by the earlier equation by exactly half the output voltage ripple. The output voltage that is targeted for regulation may then be appended according to the voltage ripple. This can be seen below:

$$V_{OUT_ACTUAL} = V_{OUT_SET} + ½\Delta V_{OUT} = V_{OUT_SET} + ½\Delta I_L \times R_{ESR} \quad (17)$$

Efficiency Calculations

One of the most important parameters to calculate during the design stage is the expected efficiency of the system. This can help determine optimal FET selection and can be used to calculate expected temperature rise of the individual components. The individual losses of each component are broken down and the equations are listed below:

Quiescent Current

The quiescent current consumed by the LM1771 is one of the major sources of loss within the controller. However, from a system standpoint this is usually less than 0.5% of the overall efficiency. Therefore, it could easily be omitted but is shown for completeness:

$$P_{IQ} = V_{IN} \times I_Q \quad (18)$$

Conduction Loss

There are three losses associated with the external FETs. From the DC standpoint there is the I-squared R loss, caused by the on resistance of the FET. This can be modeled for the PMOS by:

$$P_{P_COND} = D \times R_{DSON_PMOS} \times I_{OUT}^2 \quad (19)$$

and the NMOS by:

$$P_{N_COND} = (1 - D) \times R_{DSON_NMOS} \times I_{OUT}^2 \quad (20)$$

Switching Loss

The next loss is the switching loss that is caused by the need to charge and discharge the gate capacitance of the FETs every cycle. This can be approximated by:

$$P_{P_SWITCH} = V_{IN} \times Q_{g_PMOS} \times f_{SW} \quad (21)$$

for the PMOS, and the same approach can be adapted for the NMOS:

$$P_{N_SWITCH} = V_{IN} \times Q_{g_NMOS} \times f_{SW} \quad (22)$$

Transitional Loss

The last FET power loss is the transitional loss. This is caused by switching the PMOS while it is conducting current. This approach only models the PMOS transition, the NMOS loss is considered negligible because it has minimal drain to source voltage when it switches due to the conduction of the body diode. Therefore the transitional loss of the PMOS can be modeled by:

$$P_{P_TRANSITIONAL} = 0.5 \times V_{IN} \times I_{OUT} \times f_{SW} \times (t_r + t_f) \quad (23)$$

t_r and t_f are the rise and fall times of the FET and can be found in their corresponding datasheet. Typically these numbers are simulated using a 6Ω drive, which corresponds well to the LM1771. Given this, no adjustment is needed.

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DCR Loss

The last source of power loss in the system that needs to be calculated is the loss associated with the inductor resistance (DCR) which can be calculated by:

$$P_{DCR} = R_{DCR} \times I_{OUT}^2 \quad (24)$$

Efficiency

The efficiency, η, can then be calculated by summing all the power losses and then using the equation below:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSSES}} \quad (25)$$

Thermals

By breaking down the individual power loss in each component it makes it easy to determine the temperature rise of each component. Generally the expected temperature rise of the LM1771 is extremely low as it is not in the power path. Therefore the only two items of concern are the PMOS and the NMOS. The power loss in the PMOS is the sum of the conduction loss and transitional loss, while the NMOS only has conduction loss. It is assumed that any loss associated with the body diode conduction during the dead-time is negligible.

For completeness of design it is important to watch out for the temperature rise of the inductor. Assuming the inductor is kept out of saturation the predominant loss will be the DC copper resistance. At higher frequencies, depending on the core material, the core loss could approach or exceed the DCR losses. Consult with the inductor manufacturer for appropriate temp curves based on current.

Layout

The LM1771, like all switching regulators, requires careful attention to layout to ensure optimal performance. The following steps should be taken to aid in the layout. For more information refer to Application Note AN-1299 SNVA074.

1. Ensure that the ground connections of the input capacitor, output capacitor and NMOS are as close as possible. Ideally these should all be grounded together in close proximity on the component side of the board.
2. Keep the switch node small to minimize EMI without degrading thermal cooling of the FETs.
3. Locate the feedback resistors close to the IC and keep the feedback trace as short as possible. Do not run any feedback traces near the switch node.
4. Keep the gate traces short and keep them away from the switch node as much as possible.
5. If a small bypass capacitor is used on V_{IN} (0.1µF) place it as close to the pin, with the ground connection as close to the chip ground as possible.

Typical Application Circuit

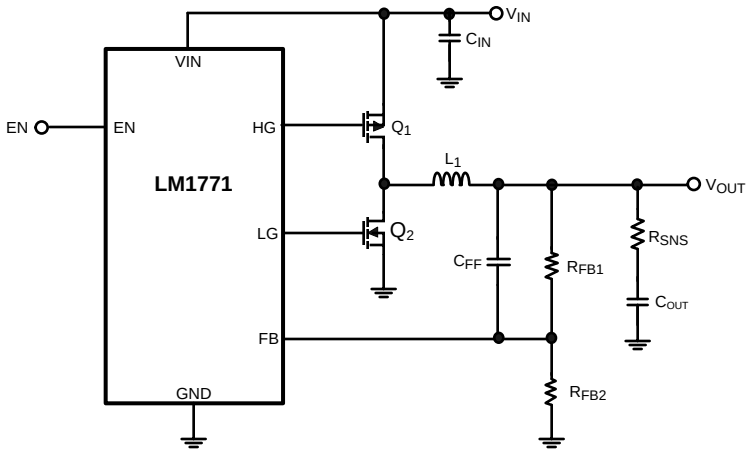

Figure 21. Example Circuit Schematic

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Bill of Materials (5V to 1.8V Conversion, f_{SW} = 1090kHz, I_{OUT} = 2A)

Designator	Description	Part Number	Quantity	Vendor
U_1	LM1771, 500ns	LM1771S	1	Texas Instruments
Q_1	PMOS	Si3867DV	1	Siliconix
Q_2	NMOS	Si3460DV	1	Siliconix
C_{IN}	22µF Capacitor, 0805	GRM21BR60J226ME39	1	Murata
C_{OUT}	100µF Capacitor, 6.3V, 100mΩ	TPSY107M006R0100	1	AVX
R_{FB1}	12.4kΩ Resistor, 0603	CRCW06031242F	1	Vishay
R_{FB2}	10kΩ Resistor, 0603	CRCW06031002F	1	Vishay
C_{FF}	1nF Capacitor, 0603	VJ0603102KXXA	1	Vishay
L	3.3µH Inductor	MSS7341-332NLB	1	Coilcraft

Bill of Materials (5V to 3.3V Conversion, f_{SW} = 500kHz, I_{OUT} = 5A)

Designator	Description	Part Number	Quantity	Vendor
U_1	LM1771, 200ns	LM1771U	1	Texas Instruments
Q_1	PMOS	Si9433BDY	1	Siliconix
Q_2	NMOS	Si4894DY	1	Siliconix
C_{IN}	100µF Capacitor, 1812	GRM43SR60J107ME20B	1	Murata
C_{OUT}	150µF Capacitor, 6.3V, 70mΩ	NOSD157M006R0070	1	AVX
R_{FB1}	29.4kΩ Resistor, 0805	CRCW08052942F	1	Vishay
R_{FB2}	10kΩ Resistor, 0805	CRCW08051002F	1	Vishay
C_{FF}	1nF Capacitor, 0805	VJ0805102KXXA	1	Vishay
L	2.2µH Inductor	DO3316P-222	1	Coilcraft

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REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	17

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM1771SMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SNRB	Samples
LM1771SSD/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	1771S	Samples
LM1771TMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SNSB	Samples
LM1771TSD/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	1771T	Samples
LM1771UMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SNTB	Samples
LM1771USD/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	1771U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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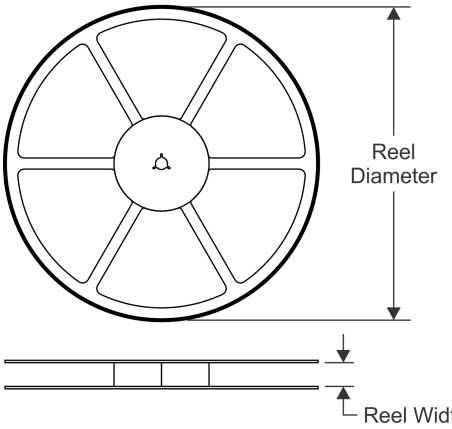
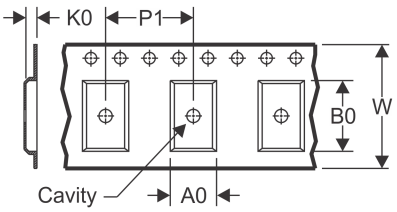
TAPE AND REEL INFORMATION

REEL DIMENSIONS

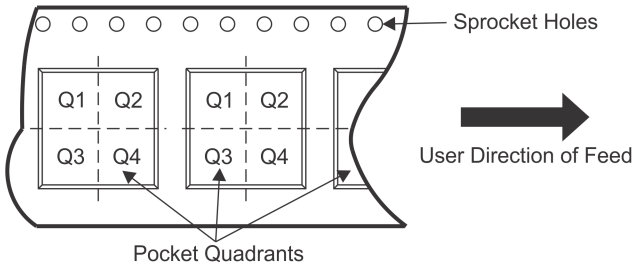


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

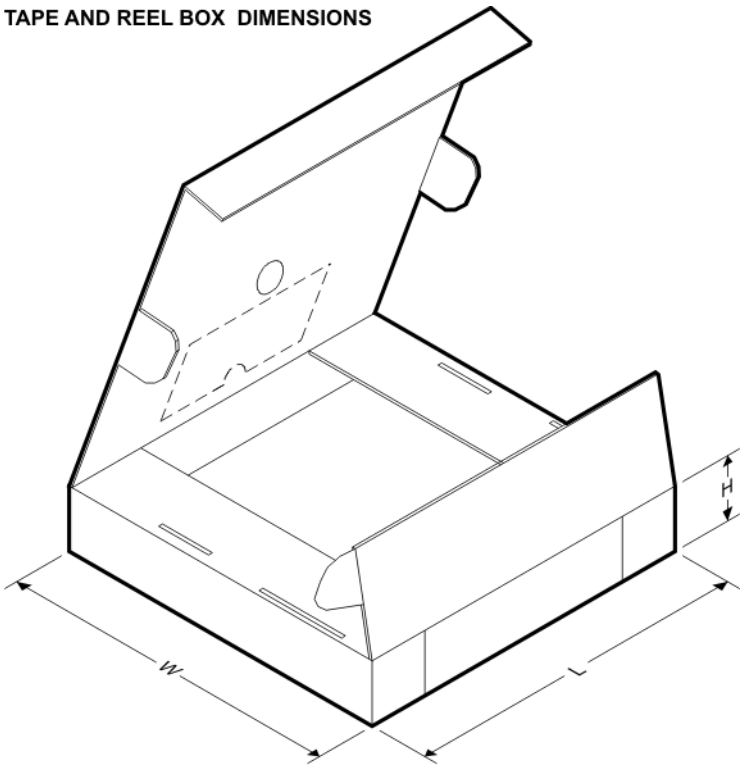
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM1771SMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM1771SSD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM1771TMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM1771TSD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM1771UMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM1771USD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

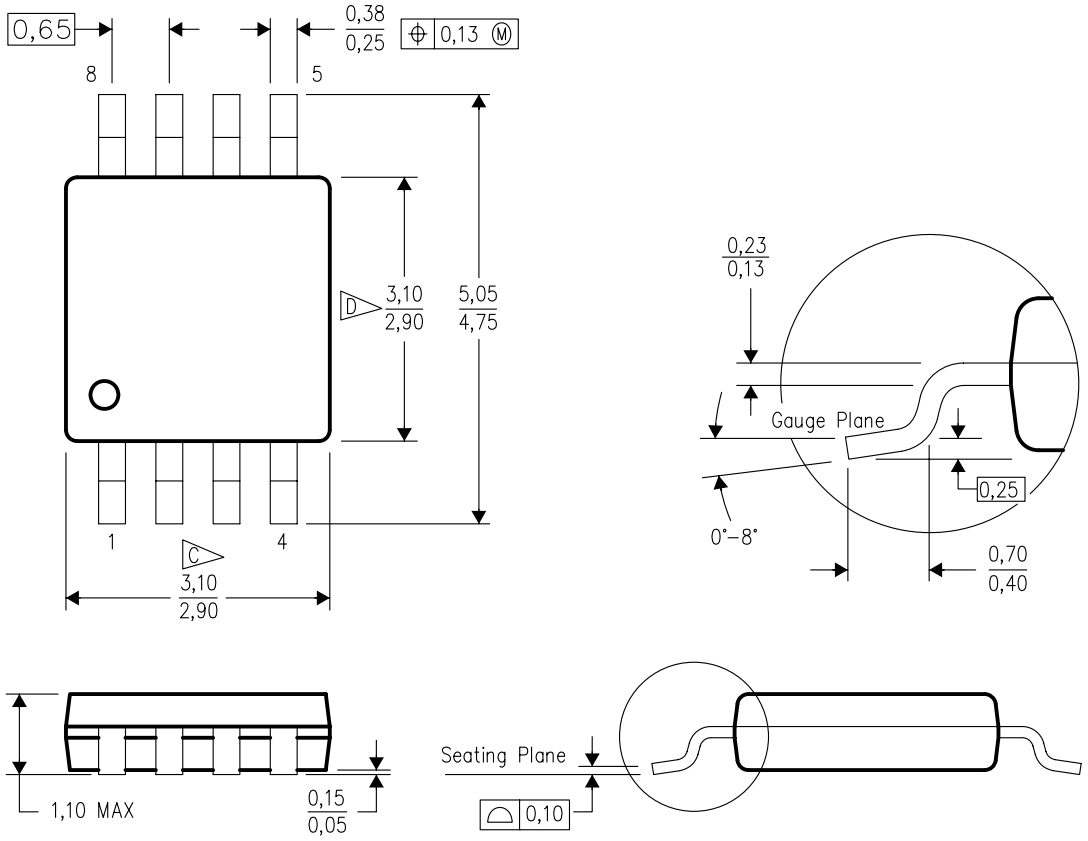
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM1771SMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM1771SSD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LM1771TMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM1771TSD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LM1771UMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM1771USD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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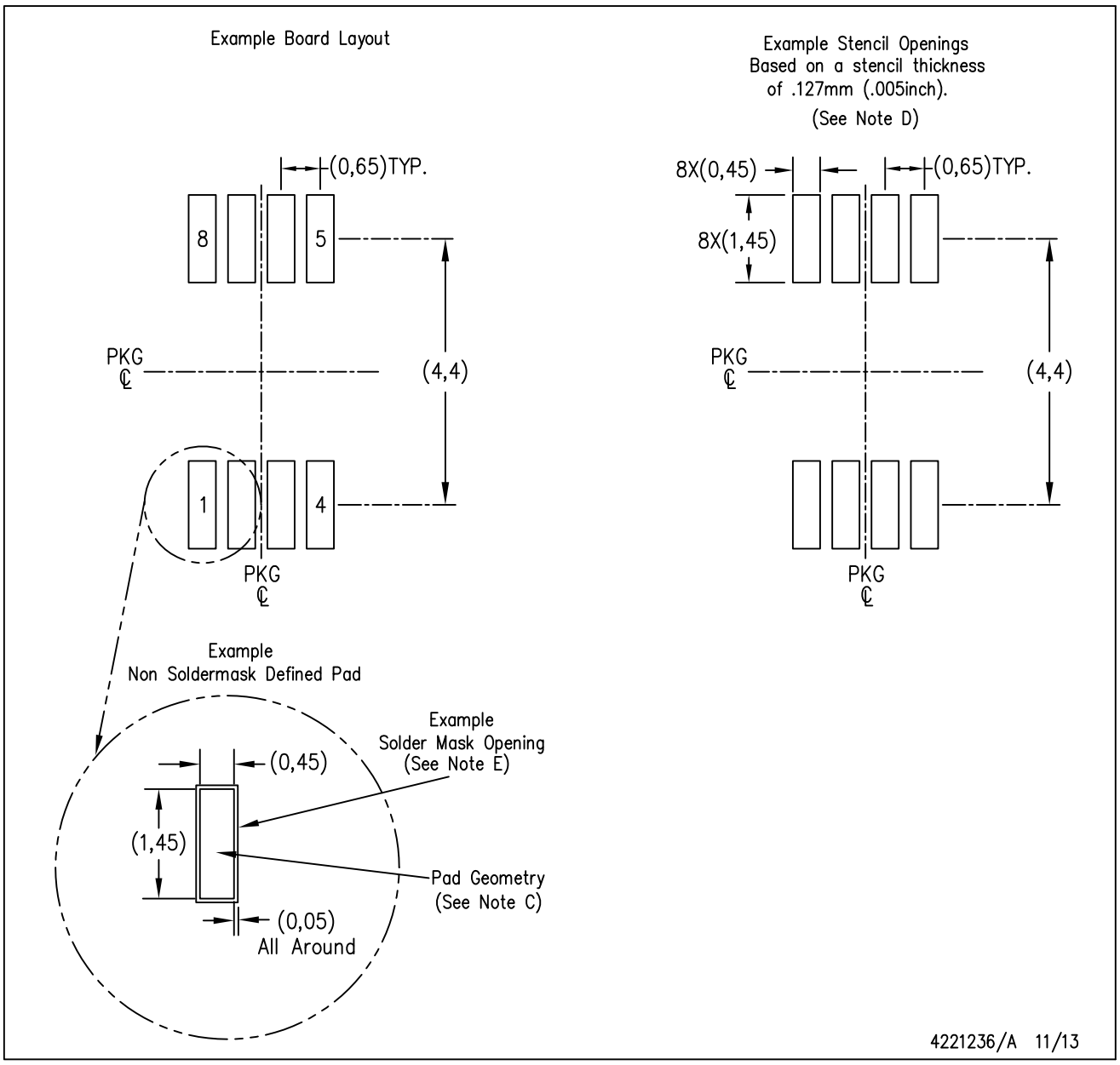
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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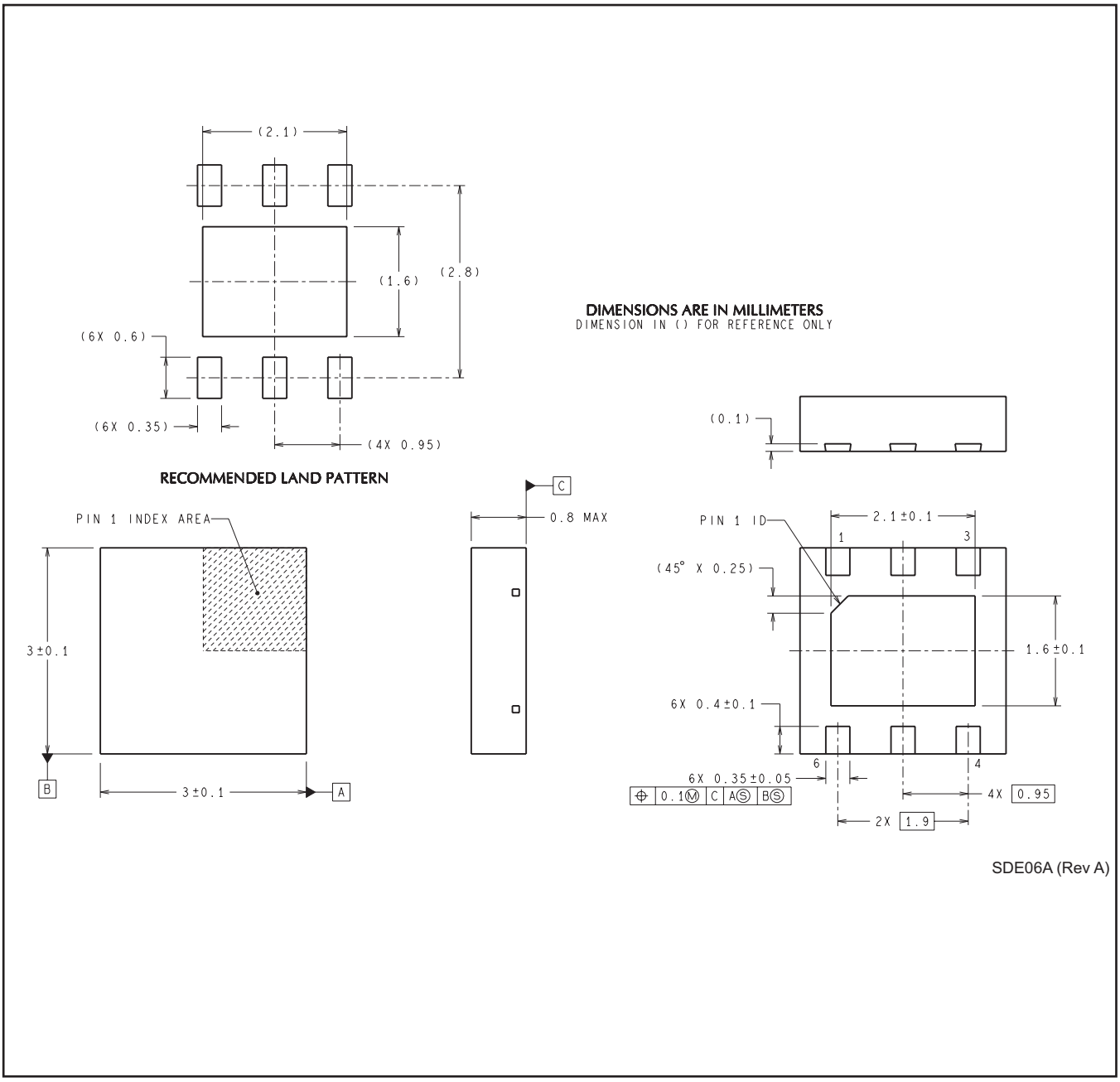

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