

MDU5512

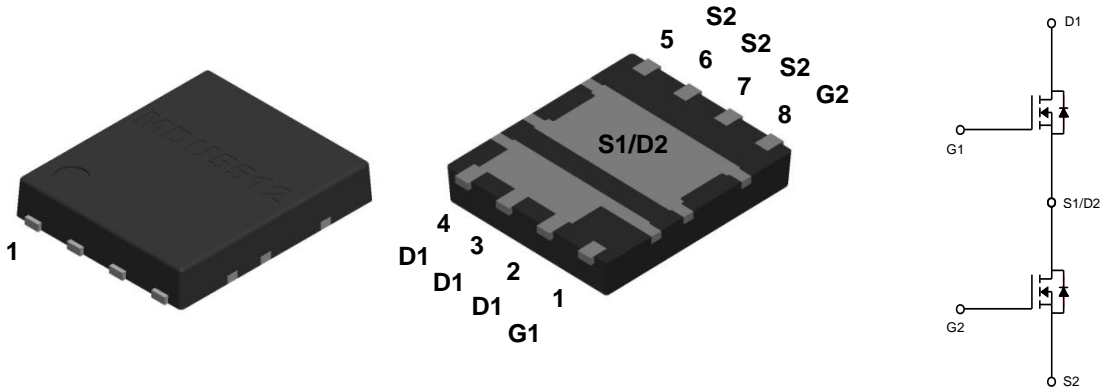
Dual Asymmetric N-channel Trench MOSFET 30V

General Description

The MDU5512 uses advanced MagnaChip's MOSFET Technology, which provides high performance in on-state resistance, fast switching performance and excellent quality. MDU5512 is suitable for DC/DC converter and general purpose applications.

Features

- | | |
|---|--|
| FET1
<ul style="list-style-type: none"> ▫ $V_{DS} = 30V$ ▫ $I_D = 46.1A$ ▫ $R_{DS(ON)} < 8.9m\Omega$ ▫ $< 12.5m\Omega$ ▫ 100% UIL Tested ▫ 100% Rg Tested | FET2
<ul style="list-style-type: none"> $V_{DS} = 30V$ $I_D = 80A @ V_{GS} = 10V$ $< 3.6m\Omega @ V_{GS} = 10V$ $< 4.5m\Omega @ V_{GS} = 4.5V$ |
|---|--|



Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	FET1	FET2	Unit
Drain-Source Voltage	V_{DSS}	30		V
Gate-Source Voltage	V_{GSS}	± 20	± 12	V
Continuous Drain Current ⁽¹⁾	$T_C=25^\circ C$	46.1	80	A
	$T_C=100^\circ C$	29.2	70.4	
	$T_A=25^\circ C$	11.3	18.2	
	$T_A=70^\circ C$	9.0	14.5	
Pulsed Drain Current	I_{DM}	100	200	A
Power Dissipation	$T_C=25^\circ C$	31.3	78.1	W
	$T_C=100^\circ C$	12.5	31.3	
	$T_A=25^\circ C$	1.9	2.1	
	$T_A=70^\circ C$	1.2	1.3	
Single Pulse Avalanche Energy ⁽²⁾	E_{AS}	53	171	mJ
Junction and Storage Temperature Range	T_J, T_{stg}	-55~150		°C

Thermal Characteristics

Characteristics	Symbol	FET1	FET2	Unit
Thermal Resistance, Junction-to-Ambient ⁽¹⁾	$R_{\theta JA}$	67	60	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4	1.6	

Ordering Information

Part Number	Temp. Range	Package	Packing	RoHS Status
MDU5512URH	-55~150°C	Dual PDFN56	Tape & Reel	Halogen Free

FET1 Electrical Characteristics (Ta =25°C)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A, V_{GS} = 0V$	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.3	1.8	2.4	
Drain Cut-Off Current	I_{DSS}	$V_{DS} = 30V, V_{GS} = 0V$	-	-	1	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 0.1	
Drain-Source ON Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 11.5A$	-	7.4	8.9	m Ω
		$V_{GS} = 4.5V, I_D = 11.5A$	-	10.0	12.5	
Forward Transconductance	g_{fs}	$V_{DS} = 5V, I_D = 11.5A$	-	35	-	S
Dynamic Characteristics						
Total Gate Charge	$Q_{g(10V)}$	$V_{DS} = 15.0V, I_D = 11.5A, V_{GS} = 10V$	13	17.3	21.6	nC
Total Gate Charge	$Q_{g(4.5V)}$		6.2	8.2	10.3	
Gate-Source Charge	Q_{gs}			3.0		
Gate-Drain Charge	Q_{gd}			2.7		
Input Capacitance	C_{iss}	$V_{DS} = 15.0V, V_{GS} = 0V, f = 1.0MHz$	750	1000	1250	pF
Reverse Transfer Capacitance	C_{oss}		147	196	245	
Output Capacitance	C_{rss}		60	80	100	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=15V, R_L=0.75\Omega, I_D=10A, V_{GS}=10V, R_g=3\Omega$	-	7.3	-	ns
Rise Time	t_r		-	10.9	-	
Turn-Off Delay Time	$t_{d(off)}$		-	25.6	-	
Fall Time	t_f		-	7.5	-	
Gate Resistance	R_g	$f=1\text{ MHz}$	-	1.2	2.0	Ω
Drain-Source Body Diode Characteristics						
Source-Drain Diode Forward Voltage	V_{SD}	$I_S = 1A, V_{GS} = 0V$	-	0.7	1.0	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 11.5A, dI/dt = 150A/\mu s$	-	22.6	29.4	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	20.6	26.8	nC

Note :

- Surface mounted FR-4 board by JEDEC (jesd51-7). Continuous current at $T_C=25^\circ C$ is silicon limited.
- E_{AS} is tested at starting $T_j = 25^\circ C, L = 0.1mH, I_{AS} = 18.2A, V_{DD} = 27V, V_{GS} = 10V$

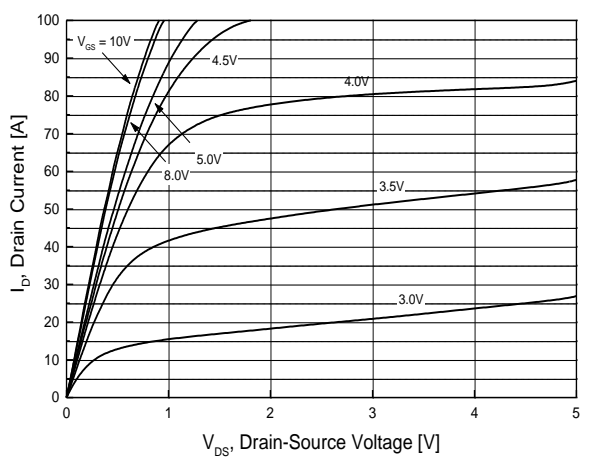


Fig.1 On-Region Characteristics

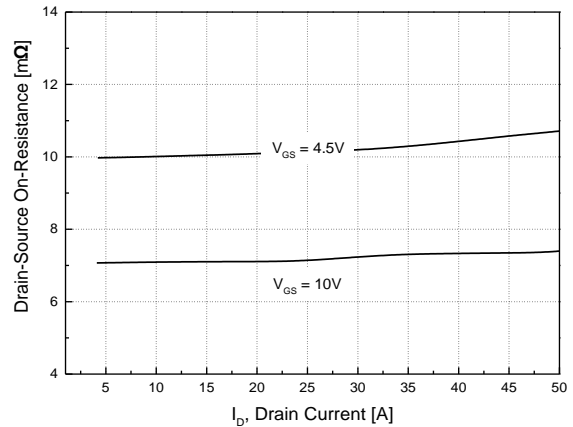


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

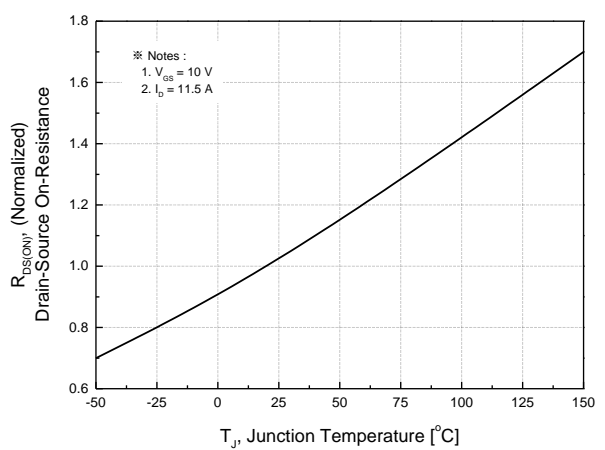


Fig.3 On-Resistance Variation with

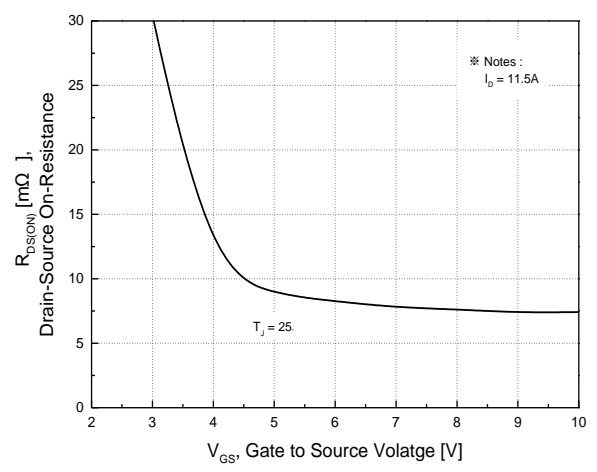


Fig.4 On-Resistance Variation with Gate to Source Voltage

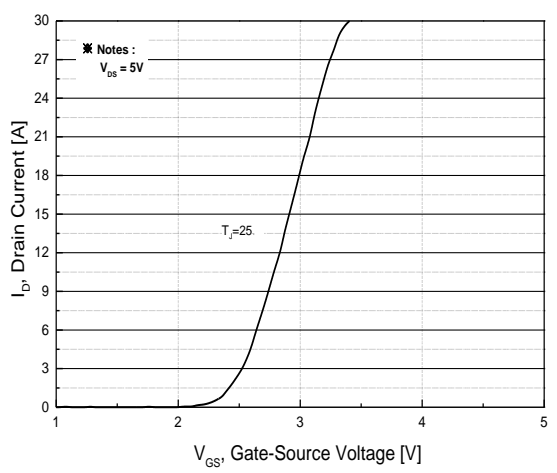


Fig.5 Transfer Characteristics

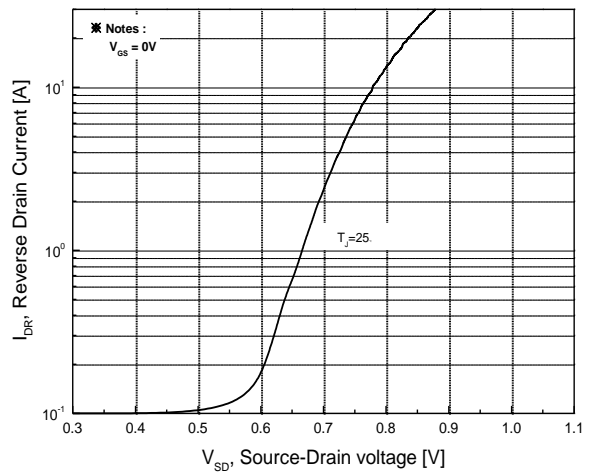


Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature

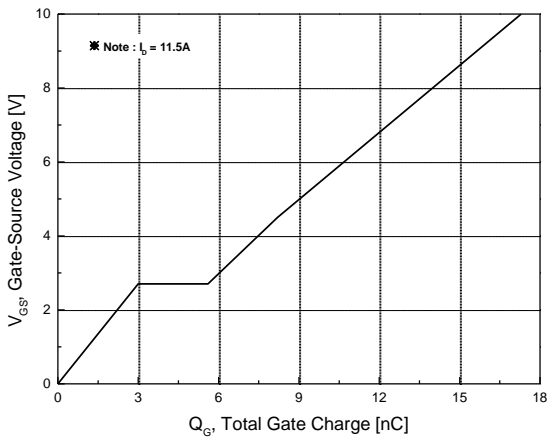


Fig.7 Gate Charge Characteristics

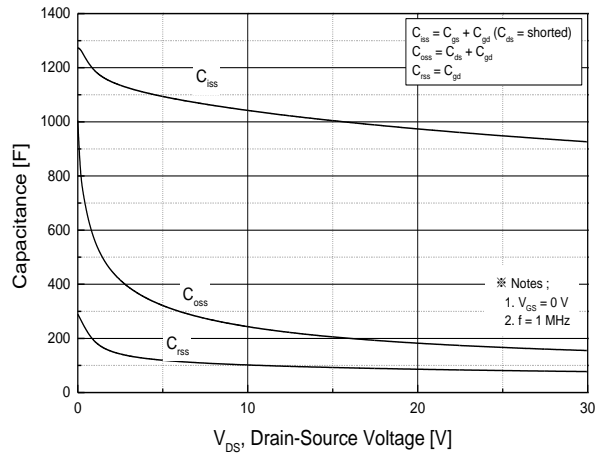


Fig.8 Capacitance Characteristics

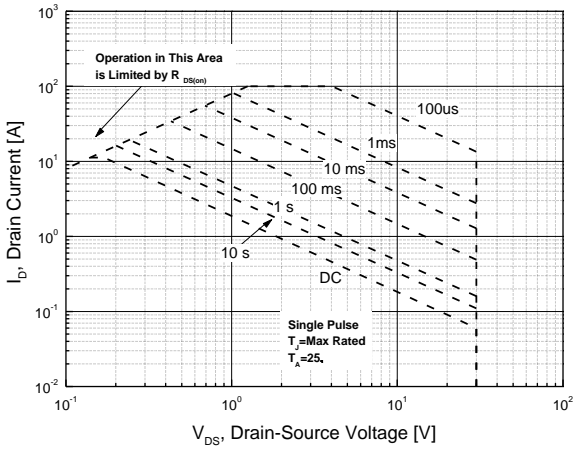


Fig.9 Maximum Safe Operating Area

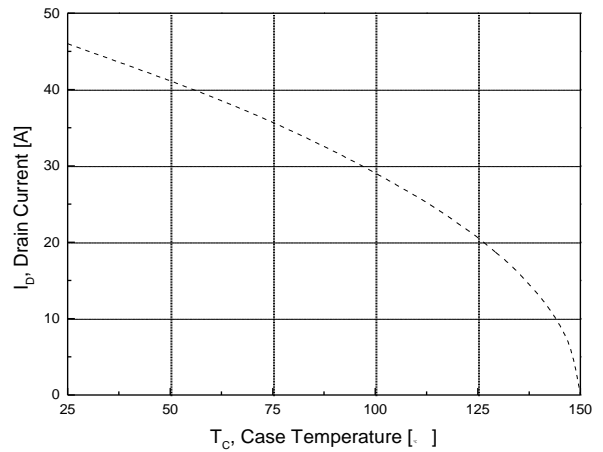


Fig.10 Maximum Drain Current vs. Case Temperature

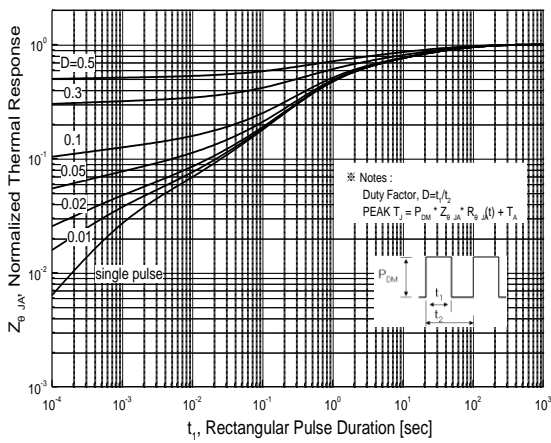


Fig.11 Transient Thermal Response Curve

FET2 Electrical Characteristics (Ta =25°C)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A, V_{GS} = 0V$	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	1.5	2.0	V
Drain Cut-Off Current	I_{DSS}	$V_{DS} = 30V, V_{GS} = 0V$	-	-	1	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 12V, V_{DS} = 0V$	-	-	± 0.1	μA
Drain-Source ON Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	2.9	3.6	$m\Omega$
		$V_{GS} = 4.5V, I_D = 20A$	-	3.3	4.5	$m\Omega$
Forward Transconductance	g_{fs}	$V_{DS} = 5V, I_D = 20A$	-	91	-	S
Dynamic Characteristics						
Total Gate Charge	$Q_{g(10V)}$	$V_{DS} = 15.0V, I_D = 20A, V_{GS} = 10V$	57.3	76.4	95.5	nC
Total Gate Charge	$Q_{g(4.5V)}$		26	34.7	43.3	
Gate-Source Charge	Q_{gs}		-	9.7	-	
Gate-Drain Charge	Q_{gd}		-	9.7	-	
Input Capacitance	C_{iss}	$V_{DS} = 15.0V, V_{GS} = 0V, f = 1.0MHz$	3138	4184	5230	pF
Reverse Transfer Capacitance	C_{oss}		406	542	678	
Output Capacitance	C_{riss}		180	241	301	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DS} = 15.0V, R_L = 1.5\Omega, R_G = 3.0\Omega$	-	15.5	-	ns
Rise Time	t_r		-	10.9	-	
Turn-Off Delay Time	$t_{d(off)}$		-	74.9	-	
Fall Time	t_f		-	10.3	-	
Gate Resistance	R_g	$f=1 MHz$	-	1.2	2.0	Ω
Drain-Source Body Diode Characteristics						
Source-Drain Diode Forward Voltage	V_{SD}	$I_S = 1.0A, V_{GS} = 0V$	-	0.7	1.0	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20A, di/dt = 150A/\mu s$	-	31.1	40.4	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	40.8	53.0	nC

Note :

- Surface mounted FR-4 board by JEDEC (jesd51-7). Continuous current at $T_C=25^\circ C$ is silicon limited.
- E_{AS} is tested at starting $T_j = 25^\circ C, L = 0.1mH, I_{AS} = 32.5A, V_{DD} = 27V, V_{GS} = 10V$

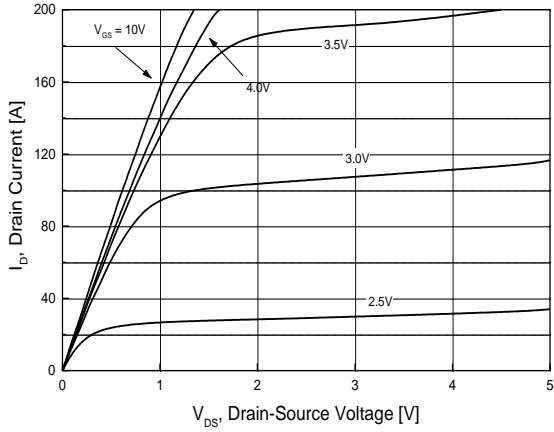


Fig.1 On-Region Characteristics

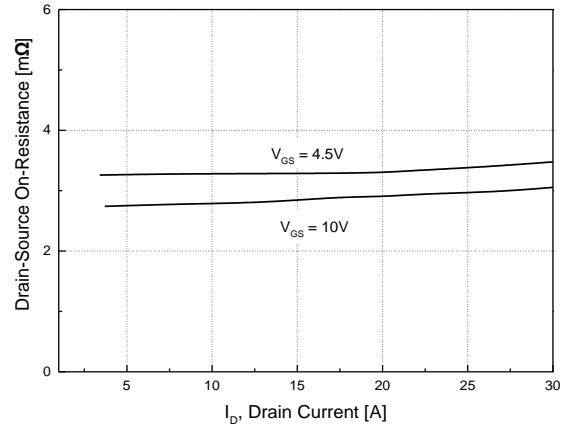


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

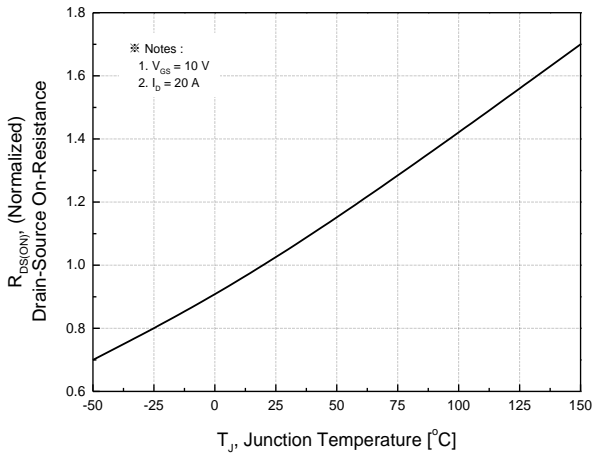


Fig.3 On-Resistance Variation with Junction Temperature

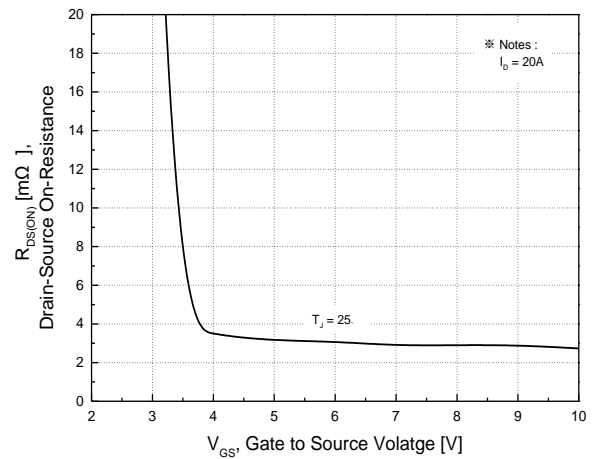


Fig.4 On-Resistance Variation with Gate to Source Voltage

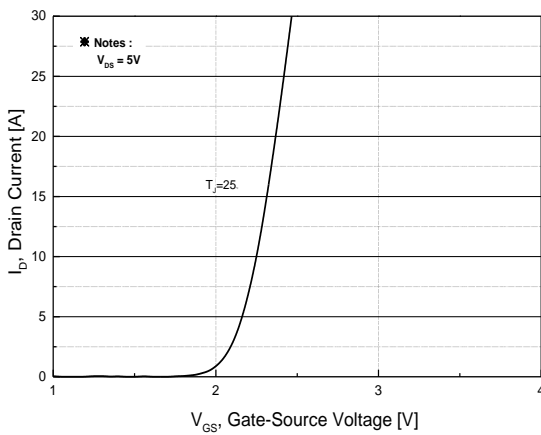


Fig.5 Transfer Characteristics

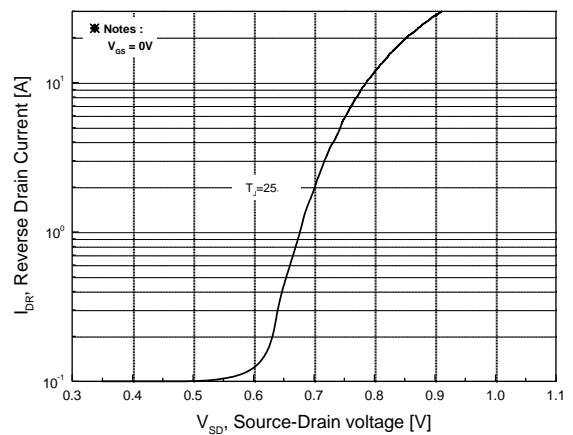


Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature

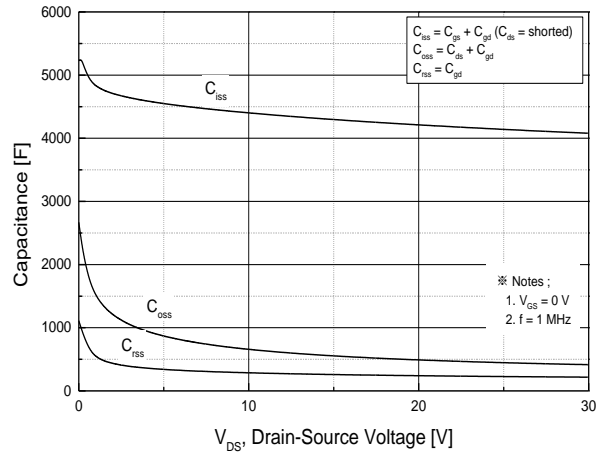
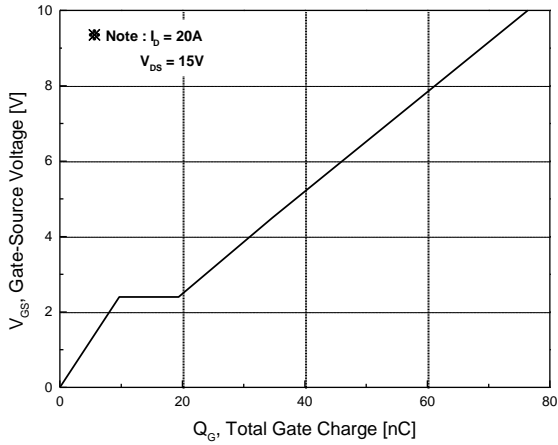
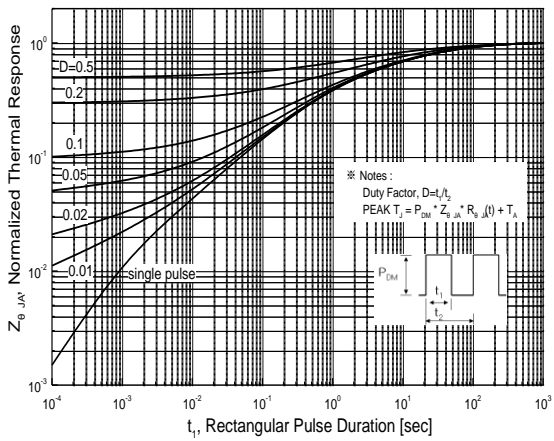
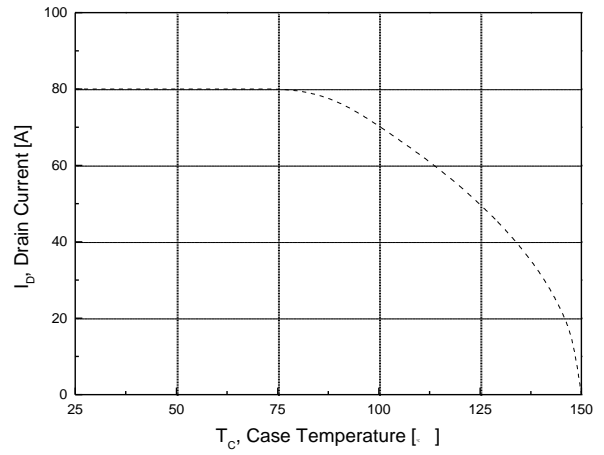


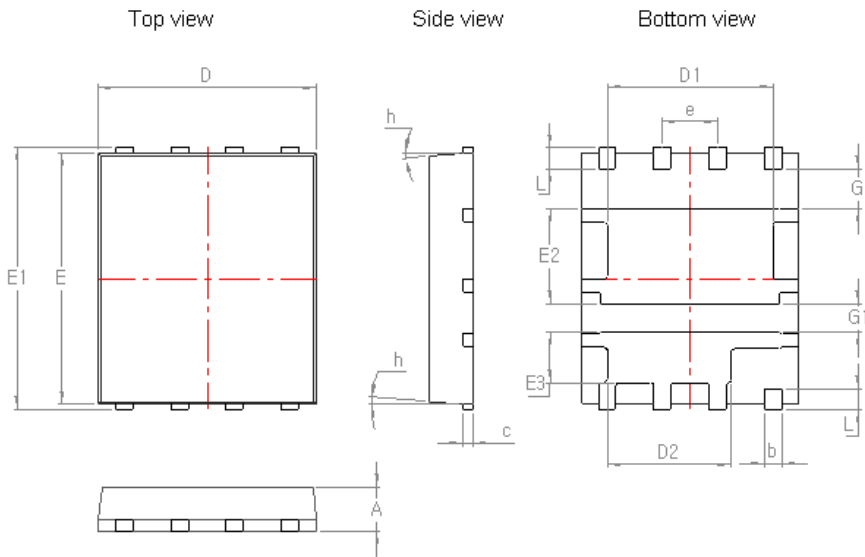
Fig.9 Maximum Safe Operating Area



Package Dimension

Dual PDFN56 (5x6mm)

Dimensions are in millimeters, unless otherwise specified



Symbol	Dimension [mm]		
	Min	Nom	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.30
D	4.80	5.00	5.20
D1	3.60	3.80	4.00
D2	2.64	2.84	3.04
E	5.70	5.75	5.80
E1	5.90	6.00	6.10
E2	2.00	2.25	2.50
E3	1.10	1.20	1.30
e	1.27 BSC		
G	0.50	-	-
G1	0.40	0.60	0.80
h	0°	-	12°
L	0.38	0.55	0.71

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