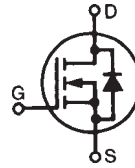
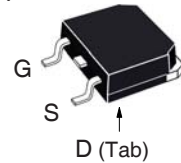


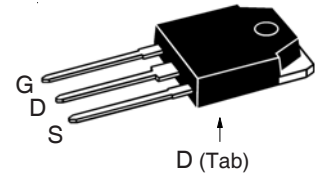
**Polar3™ HiperFET™
Power MOSFET**
**IXFT60N50P3
IXFQ60N50P3
IXFH60N50P3**
 $V_{DSS} = 500V$
 $I_{D25} = 60A$
 $R_{DS(on)} \leq 100m\Omega$

 N-Channel Enhancement Mode
 Avalanche Rated
 Fast Intrinsic Rectifier


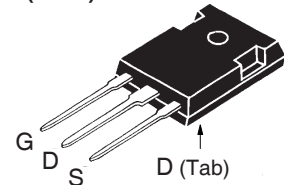
TO-268 (IXFT)



TO-3P (IXFQ)



TO-247 (IXFH)


 G = Gate D = Drain
 S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	500	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	500	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ C$	60	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	150	A
I_A	$T_C = 25^\circ C$	30	A
E_{AS}	$T_C = 25^\circ C$	1	J
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	35	V/ns
P_D	$T_C = 25^\circ C$	1040	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	1.6mm (0.062in.) from Case for 10s	300	$^\circ C$
T_{sold}	Plastic Body for 10 seconds	260	$^\circ C$
M_d	Mounting Torque (TO-247 & TO-3P)	1.13 / 10	Nm/lb.in.
Weight	TO-268	4.0	g
	TO-3P	5.5	g
	TO-247	6.0	g

Symbol	Test Conditions ($T_J = 25^\circ C$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 1mA$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 4mA$	3.0		5.0 V
I_{GSS}	$V_{GS} = \pm 30V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			25 μA 2 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			100 m Ω

Features

- Fast Intrinsic Rectifier
- Avalanche Rated
- Low $R_{DS(ON)}$ and Q_G
- Low Package Inductance

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- Laser Drivers
- AC and DC Motor Drives
- Robotics and Servo Controls

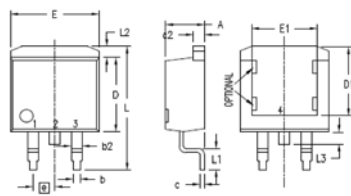
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 20\text{V}, I_D = 0.5 \cdot I_{D25}$, Note 1	35	60	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		6250	pF
C_{oss}			680	pF
C_{rss}			5	pF
R_{Gi}	Gate Input Resistance		1.0	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 1\Omega$ (External)		18	ns
t_r			16	ns
$t_{d(off)}$			37	ns
t_f			8	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$		96	nC
Q_{gs}			28	nC
Q_{gd}			26	nC
R_{thJC}				0.12 $^\circ\text{C/W}$
R_{thCS}	(TO-247 & TO-3P)	0.25		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_s	$V_{GS} = 0\text{V}$			60 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			240 A
V_{SD}	$I_F = I_s, V_{GS} = 0\text{V}$, Note 1			1.4 V
t_{rr}	$I_F = 30\text{A}, -di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GS} = 0\text{V}$			250 ns
I_{RM}			11	A
Q_{RM}			1.0	μC

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

TO-263 Outline



- 1 - GATE
- 2 - DRAIN (COLLECTOR)
- 3 - SOURCE (EMITTER)
- 4 - DRAIN (COLLECTOR) OUTLINE SIDE

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.160	.190	4.06	4.83
A1	.080	.110	2.03	2.79
b	.020	.039	0.51	0.99
b2	.045	.055	1.14	1.40
c	.016	.029	0.40	0.74
c2	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D1	.315	.350	8.00	8.89
E	.380	.410	9.65	10.41
E1	.245	.320	6.22	8.13
e	.100 BSC		2.54 BSC	
L	.575	.625	14.61	15.88
L1	.090	.110	2.29	2.79
L2	.040	.055	1.02	1.40
L3	.050	.070	1.27	1.78
L4	0	.005	0	0.13

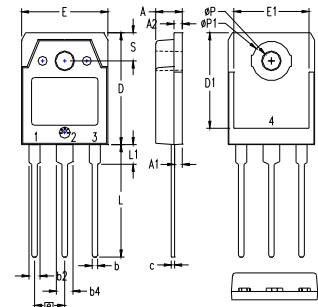
ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

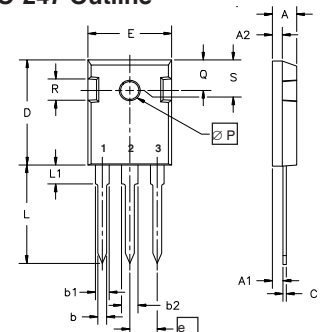
TO-3P (IXFQ) Outline



- 1 - GATE
- 2 - DRAIN (COLLECTOR)
- 3 - SOURCE (EMITTER)
- 4 - DRAIN (COLLECTOR)

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.193	4.70	4.90
A1	.051	.059	1.30	1.50
A2	.057	.065	1.45	1.65
b	.035	.045	0.90	1.15
b2	.075	.087	1.90	2.20
b4	.114	.126	2.90	3.20
c	.022	.031	0.55	0.80
D	.780	.799	19.80	20.30
D1	.665	.677	16.90	17.20
E	.610	.622	15.50	15.80
E1	.531	.539	13.50	13.70
e	.215 BSC		5.45 BSC	
L	.779	.795	19.80	20.20
L1	.134	.142	3.40	3.60
ϕP	.126	.134	3.20	3.40
$\phi P1$.272	.280	6.90	7.10
S	.193	.201	4.90	5.10

TO-247 Outline



- Terminals: 1 - Gate 2 - Drain
3 - Source

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A ₁	2.2	2.54	.087	.102
A ₂	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b ₁	1.65	2.13	.065	.084
b ₂	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ϕP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15 BSC		242 BSC	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

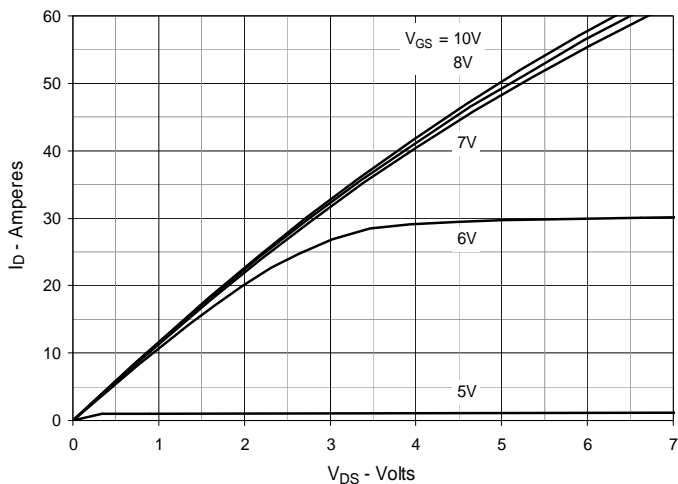


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

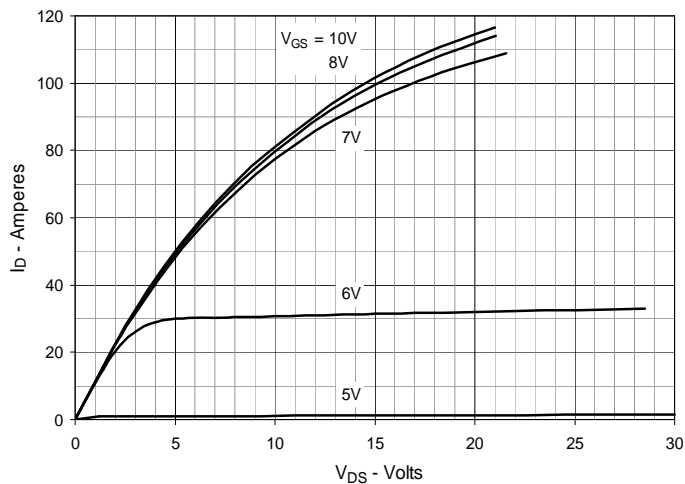


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

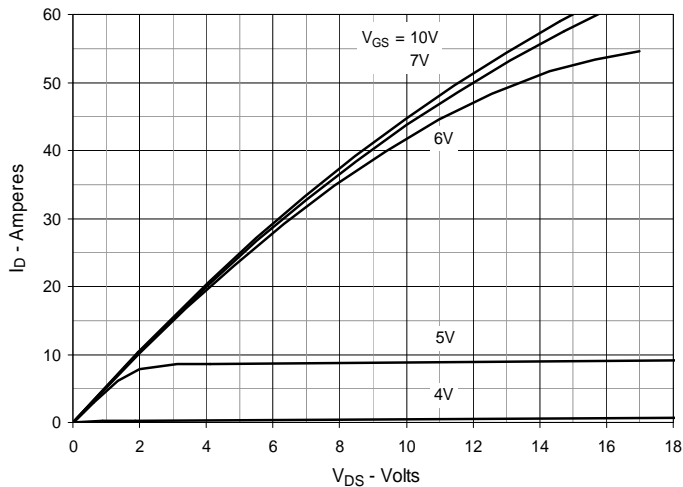


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 30\text{A}$ Value vs. Junction Temperature

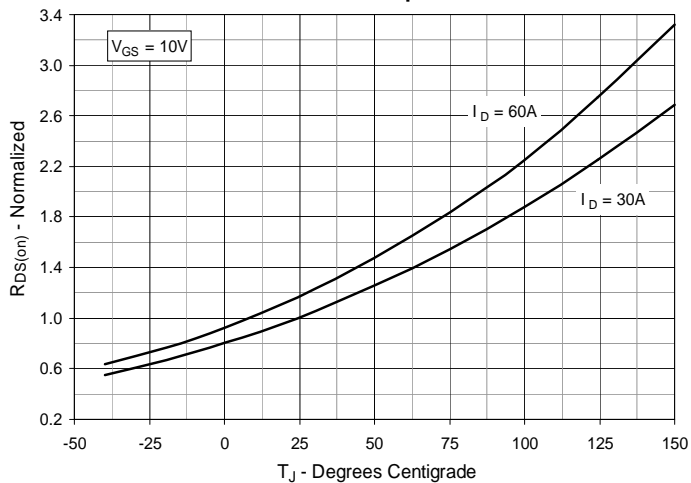


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 30\text{A}$ Value vs. Drain Current

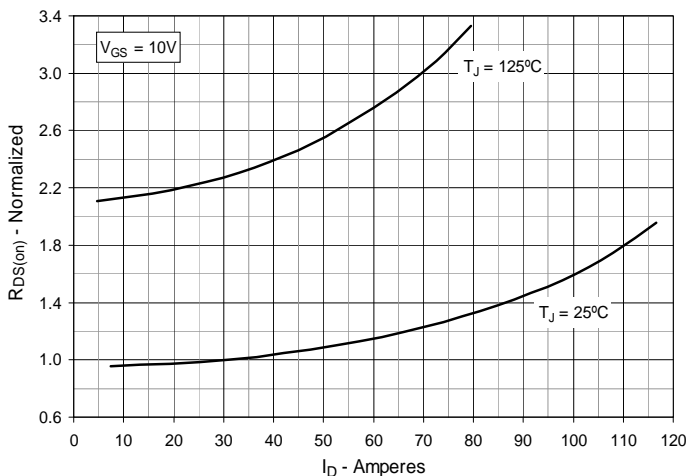


Fig. 6. Maximum Drain Current vs. Case Temperature

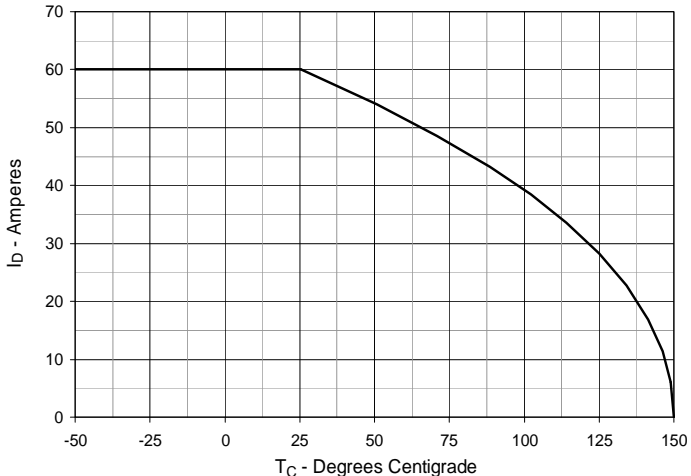


Fig. 7. Input Admittance

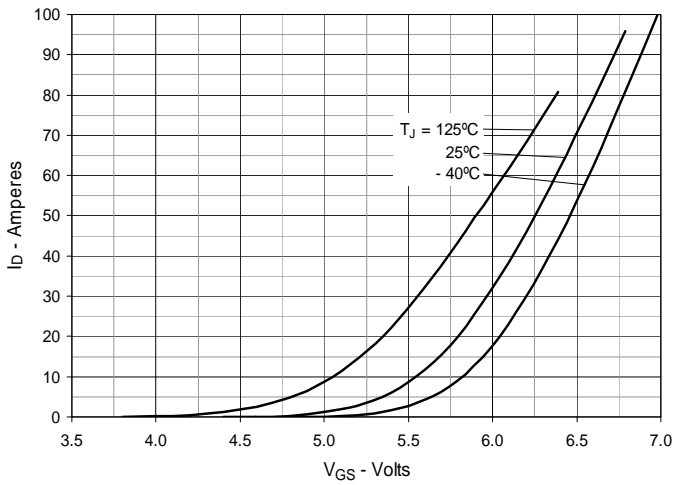


Fig. 8. Transconductance

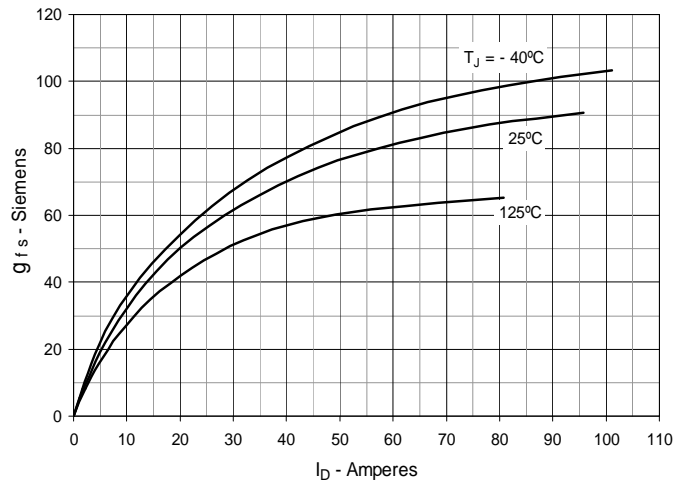


Fig. 9. Forward Voltage Drop of Intrinsic Diode

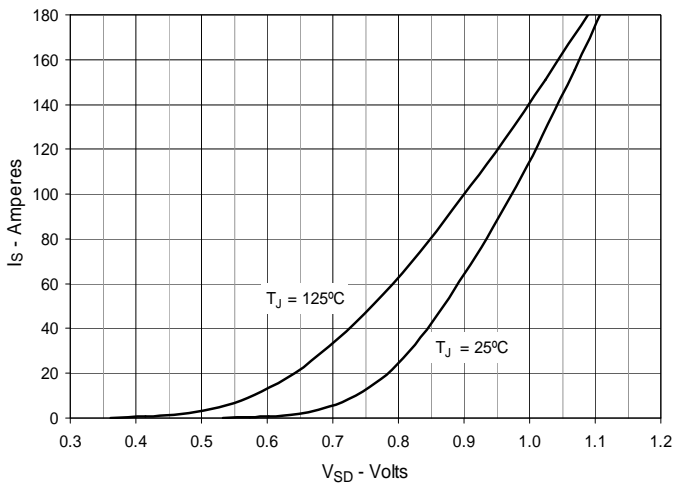


Fig. 10. Gate Charge

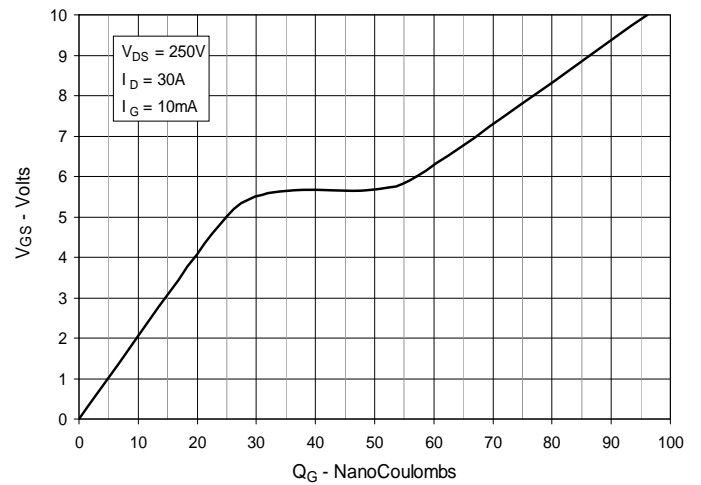


Fig. 11. Capacitance

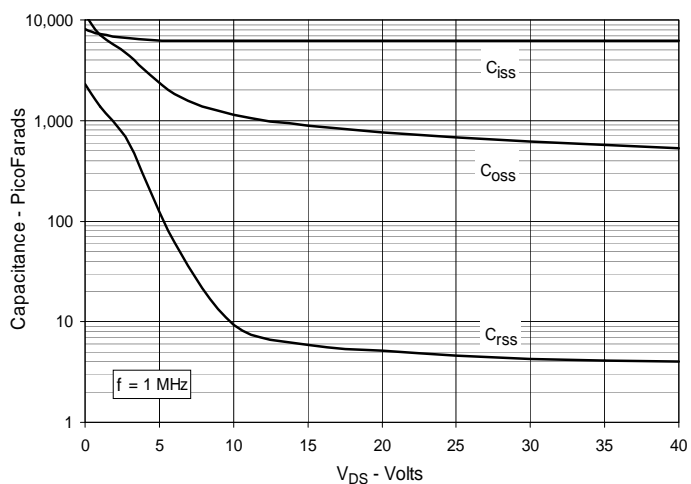


Fig. 12. Forward-Bias Safe Operating Area

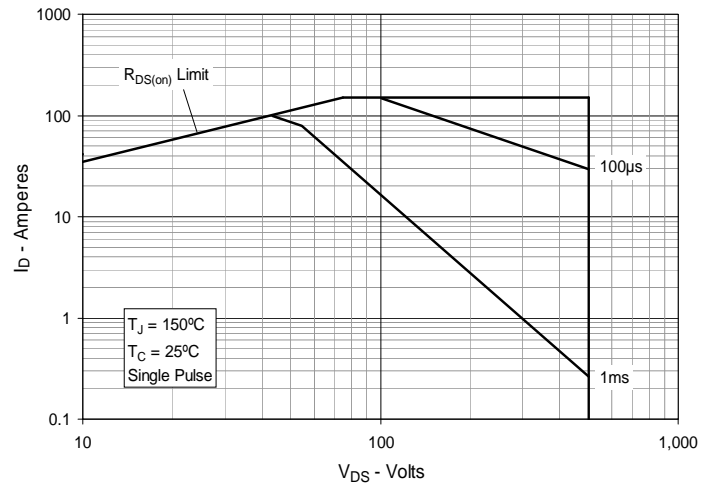


Fig. 13. Maximum Transient Thermal Impedance

