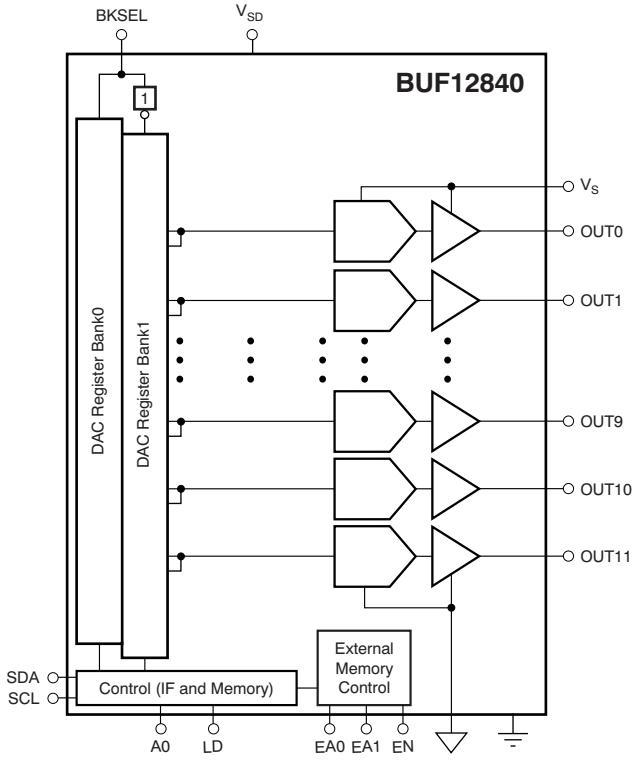
Programmable Gamma-Voltage Generator with Integrated Two-Bank Memory and External EEPROM

FEATURES

- **10-BIT RESOLUTION**
- **12-CHANNEL P-GAMMA**
- **READS FROM EXTERNAL EEPROM**
- **TWO INDEPENDENT PIN-SELECTABLE MEMORY BANKS**
- **RAIL-TO-RAIL OUTPUT:**
  - **300mV Min Swing-to-Rail (10mA)**
  - **200mV Min Swing-to-Rail (5mA)**
- **LOW SUPPLY CURRENT**
- **SUPPLY VOLTAGE: 9V to 20V**
- **DIGITAL SUPPLY: 2V to 5.5V**
- **TWO-WIRE INTERFACE: Supports 400kHz and 3.4MHz Operation**

APPLICATIONS

- **TFT-LCD REFERENCE DRIVERS**



DESCRIPTION

The BUF12840 offers 12 programmable gamma channels with external electrically erasable programmable read-only memory (EEPROM) read capabilities.

The BUF12840 has two separate memory banks that allow simultaneous storage of two different gamma curves to facilitate switching between gamma curves.

All gamma channels offer a rail-to-rail output that typically swings to within 200mV of either supply rail with a 5mA load. All channels are programmed using a two-wire interface that supports standard operations up to 400kHz and high-speed data transfers up to 3.4MHz.

The BUF12840 is manufactured using Texas Instruments' proprietary, state-of-the-art, high-voltage CMOS process. This process offers very dense logic and high supply voltage operation of up to 20V. The BUF12840 is offered in a QFN-24 package, and is specified from –40°C to +95°C.

RELATED PRODUCTS

FEATURES	PRODUCT
22-Channel Gamma Correction Buffer	BUF22821
12-Channel Gamma Correction Buffer	BUF12800
20-Channel Programmable Buffer, 10-Bit, V_{COM}	BUF20800
16-/20-Channel Programmable Buffer with Memory	BUF20820
Programmable V_{COM} Driver	BUF01900
18V Supply, Traditional Gamma Buffers	BUF11704
22V Supply, Traditional Gamma Buffers	BUF11705

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
BUF12840	VQFN-24	RGE	BUF12840	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER		BUF12840	UNIT
Supply Voltage	V_S	+22	V
Supply Voltage	V_{SD}	+6	V
Supply Input Terminals, SCL, SDA, A0, BKSEL, EA0, EA1, EN, LD: Voltage		–0.5 to +6	V
Supply Input Terminals, SCL, SDA, A0, BKSEL, EA0, EA1, EN, LD: Current		±10	mA
Output Short-Circuit(2)		Continuous	
Operating Temperature		–40 to +95	°C
Storage Temperature		–65 to +150	°C
Junction Temperature	T_J	+125	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Short-circuit to ground. Exposed thermal die is soldered to the PCB using thermal vias. Refer to Texas Instruments application report *QFN/SON PCB Attachment (SLUS271)*.

THERMAL INFORMATION

THERMAL METRIC(1)		BUF12840 RGE 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	35.6	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	40.5	
θ_{JB}	Junction-to-board thermal resistance	10.0	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	9.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	3.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = –40°C to +95°C.**
At T_A = +25°C, V_S = +18V, and V_{SD} = +5V, unless otherwise noted.

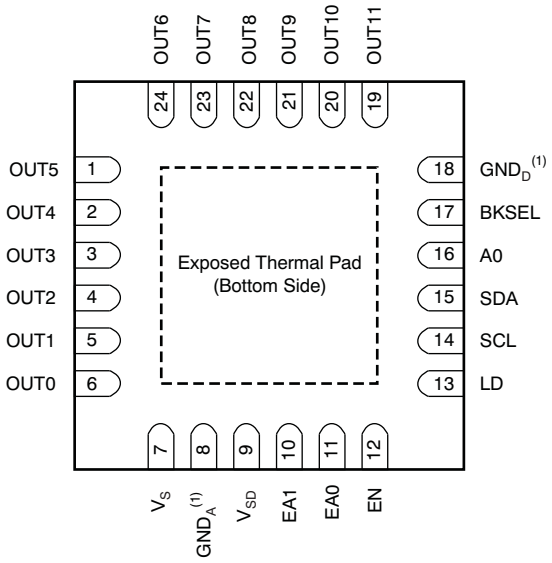
PARAMETER		CONDITIONS	BUF12840 MIN	BUF12840 TYP	BUF12840 MAX	UNIT
ANALOG GAMMA BUFFER CHANNELS						
Reset value		Code 0		0		V
OUT1 to OUT12 output swing: high		**Code = 1023, sourcing 10mA**	**17.7**	**17.85**		**V**
OUT1 to OUT12 output swing: low		**Code = 0, sinking 10mA**		**0.07**	**0.3**	**V**
OUT1 to OUT12 output swing: high		**Code = 1023, sourcing 5mA**	**17.8**	**17.9**		**V**
OUT1 to OUT12 output swing: low		**Code = 0, sinking 5mA**		**0.07**	**0.2**	**V**
Continuous output current		See note (1)		30		mA
Output accuracy		Code 512		±20	±50	mV
vs Temperature		**Code 512**		**±25**		**µV/°C**
Integral nonlinearity	INL	V_{OUT} = GND + 0.3V to V_S – 0.3V		0.3		Bits
Differential nonlinearity	DNL	V_{OUT} = GND + 0.3V to V_S – 0.3V		0.3		Bits
Load regulation, 10mA	REG	Code 512 or V_{CC}/2, I_{OUT} = +5mA to –5mA step		0.5	1.5	mV/mA
ANALOG POWER SUPPLY						
Operating range			9		20	V
Total analog supply current	I_S	Outputs at midscale with no load		6.5	10	mA
Over temperature					**19**	**mA**
DIGITAL INPUT/OUTPUT (2)						
Logic 1 input voltage	V_{IH}		0.7 × V_{SD}			V
Logic 0 input voltage	V_{IL}				0.3 × V_{SD}	V
Logic 0 output voltage	V_{OL}	I_{SINK} = 3mA		0.15	0.4	V
Input leakage				±0.01	±10	µA
Clock frequency	**f_{CLK}**	**Standard/Fast mode**			**400**	**kHz**
		High-Speed mode			**3.4**	**MHz**
EEPROM read clock speed		Master mode	71	87	100	kHz
BANK switching delay		LD pin = 0, V_{OUT} = 50% of code 1023		7	10	µs
DIGITAL POWER SUPPLY						
Operating range	V_{SD}		2.0		5.5	V
Digital supply current (1)	I_{SD}	Two-Wire bus inactive		90	150	µA
Over temperature				**115**	**175**	**µA**
Power-on reset	POR		1.1	1.5	1.7	V
TEMPERATURE RANGE						
Specified range			–40		+95	°C
Operating range		Junction temperature < +125°C	–40		+95	°C
Storage range			–65		+150	°C

(1) Observe maximum power dissipation. Exposed thermal die is soldered to the PCB using thermal vias. Refer to Texas Instruments application report *QFN/SON PCB Attachment (SLUS271)*.
(2) Refers to pins EA0, EA1, EN, LD, SCL, SDA, A0, and BKSEL.

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PIN CONFIGURATION

RGE PACKAGE
4mm × 4mm VQFN-24
(TOP VIEW)



NOTE: (1) GND_A and GND_D must be connected together.

PIN DESCRIPTIONS

PIN NO.	NAME	DESCRIPTION
1	OUT5	DAC output 5
2	OUT4	DAC output 4
3	OUT3	DAC output 3
4	OUT2	DAC output 2
5	OUT1	DAC output 1
6	OUT0	DAC output 0
7	V_S	V_S connected to analog supply
8	GND_A	Analog ground; must be connected to digital ground (GND_D)
9	V_{SD}	Digital supply; connected to logic supply
10	EA1	EEPROM select bit 1. EA1 should be tied to logic '0' if autoread is not used.
11	EA0	EEPROM select bit 0. EA0 should be tied to logic '0' if autoread is not used.
12	EN	EEPROM enable. EN must be '0' if autoread is not used.
13	LD	Latch pin
14	SCL	Serial clock
15	SDA	Serial data
16	A0	Slave address
17	BKSEL	Bank select
18	GND_D	Digital ground; must be connected to digital ground (GND_A)
19	OUT11	DAC output 11
20	OUT10	DAC output 10
21	OUT9	DAC output 9
22	OUT8	DAC output 8
23	OUT7	DAC output 7
24	OUT6	DAC output 6

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TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +18V, and V_{SD} = +5V, unless otherwise noted.

OUTPUT VOLTAGE vs OUTPUT CURRENT (Channels 1–12)

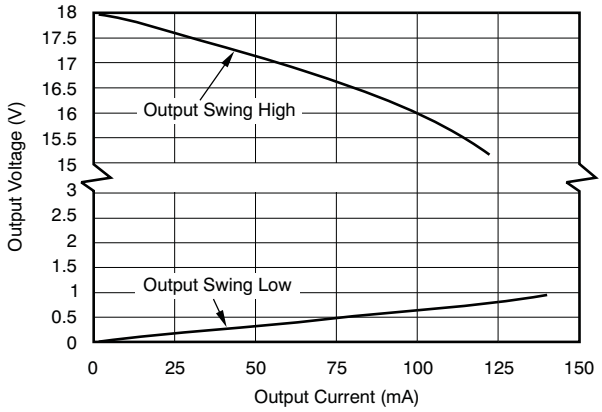


Figure 1.

ANALOG SUPPLY CURRENT HISTOGRAM

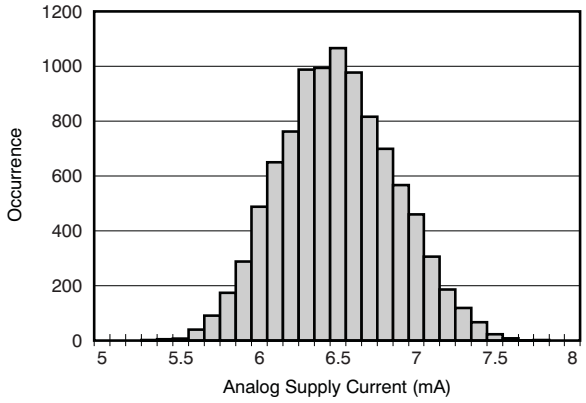


Figure 2.

ANALOG SUPPLY CURRENT vs TEMPERATURE

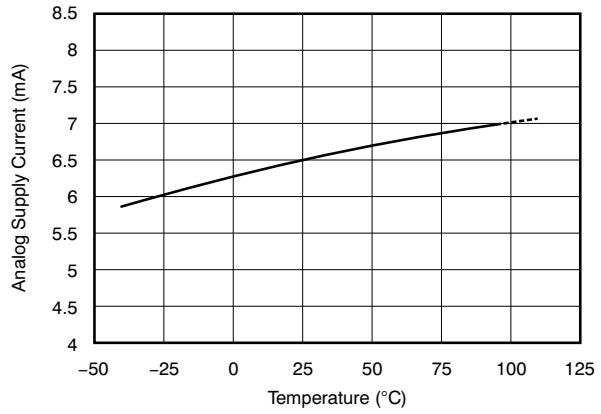


Figure 3.

OUTPUT VOLTAGE vs TEMPERATURE

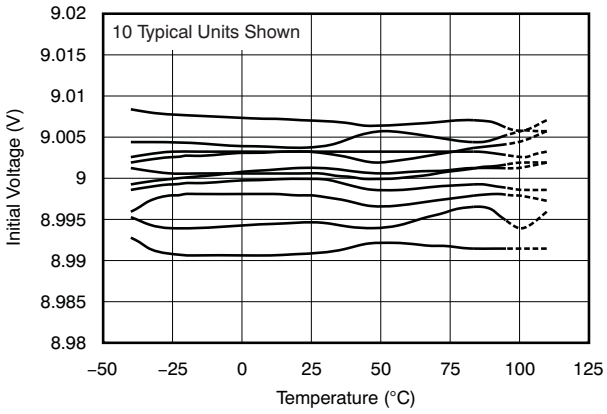


Figure 4.

DIGITAL SUPPLY CURRENT vs TEMPERATURE

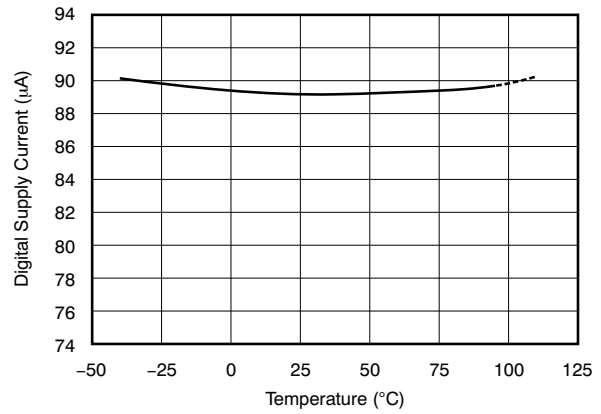


Figure 5.

DIFFERENTIAL LINEARITY ERROR

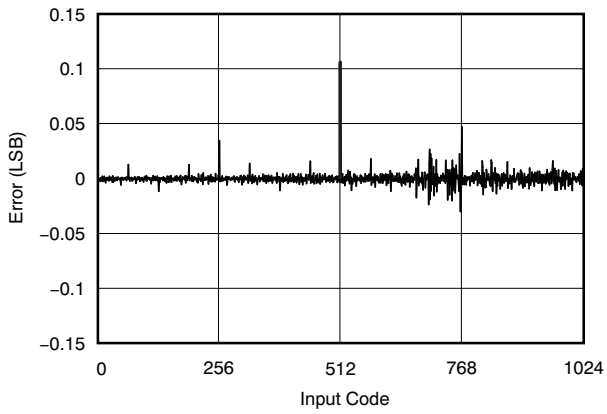


Figure 6.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +18V, and V_{SD} = +5V, unless otherwise noted.

INTEGRAL LINEARITY ERROR

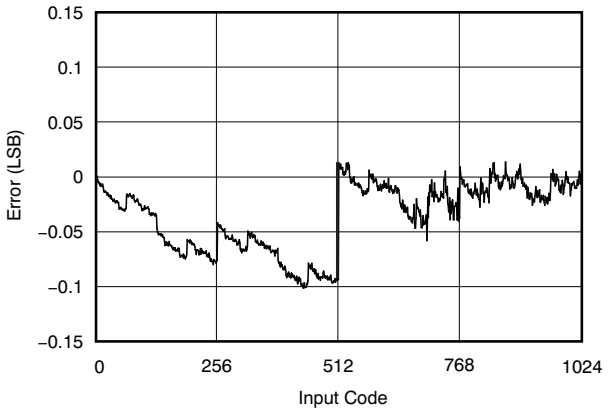


Figure 7.

BKSEL SWITCHING TIME DELAY (LD Pin = 0)

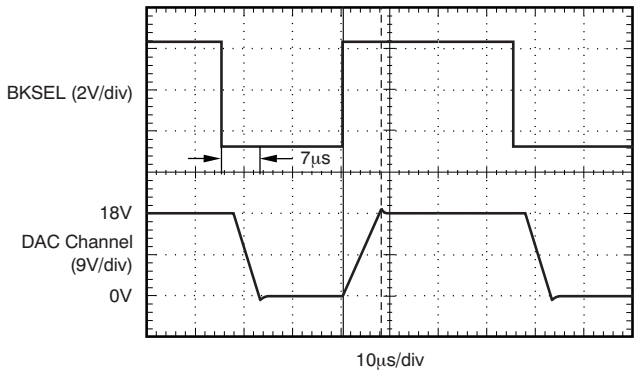


Figure 8.

LARGE-SIGNAL STEP RESPONSE

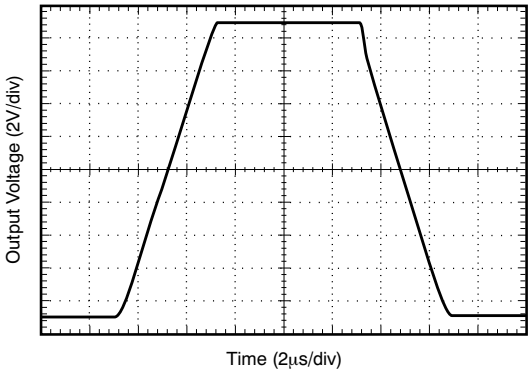


Figure 9.

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APPLICATION INFORMATION

GENERAL

The BUF12840 programmable voltage reference allows fast and easy adjustment of 12 programmable gamma reference outputs, each with 10-bit resolution. The BUF12840 is programmed through a high-speed, two-wire interface. The final gamma values can be automatically loaded from an external EEPROM. The BUF12840 has two separate memory banks, allowing simultaneous storage of two different gamma curves to facilitate dynamic switching between gamma curves.

The BUF12840 can be powered using an analog supply voltage from 9V to 20V, and a digital supply from 2V to 5.5V. The digital supply must be applied before the analog supply to avoid excessive current and power consumption, or possibly even damage to the device if left connected only to the analog supply for extended periods of time. See Figure 10 for a typical configuration of the BUF12840. Note that the analog power, V_S, does not need to be on during any interface communication.

TWO-WIRE BUS OVERVIEW

The BUF12840 communicates over an industry-standard, two-wire interface to receive data in slave mode. This model uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from low to high while SCL is high. The BUF12840 acts as a slave device after 10ms; before that, it is the master and drives SCL and SDA.

ADDRESSING THE BUF12840

The address of the BUF12840 is 111010x, where *x* is the state of the A0 pin. When the A0 pin is low, the device acknowledges on address 74h (1110100). If the A0 pin is high, the device acknowledges on address 75h (1110101). Table 1 shows the A0 pin settings and the BUF12840 address options.

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

Table 1. Quick Reference of BUF12840 Addresses

BUF12840 ADDRESS	ADDRESS
A0 pin is low (device acknowledges on address 74h)	1110100
A0 pin is high (device acknowledges on address 75h)	1110101

Table 2. Quick Reference of Command Codes

COMMAND	CODE
General-Call Reset	Address byte of 00h followed by a data byte of 06h.
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code.

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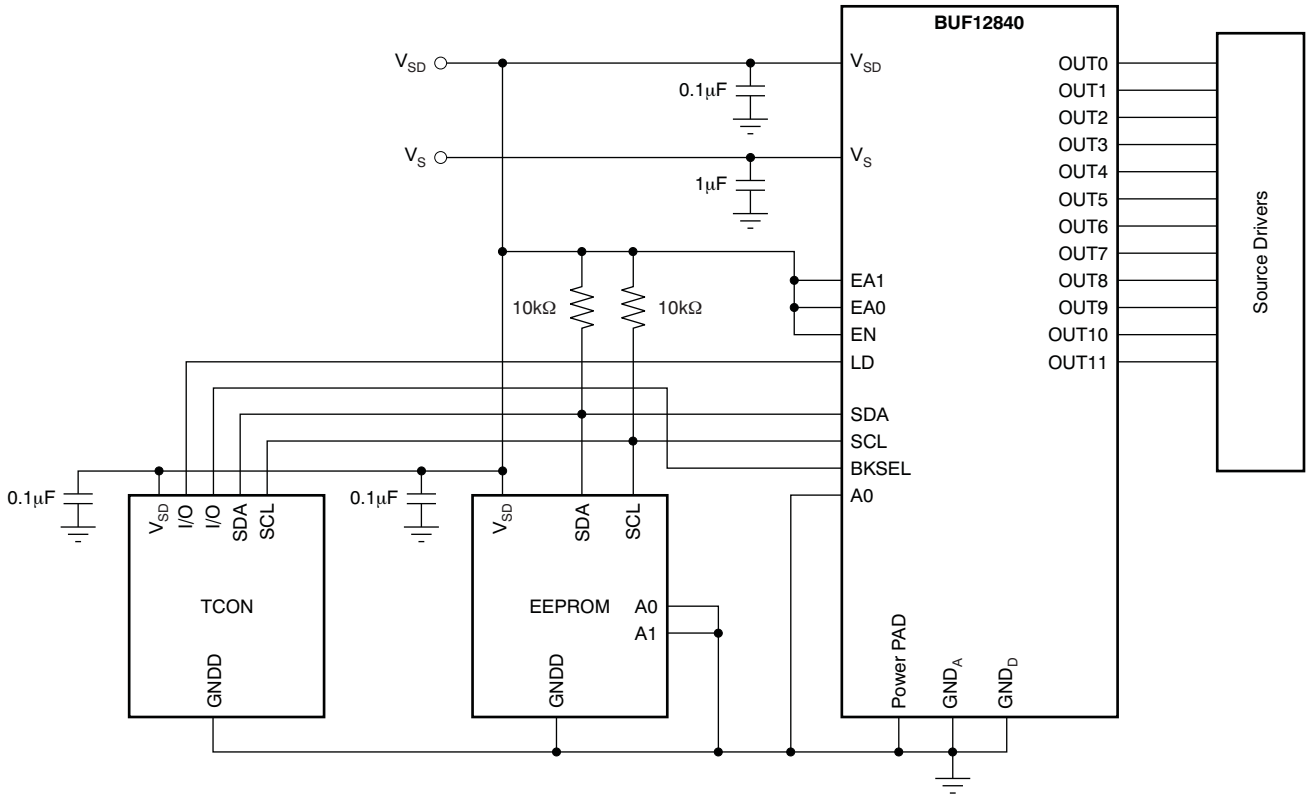


Figure 10. Typical Application Configuration

DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (also called Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF12840 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001 xxx, with SCL ≤ 400kHz, following the START condition; where *xxx* are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. Table 2 provides a reference for the High-speed mode command code. (Note that this configuration is different from normal address bytes—the low bit does not indicate read/write status.) The BUF12840 responds to the High-speed command regardless of the value of these last three bits. The BUF12840 does not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. Upon receiving a master code, the BUF12840 switches on its Hs mode filters, and communicates at up to 3.4MHz. Additional high-speed transfers may be transmitted without resending the Hs mode byte by generating a repeat START without a STOP. The BUF12840 switches out of Hs mode with the next STOP condition.

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DAC VOLTAGE OUTPUT CODE

Buffer output values are determined by the analog supply voltage (V_S) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1:

$$V_{OUT} = V_S \times \left(\frac{CODE}{1024} \right)$$

Where:

CODE can vary from 0 to 1023. (1)

The BUF12840 outputs are capable of a full-scale voltage output change in typically 5µs, see Figure 9; no intermediate steps are required. The outputs are also capable of a full-scale output change using the BKSEL or LD pin in typically 7µs, see Figure 8.

SOFTWARE DAC OUTPUT UPDATE

Because the BUF12840 features a double-buffered register structure, updating the digital-to-analog converter (DAC) **register** is not the same as updating the DAC **output voltage**. There are two methods for updating the DAC output voltages.

Method 1: Method 1 is used when it is desirable to have the DAC output voltage change immediately after writing to a DAC register. For each write transaction, the master sets data bit 15 to a '1'. The DAC output voltage update occurs after receiving the 16th data bit for the currently-written register, as shown in Figure 11.

Method 2: Method 2 is used when it is desirable to have all DAC output voltages change at the same time. First, the master writes to the desired DAC channels with data bit 15 a '0'. Then, when writing the last desired DAC channel, the master sets data bit 15 to a '1'. All DAC channels are updated at the same time after receiving the 16th data bit.

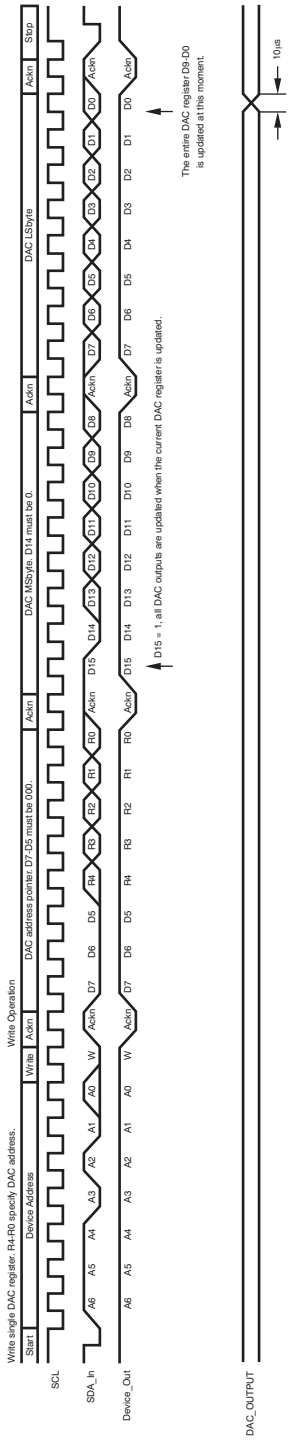


Figure 11. Write DAC_OUT Register Timing

EEPROM ADDRESS SELECT PINS

EA0 and EA1 are used to select the proper EEPROM size. Table 4 shows the start and stop address to load each of the DAC registers. The state of the select pins must be set before the auto read function is activated.

Enable Pin

The status of EN at power-on reset (POR) determines the modes of operation of the BUF12840, as described in Table 3. If EN = 1, the BUF12840 acts as a master; after the data download finishes, the BUF12840 enters slave mode. If EN = 0, the BUF12840 skips the master mode and enters slave mode directly. Once in slave mode after POR, changing the status of EN has no effect on the BUF12840 unless the user issues a GCR (general-call reset) or RA (read again) command.

Table 3. EN Modes of Operation

ENABLE EN	LOGIC LEVEL	EEPROM AUTO READ
Low	0	Disabled
High	1	Enabled

After a POR condition is detected by the BUF12840, a 10ms window occurs. As long as EN goes high in this window, the BUF12840 downloads data from the EEPROM. It is recommended that this pin be tied to DVDD if the application allows. However, if only slave mode operation is needed, EN should be tied to DVSS; it is recommended that after POR occurs wait at least 15ms before addressing the BUF12840. Figure 12 shows how EN affects the operation of the BUF12840 in a typical application.

The BUF12840 tries to read up to 10 times spaced 1ms apart during POR, which can occur if the EEPROM is not ready or if the two-wire bus is kept busy by another device. By the end of the tenth attempt, if the download cannot be started, the BUF12840 goes into slave mode. This action ensures that the BUF12840 enters slave mode within 25ms from the POR condition, regardless if the download is successful or not.

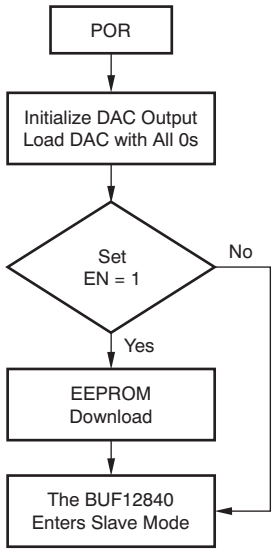


Figure 12. Effect of EN in a Typical Set Up

Table 4. EEPROM Configuration

EA0	EA1	REGISTER BANK0		REGISTER BANK1		ACCEPTABLE EEPROM(1)(2)
		START WORD ADDRESS	END WORD ADDRESS	START WORD ADDRESS	END WORD ADDRESS	
0	0	0	23	24	47	1k, 2k, 4k, 8k, 16k
0	1	361	384	405	428	2k, 4k, 8k, 16k
1	0	0	23	24	47	32k, 64k, 128k, 256k and larger
1	1	361	384	405	428	32k, 64k, 128k, 256k and larger

(1) Any applicable EEPROM chip select pins (A2, A1, A0) must be hardwired to GND.
(2) When EA0 = 0 and EA1 = 1, it is required that the types of EEPROM that supports Page/Block address definition with chip select pins (for example, A0 is part of the Word Address).

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POWER-ON RESET (POR) AUTO READ FUNCTION

Figure 14 depicts the BUF12840 POR Master Mode auto read function and timing. The BUF12840 makes the first attempt to read the external EEPROM 5ms after the POR (power-on reset) condition is met, as shown in Figure 13. Following the initial 5ms wait period, the BUF12840 queries the EEPROM with a digital word that includes an EEPROM address and acknowledge request. If communication with the EEPROM is established, the download finishes in 10ms.

However, if the first read attempt is not successful, the BUF12840 waits for 1ms and then tries to start the download again. This process repeats itself until a successful acknowledge from the EEPROM is detected or until 10 read attempts have been made. If at any time during this process the BUF12840 does detect a successful acknowledge from the EEPROM and the EN pin is properly set, the BUF12840 initiates the upload and reads the contents of the EEPROM, which takes approximately 10ms to complete. The DAC outputpower-on reset value is 0V. The state of V_S (analog supply voltage) does not affect POR or the auto read function.

Immediately after power up, all DAC outputs are set to 0V. During the auto-read function, values are written into the DAC registers as they are being read from the EEPROM. Once the auto-read function is complete, all values are simultaneously loaded from the DAC registers to the DAC outputs. Therefore, all values change together. This action is performed regardless of the state of the LD pin and occurs by default after auto-read is completed.

Once the information is downloaded from the EEPROM, the BUF12840 automatically goes into slave mode, where all slave mode operations are supported. The BUF12840 remains in slave mode until another POR, GCR (general-call reset), or RA (read again) condition is met.

The EN pin should be set to a high level within 15ms of crossing the POR condition. If the EN pin active high state is not detected during the first 10 query attempts, the BUF12840 automatically enters slave mode. If the master mode auto read function must be terminated at any time during the auto read process, the EN pin can be set to a low '0' level that forces the BUF12840 into slave mode and the automatic download process to stop. If an EEPROM acknowledge is not detected during the possible 10 read attempts, the BUF12840 automatically goes into slave mode following the tenth read attempt. Note that the analog power, V_S, does not need to be on during any interface communication.

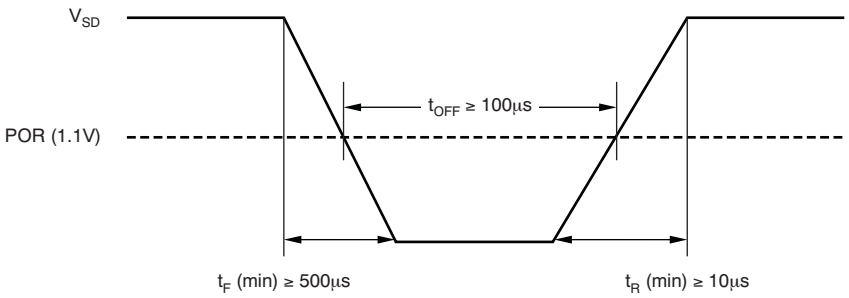


Figure 13. POR

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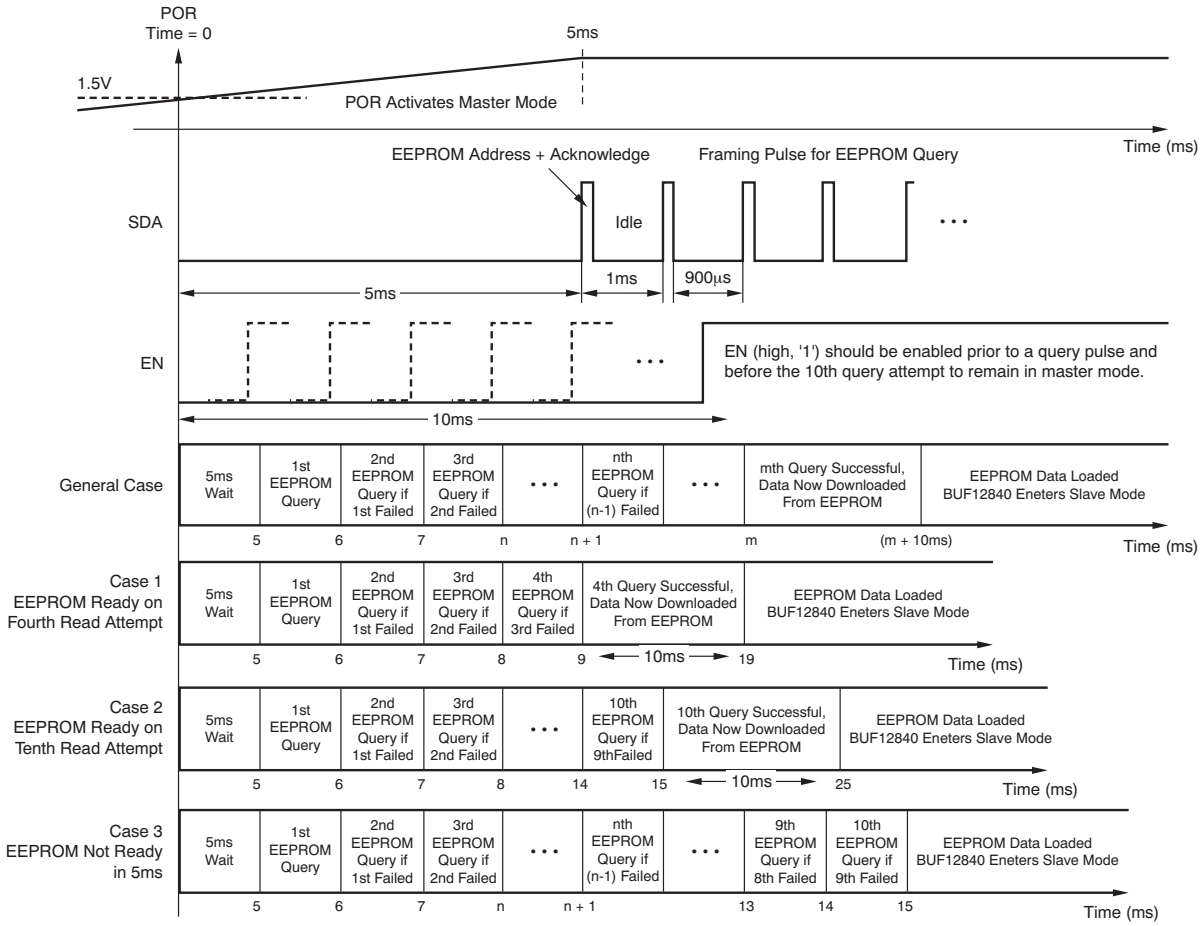


Figure 14. POR Master Mode Auto Read Function and Timing Diagram

MASTER MODE CLOCK SPEED

In master mode, the BUF12840 generates it own clock and puts it on the SCL pin. The frequency is nominally 87kHz, with a maximum value of 100kHz and a minimum value of 71kHz. When the BUF12840 has exclusive access to the two-wire bus, it takes a maximum of 10ms to download both banks of data from the moment power becomes valid. However, when the BUF12840 is in master mode, if there is contention on the two-wire bus because of another active master, the BUF12840 activates its clock synchronization and arbitration engine. In this case, it may take longer for the BUF12840 to finish the download.

The BUF12840 can only synchronize with other masters that operate in Standard Mode (clock speed ≤ 100kHz). It is not recommended to have another master with higher speed operating at the same time. Note that once in slave mode, the BUF12840 supports clock speeds up to 3.4MHz.

GENERAL-CALL RESET

The BUF12840 responds to software general-call reset (GCR). Upon receiving a GCR command, the BUF12840 enters master mode and downloads data from the EEPROM as if the power supply was just switched on.

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READ AGAIN

When the BUF12840 is in slave mode, a read again (RA) command can be issued to restart an EEPROM data download. The RA command follows this process:

1. Send the BUF12840 device address with write bit: *11101000* if A0 = 0 or *11101010* if A0 = 1; the BUF12840 acknowledges this byte.
2. Send register address *00011100*; the BUF12840 acknowledges this byte.
3. Send two bytes of data *xxxxxxxx* and *xxxxxxx1*, where *x* is *don't care*; the BUF12840 acknowledges both bytes.

DAC OUTPUT UPDATE (Using the LD Pin)

Because the BUF12840 features a double-buffered register structure, updating the **DAC register** is not the same as updating the **DAC output voltage**. There are three methods for launching transferred data from the storage registers into the DACs to update the DAC output voltage. It is essential that BKSEL be set to the desired bank because BKSEL determines which bank is loaded.

Method 1: Set the latch pin low (LD = low) to update each DAC output voltage whenever its corresponding register is updated.

Method 2: Set LD high to allow all DAC output voltages to retain the respective values during data transfer until LD goes low, which simultaneously updates the output voltages of all 12 DACs to the new register values.

Method 3 (software mode): LD is maintained high and all 12 DACs are updated when the master writes a '1' in bit 15 of any DAC register. The update occurs after receiving the 16-bit data for the currently-written register.

Use methods 2 and 3 to transfer a future data set into the first bank of registers in advance to prepare for a very fast update of DAC output voltages.

The general-call reset (GCR) and the power-up reset updates the DACs regardless of the state of the latch pin. For a list of DAC addresses; see Table 5.

BKSEL PIN

The BUF12840 has the ability to store two distinct gamma curves in two different memory banks. One of the two available banks is selected using the external input pin, BKSEL. When this pin is low, BANK0 is selected; when this pin is high, BANK1 is selected.

The two-wire master also has the ability to update (acquire) the DAC registers with the last programmed nonvolatile memory values using software control. The bank to be acquired depends on the state of BKSEL.

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WRITE BOTH BANKS OF DAC REGISTERS

In slave mode, writes to both banks are accomplished through the two-wire bus; there are different register address for the two banks. The BKSEL pin does not impact writing to each of the banks. Table 5 details the DAC addresses for each bank.

DAC_OUT voltages update with the appropriate bank values based on a combination of LD and BKSEL pins.

Case 1: DAC_OUT updates to BANK1 because the LD pin is low and BKSEL is high. **Case 2:** DAC_OUT updates to BANK0 because BKSEL and the LD pin are low. **Case 3:** DAC_OUT does not update when the LD pin is high. **Case 4:** DAC_OUT updates to BANK0 because the LD pin and BKSEL are low. **Case 5:** DAC_OUT updates to BANK1 because the LD pin is low and BKSEL is high.

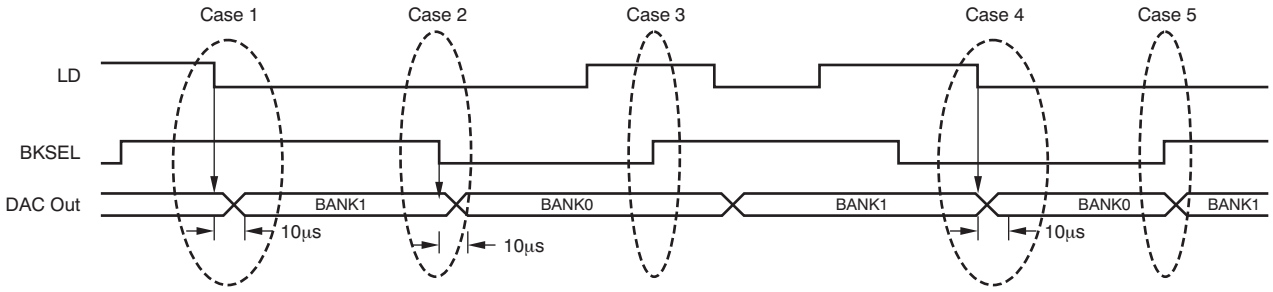


Figure 15. LD/BKSEL Function and DAC Output TIming Diagram

Table 5. BANK0 and BANK1 DAC Addresses

GAMMA BUFFER OUTPUT	BANK0						BANK1					
	REGISTER	R4	R3	R2	R1	R0	REGISTER	R4	R3	R2	R1	R0
OUT0	Register 0 BANK0	0	0	0	0	0	Register 0 BANK1	1	0	0	0	0
OUT1	Register 1 BANK0	0	0	0	0	1	Register 1 BANK1	1	0	0	0	1
OUT2	Register 2 BANK0	0	0	0	1	0	Register 2 BANK1	1	0	0	1	0
OUT3	Register 3 BANK0	0	0	0	1	1	Register 3 BANK1	1	0	0	1	1
OUT4	Register 4 BANK0	0	0	1	0	0	Register 4 BANK1	1	0	1	0	0
OUT5	Register 5 BANK0	0	0	1	0	1	Register 5 BANK1	1	0	1	0	1
OUT6	Register 6 BANK0	0	0	1	1	0	Register 6 BANK1	1	0	1	1	0
OUT7	Register 7 BANK0	0	0	1	1	1	Register 7 BANK1	1	0	1	1	1
OUT8	Register 8 BANK0	0	1	0	0	0	Register 8 BANK1	1	1	0	0	0
OUT9	Register 9 BANK0	0	1	0	0	1	Register 9 BANK1	1	1	0	0	1
OUT10	Register 10 BANK0	0	1	0	1	0	Register 10 BANK1	1	1	0	1	0
OUT11	Register 11 BANK0	0	1	0	1	1	Register 11 BANK1	1	1	0	1	1

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TIMING DIAGRAMS

Figure 16 describes the timing operations on the BUF12840. Parameters for Figure 16 are defined in Table 6. Bus definitions are:

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low, while the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition, denoted as *S* in Figure 16.

Stop Data Transfer: A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer terminates with a repeated START or STOP condition, denoted as *P* in Figure 16.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges data transfer.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, data transfer termination can be signaled by the master generating a Not-Acknowledge on the last byte that has been transmitted by the slave.

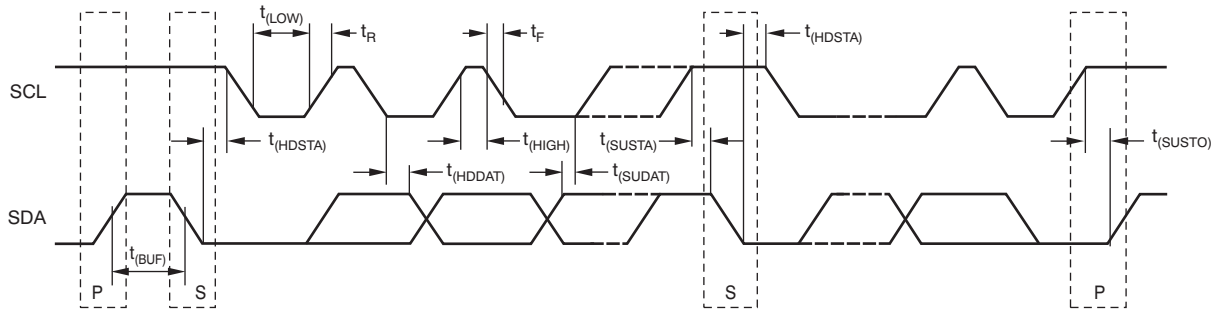


Figure 16. Two-Wire Timing Diagram

Table 6. Timing Characteristics for Figure 16

PARAMETER		STANDARD MODE		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
SCL operating frequency	$f_{(SCL)}$	0	0.1	0	0.4	0	3.4	MHz
Bus free time between STOP and START condition	$t_{(BUF)}$	4000		600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	100		100		100		ns
Repeated START condition setup time	$t_{(SUSTA)}$	100		100		100		ns
STOP condition setup time	$t_{(SUSTO)}$	100		100		100		ns
Data hold time	$t_{(HDDAT)}$	1(1)		0(1)		0(2)		ns
Data setup time	$t_{(SUDAT)}$	250		100		10		ns
SCL clock low period	$t_{(low)}$	4700		1300		160		ns
SCL clock high period	$t_{(high)}$	4000		600		60		ns
Clock/data fall time	t_F		300		300		160	ns
Clock/data rise time	t_R		300		300		160	ns
for SCLK ≤ 100kHz			1000		1000			ns

(1) For cases with a fall time of SCL less than 20ns and/or the rise time or fall time of SDA less than 20ns, the hold time should be greater than 20ns.
(2) For cases with a fall time of SCL less than 10ns and/or the rise or fall time of SDA less than 10ns, the hold time should be greater than 10ns.

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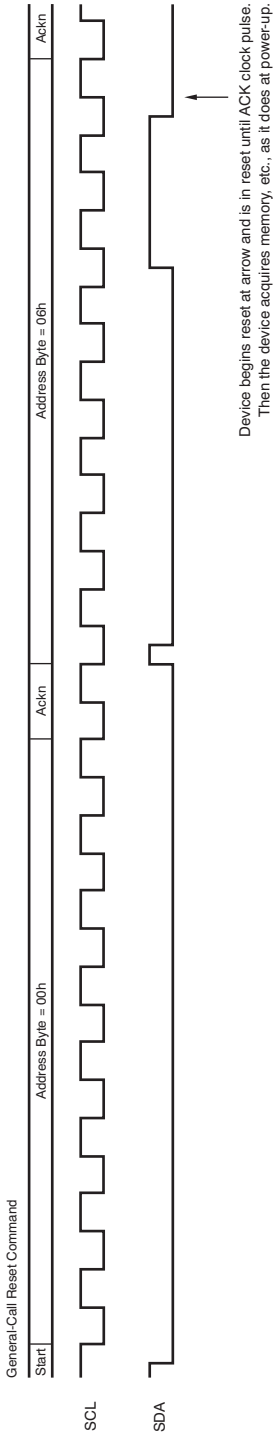


Figure 17. General-Call Reset Timing

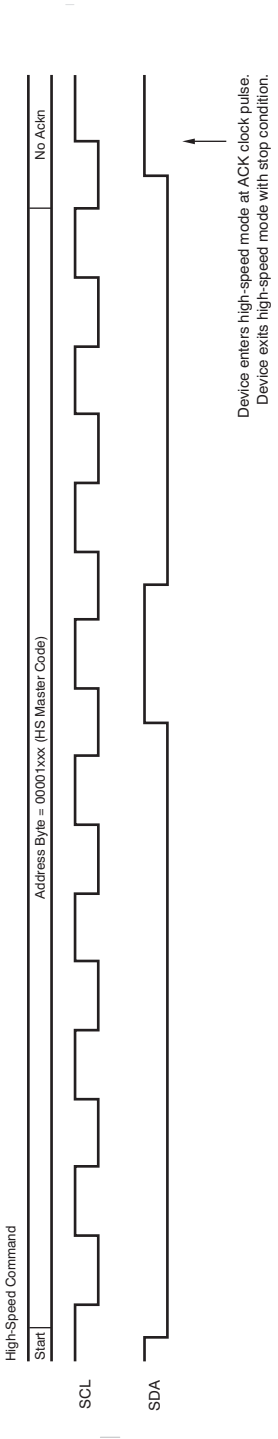


Figure 18. High-Speed Mode Timing

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DYNAMIC GAMMA CONTROL

Dynamic gamma control is a technique used to improve the picture quality in LCD TV applications. The brightness in each picture frame is analyzed and the gamma curves are adjusted on a frame-by-frame basis. The gamma curves are typically updated during the short vertical blanking period in the video signal. Figure 19 shows a block diagram using the BUF12840 for dynamic gamma control.

The BUF12840 is ideally suited for rapidly changing the gamma curves as a result of its unique topology:

- Double register input structure to the DAC
- Fast serial interface
- Simultaneous updating of all DACs by software. See the *Read/Write Operations* section to write to all registers and the *Output Latch* sections.

END-USER SELECTED GAMMA CONTROL

The double register input structure saves programming time by allowing updated DAC values to be pre-stored into the first register bank. Storage of this data can occur while a picture is still being displayed. Because the data are only stored into the first register bank, the DAC output values remain unchanged—the display is unaffected. During the vertical sync period, the DAC outputs (and therefore, the gamma voltages) can be quickly updated either by using an additional control line connected to the LD pin, or through software—writing a '1' in bit 15 of any DAC register. For details on the operation of the double register input structure, see the *Output Latch* section.

Example: Update all 12 registers simultaneously via software.

Step 1: Check if the LD pin is placed in a high state.

Step 2: Write DAC registers 1-12 with bit 15 always '0'.

Step 3: Write any DAC register a second time with identical data. Make sure that bit 15 is '1'. All DAC channels are updated simultaneously after receiving the last bit of data.

Example: Update all 12 registers simultaneously via hardware.

Step 1: Toggle the BKSEL pin to the desired gamma curve, either Bank0 or Bank1.

Step 2: Toggle the LD pin low. When this occurs, all 12 internal DAC registers are updated after 1µs. The output then slews to the new voltage level. The time to change between two gamma voltage settings is then dependent on the slew rate of the DAC plus the gamma buffer and the change in voltage required. This value can be obtained by referring to the *Large-Signal Step Response* curve (Figure 9).

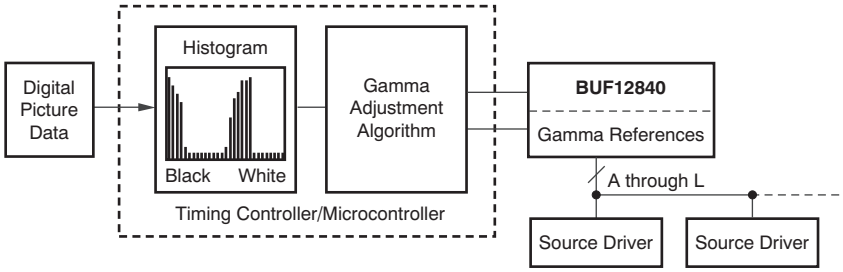


Figure 19. Dynamic Gamma Control

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READ/WRITE OPERATIONS

The BUF12840 is able to read from a single DAC or multiple DACs, or write to the register of a single DAC, or multiple DACs in a single communication transaction. DAC addresses for BANK0 begin with 00000, which corresponds to Register 0, through 01011, which corresponds to Register 11. DAC addresses for BANK1 begin with 10000, which corresponds to Register 0, through 11011, which corresponds to Register 11; see Table 5. Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH performs a read transaction.

Writing

To write to a single DAC register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF12840 acknowledges this byte.
3. Send a DAC address byte. Bits D7−D5 are unused and should be set to 0. Bits D4−D0 are the DAC address; see Table 5. Only DAC addresses 00000 to 01011 and 10000 to 11011 are valid and acknowledged.
4. Send two bytes of data for the specified DAC. Begin by sending the most significant byte first (bits D15−D8, of which only bits D9 and D8 are used), followed by the least significant byte (bits D7−D0). The DAC register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

   See Figure 20.

The BUF12840 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register is not updated. Updating the DAC register is not the same as updating the DAC output voltage; see the *Output Latch* section.

The process of updating multiple registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the addressed register, the master continues to send data for the next register. The BUF12840 automatically and sequentially steps through subsequent registers as additional data are sent. The process continues until all desired registers have been updated or a STOP condition is sent.

To write to multiple registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF12840 acknowledges this byte.
3. Send either the Register 0 address byte to start at the first DAC or send the address of whichever DAC is the first to be updated. The BUF12840 begins with this DAC and steps through subsequent DACs in sequential order.
4. Send the bytes of data. The first two bytes are for the DAC addressed in step 3. Its register is automatically updated after receiving the second byte. The next two are for the following DAC. The DAC register is updated after receiving the fourth byte. The last two bytes are for Register 11. The DAC register is updated after receiving the 24th byte. For each DAC, begin by sending the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning), followed by the least significant byte (bits D7−D0).
5. Send a STOP condition on the bus.

   See Figure 21.

When the DAC registers are written through a two-wire communication, changing the BKSEL pin does not affect the communication because the banks have different addresses. However, when loading the DACs through an I^2C communication, the bank to be loaded is decided by the BKSEL pin. Therefore, if the BKSEL pin is switched during a two-wire load, the new value of BKSEL determines the bank that is loaded.

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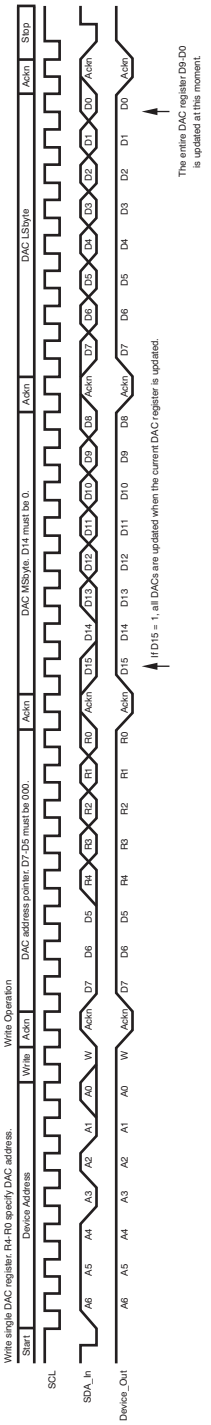


Figure 20. Write SIngle DAC Register Timing

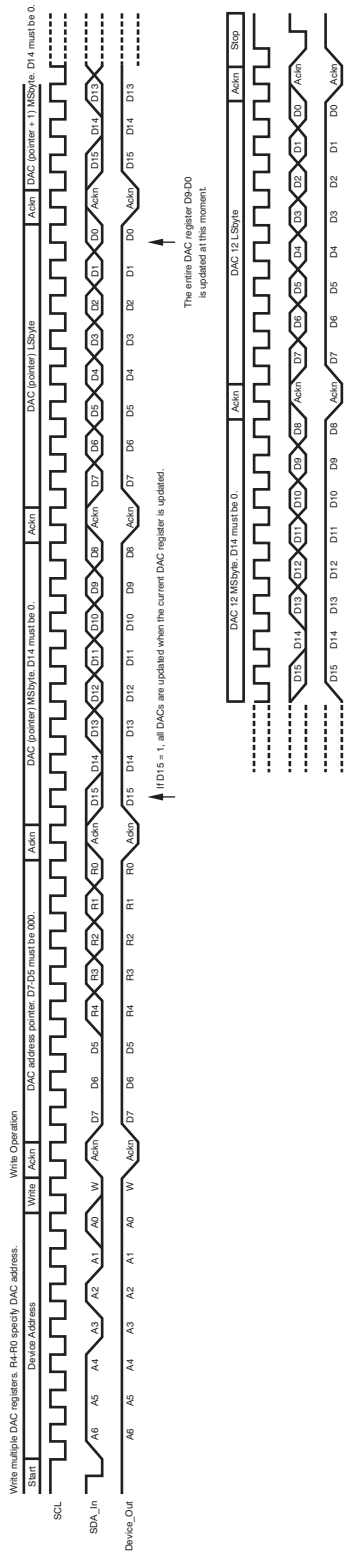


Figure 21. Write Multiple DACs Register Timing

The BUF12840 acknowledges each byte. To terminate communication, send a STOP or START condition on the bus. Only DACs that have received both bytes are updated.

Reading

To read the register of one DAC:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF12840 acknowledges this byte.
3. Send a DAC address byte. Bits D7−D5 are unused and should be set to 0. Bits D4−D0 are the DAC address; see Table 5. Only DAC addresses 00000 to 01011 and 10000 to 11011 are valid and acknowledged.
4. Send a START or STOP/START condition on the bus.
5. Send correct device address and read/write bit = HIGH. The BUF12840 acknowledges this byte.
6. Receive two bytes of data. They are for the specified DAC. The first received byte is the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning); the next is the least significant byte (bits D7−D0).
7. Acknowledge after receiving each byte.
8. Send a STOP condition on the bus.

See Figure 22.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.

To read multiple DAC registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF12840 acknowledges this byte.
3. Send either the Register 0 address byte to start at the first DAC or send the address byte for whichever DAC is the first in the sequence of DACs to be read. The BUF12840 begins with this DAC and steps through subsequent DACs in sequential order.
4. Send the device address and read/write bit = HIGH.
5. Receive bytes of data. The first two bytes are for the specified DAC. The first received byte is the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning). The next byte is the least significant byte (bits D7−D0).
6. Acknowledge after receiving each byte.
7. When all desired DACs have been read, send a STOP or START condition on the bus.

See Figure 23.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.

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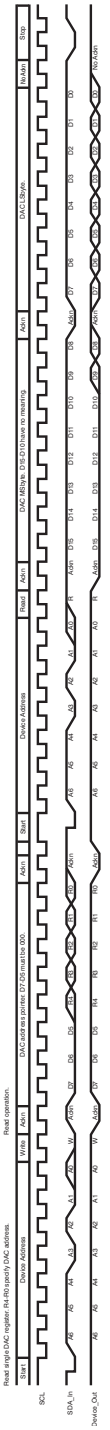


Figure 22. Read Single Register Timing

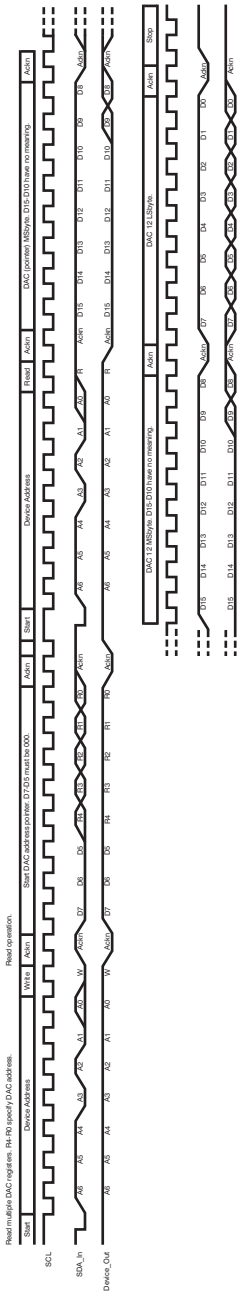


Figure 23. Read Multiple DACs Register Timing

OUTPUT PROTECTION

The BUF12840 output stages can safely source and sink the current levels indicated in Figure 1. However, there are other modes where precautions must be taken to prevent to the output stages from being damaged by excessive current flow. The outputs (OUT1 through OUT12) include electrostatic discharge (ESD) protection diodes, as shown in Figure 24. Normally, these diodes do not conduct and are passive during typical device operation. Unusual operating conditions can occur where the diodes may conduct, potentially subjecting them to high, even damaging current levels. These conditions are most likely to occur when a voltage applied to an output exceeds (V_S) + 0.5V, or drops below GND – 0.5V.

One common scenario where this condition can occur is when the output pin is connected to a sufficiently large capacitor, and the BUF12840 power-supply source (V_S) is suddenly removed. Removing the power-supply source allows the capacitor to discharge through the current-steering diodes. The energy released during the high current flow period causes the power dissipation limits of the diode to be exceeded. Protection against the high current flow may be provided by placing a Schottky diode, as shown in Figure 24. This diode must be capable of discharging the capacitor without allowing more than 0.5V to develop across the internal ESD current-steering diodes. It is not recommended that large capacitors be connected to the output of the gamma buffers.

Figure 25 shows a simplified schematic of the input pins A0, BKSEL, EN, EA0, EA1, and LD. As shown, there are no ESD cells or diodes to supply; therefore, the input to the device can go above supply but must be lower than 6V.

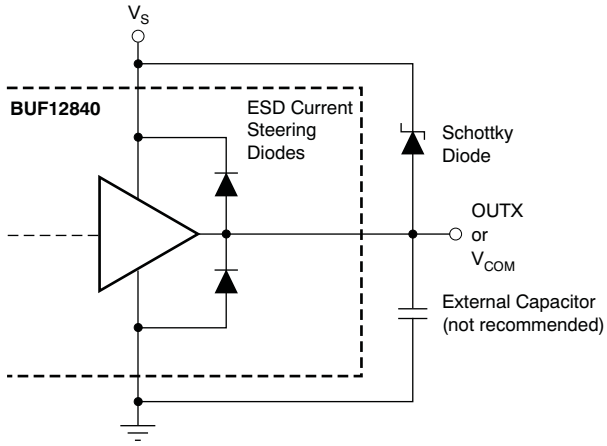


Figure 24. Output Pins ESD Protection Current-Steering Diodes

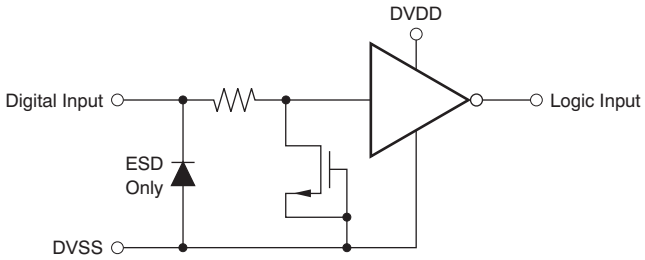


Figure 25. Digital Input Model

Figure 26 shows a simplified schematic of the SDA and SCL input/output pins. As shown, there are no ESD cells or diodes to supply; therefore, the input to the device can go above ground but must be lower than 6V.

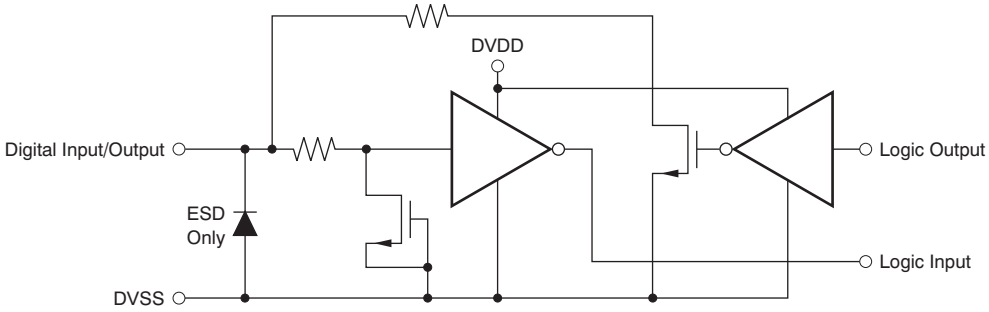


Figure 26. Digital Input/Output Model

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October, 2010) to Revision A	Page
• Corrected error in x-axis value for Figure 9	6

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF12840AIRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 95	BUF 12840	Samples
BUF12840AIRGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 95	BUF 12840	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

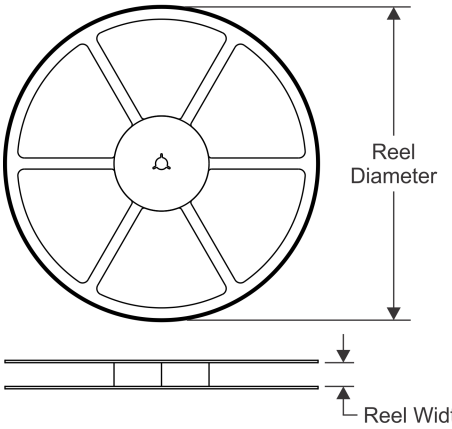
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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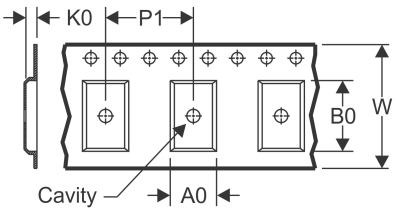
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

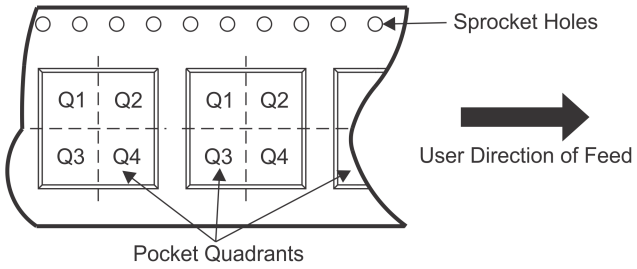


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

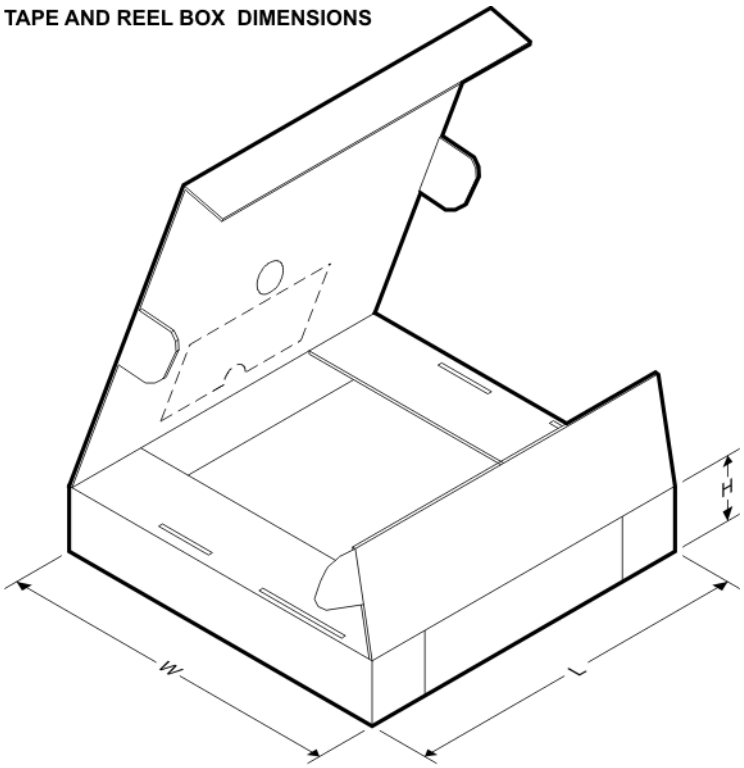
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF12840AIRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

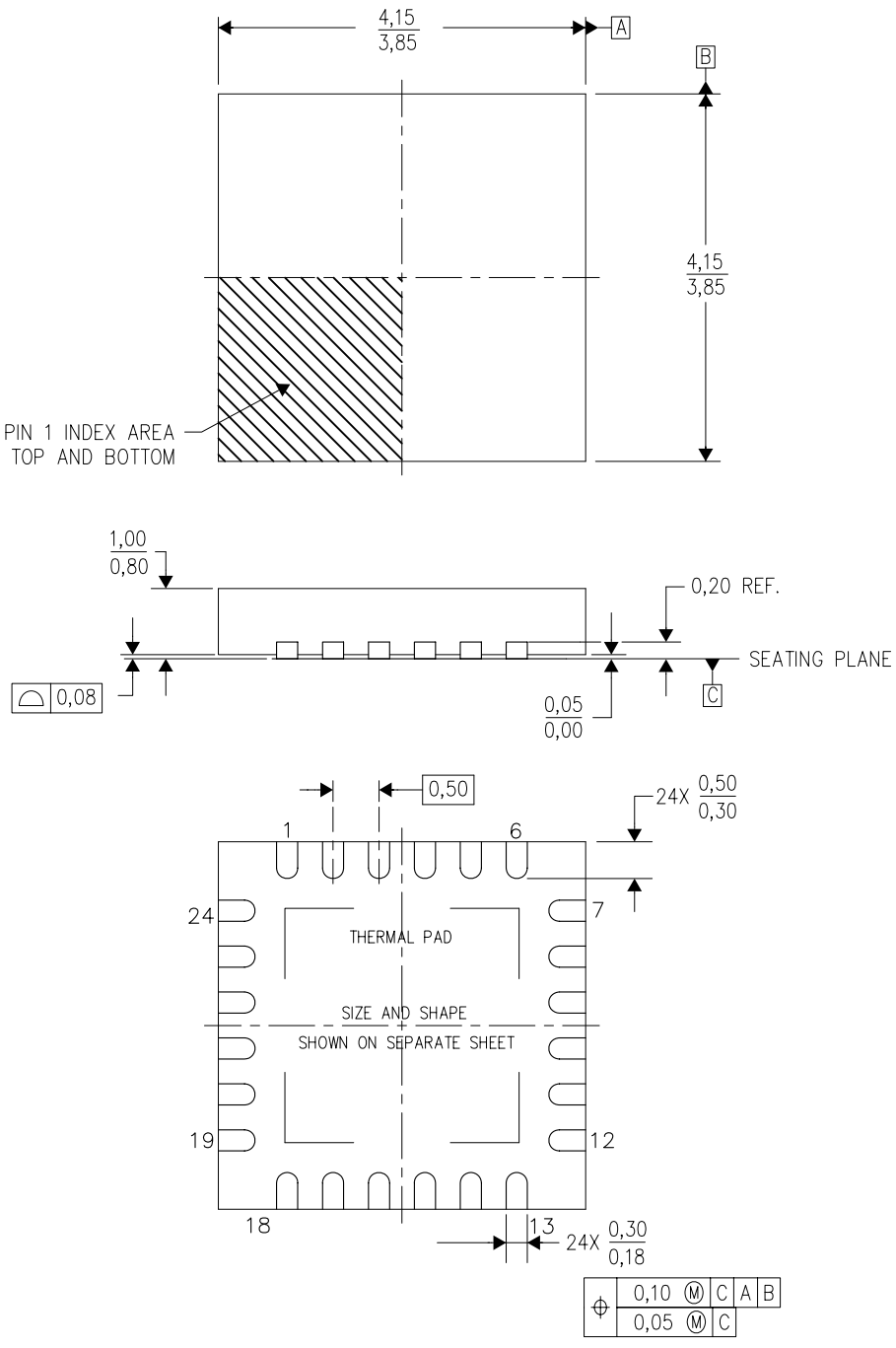
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF12840AIRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

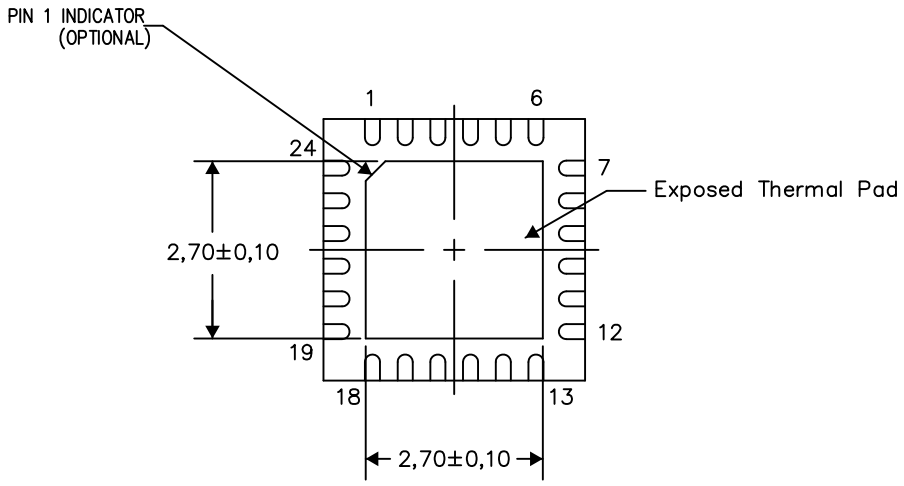
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



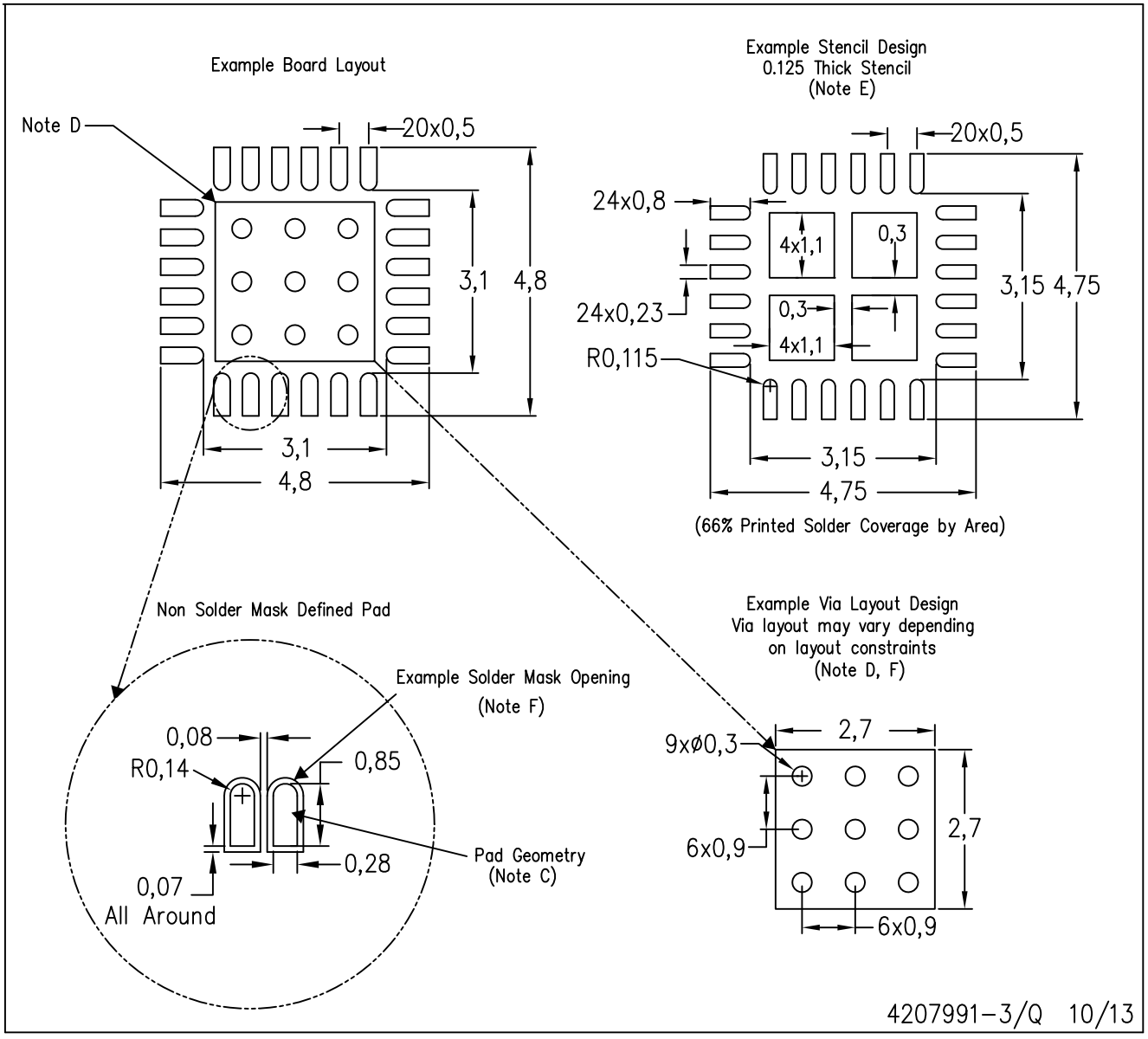
Bottom View

Exposed Thermal Pad Dimensions

4206344–4/AE 10/13

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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