



## UIC811

## LINEAR INTEGRATED CIRCUIT

### MICROPROCESSOR RESET CIRCUITS

#### DESCRIPTION

The UTC **UIC811** series are resetting circuits which can monitor power supplies especially in microprocessor based systems.

In normal operation, the UTC **UIC811** series can assert a reset under any of the following situation: the power supply drops below a designated reset threshold level (which is available for 3V or 3.3V or 5V system) or  $\overline{MR}$  is forced low.

There is an internal active low  $\overline{RESET}$  output which has already been guaranteed to remain asserted for at 140ms least while  $V_{CC}$  rises above the designed threshold level.

#### FEATURES

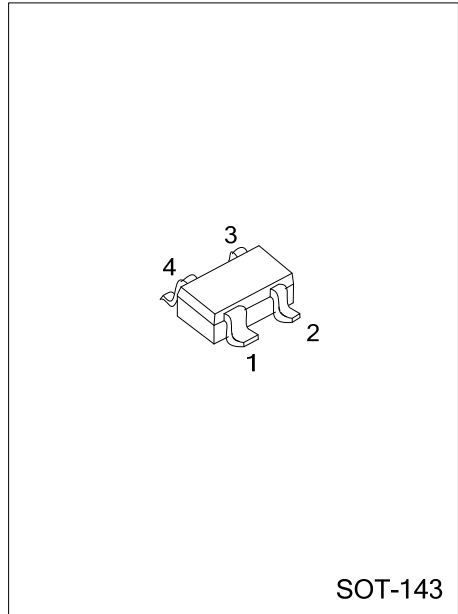
- \* Voltage monitor for 3V or 3.3V or 5V power supplies
- \* Valid  $\overline{RESET}$  remains with  $V_{CC}$  as low as 1V
- \* Typical supply current: 5 $\mu$ A
- \* Fixed 140ms minimum reset pulse width
- \* With Manual reset input
- \* Halogen Free

#### ORDERING INFORMATION

Ordering Number	Package	Packing
UIC811G-x-AD4-R	SOT-143	Tape Reel

Note: x: Output Voltage, refer to Marking Information.

<p>UIC811G-x-AD4-R</p> <p>(1) Packing Type (2) Package Type (3) Output Voltage Code (4) Halogen Free</p>	<p>(1) R: Tape Reel (2) AD4: SOT-143 (3) x: Refer to Marking Information (4) G: Halogen Free</p>
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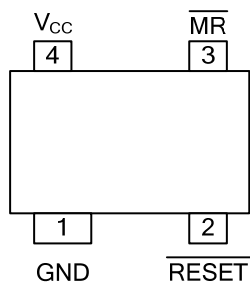
# UIC811

## LINEAR INTEGRATED CIRCUIT

### MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
SOT-143	A : 2.63V B : 2.93V C : 3.08V D : 4.00V E : 4.38V F : 5.00V	

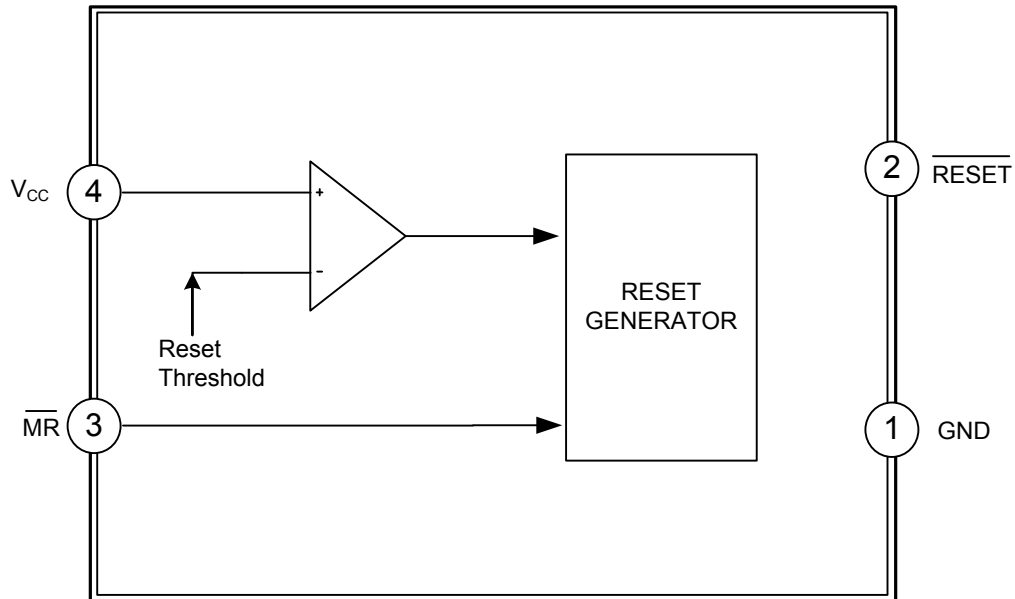
### PIN CONFIGURATION



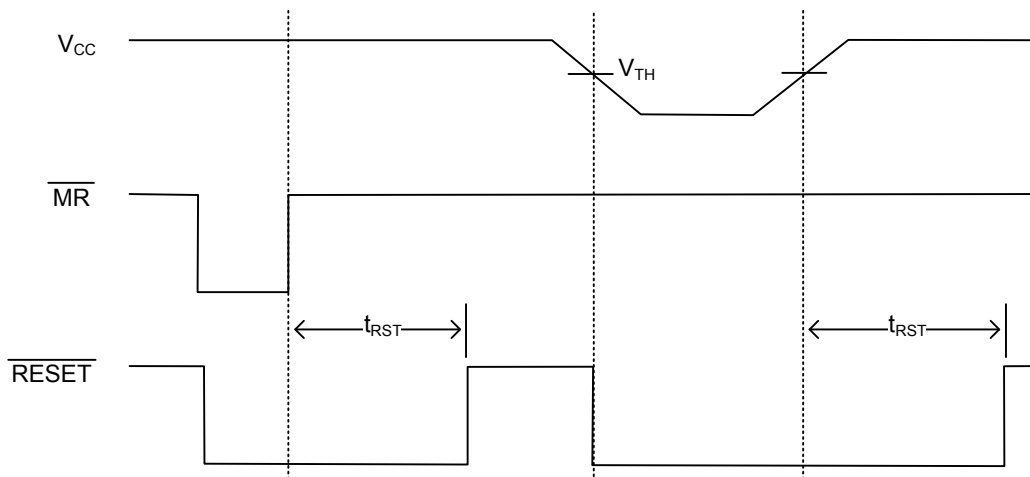
### PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground
2	RESET	This pin will fall low after the $V_{CC}$ 's falling below the reset threshold voltage and it also can remain asserted for at least 140ms min after $V_{CC}$ 's rising upon the reset threshold.
3	MR	Input of manual reset. A reset can be forced by a logic low on MR . As the MR is held low, the reset will remain asserted, and until the MR rise high, the reset will remain 140ms min at least. When it is float that means it is unused.
4	$V_{CC}$	Input of power supply.

## ■ BLOCK DIAGRAM



## ■ FUNCTIONAL DIAGRAM



Reset Timing Diagram

### ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	$V_{CC}$	-0.3~+6.0	V
Input Current ( $V_{CC}, \overline{MR}$ )	$I_{IN}$	20	mA
Output Current ( $\overline{RESET}$ )	$I_{OUT}$	20	mA
Rate of Rise	$V_{CC(RR)}$	100	V/ $\mu$ s
Power Dissipation ( $T_a = +70^\circ\text{C}$ )	$P_D$	320	mW
Operating Temperature	$T_{OPR}$	-40~+85	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-65~+150	$^\circ\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The device is not guaranteed to function outside its operating rating.

### ■ ELECTRICAL CHARACTERISTICS

**UIC811-A (2.63V)** ( $V_{CC} = 3\text{V}$ ,  $T_a = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	$V_{CC}$	$T_a = -40 \sim +85^\circ\text{C}$	1		6	V
Supply Current	$I_{CC}$	$V_{CC} = 3.0\text{V}$ , no load		5	10	$\mu\text{A}$
Reset Voltage Threshold	$V_{TH}$		2.55	2.63	2.70	V
Reset Timeout Period	$t_{RST}$		140	240	560	ms
$\overline{RESET}$ Output Voltage	$V_{OH}$	$I_{SOURCE} = 500\mu\text{A}$	2.4			V
	$V_{OL}$	$V_{CC} = V_{TH} \text{ min}$ , $I_{SINK} = 1.2\text{mA}$ $V_{CC} > 1\text{V}$ , $I_{SINK} = 50\mu\text{A}$ , $T_a = -40 \sim +85^\circ\text{C}$			0.3	V
$\overline{MR}$ Input Threshold	$V_{IH}$		2.1			V
	$V_{IL}$				0.75	V
$\overline{MR}$ Minimum Pulse Width			10			$\mu\text{s}$
$\overline{MR}$ to Reset Delay				0.5		$\mu\text{s}$
$\overline{MR}$ Pull-Up Resistance			10	20	30	k $\Omega$
$\overline{MR}$ Glitch Immunity				100		ns

**UIC811-B (2.93V)** ( $V_{CC} = 3.3\text{V}$ ,  $T_a = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	$V_{CC}$	$T_a = -40 \sim +85^\circ\text{C}$	1		6	V
Supply Current	$I_{CC}$	$V_{CC} = 3.3\text{V}$ , no load		5	10	$\mu\text{A}$
Reset Voltage Threshold	$V_{TH}$		2.85	2.93	3.00	V
Reset Timeout Period	$t_{RST}$		140	240	560	ms
$\overline{RESET}$ Output Voltage	$V_{OH}$	$I_{SOURCE} = 500\mu\text{A}$	2.64			V
	$V_{OL}$	$V_{CC} = V_{TH} \text{ min}$ , $I_{SINK} = 1.2\text{mA}$ $V_{CC} > 1\text{V}$ , $I_{SINK} = 50\mu\text{A}$ , $T_a = -40 \sim +85^\circ\text{C}$			0.3	V
$\overline{MR}$ Input Threshold	$V_{IH}$		2.31			V
	$V_{IL}$				0.825	V
$\overline{MR}$ Minimum Pulse Width			10			$\mu\text{s}$
$\overline{MR}$ to Reset Delay				0.5		$\mu\text{s}$
$\overline{MR}$ Pull-Up Resistance			10	20	30	k $\Omega$
$\overline{MR}$ Glitch Immunity				100		ns

### ■ ELECTRICAL CHARACTERISTICS(Cont.)

**UIC811-C (3.08V)** ( $V_{CC} = 3.3V$ ,  $T_a = 25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	$V_{CC}$	$T_a = -40 \sim +85^\circ C$	1		6	V
Supply Current	$I_{CC}$	$V_{CC} = 3.3V$ , no load		5	10	$\mu A$
Reset Voltage Threshold	$V_{TH}$		3.00	3.08	3.15	V
Reset Timeout Period	$t_{RST}$		140	240	560	ms
Reset Output Voltage	$V_{OH}$	$I_{SOURCE} = 500\mu A$	2.64			V
	$V_{OL}$	$V_{CC} = V_{TH} \text{ min, } I_{SINK} = 1.2mA$ $V_{CC} > 1V, I_{SINK} = 50\mu A, T_a = -40 \sim +85^\circ C$			0.3	V
$\overline{MR}$ Input Threshold	$V_{IH}$		2.31			V
	$V_{IL}$				0.825	V
$\overline{MR}$ Minimum Pulse Width			10			$\mu S$
$\overline{MR}$ to Reset Delay				0.5		$\mu S$
$\overline{MR}$ Pull-Up Resistance			10	20	30	k $\Omega$
$\overline{MR}$ Glitch Immunity				100		ns

**UIC811-D (4.00V)** ( $V_{CC} = 5V$ ,  $T_a = 25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	$V_{CC}$	$T_a = -40 \sim +85^\circ C$	1		6	V
Supply Current	$I_{CC}$	$V_{CC} = 5.0V$ , no load		5	15	$\mu A$
Reset Voltage Threshold	$V_{TH}$		3.89	4.00	4.10	V
Reset Timeout Period	$t_{RST}$		140	240	560	ms
Reset Output Voltage	$V_{OH}$	$I_{SOURCE} = 800\mu A$	3.5			V
	$V_{OL}$	$V_{CC} = V_{TH} \text{ min, } I_{SINK} = 3.2mA$ $V_{CC} > 1V, I_{SINK} = 50\mu A, T_a = -40 \sim +85^\circ C$			0.4	V
$\overline{MR}$ Input Threshold	$V_{IH}$		2.3			V
	$V_{IL}$				0.8	V
$\overline{MR}$ Minimum Pulse Width			10			$\mu S$
$\overline{MR}$ to Reset Delay				0.5		$\mu S$
$\overline{MR}$ Pull-Up Resistance			10	20	30	k $\Omega$
$\overline{MR}$ Glitch Immunity				100		ns

**UIC811-E (4.38V)** ( $V_{CC} = 5V$ ,  $T_a = 25^\circ C$ , unless otherwise specified)

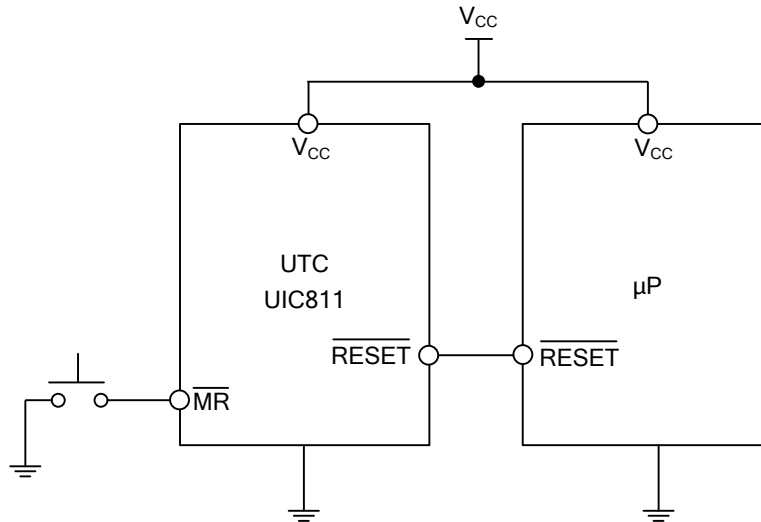
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	$V_{CC}$	$T_a = -40 \sim +85^\circ C$	1		6	V
Supply Current	$I_{CC}$	$V_{CC} = 5.0V$ , no load		5	15	$\mu A$
Reset Voltage Threshold	$V_{TH}$		4.25	4.38	4.50	V
Reset Timeout Period	$t_{RST}$		140	240	560	ms
Reset Output Voltage	$V_{OH}$	$I_{SOURCE} = 800\mu A$	3.5			V
	$V_{OL}$	$V_{CC} = V_{TH} \text{ min, } I_{SINK} = 3.2mA$ $V_{CC} > 1V, I_{SINK} = 50\mu A, T_a = -40 \sim +85^\circ C$			0.4	V
$\overline{MR}$ Input Threshold	$V_{IH}$		2.3			V
	$V_{IL}$				0.8	V
$\overline{MR}$ Minimum Pulse Width			10			$\mu S$
$\overline{MR}$ to Reset Delay				0.5		$\mu S$
$\overline{MR}$ Pull-Up Resistance			10	20	30	k $\Omega$
$\overline{MR}$ Glitch Immunity				100		ns

■ ELECTRICAL CHARACTERISTICS(Cont.)

**UIC811-F (5.0V)** ( $V_{CC} = 5.5V$ ,  $T_a = 25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	$V_{CC}$	$T_a = -40 \sim +85^\circ C$	1		6	V
Supply Current	$I_{CC}$	$V_{CC} = 5.0V$ , no load			25	$\mu A$
Reset Voltage Threshold	$V_{TH}$		4.85	5	5.15	V
Reset Timeout Period	$t_{RST}$		140	240	560	ms
Reset Output Voltage	$V_{OH}$	$I_{SOURCE} = 800\mu A$	4.55			V
	$V_{OL}$	$V_{CC} = V_{TH} \text{ min, } I_{SINK} = 3.2mA$ $V_{CC} > 1V, I_{SINK} = 50\mu A, T_a = -40 \sim +85^\circ C$			0.4	V
MR Input Threshold	$V_{IH}$		2.45			V
	$V_{IL}$				0.8	V
MR Minimum Pulse Width			10			$\mu S$
MR to Reset Delay				0.5		$\mu S$
MR Pull-Up Resistance			10	20	30	$k\Omega$
MR Glitch Immunity				100		ns

### ■ TYPICAL APPLICATION CIRCUIT



### ■ APPLICATION INFORMATION

#### Microprocessor Reset

As soon as  $V_{CC}$  falls below the reset threshold voltage, the  $\overline{\text{RESET}}$  pin is asserted. But the  $\overline{\text{RESET}}$  pin can keep asserted for a period of 140ms after  $V_{CC}$  rose above the reset threshold voltage. After a power failure the reset operation can keep the processor being reset and powers up properly.

#### $V_{CC}$ Transients

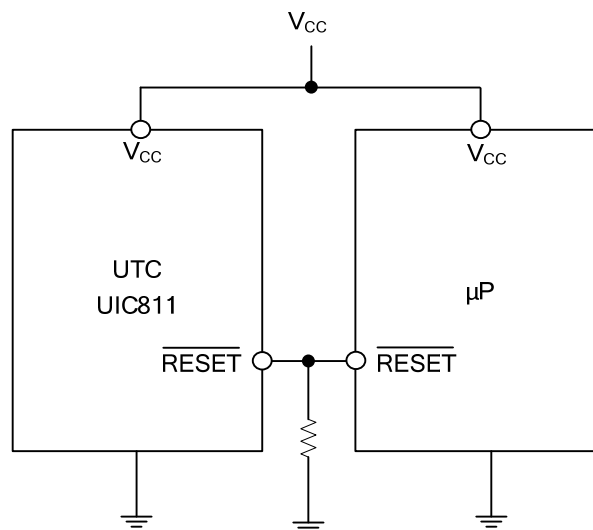
The UTC **UIC811** series won't cause a reset typically as this situation: a negative-going transient 125mV below the reset threshold with a duration of 20μs or less.

#### Interfacing to Bidirectional Reset Pins

Connecting a 4.7kΩ resistor in series with the UTC **UIC811** series output and the μP reset pin can make the UTC **UIC811** series interface with μPs with bidirectional reset pins.

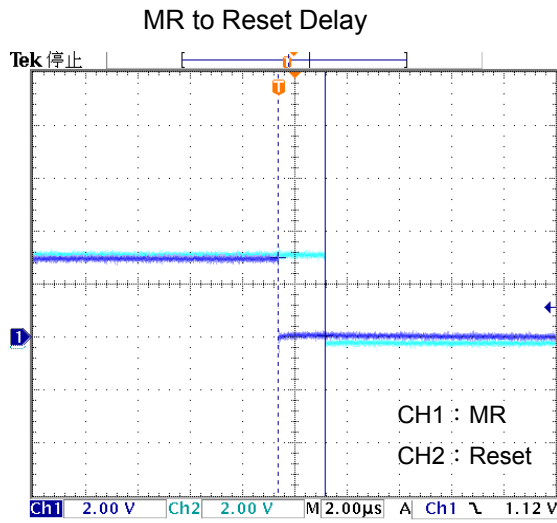
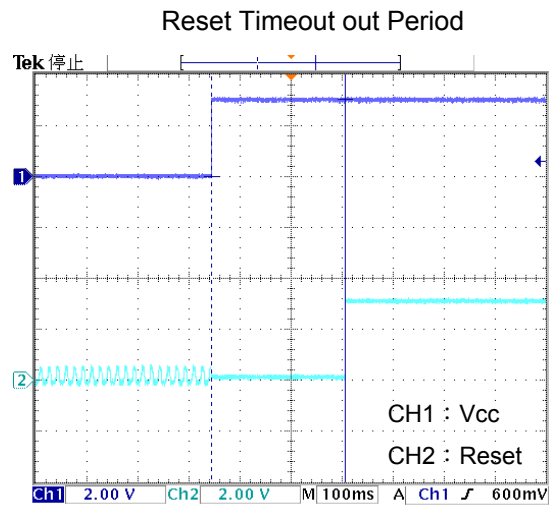
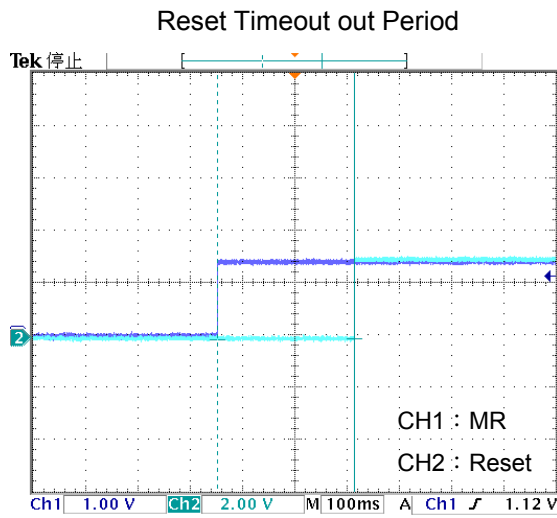
#### $\overline{\text{RESET}}$ Valid at Low Voltage

As the figure below, adding a resistor which is recommended 100kΩ can ensure the  $\overline{\text{RESET}}$  output remains low with  $V_{CC}$  down to 0V. The size of the resistor should be not too large which will load the output excessively and not too small which can pull-down any stray leakage currents.



Reset Valid to  $V_{CC} = 0V$

### ■ TYPICAL CHARACTERISTICS





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