ATA8210/ATA8215

UHF ASK/FSK Receiver

SUMMARY DATASHEET

Features

- AVR® microcontroller core with 1Kbyte SRAM and 24Kbyte RF library in firmware (ROM)
- Atmel® ATA8210: 20Kbyte of user Flash
- Atmel ATA8215: No user memory — RF library in firmware only
- Supported frequency ranges
  - Low-band 310MHz to 318MHz, 418MHz to 477MHz
  - High-band 836MHz to 956MHz
  - 315.00MHz/433.92MHz/868.30MHz and 915.00MHz with one 24.305MHz crystal
- Low current consumption
  - 9.8mA for RXMode (Low-band), 1.2mA for 21ms cycle three-channel polling
- Typical OFFMode current of 5nA (maximum 600nA at Vs = 3.6V and T = 85°C)
- Supports the 0dBm class of ARIB STD-T96
- Input 1dB compression point
  - –48dBm (full sensitivity level)
  - –20dBm (active antenna damping)
- Programmable channel frequency with fractional-N PLL
  - 93Hz resolution for Low-band
  - 185Hz resolution for High-band
- FSK deviation ±0.375kHz to ±93kHz
- FSK sensitivity (Manchester coded) at 433.92MHz
  - –108.5dBm at 20Kbit/s Δf = ±20kHz BWIF = 165kHz
  - –111dBm at 10Kbit/s Δf = ±10kHz BWIF = 165kHz
  - –114dBm at 5Kbit/s Δf = ±5kHz BWIF = 165kHz
  - –122.5dBm at 0.75Kbit/s Δf = ±0.75kHz BWIF = 25kHz
- ASK sensitivity (Manchester coded) at 433.92MHz
  - –110.5dBm at 20Kbit/s BWIF = 80kHz
  - –125dBm at 0.5Kbit/s BWIF = 25kHz
- Programmable Rx-IF bandwidth 25kHz to 366kHz (approximately 10% steps)
- Blocking (BWIF = 165kHz): 64dBc at frequency offset = 1MHz and 48dBc at 225kHz
- High image rejection: 55dB at 315MHz/433.92MHz and 47dB at 868.3MHz/915MHz without calibration
- Supported data rate in buffered mode 0.5Kbit/s to 80Kbit/s (120Kbit/s NRZ)

This is a summary document. The complete document is available under request. For more information, please contact your local Atmel sales office.

- Supports pattern-based wake-up and start of frame identification
- Flexible service configuration concept with on-the-fly (OTF) modification (in IDLEMode) of SRAM service parameters (data rate, …)
  - Each service consists of
    - One service-specific configuration part
    - Three channel-specific configuration parts
  - Three service configurations are located in EEPROM
  - Two service configurations are located in SRAM and can be modified via SPI or embedded application software
- Digital RSSI with very high relative accuracy of ±1dB thanks to digitized IF processing
- Programmable clock output derived from crystal frequency
- 1024byte EEPROM data memory for receiver configuration
- SPI interface for Rx data access and receiver configuration
- 500Kbit SPI data rate for short periods on SPI bus and host controller
- On demand services (SPI or API) without polling or telegram reception
- Integrated temperature sensor
- Self check and calibration with temperature measurement
- Configurable EVENT signal indicates the status of the IC to an external microcontroller
- Automatic low-power channel polling
- Flexible polling configuration concerning timing, order and participating channels
- Fast reaction time
- Power-up (typical 1.5ms, OFFMode -> RXMode)
- Supports mixed ASK/FSK telegrams
- Non-byte aligned data reception
- Software customization
- Antenna diversity with external switch via GPIO control
- Antenna diversity with internal SPDT switch
- Supply voltage range 1.9V to 3.6V
- Temperature range –40°C to +85°C
- ESD protection at all pins (±4kV HBM, ±200V MM, ±750V FCDM)
- Small 5×5mm QFN32 package/pitch 0.5mm
- Suitable for applications governed by EN 300 220 and FCC part 15, title 47

Typical Applications

- Remote control systems, e.g., garage door openers
- Smart RF applications
- Telemetering systems
- Wireless alarm and security systems
- Home and building automation
- Weather stations

1. General Product Description

1.1 Introduction

The Atmel® ATA8210/15 is a highly integrated, low-power UHF ASK/FSK RF receiver with an integrated AVR® microcontroller.

The Atmel ATA8210/15 is partitioned into three sections; an RF front end, a digital baseband and the low-power 8-bit AVR microcontroller. The product is designed for the ISM frequency bands in the ranges of 310MHz to 318MHz, 418MHz to 477MHz and 836MHz to 956MHz. The external part count is kept to a minimum due to the very high level of integration in this device. By combining outstanding RF performance with highly sophisticated baseband signal processing, robust wireless communication can be easily achieved. The receive path uses a low-IF architecture with an integrated double quadrature receiver and digitized IF processing. This results in high image rejection and excellent blocking performance. In addition, highly flexible and configurable baseband signal processing allows the receiver to operate in several scanning, wake-up and automatic self-polling scenarios. For example, during polling the IC can scan for specific message content (IDs) and save valid telegram data in the FIFO buffer for later retrieval. The device integrates two receive paths that enable a parallel search for two telegrams with different modulations, data rates, wake-up conditions, etc.

The Atmel ATA8210/15 implements a flexible service configuration concept and supports up to 15 channels. The channels are grouped into five service configurations with three channels each. Three service configurations are located in the EEPROM. Two service configurations are located in the SRAM to allow on-the-fly modifications during IDLEMode via SPI commands or application software. The application software is located in the Flash for Atmel ATA8210. Highly configurable and autonomous scanning capability enables flexible polling scenarios with up to 15 channels. The configuration of the receiver is stored in a 1024byte EEPROM. The SPI interface enables external control and device reconfiguration.

Table 1-1. Program Memory Comparison of Atmel ATA8210/15 Devices

Device	Atmel Firmware ROM	User Flash	User ROM
Atmel ATA8210	24Kbyte	20Kbyte	-
Atmel ATA8215	24Kbyte	-	-

In the Atmel ATA8210 the internal microcontroller with 20Kbyte user Flash can be used to add custom extensions to the Atmel firmware. The Atmel ATA8215 embeds only the firmware ROM without user memory.

The debugWIRE and ISP interface are available for programming purposes.

Compatibility to the Atmel ATA8510/15

The Atmel ATA8210/15 is pin-to-pin compatible with the Atmel ATA8510/15 transceivers. The Rx performance of the receivers matches that of the transceivers.

1.2 System Overview

Figure 1-1. Circuit Overview

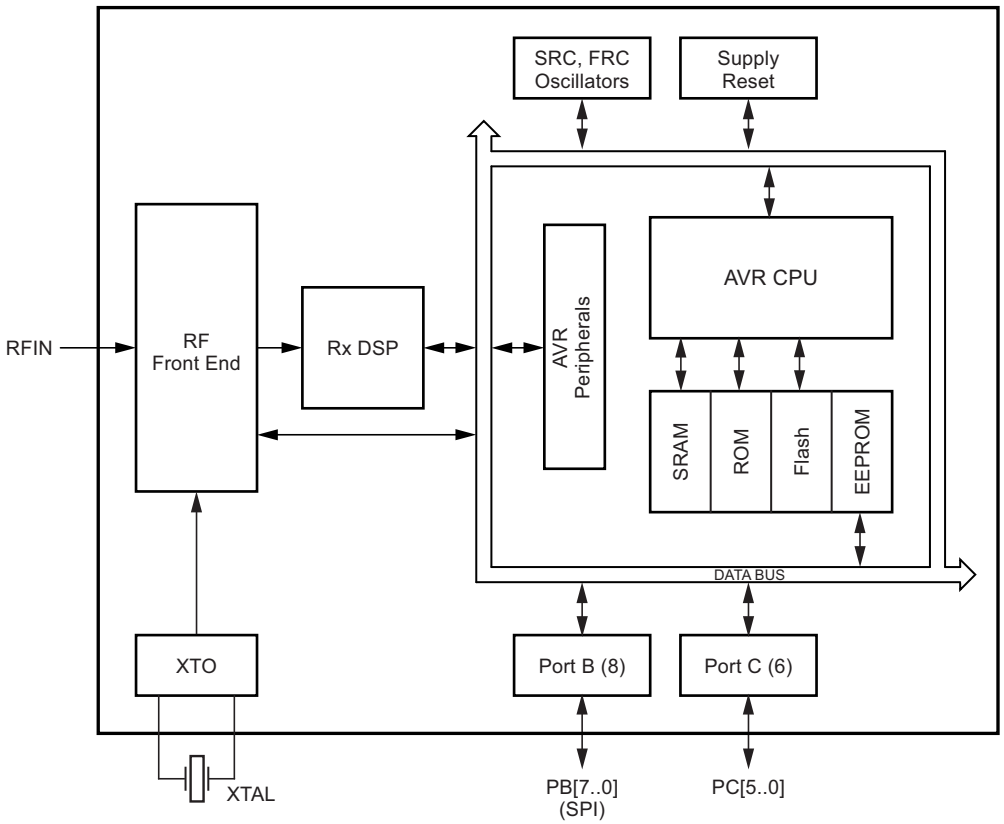


Figure 1-1 shows an overview of the main functional blocks of the Atmel® ATA8210/15. External control of the Atmel ATA8210/15 is performed through the SPI pins SCK, MOSI, MISO, and NSS on port B. The configuration of the Atmel ATA8210/15 is stored in the EEPROM and a large portion of the functionality is defined by the firmware located in the ROM and processed by the AVR®. An SPI command can trigger the AVR to configure the hardware according to settings that are stored in the EEPROM and start up a given system mode (e.g., RXMode, or PollingMode). Internal events such as “Start of Telegram” or “FIFO empty” are signaled to an external microcontroller on pin 28 (PB6/EVENT).

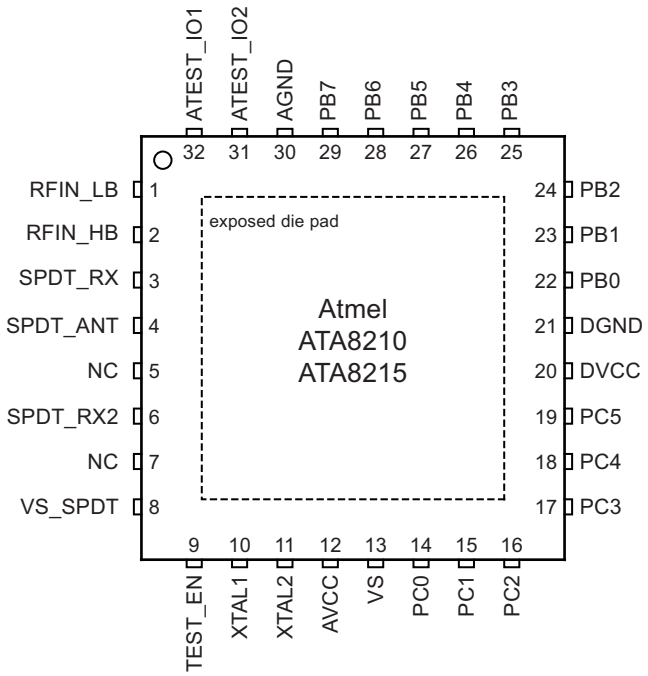
During the start-up of a service, the relevant part of the EEPROM content is copied to the SRAM. This allows faster access by the AVR during the subsequent processing steps and eliminates the need to write to the EEPROM during runtime because parameters can be modified directly in the SRAM. As a consequence the user does not need to observe the EEPROM read/write cycle limitations.

It is important to note that all PWRON and NPWRON pins (PC1..5, PB4, PB7) are active in OFFMode. This means that even if the Atmel ATA8210/15 is in OFFMode and the DVCC voltage is switched off, the power management circuitry within the Atmel ATA8210/15 biases these pins with VS.

AVR ports can be used as button inputs, external LNA supply voltage (RX_ACTIVE), LED drivers, EVENT pin, switching control for additional SPDT switches, general purpose digital inputs, or wake-up inputs, etc. Some functionality of these ports is already implemented in the firmware and can be activated by adequate EEPROM configurations. Other functionality is available only through custom software residing in the 20Kbyte Flash program memory (Atmel ATA8210).

1.3 Pinning

Figure 1-2. Pin Diagram



Note: The exposed die pad is connected to the internal die.

Table 1-2. Pin Description

Pin No.	Pin Name	Type	Description	
1	RFIN_LB	Analog	LNA input for Low-band frequency range (< 500MHz)	
2	RFIN_HB	Analog	LNA input for High-band frequency range (> 500MHz)	
3	SPDT_RX	Analog	Rx switch output (damped signal output)	
4	SPDT_ANT	Analog	Antenna input (RXMode) of the SPDT switch	
5	NC	–	Open in application	
6	SPDT_RX2	Analog	Rx switch output 2	
7	NC	–	Open in application	
8	VS_SPDT	Analog	SPDT supply connect to GND	
9	TEST_EN	–	Test enable, connected to GND in application	
10	XTAL1	Analog	Crystal oscillator pin 1 (input)	
11	XTAL2	Analog	Crystal oscillator pin 2 (output)	
12	AVCC	Analog	RF front end supply regulator output	
13	VS	Analog	Main supply voltage input	
14	PC0	Digital	Main Alternate	: AVR Port C0 : PCINT8 / NRESET / DebugWIRE
15	PC1	Digital	Main Alternate	: AVR Port C1 : NPWRON1 / PCINT9 / EXT_CLK
16	PC2	Digital	Main Alternate	: AVR Port C2 : NPWRON2 / PCINT10 / TRPA

Table 1-2. Pin Description (Continued)

Pin No.	Pin Name	Type	Description	
17	PC3	Digital	Main Alternate	: AVR Port C3 : NPWRON3 / PCINT11 / TMDO
18	PC4	Digital	Main Alternate	: AVR Port C4 : NPWRON4 / PCINT12 / INT0
19	PC5	Digital	Main Alternate	: AVR Port C5 : NPWRON5 / PCINT13 / TRPB / TMDO_CLK
20	DVCC	–	Digital supply voltage regulator output	
21	DGND	–	Digital ground	
22	PB0	Digital	Main Alternate	: AVR Port B0 : PCINT0 / CLK_OUT
23	PB1	Digital	Main Alternate	: AVR Port B1 : PCINT1 / SCK
24	PB2	Digital	Main Alternate	: AVR Port B2 : PCINT2 / MOSI (SPI Master Out Slave In)
25	PB3	Digital	Main Alternate	: AVR Port B3 : PCINT3 / MISO (SPI Master In Slave Out)
26	PB4	Digital	Main Alternate	: AVR Port B4 : PWRON / PCINT4 / LED1 (strong high side driver)
27	PB5	Digital	Main Alternate	: AVR Port B5 : PCINT5 / INT1 / NSS
28	PB6	Digital	Main Alternate	: AVR Port B6 : PCINT6 / EVENT (firmware controlled external microcontroller event flag)
29	PB7	Digital	Main Alternate	: AVR Port B7 : NPWRON6/ PCINT7/ RX_ACTIVE (strong high side driver) / LED0 (strong low side driver)
30	AGND	–	Analog ground	
31	ATEST_IO2	–	RF front end test I/O 2 connected to GND in application	
32	ATEST_IO1	–	RF front end test I/O 1 connected to GND in application	
	GND	–	Ground/backplane on exposed die pad	

1.3.1 Typical 5V Application Circuit with External Microcontroller

Figure 1-3. Typical Application Circuit with External Microcontroller

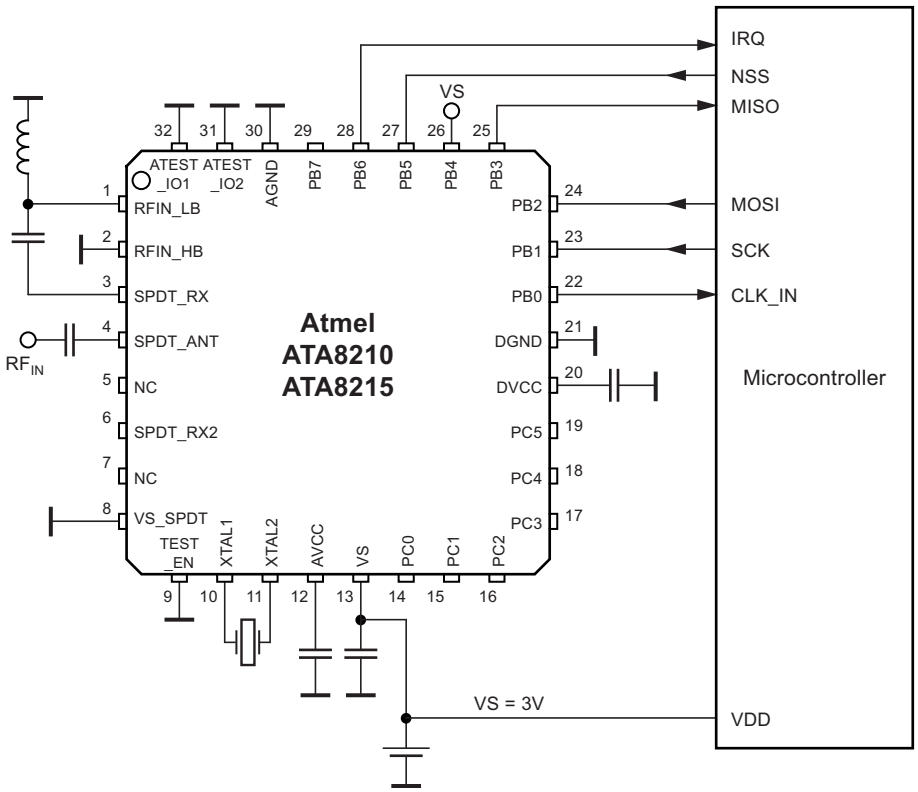


Figure 1-3 shows a typical application circuit with an external host microcontroller running from a 3V voltage regulator. The pin PB4 (PWRON) is directly connected to VS and the Atmel ATA8210/15 enters the IDLEMode after power-on. In this configuration the Atmel ATA8210/15 can work autonomously and the microcontroller stays powered down to keep current consumption low while remaining sensitive to RF telegrams.

To achieve a low current in IDLEMode the Atmel ATA8210/15 can be configured in the EEPROM to work with the RC oscillator. The Atmel ATA8210/15 can also be configured for autonomous multi-channel and multi-application PollingMode. The external microcontroller is notified by an event on pin 28 (EVENT) if an appropriate RF message is received. Until this event, the Atmel ATA8210/15 periodically switches to RXMode, checks the different services and channels configured in the EEPROM, and returns to
power-down while the external host microcontroller is still in deep sleep mode to keep average current low. Once a valid RF message is detected, it can be buffered inside of the Atmel ATA8210/15 to enable a microcontroller wake-up and retrieval of buffered data.

RF_IN is matched to SPDT_RX by absorbing the parasitics of the SPDT switch into the matching network, hence the SPDT_ANT is a 50Ω RX port.

An external crystal, together with the fractional-N PLL within the Atmel® ATA8210/15 is used to fix the RX frequency. Accurate load capacitors for this crystal are integrated, to reduce system part count and cost. Only three supply blocking capacitors are needed to decouple the different supply voltages AVCC, DVCC and VS of the Atmel ATA8210/15. The exposed die pad is the RF and analog ground of the Atmel ATA8210/15. It is directly connected to AGND via a fused lead. For applications operating in the 868.3MHz or 915MHz frequency bands, a High-band RF input is supplied, RFIN_HB, and must be used instead of RFIN_LB. The Atmel ATA8210/15 is controlled using specific SPI commands via the SPI interface and an internal EEPROM for application specific configuration. This application is compatible to the Atmel ATA8510/15, therefore, the same application board can be used for both devices, just the population of the TX path is not required for the Atmel ATA8210/15.

2. System Functional Description

2.1 Overview

2.1.1 Service-based Concept

The Atmel® ATA8210/15 is a highly configurable UHF receiver. The configuration is stored in an internal 1024-byte EEPROM. The master system control is performed by firmware. General chip-wide settings are loaded from the EEPROM to hardware registers during system initialization. During start-up of a receive mode the specific settings are loaded from the EEPROM or SRAM to the current service in the SRAM and from there to the corresponding hardware registers.

A complete configuration set of the receiver is called “service” and includes RF settings, demodulation settings, and telegram handling information. Each service contains three channels which differ in the RF receive frequencies.

The Atmel ATA8210/15 supports five services which can be configured in various ways to meet customer requirements. Three service configurations are located in the EEPROM space. They are fixed configurations which should not be changed during runtime.

Two service configurations are located in the SRAM space and can be modified by USER SW in a Flash application or by an SPI command during IDLEMode.

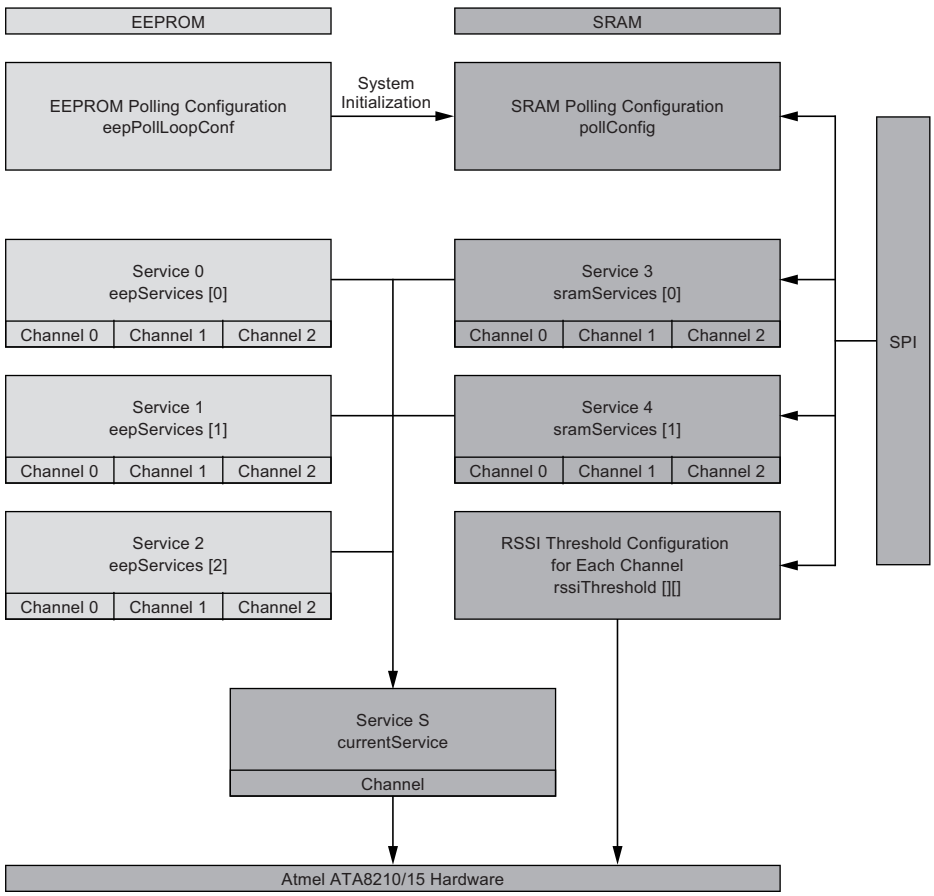
A service consists of

- One service-specific configuration part
- Three channel-specific configuration parts

Further configurations for PollingMode and RSSI are available and can be modified in IDLEMode via an SPI command and/or User SW.

Figure 2-1 gives an overview on the service based-concept.

Figure 2-1. Service-based Concept Overview



2.1.2 Supported Telegrams

2.1.2.1 Telegram Structure

The Atmel® ATA8210/15 supports the reception of a wide variety of telegrams and protocols. Generally no special structure is required from a telegram to be received by the Atmel ATA8210/15. However, designated hardware and software features are built in for the blocks that are depicted in Figure 2-2. Using this structure or parts of it can increase the sensitivity and robustness of the broadcast.

Figure 2-2. Telegram Structure

Desync:

The de-synchronization is usually a coding violation with a length of several symbols that should provoke a defined restart of the receiver. The use of a de-synchronization leads to more deterministic receiver behavior, reducing the required preamble length. This can be favorable in timing-critical and energy-critical applications.

Preamble:

The preamble is a pattern that is sent before the actual data payload to synchronize the receiver and provide the starting point of the payload. A very regular pattern (e.g., 1-0-1-0...) is recommended for synchronization (“wake-up pattern, WUP”, sometimes also called “pre-burst”) while a unique, well-defined pattern of up to 32 symbols is required to mark the start of the data payload (“start frame identifier, SFID” or “start bit”). In polling scenarios the WUP can be tens or hundreds of ms long.

Data Payload:

The data payload contains the actual information content of the telegram. It can be NRZ or Manchester-coded. The length of the payload is application dependent, typically 1..64 bytes.

Checksum:

A checksum can be calculated across the data payload to verify that the data have been received correctly. A typical example is an 8-bit CRC checksum. Data bits at the beginning of the payload can be excluded from the CRC calculation.

Stop Sequence:

The stop sequence is a short data pattern (typically 2 to 6 symbols) to mark the end of the telegram. A coding violation can be used to prevent additional (non-deterministic) data from being received.

2.1.2.2 NRZ and Manchester Coding

Within this document the following wording is used:

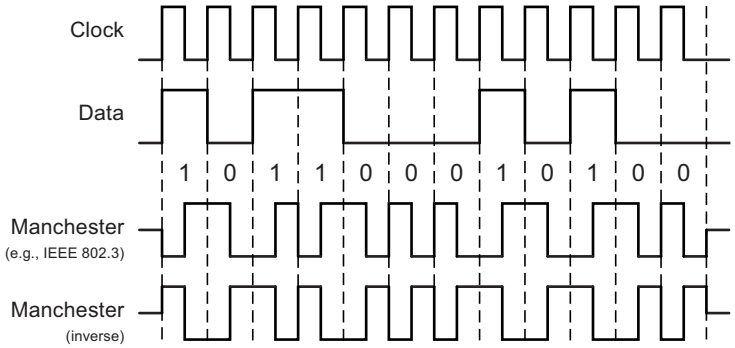
The expression data “bit” describes the real information content that is to be broadcast. This information can be coded in “symbols” (sometimes also called “chips”) which are then physically transmitted from sender to receiver. The receiver has to decode the “symbols” back into data “bits” to access the information. The “symbol rate” is therefore always greater or equal to the “bit rate”.

The Atmel ATA8210/15 supports two coding modes: Manchester coding and non-return-to-zero (NRZ) coding.

NRZ coding is implemented in a straightforward manner: One bit is represented by one symbol.

Manchester coding implements two symbols per data bit. There is always a transition between the two symbols of one data bit so that one data bit always consists of a “0” and a “1”. The polarity can be either way as shown in Figure 2-3 on page 10.

Figure 2-3. Manchester Code

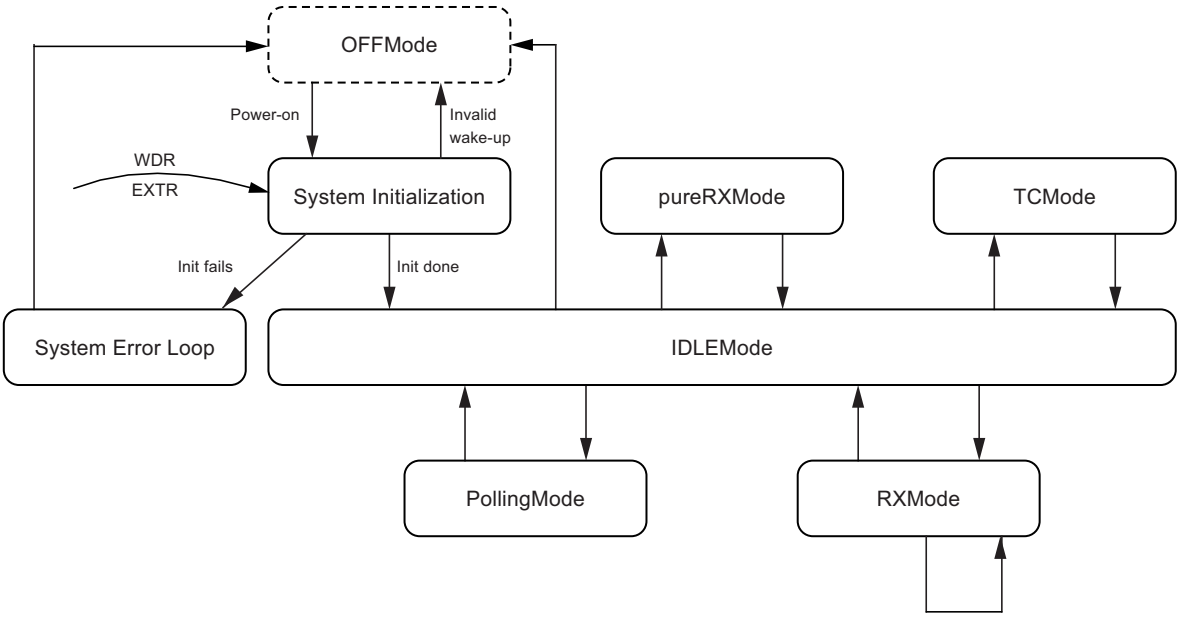


Manchester coding has many advantages such as simple clock recovery, no DC component, and error detection by code violation. Drawbacks are the coding/decoding effort and the increased symbol rate which is twice the data rate.

2.2 Operating Modes Overview

This section gives an overview of the operating modes supported by the Atmel® ATA8210/15 as shown in Figure 2-4.

Figure 2-4. Operating Modes Overview



After connecting the supply voltage to the VS pin, the Atmel ATA8210/15 always starts in OFFMode. All internal circuits are disconnected from the power supply. Therefore, no SPI communication is supported. The Atmel ATA8210/15 can be woken up by activating the PWRON pin or one of the NPWRONx pins. This triggers the power-on sequence. After the system initialization the Atmel ATA8210/15 reaches the IDLEMode.

The IDLEMode is the basic system mode supporting SPI communication and transitions to all other operating modes. There are two options of the IDLEMode requiring configuration in the EEPROM settings:

- IDLEMode(RC) with low power consumption using the fast RC (FRC) oscillator for processing
- IDLEMode(XTO) with active crystal oscillator for high accuracy clock output or timing measurements

The receive mode (RXMode) provides data reception on the selected service/channel configuration. The precondition for data reception is a valid preamble. The receiver continuously scans for a valid telegram and receives the data if all pre-configured checks are successful. The RXMode is usually enabled by the SPI command “Set System Mode”, or directly after power-on, when selected in the EEPROM setting.

The pure receive mode (pureRXMode) is a unique receive mode only available as transparent mode. There is no precondition for data reception necessary. It must be enabled in the EEPROM settings and is activated by a special use of pin 18.

In PollingMode the receiver is activated for a short period of time to check for a valid telegram on the selected service/channel configurations. The receiver is deactivated if no valid telegram is found and a sleep period with very low power consumption elapses. This process is repeated periodically in accordance with the polling configuration. The initial settings are stored in the EEPROM and copied during firmware initialization to the SRAM. This allows modification of the PollingMode timing and service/channel configuration during IDLEMode.

The tune and check mode (TCMode) offers calibration and self-checking functionality for the VCO and FRC oscillators as well as for temperature measurement, and polling cycle accuracy. This mode is activated via the SPI command “Calibrate and Check”. When selected in the EEPROM settings, tune and check tasks are also used during system initialization after power-on. Furthermore, they can also be activated periodically during PollingMode.

Table 2-1 shows the relations between the operating modes and their corresponding power supplies, clock sources, and sleep mode settings.

Table 2-1. Operating Modes versus Power Supplies and Oscillators

Operation Mode	AVR Sleep Mode	DVCC	AVCC	XTO	SRC	FRC
OFFMode	-	off	off	off	off	off
IDLEMode(RC)	Active mode Power-down(1)	on	off off	off off	on on	on off
IDLEMode(XTO)	Active mode Power-down(1)		on on	on on	on on	off off
RXMode	Active mode		on	on	on	off
PollingMode(RC) - Active period - Sleep period	 Active mode Power-down(1)		 on off	 on off	 on on	 on off
PollingMode(XTO) - Active period - Sleep period	 Active mode Power-down(1)		 on on	 on on	 on on	 off off

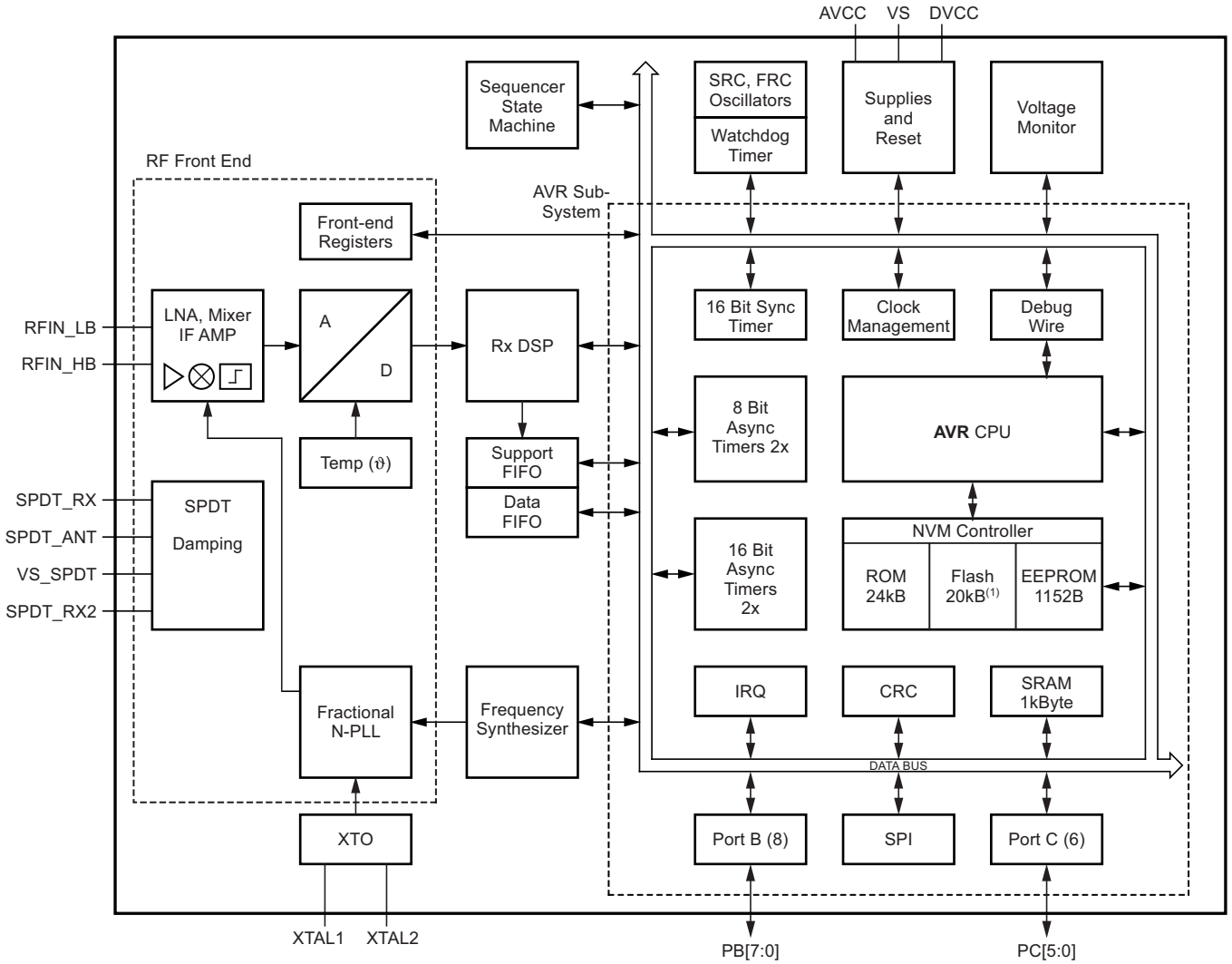
Notes: 1. During IDLEMode(RC) and IDLEMode(XTO) the AVR® microcontroller enters sleep mode to reduce current consumption. The sleep mode of the microcontroller section can be defined in the EEPROM. The power-down mode is recommended for keeping current consumption low.

3. Hardware

3.1 Overview

The Atmel® ATA8210/15 consists of an analog front end, digital signal processing blocks (DSP), an 8-bit AVR® sub-system and various supply modules such as oscillators and power regulators. A hardware block diagram of the Atmel ATA8210/15 is shown in Figure 3-1.

Figure 3-1. Block Diagram



(1) 20kByte Flash for Atmel ATA8210, no user memory for Atmel ATA8215

Together with the fractional-N PLL, the crystal oscillator (XTO) generates the local oscillator (LO) signal for the mixer in RXMode. The RF signal comes either from the Low-band input (RFIN_LB) or from the High-band input (RFIN_HB) and is amplified by the low-noise amplifier (LNA) and down-converted by the mixer to the intermediate frequency (IF) using the LO signal. A 10dB IF amplifier with low-pass filter characteristic is used to achieve enhanced system sensitivity without affecting blocking performance.

After the mixer, the IF signal is sampled using a high-resolution analog-to-digital converter (ADC).

Within the Rx digital signal processing (Rx DSP) the received signal from the ADC is filtered by a digital channel filter and demodulated. Two data receive paths, path A and path B, are included in the Rx DSP after the digital channel filter. In addition, the receive path can be configured to provide the digital output of the internal temperature sensor (Temp(ϑ)).

With the single pole double throw (SPDT) switch the RF signal from the antenna is switched to RFIN in RXMode.

The system is controlled by an AVR® CPU with 24KB firmware ROM and 20KB user Flash for the Atmel® ATA8210. 1024-byte EEPROM, 1024-byte SRAM, and other peripherals are supporting the receiver handling. Two GPIO ports, PB[7:0] and PC[5:0], are available for external digital connections, for example, as an alternate function the SPI interface is connected to port B. The Atmel ATA8210/15 is controlled by the EEPROM configuration and SPI commands and the functional behavior is mainly determined by firmware in the ROM. Much of the configuration can be modified by the EEPROM settings. The firmware running on the AVR gives access to the hardware functionality of the Atmel ATA8210/15. Extensions to this firmware can be added in the 20KB of Flash memory for the Atmel ATA8210. The Rx DSP registers are addressed directly and accessible from the AVR. A set of sequencer state machines is included to perform Rx path operations (such as enable, disable, receive) which require a defined timing parallel to the AVR program execution.

The power management contains low-dropout (LDO) regulators and reset circuits for the supply voltages VS, AVCC, and DVCC of the Atmel ATA8210/15. In OFFMode all the supply voltages AVCC and DVCC are switched off to achieve very low current consumption. The Atmel ATA8210/15 can be powered up by activating the PWRON pin or one of the NPWRON[6:1] pins because they are still active in OFFMode. The AVCC domain can be switched on and off independently from DVCC. The Atmel ATA8210/15 includes two idle modes. In IDLEMode(RC) only the DVCC voltage regulator, the FRC and SRC oscillators are active and the AVR uses a power-down mode to achieve low current consumption. The same power-down mode can be used during the inactive phases of the PollingMode. In IDLEMode(XTO) the AVCC voltage domain as well as the XTO are additionally activated.

An integrated watchdog timer is available to restart the Atmel ATA8210/15 when it is not served within the configured time-out period.

3.2 Receive Path

3.2.1 Overview

The receive path consists of a low-noise amplifier (LNA), mixer, IF amplifier, analog-to-digital converter (ADC), and an Rx digital signal processor (Rx DSP). The fractional-N PLL and the XTO deliver the local oscillator frequency in RXMode. The receive path is controlled by the RF front-end registers.

Two separate LNA inputs, one for Low-band and one for High-band, are provided to obtain optimum performance matching for each frequency range and to allow multi-band applications. A radio frequency (RF) level detector at the LNA output and a switchable damping included into the single-pole double-trough (SPDT) switch is used in the presence of large blockers to achieve enhanced system blocking performance.

The mixer converts the received RF signal to a low intermediate frequency (IF) of about 250kHz. A double-quadrature architecture is used for the mixer to achieve high image rejection. Additionally, the third-order suppression of the local oscillator (LO) harmonics makes receiving without a front-end SAW filter less critical, such as in a car key fob application.

An IF amplifier provides additional gain and improves the receiver sensitivity by 2-3dB. Because of built-in filter function, the in-band compression is degraded by 10dB, while the out-of-band compression remains unchanged.

The ADC converts the IF signal into the digital domain. Due to the high effective resolution of the ADC, the channel filter and received signal strength indicator (RSSI) can be realized in the digital signal domain. Therefore, no analog gain control (AGC) potentially leading to critical timing issues or analog filtering is required in front of the ADC. This leads to a receiver front end with excellent blocking performance up to the 1dB compression point of the LNA and mixer, and a steep digital channel filter can be used.

The Rx DSP performs the channel filtering and converts the digital output signal of the ADC to the baseband for demodulation. Due to the digital realization of these functions the Rx DSP can be adapted to the needs of many different applications. Channel bandwidth, data rate, modulation type, wake-up criteria, signal checks, clock recovery, and many other properties are configurable. The RSSI value is realized completely in the digital signal domain, enabling very high relative and absolute accuracy that is only deteriorated by the gain errors of the LNA, mixer, and ADC.

Two independent receive paths A and B are integrated in the Rx DSP after the channel filter and allow the use of different data rates, modulation types, and protocols without the need to power up the receive path more than once to decide which signal should be received. This results in a reduced polling current in several applications.

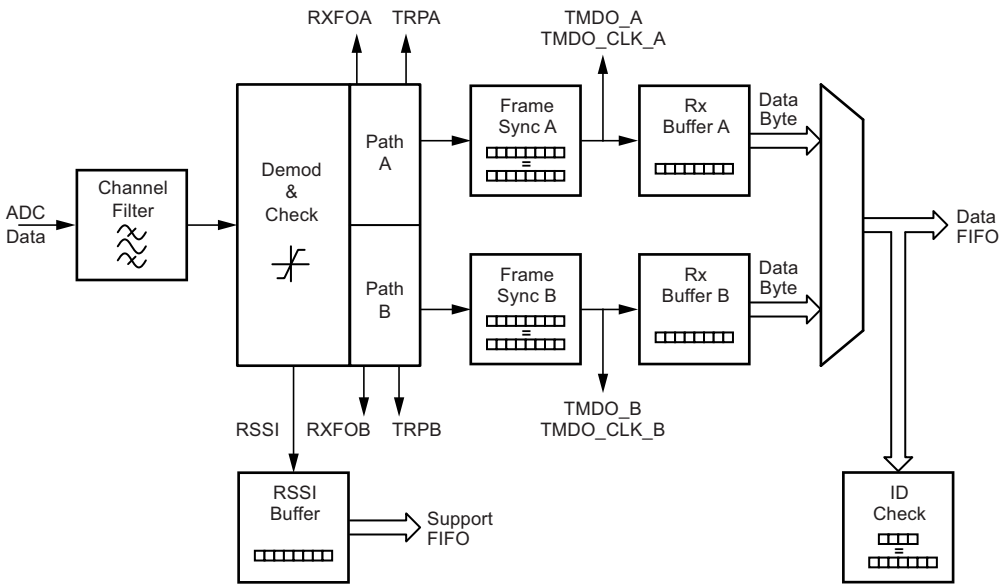
The integration of remote keyless entry (RKE), passive entry and go (PEG) and tire-pressure monitoring systems (TPM) into one module is simplified because completely different protocols can be supported and a low polling current is achieved. It is even possible to configure different receive RF bands for different applications by using the two LNA inputs. For example, a TPM receiver can be realized at 433.92MHz while a PEG system uses the 868MHz ISM band with multi-channel communication.

3.2.2 Rx Digital Signal Processing (Rx DSP)

The Rx digital signal processing (DSP) block performs the digital filtering, decoding, checking, and byte-wise buffering of the Rx samples that are derived from the ADC as shown in Figure 3-2. The Rx DSP provides the following outputs:

- Raw demodulated data at the TRPA/B pins
- Decoded data at the TMDO and TMDO_CLK pins
- Buffered data bytes toward the data FIFO and ID check block
- Auxiliary information about the signal such as the received signal strength indication (RSSI) and the frequency offset of the received signal from the selected center frequency (RXFOA/B)

Figure 3-2. Rx DSP Overview



The channel filter determines the receiver bandwidth. Its output is used for both receiving paths A and B, making it necessary to configure the filter to match both paths. The receiving paths A and B are identical and consist of an ASK/FSK demodulator with attached signal checks, a frame synchronizer which supports pattern-based searches for the telegram start and a 1-byte hardware buffer with integrated CRC checker for the received data.

Depending on the signal checks, one path is selected which writes the received data to the data FIFO and optionally to the ID check block.

The RSSI values are determined by the demodulator and written via the RSSI buffer to the support FIFO where the latest 16 values are stored for further processing.

3.3 AVR Controller

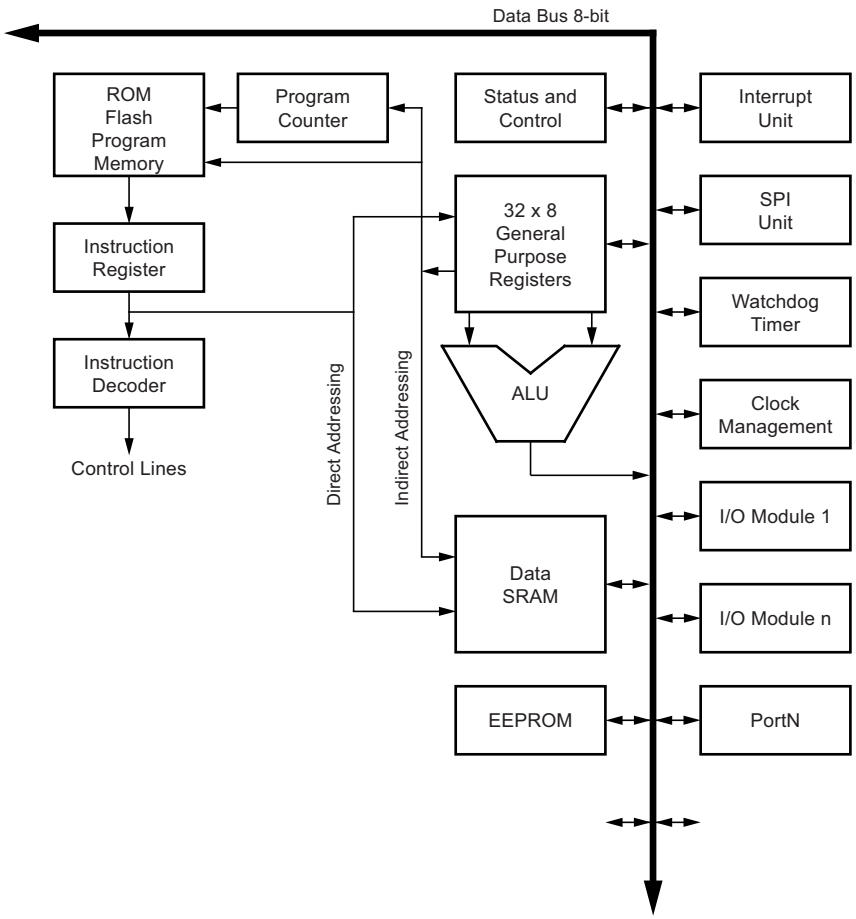
3.3.1 AVR Controller Sub-System

The AVR® controller sub-system consists of the AVR CPU core, its program memory, and a data bus with data memory and peripheral blocks attached. The receive path also has its user interfaces connected to the data bus.

3.3.2 CPU Core

The main function of the CPU core is to ensure correct program execution. For this reason, the CPU core must be able to access memories, perform calculations, control peripherals, and handle interrupts.

Figure 3-3. Overview of Architecture



In order to maximize performance and parallelism, the AVR uses a Harvard architecture—with separate memories and buses for program and data. Instructions in the program memory are executed with single-level pipelining. While one instruction is being executed, the next instruction is prefetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system reprogrammable Flash memory and ROM.

The fast-access register file contains 32 × 8-bit general purpose working registers with a single clock cycle access time. This allows a single-cycle arithmetic and logic unit (ALU) operation. In a typical ALU operation, two operands are output from the register file, the operation is executed, and the result is stored back in the register file—in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for data space addressing, enabling efficient address calculations. One of these address pointers can also be used as an address pointer for lookup tables in the Flash program memory. Referred to as ‘X,’ ‘Y,’ and ‘Z’ registers, these higher 16-bit function registers are described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The program flow is provided by conditional and unconditional jump and call instructions which are able to directly address the entire address space. Most AVR® instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

The program memory space is divided in two sections, the boot program section and the application program section. Both sections have dedicated lock bits for write and read/write protection. The store program memory (SPM) instruction that writes into the application Flash memory section must reside in the boot program section.

During interrupts and subroutine calls, the return address of the program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM—the stack size is thus only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the stack pointer (SP) in the reset routine before subroutines or interrupts are executed. The SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All interrupts have a separate interrupt vector in the interrupt vector table. The interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as control registers, SPI, and other I/O functions. The I/O memory can be accessed directly, or as the data space locations following those of the register file, 0x20 - 0x5F. In addition, the circuit has extended I/O space from 0x60 - 0x1FF and SRAM where only the ST/STS/STD and LD/LDS/LDD instructions can be used.

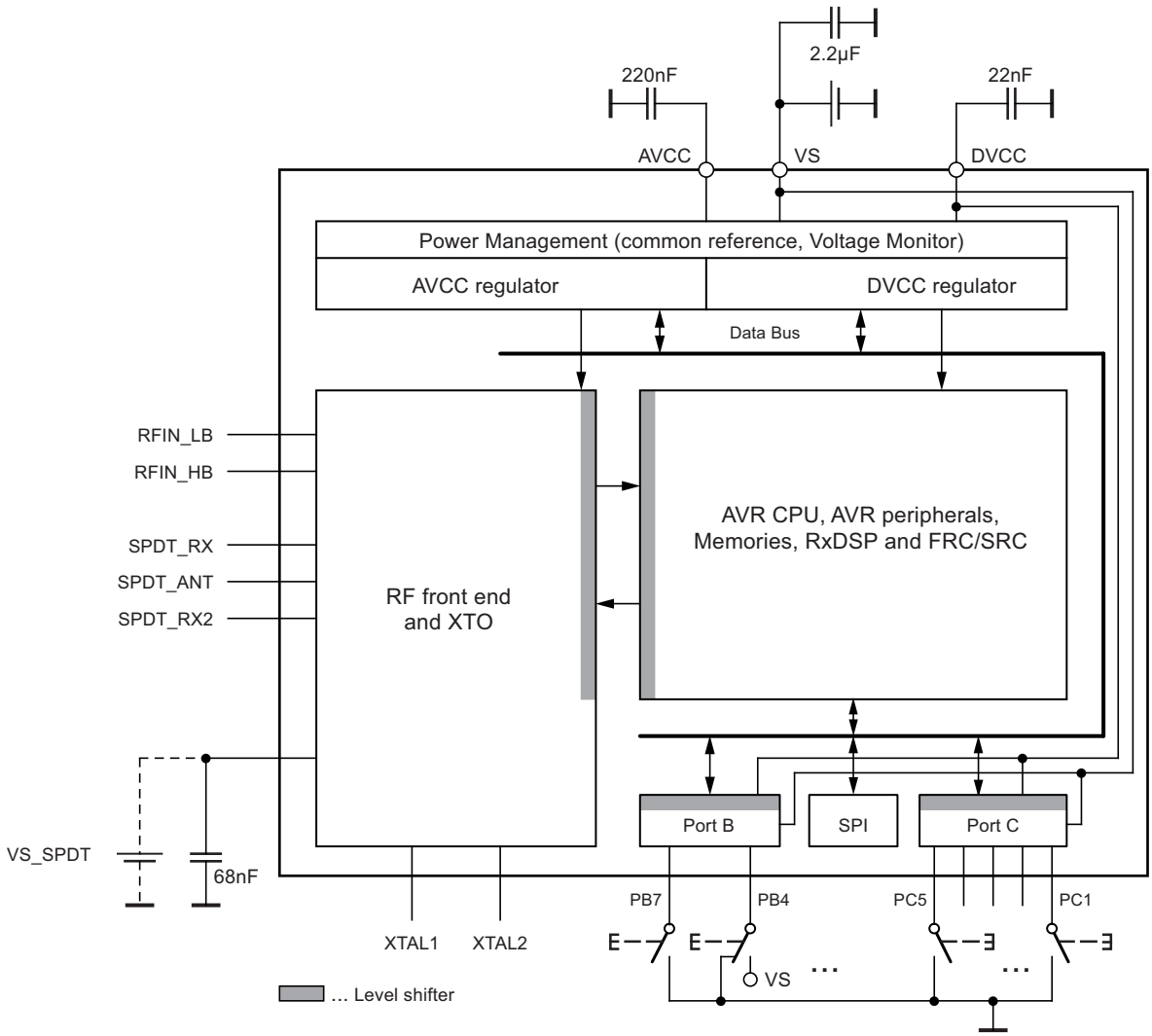
3.4 Power Management

The IC has four power domains:

1. VS – Unregulated battery voltage input
2. DVCC – Internally regulated digital supply voltage. Typical value is 1.35V.
3. AVCC – Internally regulated RF front end and XTO supply. Typical value is 1.85V.
4. VS_SPDT – This is used to achieve full PCB and RF application compatibility with Atmel® ATA8510/15, in Atmel ATA8210/15 this supply is always switched off and connected externally to the battery in 3V applications:

The Atmel ATA8210/15 can be operated from V_S= 1.9V to 3.6V.

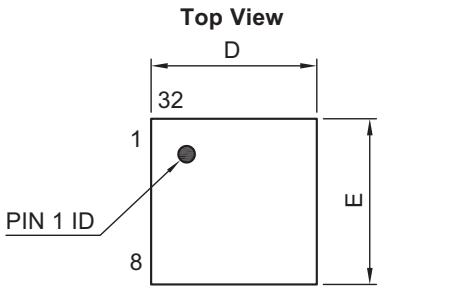
Figure 3-4. Power Supply Management

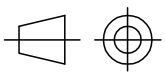


4. Ordering Information

Extended Type Number	Package	Remarks
ATA8210-WNQW	QFN32	5mm x 5mm, 6k tape and reel, PB-free, wettable flanks, with user flash
ATA8215-WNQW	QFN32	5mm x 5mm, 6k tape and reel, PB-free, wettable flanks

5. Package Information

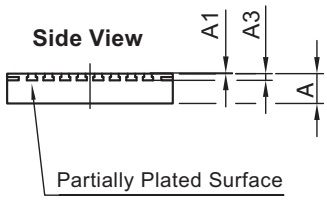


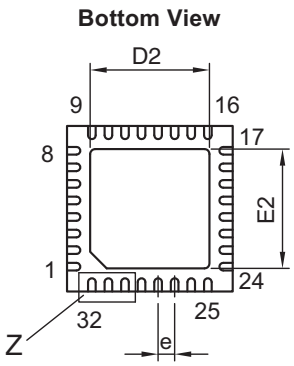


technical drawings
according to DIN
specifications

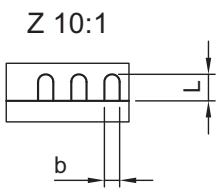
Dimensions in mm

Two Step Singulation process





COMMON DIMENSIONS (Unit of Measure = mm)				
SYMBOL	MIN	NOM	MAX	NOTE
A	0.8	0.85	0.9	
A1	0	0.035	0.05	
A3	0.16	0.21	0.26	
D	4.9	5	5.1	
D2	3.5	3.6	3.7	
E	4.9	5	5.1	
E2	3.5	3.6	3.7	
L	0.35	0.4	0.45	
b	0.2	0.25	0.3	
e		0.5		



10/18/13

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	Package: VQFN_5x5_32L Exposed pad 3.6x3.6		6.543-5124.03-4	1

6. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9344CS-INDCO-09/14	• Section 1.1 “Introduction” on page 3 updated
9344BS-INDCO-07/14	• Features on page 2 updated • Section 2.2 “Operating Modes Overview” on page 11 updated • Section 3.1 “Overview” on page 12 updated

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