RNA52A10T

Dual CMOS system–RESET IC

R03DS0078EJ0200
Rev.2.00
Dec 19, 2015

Description

The RNA52A10T incorporates two reset circuits, one with and one without a delay function, allowing the generation of separate reset signals for a microprocessor and associated system circuits. The detection voltage of each reset circuit is determined by the value of an external resistor, and the internal reference voltage is 1.0 V. The CMOS process for the RNA52A10T means that the device draws only 1.1 µA (typ.). The reset cancellation delay time is set with a high degree of accuracy by the values of a capacitor and resistor connected with the CD pin. The MR (manual reset) input pin is provided for the reset circuit with the delay function, and the reset signal is output in response to a high level on the MR input pin. The MR pin is pulled down by a 2-MΩ internal resistor. Output pins Vo1 and Vo2 are open drain.

Features

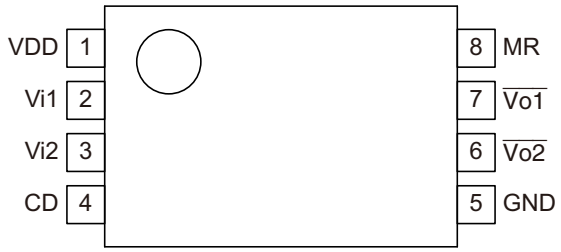
- Two CMOS reset circuits, one with and one without the delay function
- Reference voltage: 1.0 V
- Reference voltage accuracy: ± 50 mV
- Reference voltage hysteresis: 6% (typ.)
- Low current consumption: 1.1 µA (typ.)
- Delay time set by an external CR circuit
- Manual reset input
- Open-drain output
- TSSOP-8 (8-pin) package
- Operating temperature range: – 40 to 85°C
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)	Surface Treatment
RNA52A10TH5	TSSOP-8 pin	PTSP0008JC-B	T	H (3,000 pcs / Reel)	5 (Ni/Pd/Au)

Application

- Power-supply monitoring and resetting for microprocessors
- Power supply sequence control for microprocessors
- Desktop and laptop PCs
- PC peripheral devices such as printers
- Digital still cameras, digital video cameras, and PDAs
- Battery-driven products
- Wireless communications systems

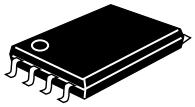
Pin Arrangement



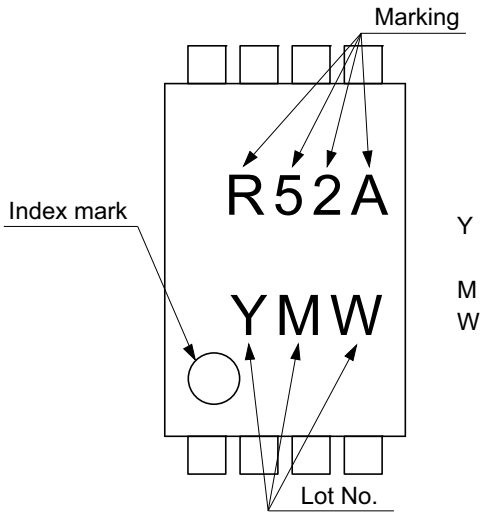
(Top view)

Outline and Article Indication

• RNA52A10T

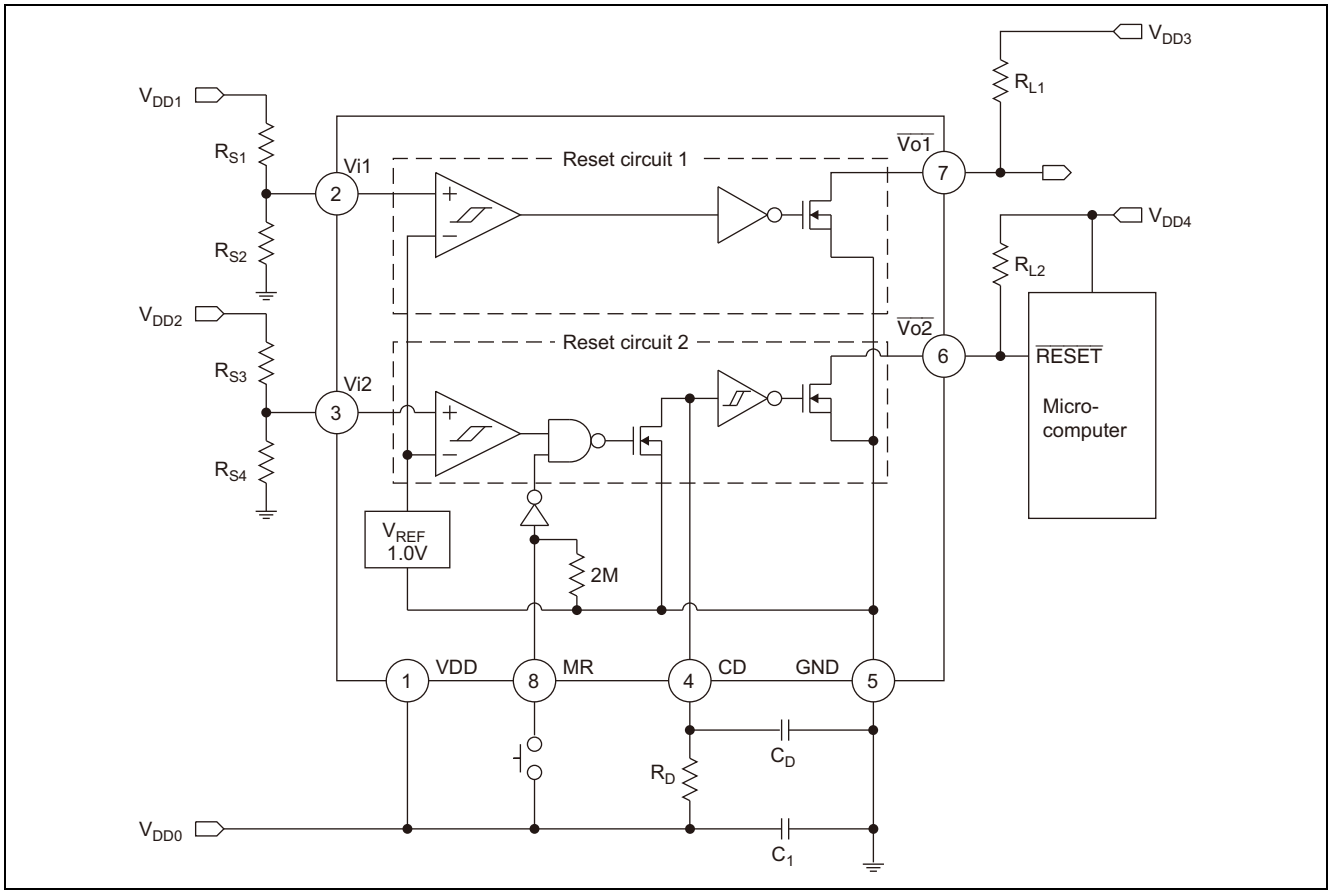


TSSOP-8



Y : Year code
(the last digit of year)
M : Month code
W : Week code

Functional Block Diagram and Typical application Circuit



Notes: 1. Please refer to the following equations to set up reset-threshold voltages for power supplies V_{DD1} and V_{DD2}, and to set up external voltage-dividing resistor pairs R_{S1} and R_{S2}, and R_{S3} and R_{S4}.

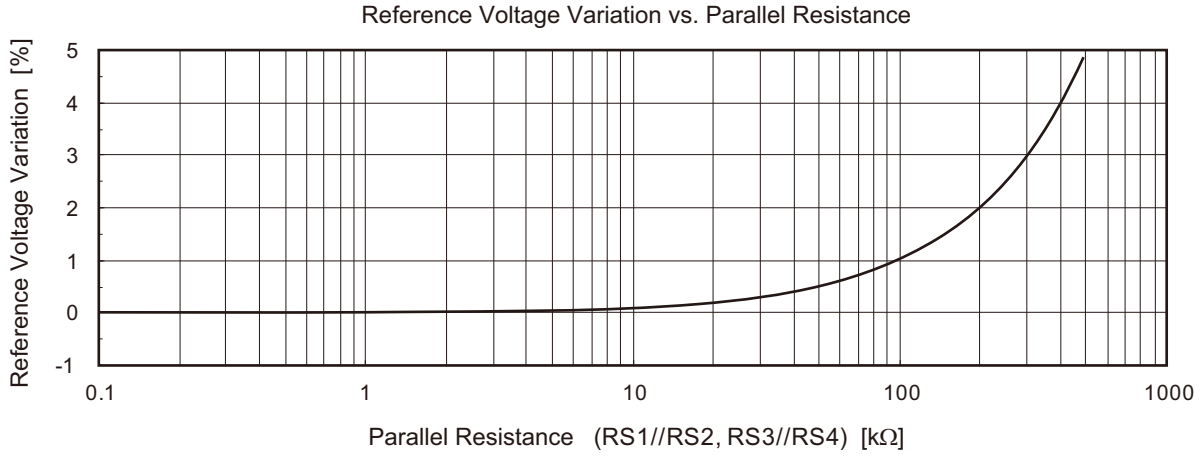
(1) V_{DD1} reset-threshold voltage = $V_{REF} \times (R_{S1}+R_{S2})/R_{S2}$

(2) V_{DD2} reset-threshold voltage = $V_{REF} \times (R_{S3}+R_{S4})/R_{S4}$

Note that values must be set up within the following range: R_{S1}, R_{S2}, R_{S3}, $R_{S4} \leq 50\ k\Omega$

See the following graph for the relationship between the reference voltage variation and the value selected for R_{S1}, R_{S2}, R_{S3} and R_{S4}.

2. For capacitor C1, select a type which has excellent frequency characteristics. For stable operation, place it between the VDD pin and the GND pin and as close as is possible to the chip.
3. The value of capacitor C_1 must suit the system environment in terms of the quality of the power supply and so forth.

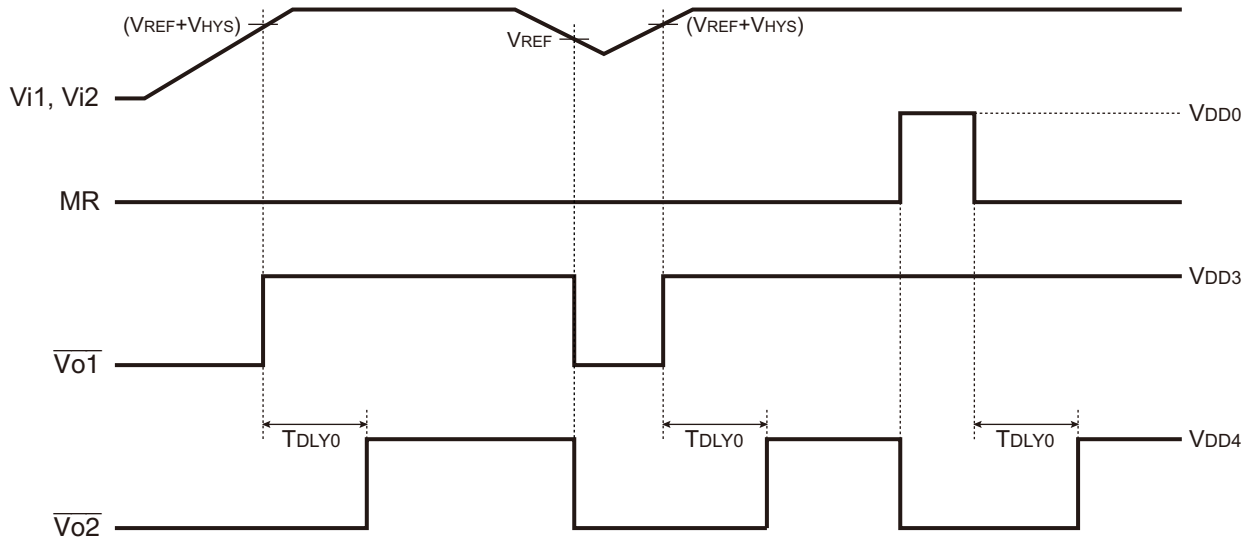


Timing Diagram

1. I/O Table

MR	Vi1, Vi2	$\overline{Vo1}$	$\overline{Vo2}$
L	≤ V_{REF}	L	L
	≥ (V_{REF}+V_{HYS})	H	H (after T_{DLY0})
H	≤ V_{REF}	L	L
	≥ (V_{REF}+V_{HYS})	H	

2. Timing Chart



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage (VDD)	V_{DD}	6.0	V
Input voltage (Vi1, Vi2, MR, CD)	V_{IN}	–0.3 to V_{DD}	V
Output voltage ($\overline{Vo1}$, $\overline{Vo2}$)	V_{OUT}	–0.3 to 6.0	V
Output current ($\overline{Vo1}$, $\overline{Vo2}$)	I_{OUT}	30	mA
Continuous power dissipation	P_T	192	mW
Operating temperature	T_{OPR}	–40 to 85	°C
Storage temperature	T_{STG}	–55 to 125	°C

Note: Ta ≤ 25°C, If Ta > 25°C, derate by 1.92 mW/°C (see figure on page 6)

Recommended Operating Conditions

Item	Symbol	Min.	Max.	Unit
Supply voltage (VDD)	V_{DD}	1.4	5.5	V
Input voltage (Vi1, Vi2, MR, CD)	V_{IN}	0	V_{DD}	V
Output voltage ($\overline{Vo1}$, $\overline{Vo2}$)	V_{OUT}	0	5.5	V
Output current ($\overline{Vo1}$, $\overline{Vo2}$)	I_{OUT}	0	15	mA
Operating temperature	T_{OPR}	–40	85	°C

Electrical Characteristics

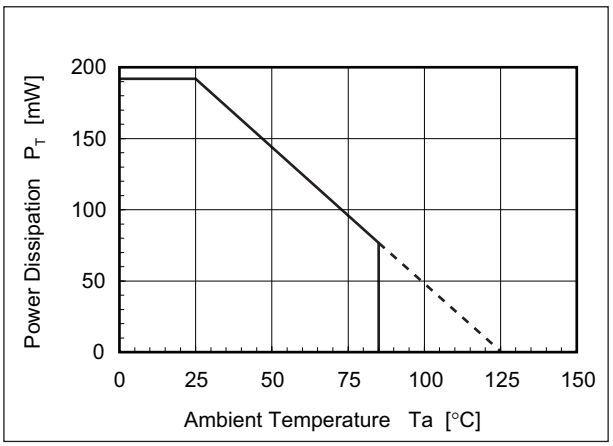
(Ta = 25°C, unless otherwise noted)

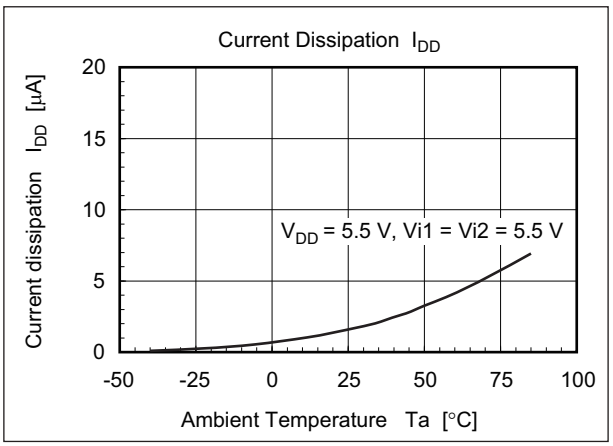
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Test Circuit
Supply voltage		V_{DD}	1.4	—	5.5	V		—
Current consumption		I_{DD}	—	1.1	19	µA	V_{DD} = 5.5 V V_{i1} = V_{i2} = 5.5 V	1
Reference voltage		V_{REF}	0.95	1.00	1.05	V	V_{DD} = 3.3 V	2
Reference voltage temperature coefficient (Reference value for design)		$\frac{\Delta V_{REF}}{V_{REF} \cdot \Delta T_a}$	—	±100	—	$\frac{ppm}{°C}$	T_a = –40 to 85°C	2
Vi1, Vi2 input hysteresis voltage		V_{HYS}	28.5 (V_{REF}×3%)	60 (V_{REF}×6%)	94.5 (V_{REF}×9%)	mV	V_{DD} = 3.3 V	2
Vi1, Vi2 input current		I_{IN}	—	0.6	2.2	µA	V_{DD} = 5.5 V V_{i1} = V_{i2} = 5.5 V	3
CD input threshold voltage		V_{DLY}	V_{DD}×0.43	V_{DD}×0.63	V_{DD}×0.83	V	V_{DD} = 3.3 V V_{i1} = V_{i2} = 1.2 V	4
$\overline{Vo1}$, $\overline{Vo2}$ low-level output voltage		V_{OL}	—	0.05	0.15	V	V_{DD} = 1.4V V_{i1} = V_{i2} = 0 V I_{OL} = 0.5 mA	5
			—	0.15	0.35	V	V_{DD} = 3.3V V_{i1} = V_{i2} = 0 V I_{OL} = 5 mA	6
$\overline{Vo1}$, $\overline{Vo2}$ output leakage current		I_{LK}	—	—	100	nA	V_{DD} = V_{O1} = V_{O2} = 5.5 V V_{i1} = V_{i2} = 1.2 V	7
$\overline{Vo2}$ Delay time [Note1]	Incomplete discharge of capacity CD	T_{DLY}	1.1	11	17	ms	V_{DD} = 3.3 V V_{i2} = 0 V→1.2 V C_D = 0.3 µF, R_D = 39 kΩ	8
	complete discharge of capacity CD	T_{DLY0}	7	11	17	ms		8
$\overline{Vo1}$ Rise response time		T_{PLH}	—	30	300	µs	V_{DD} = 3.3 V V_{i1} = 0 V→1.2 V	9
$\overline{Vo1}$, $\overline{Vo2}$ fall response time		T_{PHL}	—	30	800	µs	V_{DD} = 3.3 V V_{i1} = V_{i2} = 1.2 V→0 V C_D = 0.3 µF, R_D = 39 kΩ	10
MR low-level input voltage		V_{IL}	—	—	V_{DD}×0.2	V	V_{DD} = 3.3 V V_{i1} = V_{i2} = 1.2 V	11
MR high-level input voltage	V_{DD} < 4.5V	V_{IH}	V_{DD}×0.75	—	—	V	V_{DD} = 3.3 V V_{i1} = V_{i2} = 1.2 V	11
	V_{DD} ≥ 4.5V		V_{DD}×0.5	—	—	V	V_{DD} = 5.0 V V_{i1} = V_{i2} = 1.2 V	12
MR input pull-down resistance		R_{MR}	0.5	2	—	MΩ	V_{DD} = 5.5 V V_{MR} = 5.5 V	13

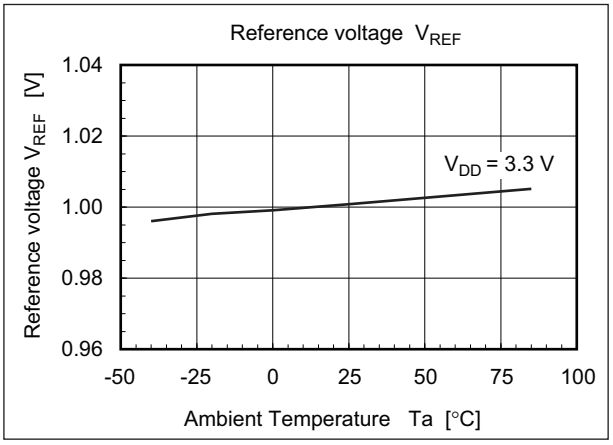
Notes: 1. When capacitor C_D is completely discharged and charging starts in the state that C_D pin voltage is 0 V, the minimum value of delay time T_{DLY0} is 7 ms. However, when the discharging time is short and charging starts in the state that the voltage does not completely fall to 0 V, the minimum value of delay time T_{DLY} is 1.1 ms. Then, the minimum value of Low time (reset time) of $\overline{Vo2}$ is 1.1 ms as the delay time T_{DLY}. Refer to Regulations for state of capacitor C_D electrical discharge and delay time on page 10 for details.

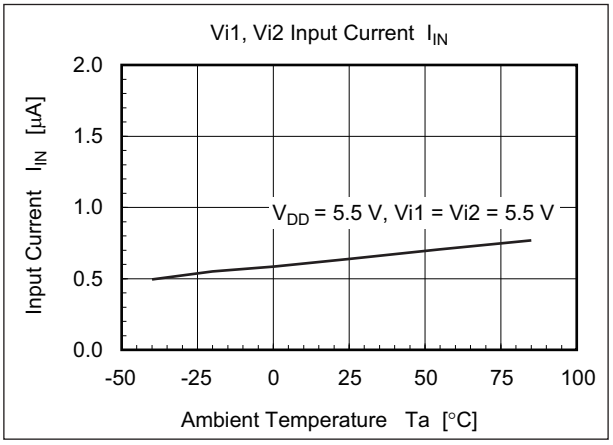
2. Refer to the characteristic curves on page 6 for temperature dependence of the main characteristics.
3. Refer to pages 8 and 9 for the test circuits.

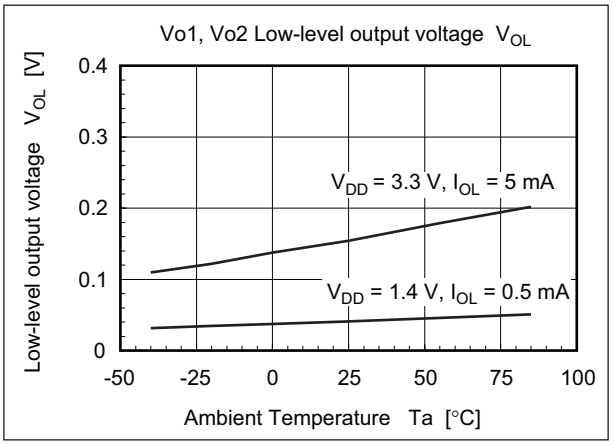
Characteristic curves

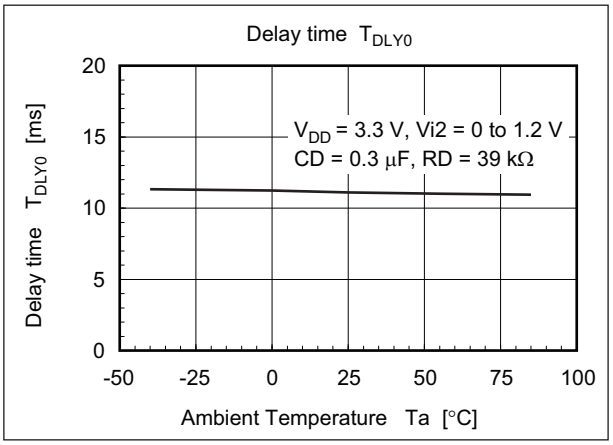


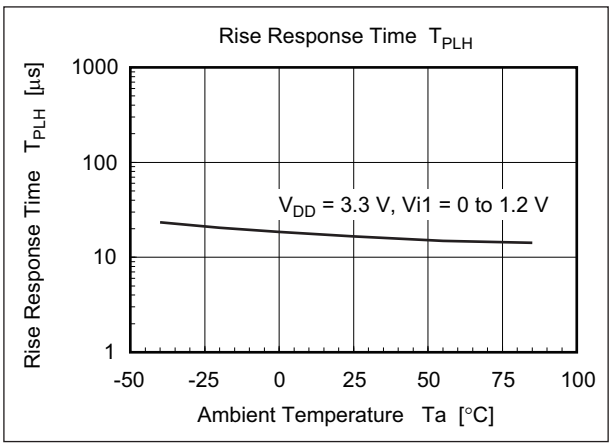


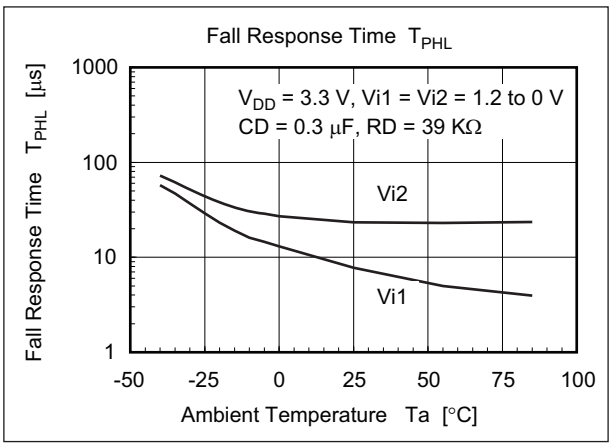








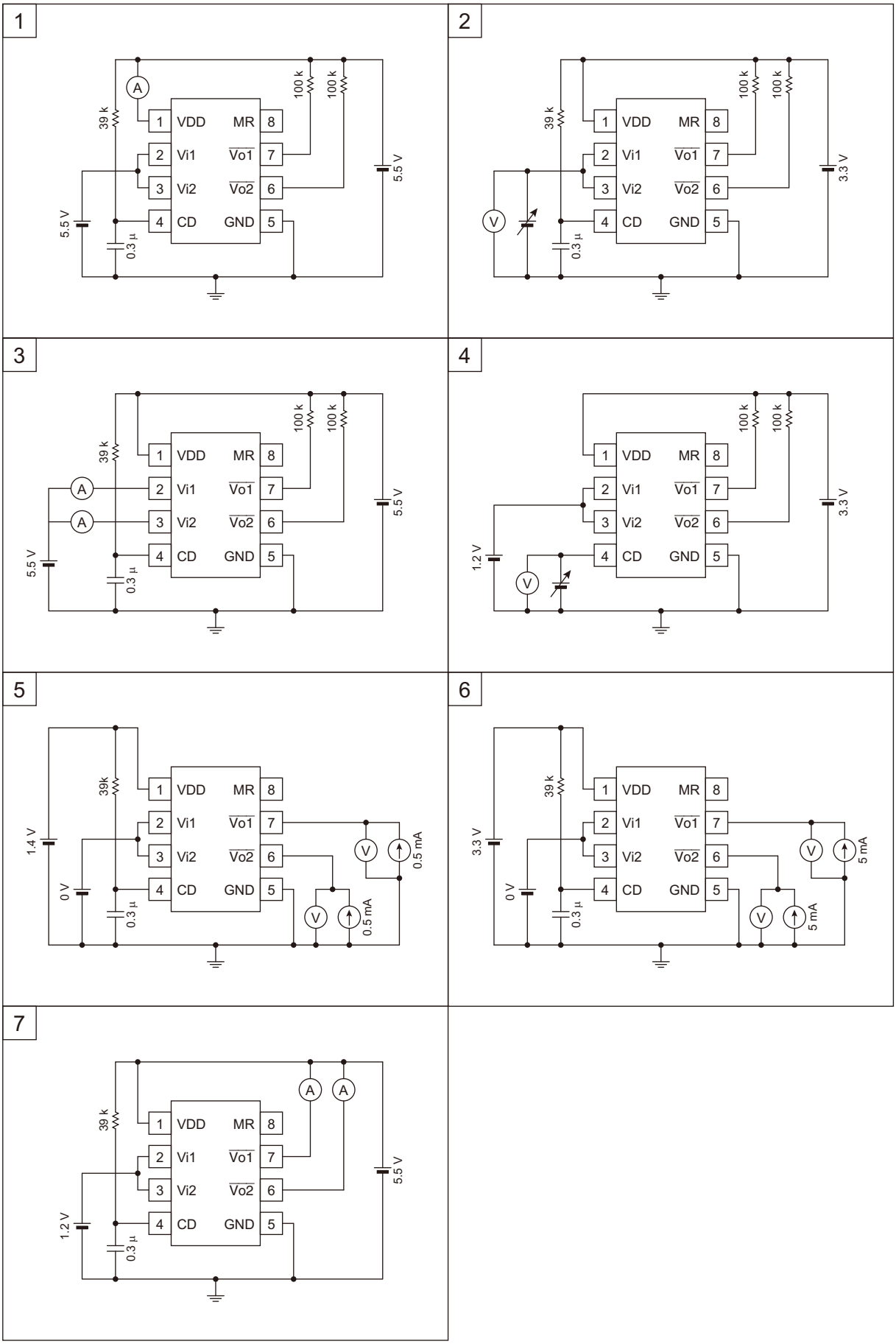




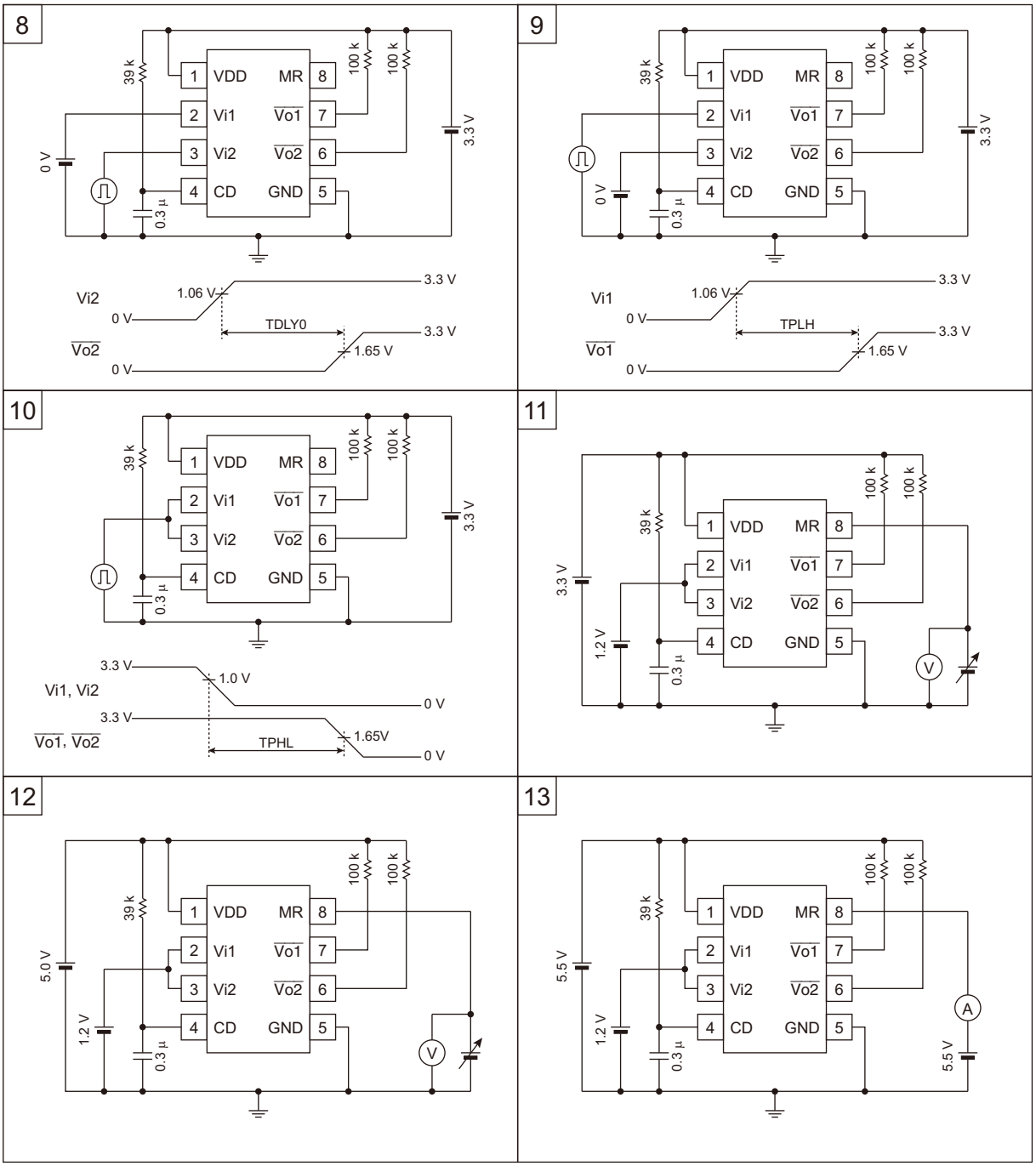
Pin Descriptions

Pin No.	Pin Name	Function
1	VDD	Power-supply pin for the chip. For stable operation, select a capacitor with superior frequency characteristics and connect it between the VDD and GND pins and as close to the chip as possible. When selecting the value of the capacitor, consider aspects of the system environment such as the quality of the power supply. Refer to the block diagram and typical application circuit on page 3 for details.
2	Vi1	Voltage input pin for reset circuit 1 (the circuit without the delay function). When the input voltage falls to or below V_{REF}, the signal output from the $\overline{Vo1}$ pin is changed to the low level. Since the input characteristic includes hysteresis, the signal output from the $\overline{Vo1}$ pin is changed from the low to the high level after the voltage input on pin Vi1 has risen to or above $V_{REF}+V_{HYS}$. The reset-threshold voltage is derived from the power-supply voltage V_{DD1} according to the division ratio set up by resistors R_{S1} and R_{S2} as described under the block diagram and typical application circuit on page 3. To avoid shifting of the reset detection voltage being shifted by input current via the Vi1 pin, select a value no greater than 25 kΩ for parallel resistors R_{S1} and R_{S2}. Refer to the graph on page 3 for details. Besides, to avoid errors due to noise in power-supply voltage V_{DD1}, select a capacitor with superior frequency characteristics and connect it between the Vi2 and GND pins.
3	Vi2	Voltage input pin for reset circuit 2 (the circuit with the delay function). When the input voltage falls to or below V_{REF}, the signal output from the $\overline{Vo2}$ pin is changed to the low level. Since the input characteristic includes hysteresis, the signal output from the $\overline{Vo2}$ pin is changed from the low to the high level after the voltage input on pin Vi2 has risen to or above $V_{REF}+V_{HYS}$ and delay time T_{DLY} has elapsed. The reset-threshold voltage is derived from the power-supply voltage V_{DD2} according to the division ratio set up by resistors R_{S3} and R_{S4} as described under the block diagram and typical application circuit on page 3. To avoid shifting of the reset detection voltage being shifted by input current via the Vi2 pin, select a value no greater than 25 kΩ for parallel resistors R_{S3} and R_{S4}. Refer to the graph on page 3 for details. Besides, to avoid errors due to noise in power-supply voltage V_{DD2}, select a capacitor with superior frequency characteristics and connect it between the Vi2 and GND pins.
4	CD	Pin for connection to the resistor (R_D) and capacitor (C_D) for setting of the delay time, T_{DLY0}. Refer to the Block Diagram and Typical Application Circuit on page 2 for an example of the connection. The relation by which the resistance and capacitance set up the delay time can be expressed as $T_{DLY0} = 0.94 \times C_D \times R_D$. Refer to this formula in determining the values of resistance and capacitance. Resistance R_D must use the one within the range of 1 k to 1 MΩ. Ensure that capacitor C_D has a value no greater than 1.3 µF. The dependence of delay time T_{DLY0} on the values of external capacitor C_D and external resistor R_D is illustrated on page 10. To avoid errors due to noise input via the CD pin, this input includes a Schmitt-trigger inverter.
5	GND	GND pin
6	$\overline{Vo2}$	Reset signal output pin for reset circuit 2 (the circuit with the delay function). The output is open-drain. The recommended value for the pull-up resistor (R_{L2}) is 3 k to 100 kΩ. When the voltage input on pin Vi2 falls to or below V_{REF}, the signal output from the $\overline{Vo2}$ pin is changed from the high to the low level. Since the input characteristic includes hysteresis, the signal output from the $\overline{Vo2}$ pin changes from the low to the high level when the voltage input on pin Vi2 rises to or above $V_{REF}+V_{HYS}$ and the set delay time T_{DLY0} has elapsed. Refer to the timing diagram on page 4 and regulations for state of capacitor C_D electrical discharge and delay time on page 10 for details.
7	$\overline{Vo1}$	Reset signal output pin for reset circuit 1 (the circuit with no delay function). The output is open-drain. The recommended value of the pull-up resistor (R_{L1}) is 3 k to 100 kΩ. When the voltage input on pin Vi1 falls to or below V_{REF}, the signal output from the $\overline{Vo1}$ pin is changed from the high to the low level. Since the characteristic includes hysteresis, the signal output from the $\overline{Vo1}$ pin changes from the low to the high level when the voltage input on pin Vi1 rises to or above $V_{REF}+V_{HYS}$. Refer to the timing diagram on page 4 for details.
8	MR	Manual reset input pin for reset circuit 2 (the circuit with the delay function). The MR signal is active high, so applying a high level to MR sets the Vo2 pin to the low level. If Vi2 > V_{REF} when the signal on the MR pin is changed back from the high to the low level, the Vo2 pin is returned from the low to the high level after a delay time T_{DLY0}. This can be set as required. The MR pin is pulled down to the GND level via an internal 2-MΩ resistor . However, we recommend connection of the pin to the GND line when it is not in use.

Test Circuits

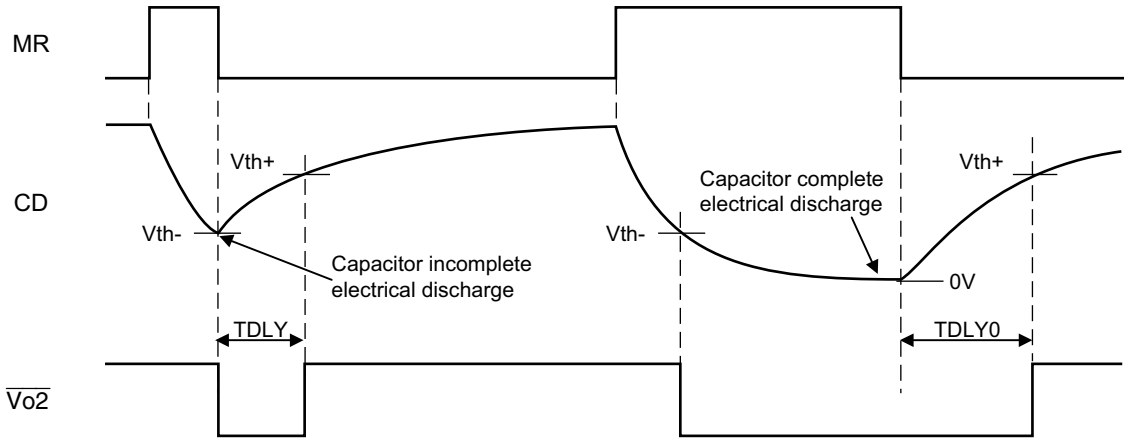


Test Circuits (cont.)

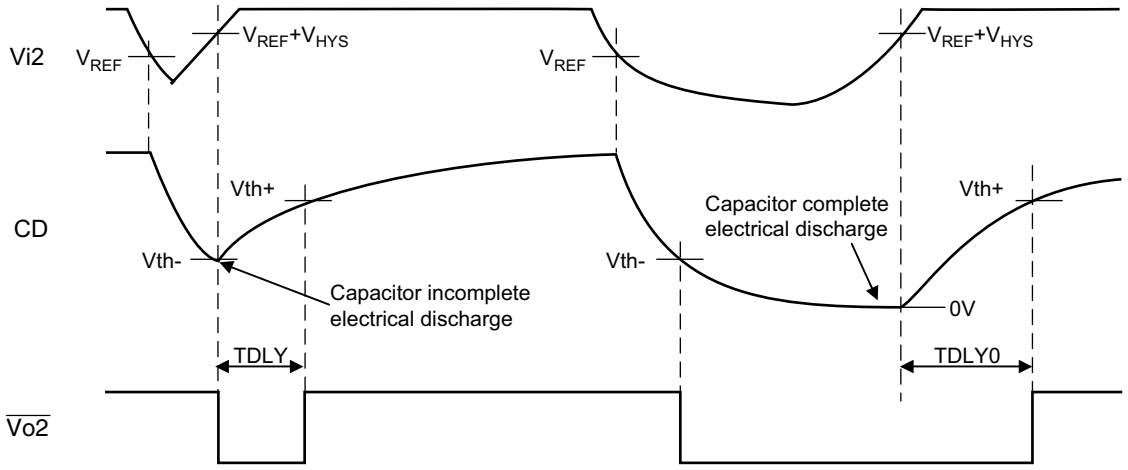


Regulations for state of capacitor C_D electrical discharge and delay time

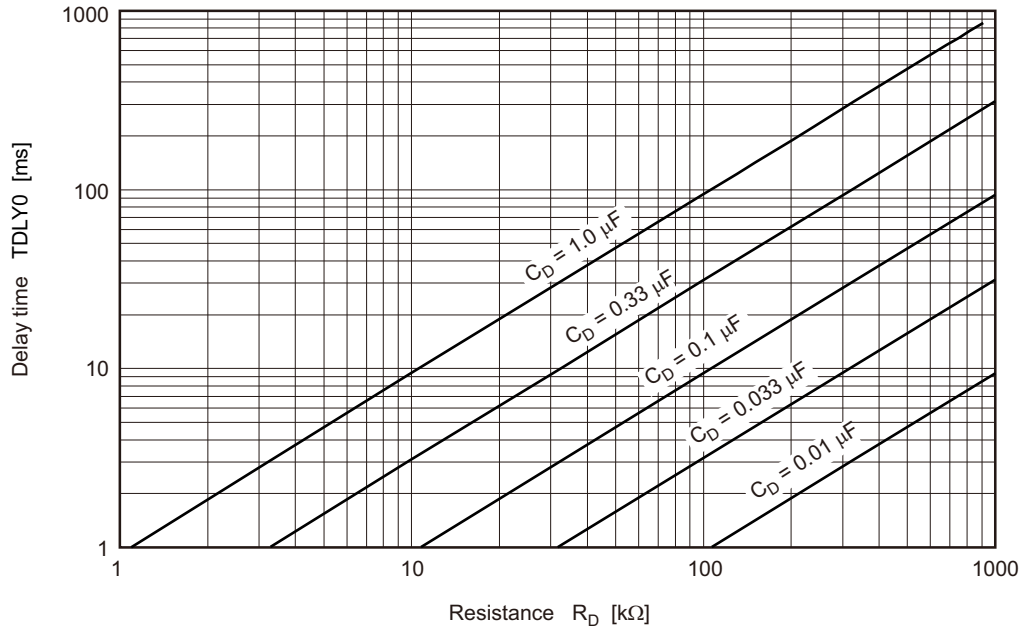
(1) Operation to MR input signal



(2) Operation to Vi2 input signal

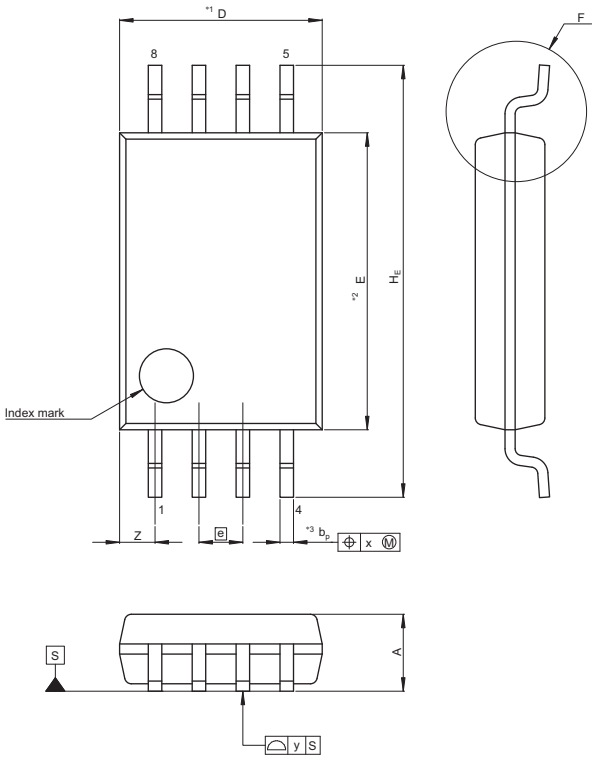


Relation between Delay Time T_{DLY} and External Component Values C_D, R_D



Package Dimensions

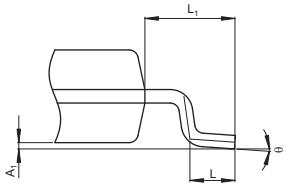
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP8-4.4x3-0.65	PTSP0008JC-B	TTP-8DAV	0.034g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	3.00	3.30
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.805
L	0.40	0.50	0.60
L_1	—	1.00	—

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Ku, Seoul, 135-920, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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