2KBIT Read/Write with ANTICOLLISION Contactless Identification Device

Description

The EM4056 is a CMOS integrated circuit intended for use in contactless Read/Write transponders.
The user's configurable 2 kbits EEPROM memory contained in the chip is organised in 125 words of 16 bits, each word can be irreversibly protected against reading or/and writing attempts.
The user can define a password and protect part or all of the memory.
Serial and identification numbers are laser programmed during IC manufacturing. A reserved application numbering may be made available and customer specific on request.
The EM4056 transmits its data towards the reader by amplitude modulation of the magnetic field and receives the commands from the reader in a similar way.
Simple set of commands allow the dialogue between the EM4056 and the reader. Read and write commands access directly to an address of memory.
The EM4056 has a built-in anticollision protocol which allows an unlimited number of transponders in the reader field to dialogue simultaneously.
The transmission antenna is the only external element required, all the other elements are integrated on chip.

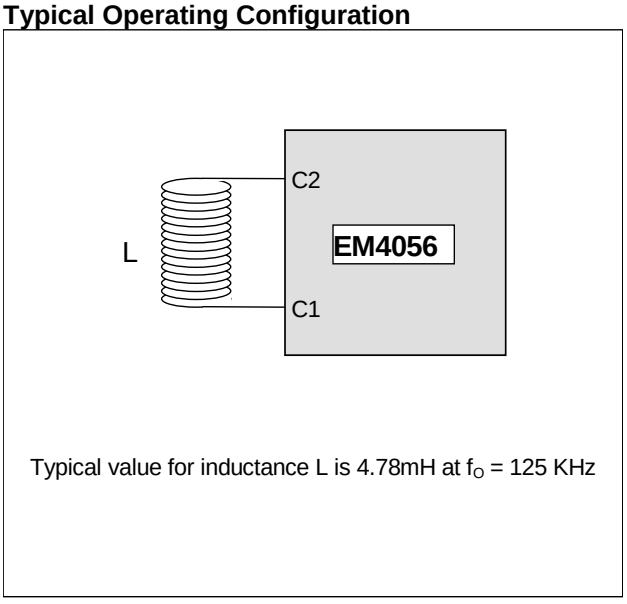
Features

- 2 kBits EEPROM organized in 125 words of 16 bits
- 3 words of 16 Bits Laser ROM for application number and serial number
- Programmable (OTP) Read and/or Write Protection on every word
- Programmable PIN coverage of the memory (0, 25, 50, 75 or 100 %)
- Power check for EEPROM Write operation
- Reader Talk First communication protocol
- Data transmission performed by Amplitude Modulation (ASK) and Biphase (CDP) coding
- Data rate 2 KBauds (Bit Period = 64 periods of carrier frequency)
- 100 to 150kHz carrier frequency
- Long range Read/Write operations
- Block check of data transmission (CRC)
- Anticollision protocol based on unique ID number(unlimited number of tags)
- PIN Code identification linked with counter of false attempts
- On chip arithmetic operation (addition, comparison of secret and non secret data, etc.)
- 340pF ± 3% on chip Resonant Capacitor
- No external supply buffer capacitance
- On chip Rectifier and Voltage Limiter

Applications

- Ticketing
- Hands free Access control
- Prothesis identification
- Prepayment devices
- Manufacturing automation with portable database
- Industrial logistics

Typical Operating Configuration



Typical value for inductance L is 4.78mH at f_O = 125 KHz

Fig. 1

A COMPANY OF THE SWATCH GROUP

Block Diagram

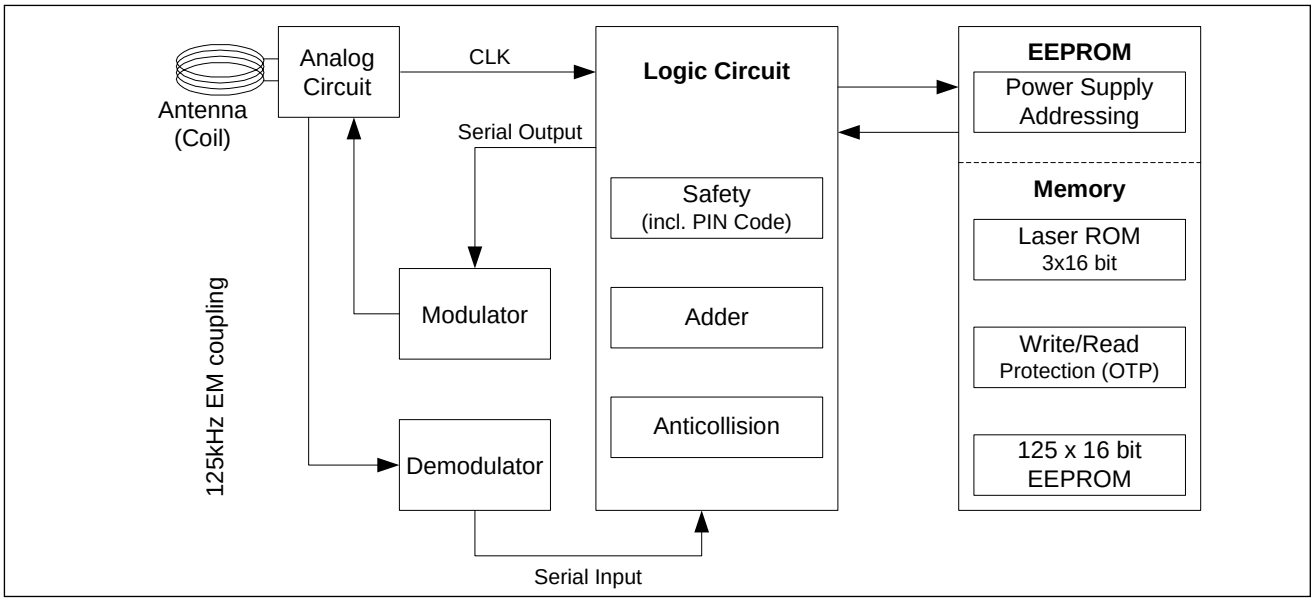


Fig. 2

System Principle

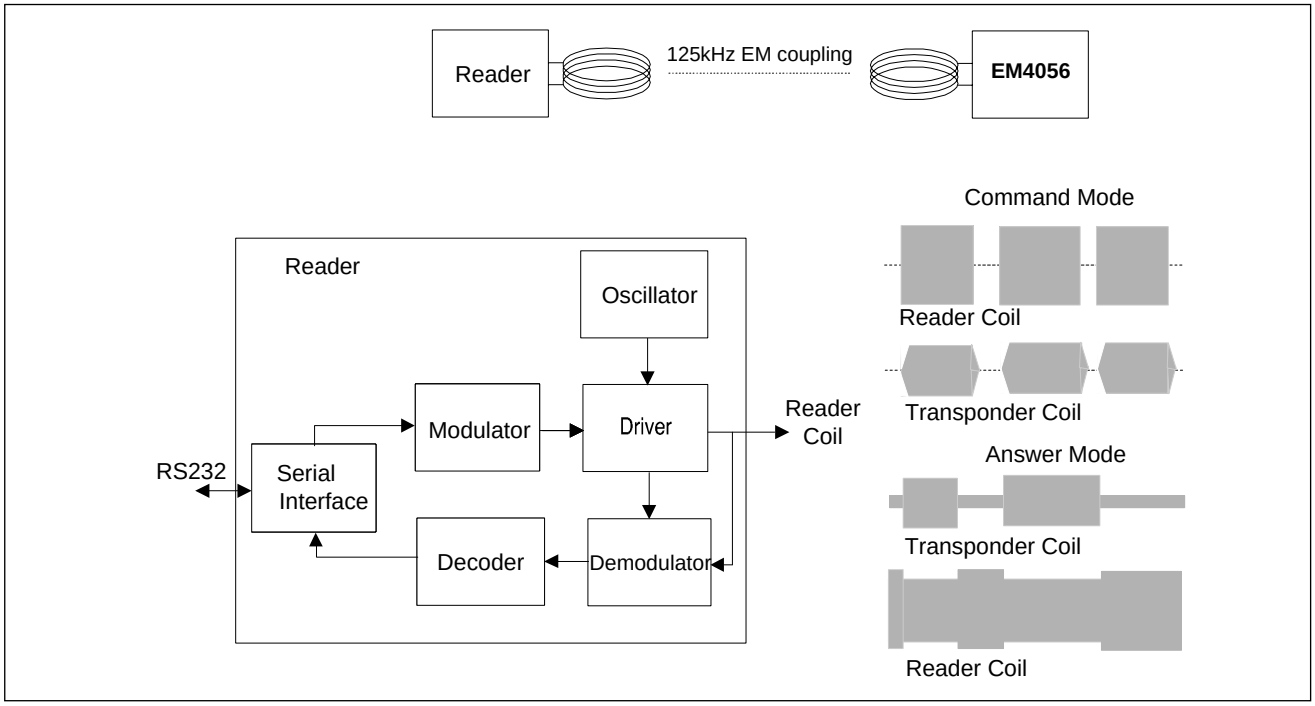


Fig. 3

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Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Voltage on Power Supply pads	V_{DD}	-0.3	6.0	V
Voltage on other pads	V_{PAD}	V_{SS} - 0.3	V_{DD}+ 0.3	V
Max. AC peak current induced on COIL1 and COIL2	I_{COIL}	- 30	+ 30	mA_p
Storage temperature	T_{STORE}	-55	+125	^oC
Operating temperature	T_{OP}	-40	+85	^oC
Electrostatic discharge max. to MIL-STS-883C method 3015	V_{ESD}		1000	V

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min	Max	Units
Max. AC Voltage on COIL	V_{COIL}		(Note 1)	V_{pp}
Max. AC coil current	I_{COIL}	-10	+10	mA_p
Carrier frequency	f_{COIL}	100	150	kHz
Operating temperature	T_{OP}	-40	+85	°C

Note 1: Defined by forcing 10mA on Coil1-Coil2

Electrical Characteristics

Unless otherwise specified : V_{DD} = 4.0 V, V_{SS} = 0 V, T_{OP} = 25°C, V_{COIL} = 4.5 V_{pp}, f_{COIL} = 125 KHz Sine wave

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage (not regulated)	$V_{POS-REG}$				(Note1)	V
Supply voltage (regulated)	V_{DD}	$V_{POS-REG}$ = max (note 1)	3.4		4.3	V
Min. EEPROM Read voltage	V_{RD}	Read mode (note 2)	2.5			V
Min. EEPROM Write voltage	V_{WR}	Write mode	2.5			V
EEPROM Read current	I_{RD}	Read mode		19	25	µA
EEPROM Write current	I_{WR}	Write mode		60	80	µA
Power check EEPROM write current	I_{PWCHK}	V_{DD} = 4.0 V		70	95	µA
EEPROM pwr check threshold voltage	V_{PWCHK}		2.52	2.75	3.10	V
EEPROM data endurance	N_{CY}	Erase all / Write all	10^5			cycle
EEPROM retention (note 3)	T_{RET}	T_{OP} = 55^{o}C after 10^5 cycles	10			year
Voltage drop V_{COIL}- V_{SS} on modulator	V_{ON}	I_{COIL} = 100 µA I_{COIL} = 5 mA			0.50 2.50	V V
Resonance capacitor	C_{COIL}		330	340	350	pF
POR voltage (high)	V_{PRH}	V_{DD} rising		2.0	2.6	V
MONOFLOP delay	T_{MONO}		25	50	85	µs
Min. voltage of clock extractor 1 (note 4)	$V_{CLK1min}$	$V_{coil1-coil2}$ (min for extraction)			4.5	V_{pp}
Min. voltage of clock extractor 2 (note 5)	$V_{CLK2min}$	$V_{coil1-coil2}$ (min for extraction)			1.0	V_{pp}

Note 1: Max. supply voltage (not regulated) is defined by forcing a DC current 10 mA_p in pins COIL1-COIL2

Note 2: The circuit is not functional under low level POR voltage

Note 3: Based on 1000 hours measurement at 150^{o}C

Note 4: Uplink

Note 5: downlink

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Timing Characteristics

Parameter	Symbol	Conditions	Typ			Units
Emission Bit Period		Modulation duration	ON	OFF	ON	RF periods
	T_{b0}	Bit 0		26	8	
	T_{b1}	Bit 1		36	8	
	T_{ab}	Start bit	8	16	8	
Reception Bit Period	T_{bit}			64		RF periods
Reception Bit Period Arbitration	T_{bitarb}			32		RF periods
Select processing time	T_{sp}			190		RF periods
Read processing time	T_{rp}			126		RF periods
Write processing time	T_{wp}			3134		RF periods
Arb1 processing time	T_{a1p}			62		RF periods
Arb2 processing time	T_{a2p}			10		RF periods
Arbitration format duration	Tarb			115		ms
Read Rom format duration	T_{ro}			24.5		
Select format duration	T_s			19.1		
Prot format duration	T_p			32.2		
Read format duration	T_r			20.3		
Write format duration	T_w			36.6		
Comp format duration	T_c			16.6		
Login format duration	T_l			35.1		
EEPROM Write duration	T_{ee}	V_{DD} = 3V		20.0		

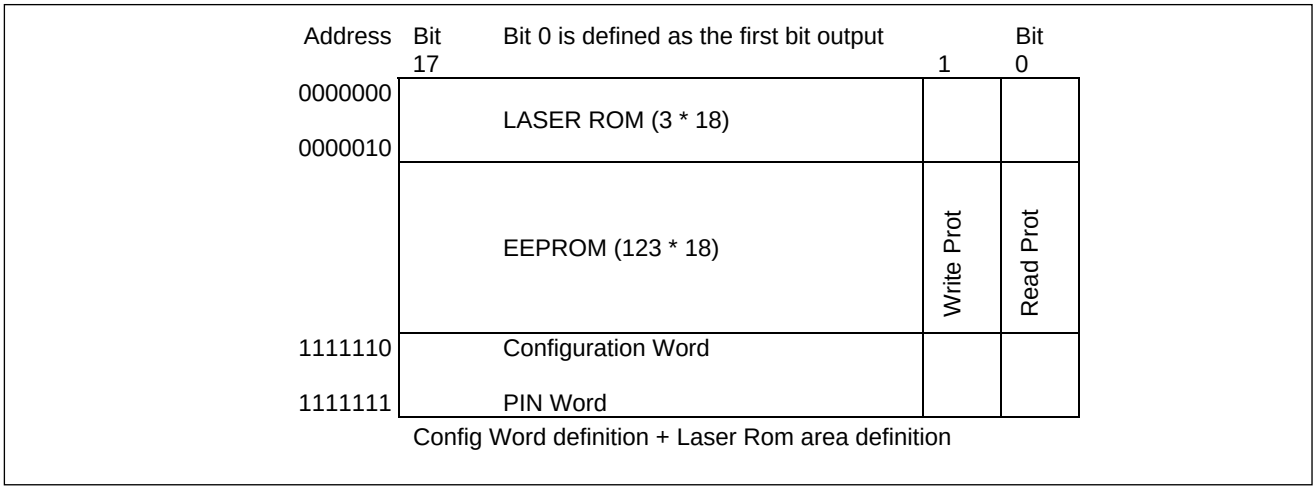
Functional Description

General

The EM4056 has a read enable bit (RdEn) realised with a flip-flop cell. If the RdEn bit is set to « 0 », the transponder is always allowed to answer otherwise it answers only on special commands.
At power on, the default value of the RdEn bit is 0. Therefore, after switching the field on, the RdEn bit of all known tags may be set by the reader in order to separate them in two groups.
The block check sequence uses a 8 bits CRC which is the same polynom for all CRC blocks.

In addition, the CRC block from the EM4056 to the reader is sent in the format of the BitVal frame (see arbitration mode) to increase the error detection rate in the reader.

Memory organisation



Config Word definition + Laser Rom area definition

Fig.4

The Read Protected and the Write Protected bit are OTP bit. Once written to one, it is definitively locked. No possibility to erase them to zero.

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ROM organisation

Address	Datas			Wp	Rp
	bit17		bit2	bit1	bit0
0000000	B15		B0	1	0
0000001	B31		B16	1	0
0000010	L7	L0 C7	C0	1	0

B31-B0 unique code number.
L7-L0 8-bit customer ID, standard version = 65hex, 101dec.
C7 – C0 CRC calculated on bits B31 to B0 and L7 to L0.
(CRC block diagram see figure 4).

Note : EM4056 with different customer ID will also have a different unique code number.

Commands structure

Command	**Code**
ReadRom	MSB 0010 LSB
SelToggle	0100
SelTag	0101
DeselTag	0110
Prot	1000
Read	1010
Write	1100
Add	1101
Comp	1110
Start Arbitration	0001
Continue if “0”	00
Continue if “1”	11
Abort Arbitration	01 or 10

CRC Block Diagram

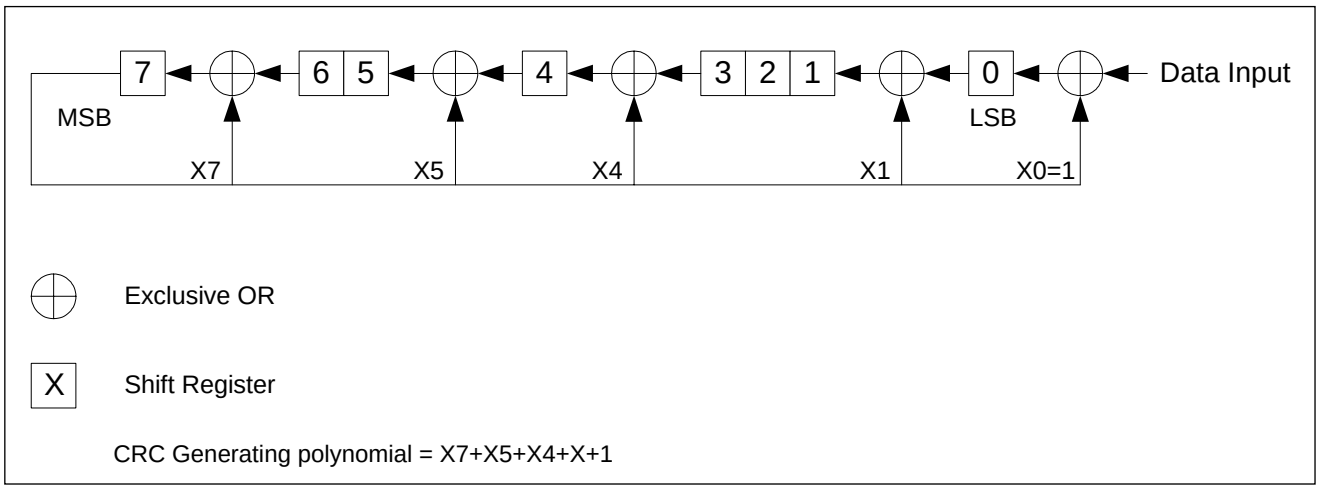


Fig. 5

In uplink the CRC is calculated on all bits of the command (startbit excluded), MSB first.
In dowlink the CRC is calculated on all bits of the answer, first bit sent by the chip first.

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ReadRom
A ReadRomEn command enables only transponders in the field with RdEn bit set to « 0 » to answer.
With this command, the address of a single new tag entered in the field can be detected because all known transponders are not allowed to answer if they are deactivated by the RdEn bit (RdEn=1). If more than one transponder answer a CRC error will be detected and it becomes necessary to perform an arbitration to find all new transponder addresses.
The command is faster than a full arbitration cycle for new tags.
The ReadRomEn command frame consists of three blocks and has a constant length of 13 bits.

The Start bit allows the transponder to synchronise to the new command frame. After the Start bit, the frame contains four bits for the Command. A CRC block of 8 bits is calculated over the Command and appended to the end.
The transponder frame has a length of 40 bits and starts with the 32 bits ROM block. A CRC block of 8 bits is calculated over the transponder address (ROM) and appended to the end.

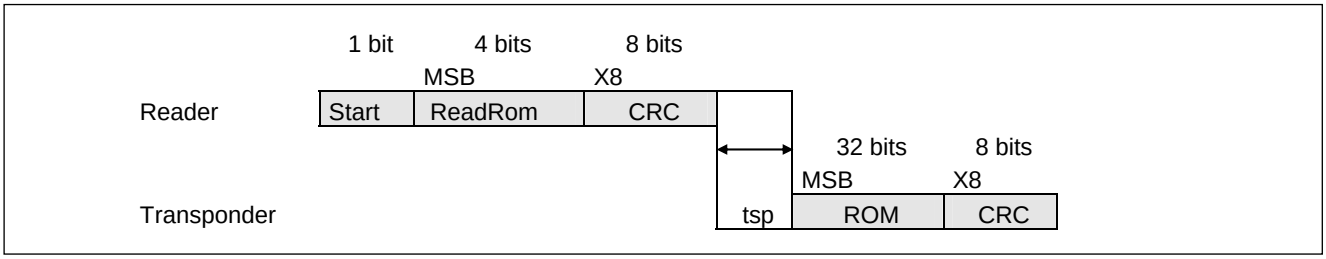


Fig. 6

SelToggle
A SelToggle command addresses a transponder and toggles the RdEn bit (0→1 or 1→0). The transponder returns a frame with the changed value of RdEn bit followed by a CRC.
The SelToggle command frame consists of four blocks and has a constant length of 45 bits.
The Start bit allows the transponder to synchronise to the new command frame. After the Start bit the frame contains four bits for the Command. Next to the Command, a sequence of 32 bits follows with the transponder address. A CRC block of 8 bits is calculated over the Command and the transponder address and appended to the end.
The transponder frame has a length of 10 bits and starts with the RdEn bit and the "not RdEn" bit. A CRC block of 8 bits is calculated over the RdEn and the "not RdEn" and appended to the end.

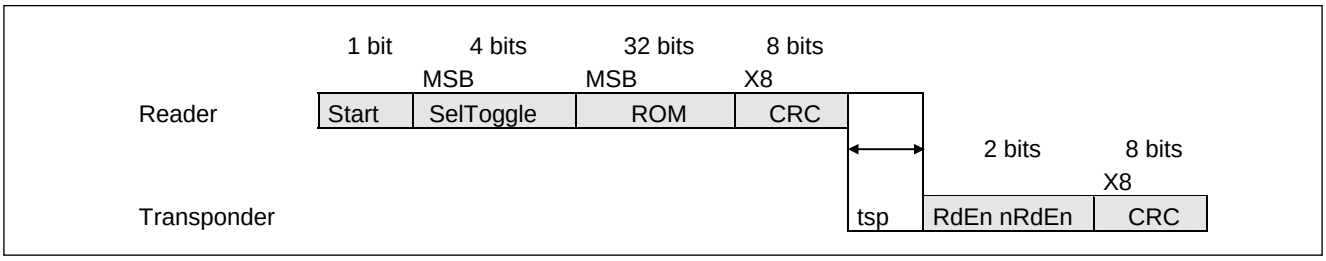


Fig. 7

SelTag
The SelTag command address a transponder with its 32 bit address (ROM) and set the flag Select to 1. After this command, the selected transponder can answer to commands : Read, Write, Prot, Add, Comp and Login.

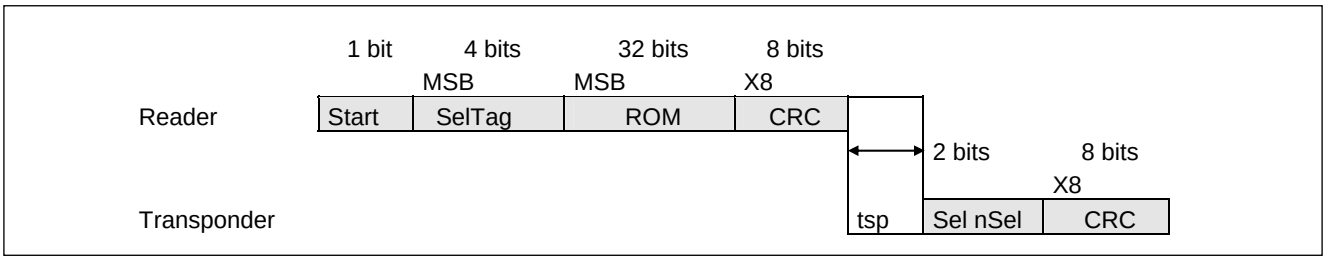


Fig. 8

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DeselTag
The DeselTag command address a transponder with its 32 bit address (ROM) and reset the flag Select to 0.

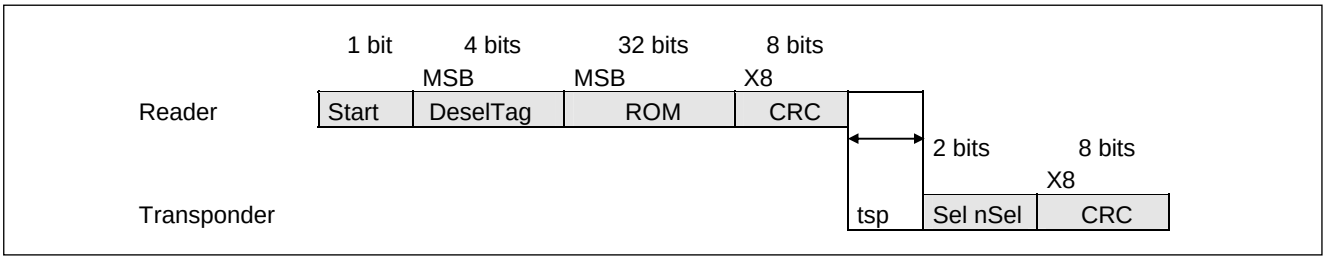


Fig. 9

Prot
Prot command for writing the 2 (OTP) protection bit (read and write) at the specified address.

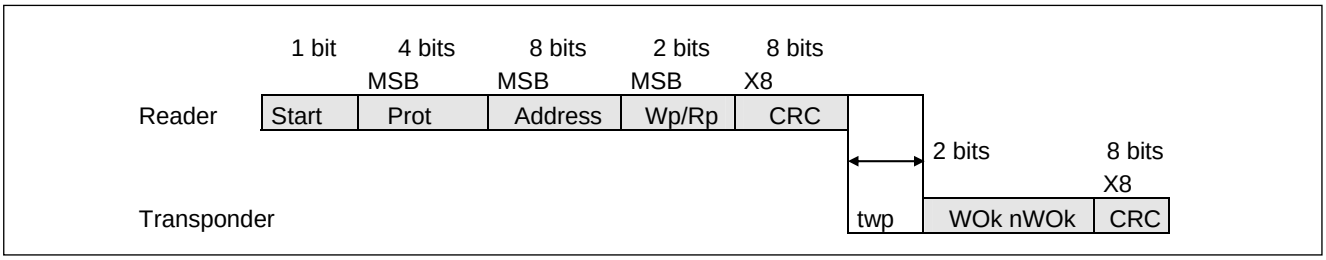


Fig. 10

Wp=1, the specified address is protected against writing.
Rp=1, the specified address is protected against reading.
WOk=1, the protection bit has been successfully written to one.

Read
Read command to get a 16-bit word located at the specified address. If the address is read protected, the circuit transmits a 65535 value.

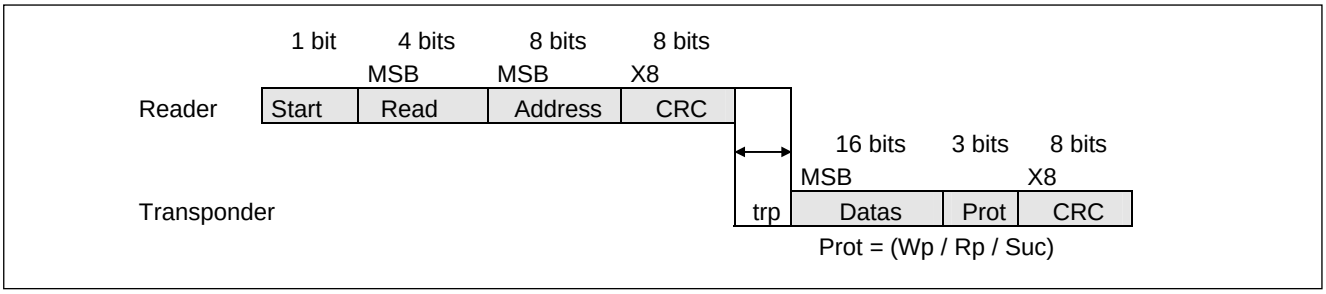


Fig. 11

Datas	Rp	Suc	Definition
12345 dec	0	0	Data = 12345
65535 dec	0	0	Data = 65535
65535 dec	1	x	Read protected
65535 dec	0	1	Read protected by PIN

Wp=1, the specified address is protected against writing.
Rp=1, the specified address is protected against reading.
Suc=1, the specified address is protected by the PIN against reading.

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Write

Write command for 16 bits of data at the specified address.

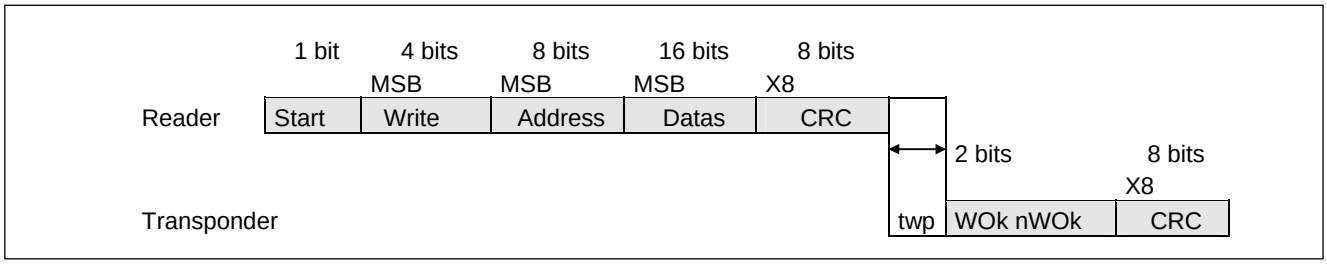


Fig. 12

WOk=1, the write operation has been successfully executed.

When a word is written at the address (Adr 126), where the configuration is located this command is restricted to write the uppermost data (Dat_15 à Dat_4), the lower address (Dat_3 to Dat_0) being reserved for safeguarding the PIN counter.

The data at the address of the configuration are:

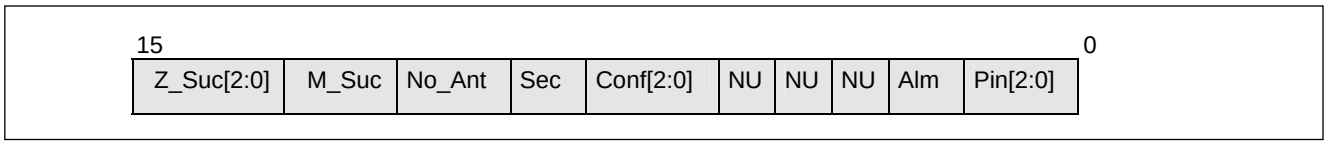


Fig. 13

where :

- M_suc : selects a internal mode for which no reading nor writing can extract or engrave valid data into the area of the memory presently protected by the PIN code.
  M_suc=1, area of memory is protected by PIN.
- Z_suc[2 :0] : determines the address area which is protected by the PIN code. (0% [000], 25%[100], 50%[101], 75 %[110] or 100%[111]).

Z_suc[2:0]	Area protected	Addresses protected
000	00 %	None, incl. PIN
100	25 %	Word 127 – Word 96
101	50 %	Word 95 – Word 64
110	75 %	Word 63 – Word 32
111	100 %	Word 31 – Word 0

- No_Ant : selects the bit "Egal_ROM" and disables the anticollision mode.
  No_Ant=1, no anticollision, the tag is always selected (Sel=1).
- Sec=1, enables the counter of false attempts for the password (PIN).
  Sec=0, counter is disabled.
- Conf[2 :0] : represents the maximum number of attempts for finding a valid PIN before definitive lock of the card for writing.
- Pin[2 :0] : represents the number of remaining attempts for finding the correct PIN.
- Alm : alarm bit indicates a permanent lock of the card against write attempts. This bit is activated as soon as the number of PIN erroneous introduction is surpassed.

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Add

Add command to add one 16-bit data word to another 16-bit data word pointed by the specified address, this command writes the sum at the specified address. It is possible to add a value to an already protected memory location that has been protected against reading, but not to a memory location that has been protected against writing attempts.

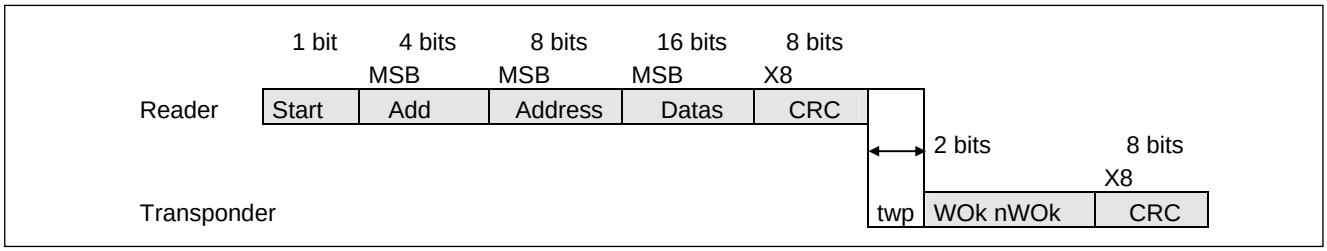


Fig. 14

Comp

Compares a 16 bits data word with another word pointed by the specified address.
It is possible to perform a comparison with a value pointed by a read protected address.
But it is impossible to compare a value with another one in the opaque area without entering the PIN. In the case of PIN violation, the result of the comparison is always false.
Ega=1, comparison successful.

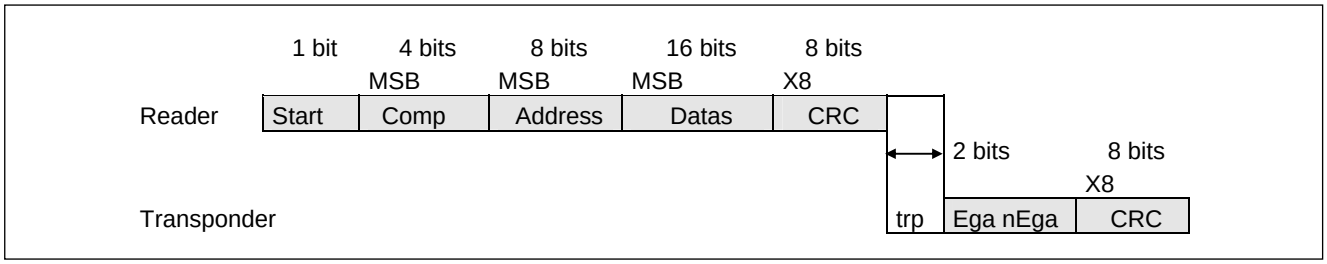


Fig. 15

Login

Compares a 16 bit data word with the PIN word at the address 127.

When a PIN comparison is made (Adr 127) and the identity is established, a write operation occurs in the EEPROM, PIN = CONF , the success bit is released (SUC = 0), the PIN counter is decremented (PIN = PIN - 1) and the corresponding new value is written in the EEPROM.

After n erroneous attempts (PIN=0), the ALM bit is set (ALM = 1), and written in the EEPROM. Since that moment the entire memory is irreversibly locked. The unprotected data words (Rp=0) remain accessible for reading the information they are containing.

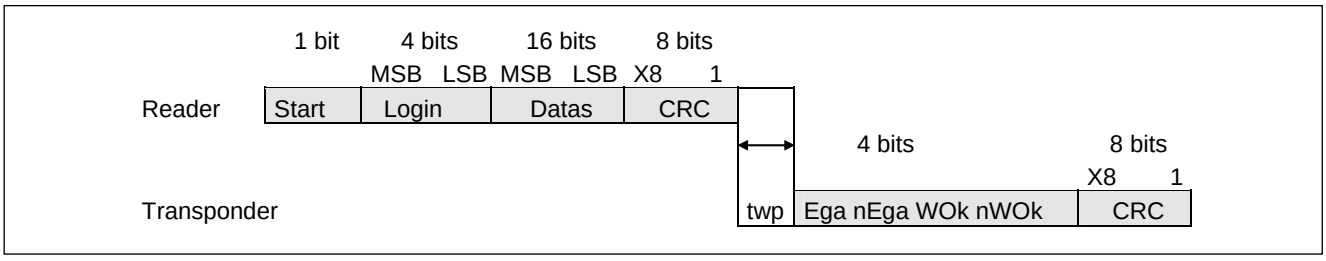


Fig. 16

Ega=1, password ok. Wok=1, writing operation successful.

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Arbitration commands

The arbitration mode is a sophisticated command avoiding collisions among transponders. The arbitration method is based on the method of multiprocessor bus arbitration.
This feature allows the identification of a transponder out of a group, even if they entered the electromagnetic field at the same time. At each arbitration, the reader detects one address of a new transponder.

The arbitration session starts with a special StartArbitration command. If the RdEn bit of the transponder is « 0 », then the transponder belongs to the active group. The arbitration commands will only act on the transponders of the active group.

StartArbitration

After the Start bit, the reader sends a command field which indicates the beginning of an arbitration cycle. An 8 bits CRC block calculated over the StartArbitration command completes this information.
The transponder returns the first BitVal frame corresponding to the LSB of its 32 bits addresses.

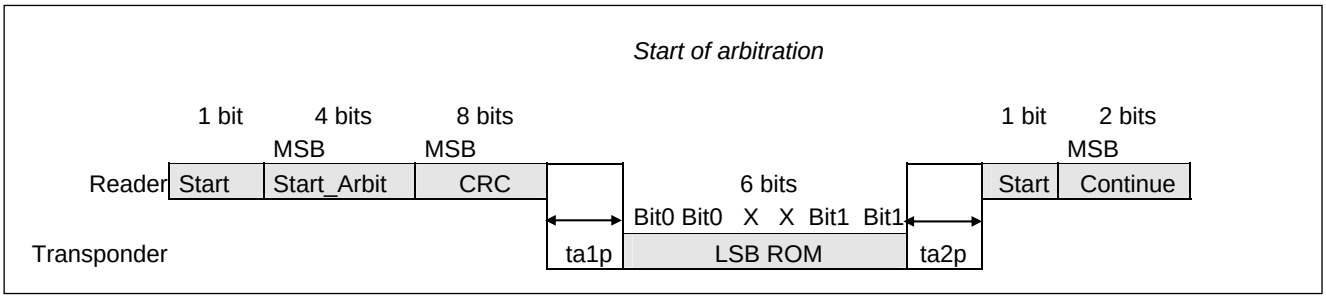


Fig. 17

BitVal *Frame*

The BitVal frame consists of 6 bits. If the Nth bit of its address is logic « 0 », the transponder sends two « 0 » at the position Bit0. If the Nth bit of its address is logic « 1 », the transponder sends two « 0 » at the positions Bit1. The bit repetition increases the transmission reliability.
The response value of the different transponders is coded with the time position of the answer. Therefore no answer conflicts are generated.
Note: Reception Bit Period is 32 RFclocks for all the arbitration (BitVal frame and CRC).

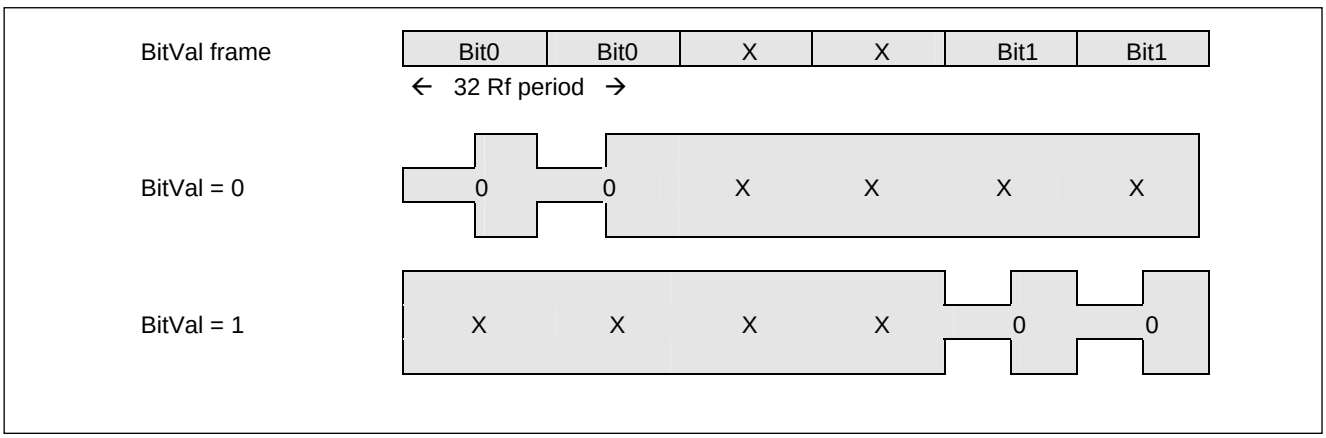


Fig. 18

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Continue *command*

After receiving the BitVal frame from the different transponders in the field the reader decides whether the tags with « 0 » or « 1 » should continue the arbitration process and communicates this with the Continue frame. The transponders whose last BitVal was not identical with the confirmation in the Continue frame stop the arbitration process and wait for a new command.

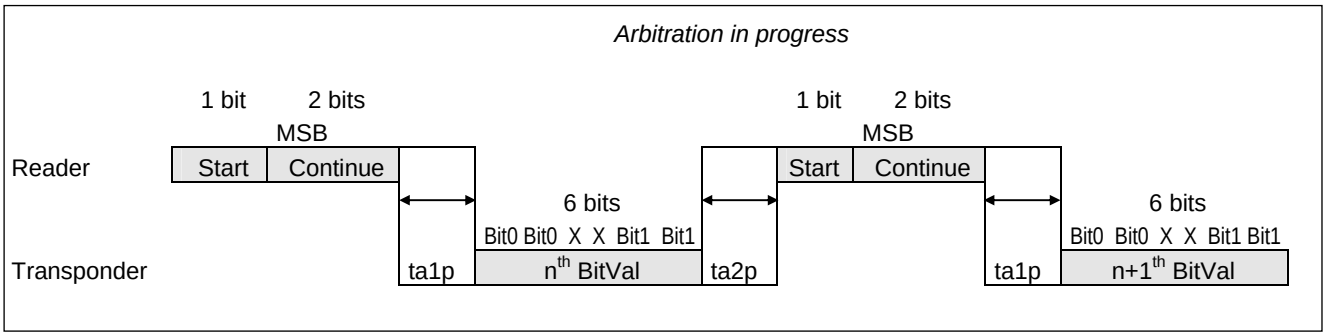


Fig. 19

When the Continue frame of the 32nd bit is processed, only one transponder is left. This new identified tag sets the RdEn bit to 1 and belongs no longer to the active group. The arbitration cycle is completed by a transponder frame for selective commands (RdEn,CRC). The CRC is calculated like a transponder frame for general commands. This means the CRC is calculated over ROM and RdEn of the transponder in order to increase the reliability of the arbitration.

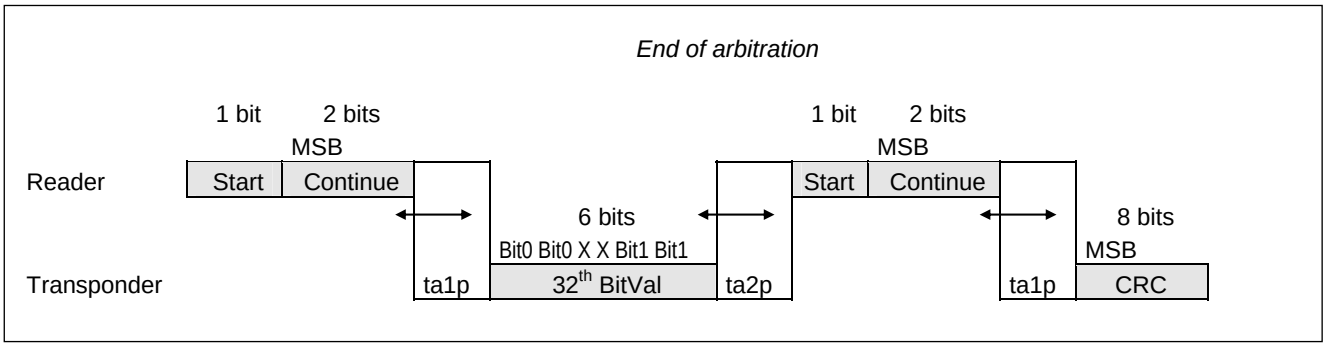


Fig. 20

To identify the address of a transponder, it takes 115 ms (including overhead as mentioned before). That makes it possible to detect about 8.7 new transponders per second, independent of the number of transponders in the electromagnetic field.

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Example of Arbitration protocol *

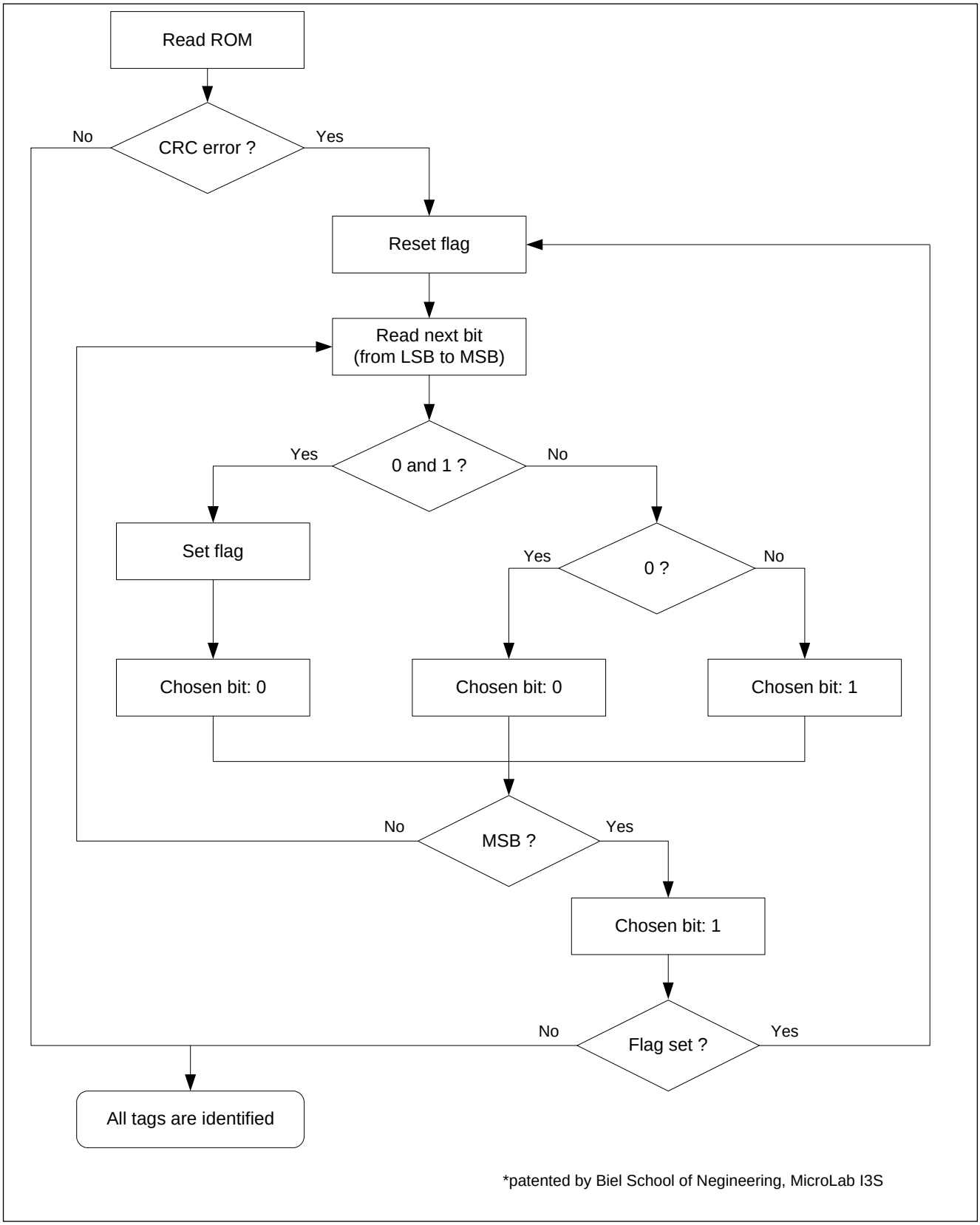


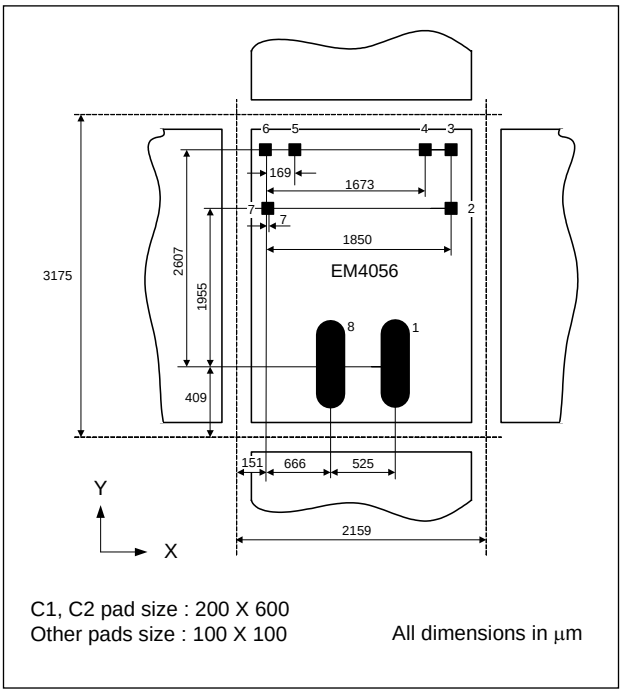
Fig. 21

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Pad Assignment

Pin	Name	Description
1	C1	coil connection
2	TEST_CLK	test pad with pull down
3	VPOS	unregulated positive supply
4	VDD	positive supply
5	TEST_OUT	test pad output
6	VSS	negative supply
7	TEST	test pad with pull down
8	C2	coil connection

Pad Location



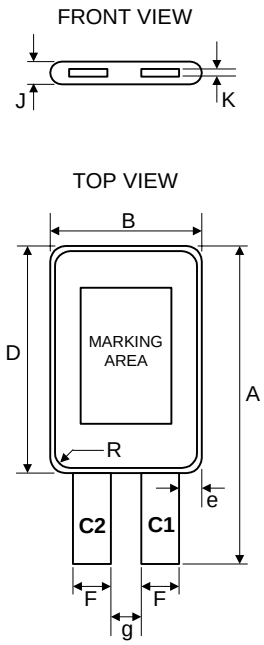
C1, C2 pad size : 200 X 600
Other pads size : 100 X 100

All dimensions in µm

Fig. 22

Package Information

CID Package

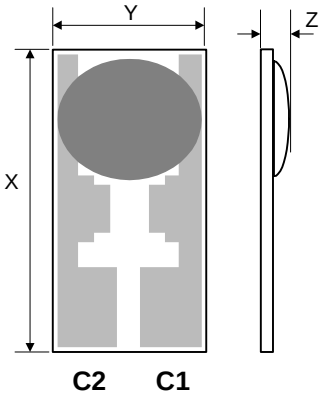


SYMBOL	MIN	TYP	MAX
A	8.2	8.5	8.8
B	3.8	4.0	4.2
D	5.8	6.0	6.2
e	0.38	0.5	0.62
F	1.25	1.3	1.35
g	0.3	0.4	0.5
J	0.42	0.44	0.46
K	0.115	0.127	0.139
R	0.4	0.5	0.6

Dimensions are in mm

Fig. 23

PCB Package



SYMBOL	MIN	TYP	MAX
X		8.0	
Y		4.0	
Z			1.0

Dimensions are in mm

Fig. 24

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Ordering Information

Part Number	Bit coding	Cycle/ bit	Package / Die Form	Delivery Form / Bumping
EM4056B6WW11E	Bi-phase	64	Unsawn wafer, 11mils thickness	With gold bumps
EM4056B6WP11	Bi-phase	64	Die in waffle pack, 11mils thickness	No bumps
EM4056B6CI2LC	Bi-phase	64	CID package, 2 pins (length = 2.5mm)	Bulk
EM4056B6CB2RC	Bi-phase	64	PCB package, 2 pins	Bulk

For other packages, please contact EM Microelectronic-Marin SA

Product Support

Check our Web Site under Products/RF Identification section.
Questions can be sent to cid@emmicroelectronic. com

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