

I²C BUS Controlled 5-Input 2-Output AV Switch Monolithic IC MM1492AF

Outline

This IC is a 5-input 2-output AV switch controlled by the I²C BUS developed for use in television. Because there are 2 outputs, it supports 2 screens and P-IN-P, and also supports an external output (monitor) pin.

Features

- (1) Serial control by I²C BUS
- (2) 5 inputs, 2 outputs
- (3) 1 Y/C (S pin) inputs, 2 outputs
- (4) The video and audio switches can be controlled independently
- (5) Built-in 6dB amp for video
- (6) Built-in Y/C (S pin) mix circuit
- (7) One of the two audio outputs has a built-in -6dB ON/OFF switch
- (8) Slave address can be changed. 90H and 92H possible.
- (9) Audio muting from external pin possible
- (10) Maintains high impedance even when I²C BUS line (SDA, SCL) power supply is off.
- (11) Built-in 3 value discrimination function built-in
- (12) Built-in power ON reset function
- (13) Supports 2 screens and P-IN-P. Also supports external output (monitor) pin.

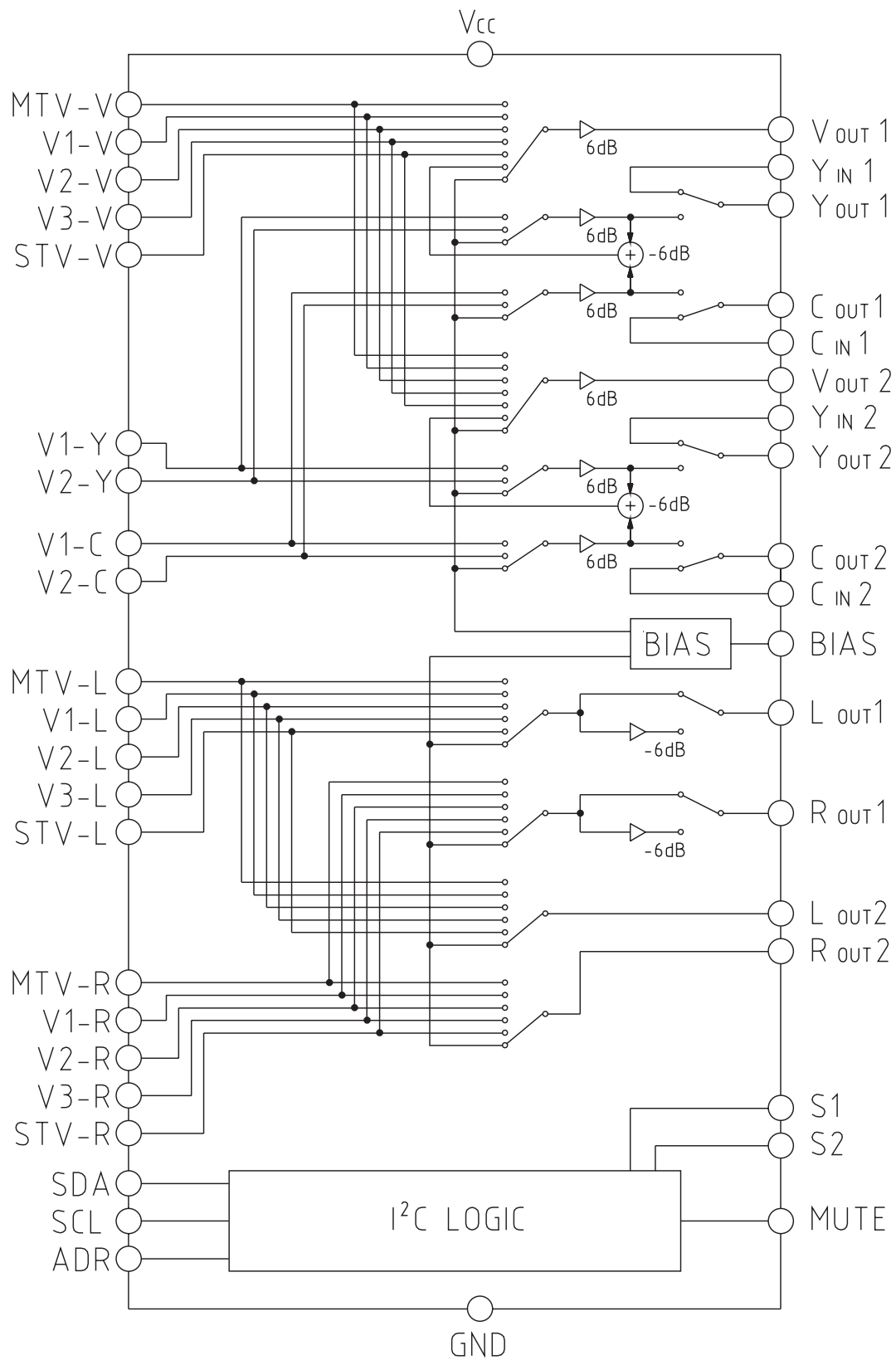
Package

SOP-44B

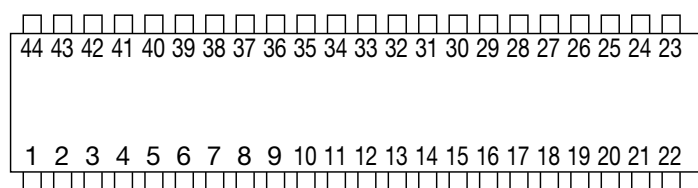
Applications

- (1) TV
- (2) Other video equipment

Block Diagram



Pin Assignment



SOP-44B

1	V1-V	12	S2	23	V _{OUT2}	34	Y _{IN1}
2	V1-L	13	V3-V	24	R _{OUT2}	35	R _{OUT1}
3	V1-Y	14	V3-L	25	C _{OUT2}	36	L _{OUT1}
4	V1-R	15	V3-R	26	L _{OUT2}	37	V _{OUT1}
5	V1-C	16	STV-V	27	Y _{OUT2}	38	BIAS
6	S1	17	STV-L	28	GND	39	Y _{OUT1}
7	V2-V	18	STV-R	29	SDA	40	V _{CC}
8	V2-L	19	Y _{IN2}	30	SCL	41	C _{OUT1}
9	V2-Y	20	ADR	31	MUTE	42	MTV-R
10	V2-R	21	C _{IN2}	32	C _{IN1}	43	MTV-V
11	V2-C	22	GND	33	GND	44	MTV-L

Pin Description

Pin No.	Pin name	Functions	Internal equivalent circuit diagram
1 3 7 9 13 16 19 34 43	V1-V V1-Y V2-V V2-Y V3-V STV-V Y _{IN2} Y _{IN1} MTV-V	Video input terminal (Composite or Y) *Sync chip clamp	
2 4 8 10 14 15 17 18 42 44	V1-L V1-R V2-L V2-R V3-L V3-R STV-L STV-R MTV-R MTV-L	Audio input terminal	

Pin No.	Pin name	Functions	Internal equivalent circuit diagram
5 11 21 32	V1-C V2-C C _{IN2} C _{IN1}	Video input terminal (Croma)	<p>* 1 5,11PIN=25kΩ、21,23PIN=12.5kΩ</p>
6 12	S1 S2	Distinction 3-effects input terminal DC Detect	
20 31	ADR Mute	Sleeve address select Audio Mute terminal	
22 28 33	GND	GND	
23 37	V _{OUT2} V _{OUT1}	Composite video out	
24 26 35 36	R _{OUT2} L _{OUT2} R _{OUT1} L _{OUT1}	Audio out terminal	
25 27 39 41	C _{OUT2} Y _{OUT2} Y _{OUT1} C _{OUT1}	S-Video out terminal	

Pin No.	Pin name	Functions	Internal equivalent circuit diagram
29	SDA	Data input from I ² C	
30	SCL	CLK input from I ² C	
38	BIAS	Internal bias terminal	
40	V _{CC}	V _{CC}	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Power supply voltage	V _{CCmax.}	12	V
Allowable loss	P _d	1100	mW

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T _{OPR}	-20~+75	°C
Operating voltage	V _{OP}	+8~+10	V

Electrical Characteristics (Except where noted otherwise, V_{CC}=9V, Ta=25°C)

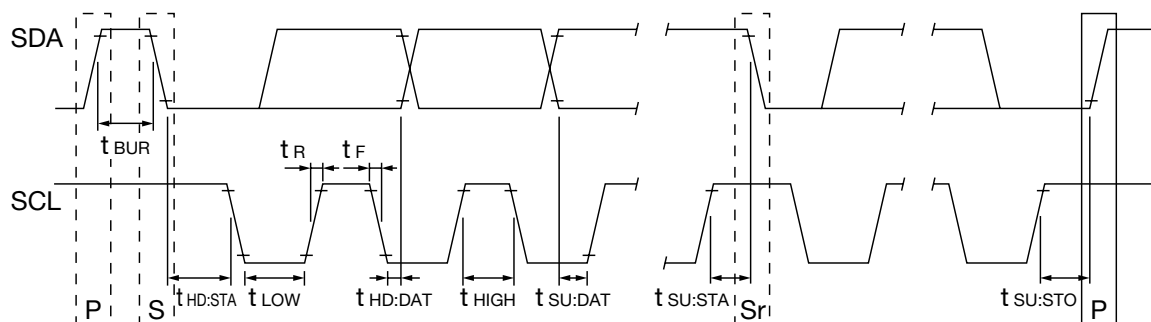
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption	I _{CC}	No signal	39	55	71	mA
V _{OUT1}						
Voltage gain	G _{V1}	SIN wave : 1V _{P-P} 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	f _{V1}	SIN wave : 1V _{P-P} 10MHz/100kHz	-1.0	0.0	1.0	dB
Differential gain	DG _{V1}	Staircase signal 1V _{P-P}	-3	0	3	%
Differential phase	DP _{V1}	Staircase signal 1V _{P-P}	-3	0	3	deg
Input dynamic ranges	DV ₁	SIN wave : 100kHz THD=1.0%	1.4	1.5		V _{P-P}
V _{OUT2}						
Voltage gain	G _{V2}	SIN wave : 1V _{P-P} 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	f _{V2}	SIN wave : 1V _{P-P} 10MHz/100kHz	-1.0	0.0	1.0	dB
Differential gain	DG _{V2}	Staircase signal 1V _{P-P}	-3	0	3	%
Differential phase	DP _{V2}	Staircase signal 1V _{P-P}	-3	0	3	deg
Input dynamic range	DV ₂	SIN wave : 100kHz THD=1.0%	1.4	1.5		V _{P-P}
Y _{OUT1}						
Voltage gain	G _{Y1}	V _n -Y : SIN wave 1V _{P-P} 100kHz	5.5	6.0	6.5	dB
	G _{Y2}	Y _{IN1} : SIN wave 2V _{P-P} 100kHz	-0.5	0.0	0.5	dB
Frequency characteristics	f _{Y1}	V _n -Y : SIN wave 1V _{P-P}	-1.0	0.0	1.0	dB
	f _{Y2}	Y _{IN1} : SIN wave 2V _{P-P}	-1.0	0.0	1.0	dB
Differential gain	DG _{Y1}	V _n -Y : Staircase signal 1V _{P-P}	-3	0	3	%
		Y _{IN1} : Staircase signal 2V _{P-P}	-3	0	3	%
Differential phase	DP _{Y1}	V _n -Y : Staircase signal 1V _{P-P}	-3	0	3	deg
		Y _{IN1} : Staircase signal 2V _{P-P}	-3	0	3	deg
Input dynamic range	D _{Y1}	V _n -Y : SIN wave 100kHz THD=1.0%	1.4	1.5		V _{P-P}
	D _{Y2}	Y _{IN1} : SIN wave 100kHz THD=1.0%	3.2	3.8		V _{P-P}
Output impedance	Z _{OY1}			(50)		Ω
Y _{OUT2}						
Voltage gain	G _{Y3}	V _n -Y : SIN wave 1V _{P-P} 100kHz	5.5	6.0	6.5	dB
	G _{Y4}	Y _{IN2} : SIN wave 2V _{P-P} 100kHz	-0.5	0.0	0.5	dB
Frequency characteristics	f _{Y3}	V _n -Y : SIN wave 1V _{P-P}	-1.0	0.0	1.0	dB
	f _{Y4}	Y _{IN2} : SIN wave 2V _{P-P}	-1.0	0.0	1.0	dB
Differential gain	DG _{Y2}	V _n -Y : Staircase signal 1V _{P-P}	-3	0	3	%
		Y _{IN2} : Staircase signal 2V _{P-P}	-3	0	3	%
Differential phase	DP _{Y2}	V _n -Y : Staircase signal 1V _{P-P}	-3	0	3	deg
		Y _{IN2} : Staircase signal 2V _{P-P}	-3	0	3	deg
Input dynamic range	D _{Y3}	V _n -Y : SIN wave 100kHz THD=1.0%	1.4	1.5		V _{P-P}
	D _{Y4}	Y _{IN2} : SIN wave 100kHz THD=1.0%	3.2	3.8		V _{P-P}
Output impedance	Z _{OY2}			(50)		Ω
C _{OUT1}						
Voltage gain	G _{C1}	V _n -C : SIN wave 1V _{P-P} 100kHz	5.5	6.0	6.5	dB
	G _{C2}	C _{IN1} : SIN wave 2V _{P-P} 100kHz	-0.5	0.0	0.5	dB
Frequency characteristics	f _{C1}	V _n -C : SIN wave 1V _{P-P}	-1.0	0.0	1.0	dB
	f _{C2}	C _{IN1} : SIN wave 2V _{P-P}	-1.0	0.0	1.0	dB
Differential gain	DG _{C1}	C _{IN1} : Staircase signal 2V _{P-P}	-3	0	3	%
Differential phase	DP _{C1}	C _{IN1} : Staircase signal 2V _{P-P}	-3	0	3	deg
Input dynamic range	D _{C1}	V _n -Y : SIN wave 100kHz THD=1.0%	2.75	3.25		V _{P-P}
	D _{C2}	Y _{IN1} : SIN wave 100kHz THD=1.0%	5.5	6.5		V _{P-P}
Input impedance	Z _{IC1}	V _n -C and C _{IN1}	10	15	20	kΩ
Output impedance	Z _{OC1}			(50)		Ω

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
C_{OUT2}						
Voltage gain	G _{C3}	V _{n-C} : SIN wave 1V _{P-P} 100kHz	5.5	6.0	6.5	dB
	G _{C4}	C _{IN2} : SIN wave 2V _{P-P} 100kHz	-0.5	0.0	0.5	dB
Frequency characteristics	f _{C3}	V _{n-C} : SIN wave 1V _{P-P}	-1.0	0.0	1.0	dB
	f _{C4}	C _{IN2} : SIN wave 2V _{P-P}	-1.0	0.0	1.0	dB
Differential gain	DG _{C2}	C _{IN1} : Staircase signal 2V _{P-P}	-3	0	3	%
Differential phase	DP _{C2}	C _{IN2} : Staircase signal 2V _{P-P}	-3	0	3	deg
Input dynamic range	DC ₃	V _{n-Y} : SIN wave 100kHz THD=1.0%	2.75	3.25		V _{P-P}
	DC ₄	Y _{IN2} : SIN wave 100kHz THD=1.0%	5.5	6.5		V _{P-P}
Input impedance	Z _{IC2}	C _{IN2}	10	15	20	kΩ
Output impedance	Z _{OC2}			(50)		Ω
L_{OUT1}						
Voltage gain	G _{L1}	SIN wave 2.5V _{P-P} 1kHz -6dB Select	-6.5	-6.0	-5.5	dB
	G _{L2}	SIN wave 2.5V _{P-P} 1kHz 0dB Select	-0.5	0.0	0.5	dB
Frequency characteristics	f _{L1}	SIN wave 2.5V _{P-P} 1MHz/1kHz	-3.0	0.0	1.0	dB
Total harmonic distortion	THD _{L1}	SIN wave 2.5V _{P-P} 1kHz		0.03	0.1	%
Input dynamic range	D _{L1}	SIN wave 1kHz THD<0.5%	2.6	2.8		V _{rms}
Output offset voltage	V _{OFFL1}	DC offset at the switching time		0	±15	mV
Input impedance	Z _{IL1}		42	60	78	kΩ
Output impedance	Z _{OL1}			(120)		Ω
L_{OUT2}						
Voltage gain	G _{L3}	SIN wave 2.5V _{P-P} 1kHz -6dB Select	-6.5	-6.0	-5.5	dB
	G _{L4}	SIN wave 2.5V _{P-P} 1kHz 0dB Select	-0.5	0.0	0.5	dB
Frequency characteristics	f _{L2}	SIN wave 2.5V _{P-P} 1MHz/1kHz	-3.0	0.0	1.0	dB
Total harmonic distortion	THD _{L2}	SIN wave 2.5V _{P-P} 1kHz		0.03	0.1	%
Input dynamic range	D _{L2}	SIN wave 1kHz THD<0.5%	2.6	2.8		V _{rms}
Output offset voltage	V _{OFFL2}	DC offset at the switching time		0	±15	mV
Output impedance	Z _{OL2}			(120)		Ω
R_{OUT1}						
Voltage gain	G _{R1}	SIN wave 2.5V _{P-P} 1kHz -6dB Select	-6.5	-6.0	-5.5	dB
	G _{R2}	SIN wave 2.5V _{P-P} 1kHz 0dB Select	-0.5	0.0	0.5	dB
Frequency characteristic	f _{R1}	SIN wave 2.5V _{P-P} 1MHz/1kHz	-3.0	0.0	1.0	dB
Total harmonic distortion	THD _{R1}	SIN wave 2.5V _{P-P} 1kHz		0.03	0.1	%
Input dynamic range	D _{R1}	SIN wave 1kHz THD<0.5%	2.6	2.8		V _{rms}
Output offset voltage	V _{OFFR1}	DC offset at the switching time		0	±15	mV
Input impedance	Z _{IR1}		42	60	78	kΩ
Output impedance	Z _{OR1}			(120)		Ω
R_{OUT2}						
Voltage gain	G _{R3}	SIN wave 2.5V _{P-P} 1kHz -6dB Select	-6.5	-6.0	-5.5	dB
	G _{R4}	SIN wave 2.5V _{P-P} 1kHz 0dB Select	-0.5	0.0	0.5	dB
Frequency characteristics	f _{R2}	SIN wave 2.5V _{P-P} 1MHz/1kHz	-3.0	0.0	1.0	dB
Total harmonic distortion	THD _{R2}	SIN wave 2.5V _{P-P} 1kHz		0.03	0.1	%
Input dynamic range	D _{R2}	SIN wave 1kHz THD<0.5%	2.6	2.8		V _{rms}
Output offset voltage	V _{OFFR2}	DC offset at the switching time		0	±15	mV
Output impedance	Z _{OR2}			(120)		Ω

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Crosstalk (★1)						
V _{OUT1}	CT _{V1}	SG1 : 4.43MHz 1V _{P-P} (At mix, SG2/3 input)		-60	-53	dB
V _{OUT2}	CT _{V2}	SG1 : 4.43MHz 1V _{P-P} (At mix, SG2/3 input)		-60	-53	dB
Y _{OUT1}	CT _{Y1}	SG2 : 4.43MHz 1V _{P-P}		-60	-53	dB
Y _{OUT2}	CT _{Y2}	SG2 : 4.43MHz 1V _{P-P}		-60	-53	dB
C _{OUT1}	CT _{C1}	SG3 : 4.43MHz 1V _{P-P}		-60	-53	dB
C _{OUT2}	CT _{C2}	SG3 : 4.43MHz 1V _{P-P}		-60	-53	dB
L _{OUT1}	CT _{L1}	1kHz 2.5V _{P-P}		-90	-80	dB
L _{OUT2}	CT _{L2}	1kHz 2.5V _{P-P}		-90	-80	dB
R _{OUT1}	CT _{R1}	1kHz 2.5V _{P-P}		-90	-80	dB
R _{OUT2}	CT _{R2}	1kHz 2.5V _{P-P}		-90	-80	dB
Terminal voltage						
Video input terminal	V _{VIP}	No signal, No load	4.6	4.9	5.2	V
V _{OUT1/2} terminal	V _{VOP}	No signal, No load	3.9	4.2	4.5	V
Y _{OUT1/2} terminal	V _{YOP}	No signal, No load	3.2	3.5	3.8	V
C _{OUT1/2} terminal	V _{COP}	No signal, No load	3.2	3.5	3.8	V
Audio input terminal	V _{AIP}	No signal, No load	4.0	4.3	4.6	V
Audio output terminal	V _{AOP}	No signal, No load	3.9	4.2	4.5	V
I²C condition (Refer to figure below)						
Input voltage L	V _{IL}		0.0		1.5	V
Input voltage H	V _{IH}		3.0		5.0	V
Low level output voltage	V _{OL}	SDA sink 3mA	0.0		0.4	V
High level input current	I _{IH}	SDA, SCL=4.5V	-10		10	V
Low level input current	I _{IL}	SDA, SCL=0.4V	-10		10	V
Clock frequency	f _{SCL}				100	kHz
Data transfer wait time	t _{BUF}		4.7			μS
SCL start hold time	t _{HD : STA}		4.0			μS
SCL low level hold time	t _{LOW}		4.7			μS
SCL high level hold time	t _{HIGH}		4.0			μS
SCL start setup time	t _{SU : STA}		4.7			μS
SDA data hold time	t _{HD : DAT}		200			nS
SDA data setup time	t _{SU : DAT}		250			nS
SCL rise-time	t _R				1000	nS
SCL fall-time	t _F				300	nS
SCL stop setup time	t _{SU : STO}		4.0			μS

(The inside of parentheses is design guarantee value.)

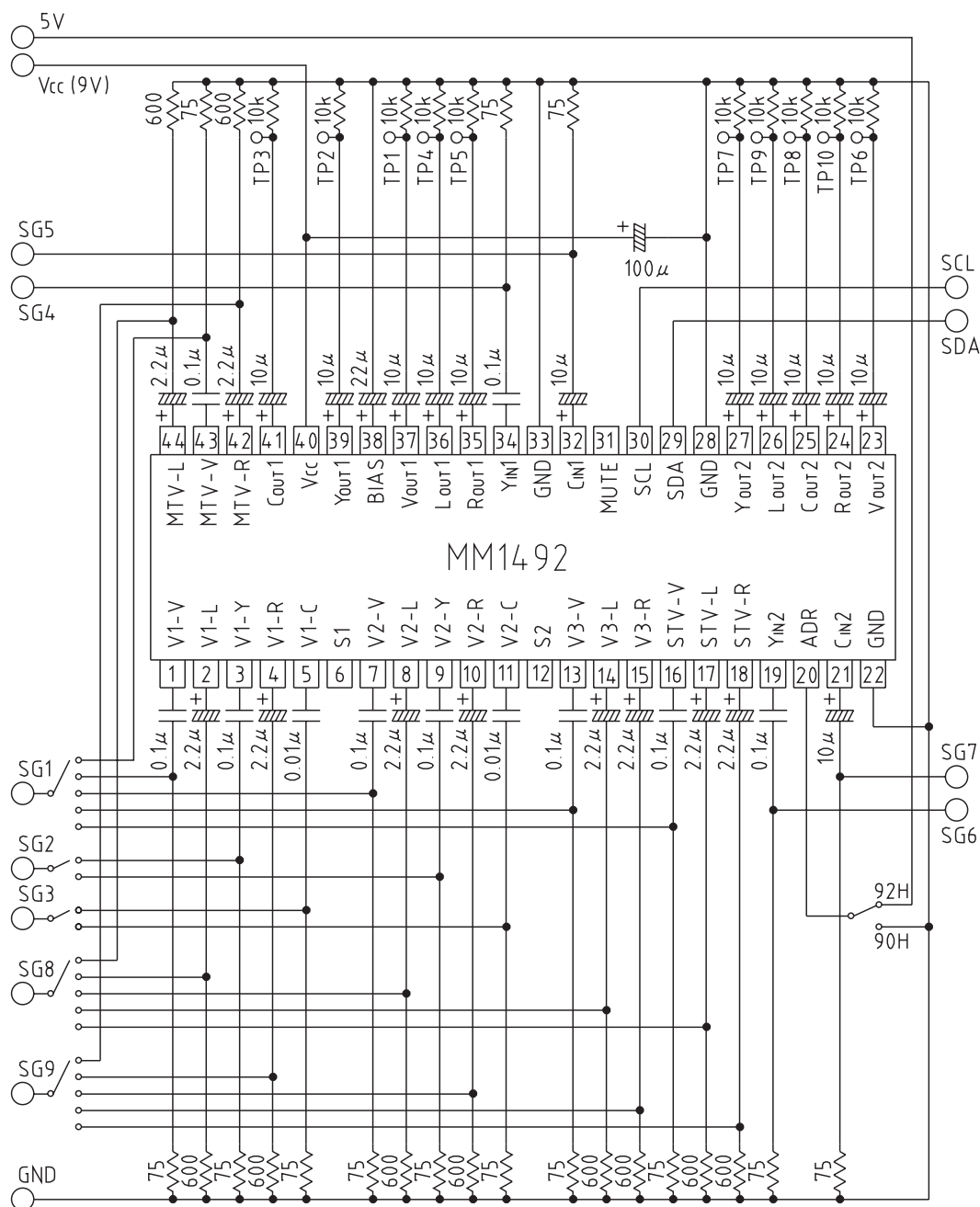
I²C condition



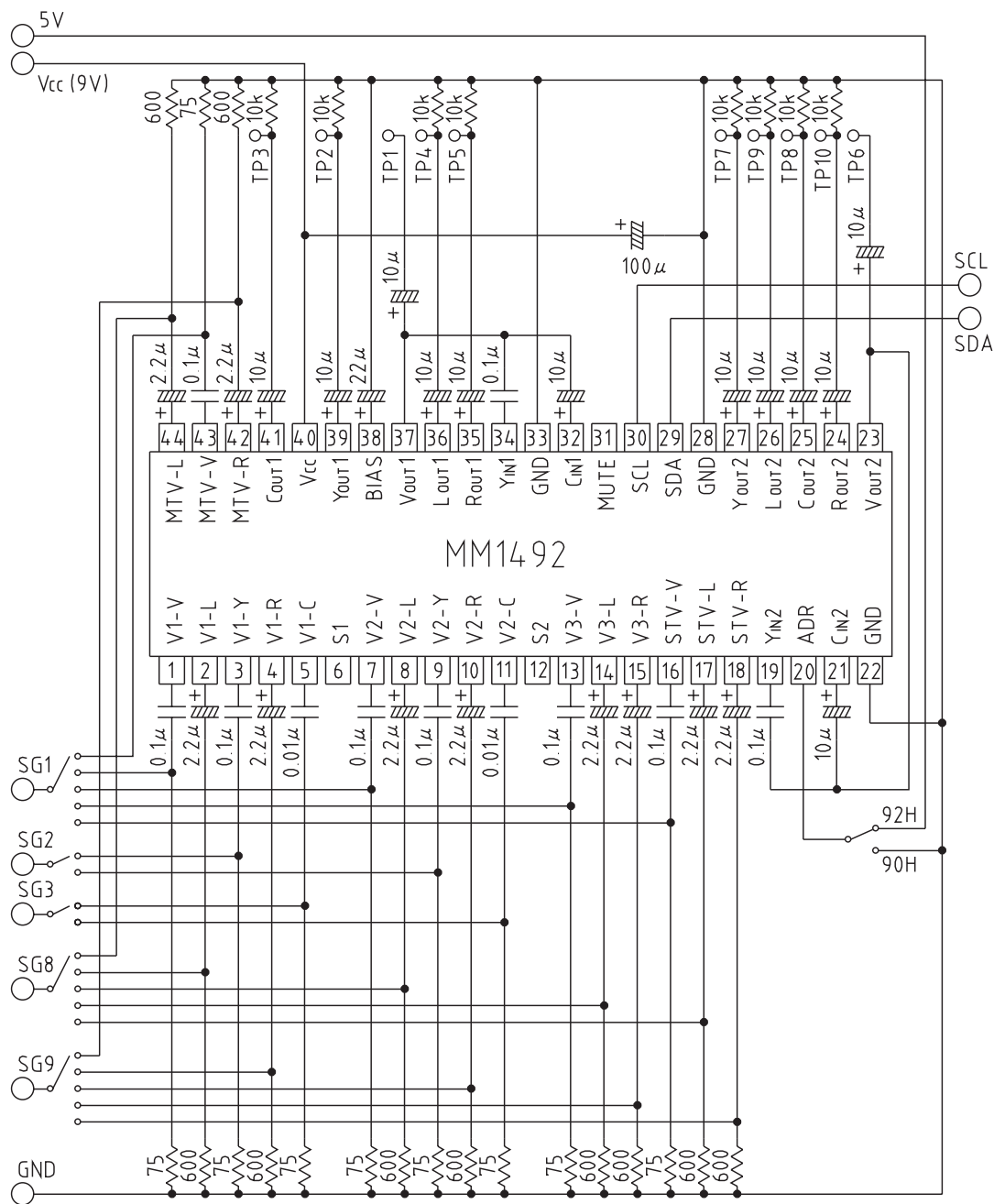
$$V_n - C = V_1 - C, V_2 - C$$

See Test Circuit 2

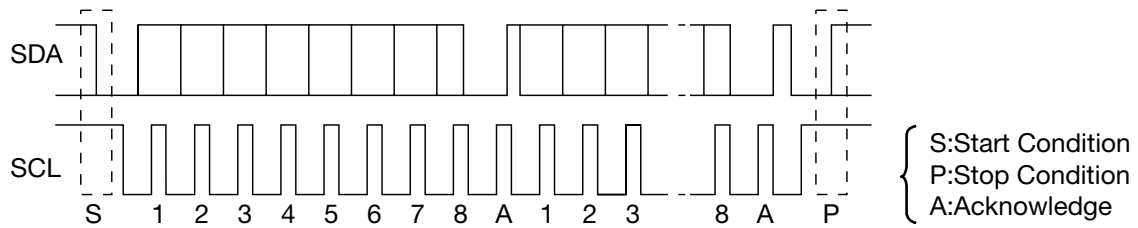
Vn-V, Vn-Y, and Y_{INN} inputs are sync chip clamped, while Vn-C and C_{INN} inputs are non-clamped.



■ Measuring Circuit 2 (Crosstalk measurement)



I²C BUS



I²C BUS is inter bus system controlled by 2 lines (SDA, SCL).

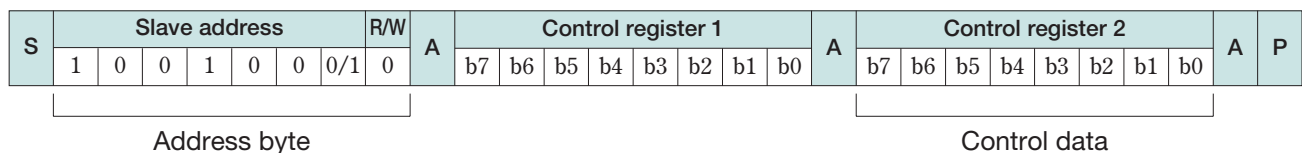
Data are transmitted and received in the units of byte and Acknowledge.

It is transmitted by MSB first from the Start conditions.

[Control registers]

Control registers are data sent from the master for determining the switch conditions.

The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.

Set the R/W bit to 0 when data are used control registers.

As MM1492 slave address, either 90H or 92H can be selected according to the ADR terminal conditions.

When ADR terminal is L, 90H is selected.

The following figure indicates the control contents of control registers and switches.

Each bit of control registers is reset to 0, when power-on.

Register	b7	b6	b5	b4	b3	b2	b1	b0
1	Audio Gain 1	S/Comp select 1	Video out1 select			Audio out1 select		
2	Audio Gain 2	S/Comp select 2	Video out2 select			Audio out2 select		

MM1492 consists of one address byte and two control data bytes (3bytes in total).

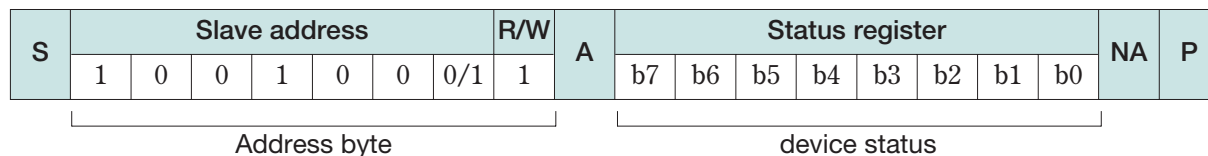
All data over the limited length (4th and subsequent bytes) are fully neglected.

For details of the control contents of switches, refer to the separate table.

[Status registers]

Status registers are data to inform the device status.

The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.

Set the R/W bit to 1 when data are used status registers.

As MM1492 slave address, either 91H or 93H can be selected according to the ADR terminal conditions.

When ADR terminal is L, 91H is selected.

Set the confirmation acknowledgement after the end of status register to non-acknowledgement.

The following figure shows the correspondence of the output data of status registers.

b7	b6	b5	b4	b3	b2	b1	b0
P-ON RESET	×	S1 OPEN	S1 SEL	S2 OPEN	S2 SEL	×	×

P-on RESET : 1 returns when the power on reset is done, 0 returns after reading data once.

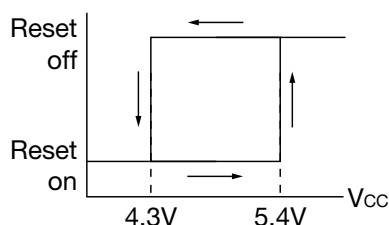
S1/S2 OPEN : S1/S2 OPEN and SEL are identified by 3 values, and output according to the S1/S2 SEL combinations in the following table.

DC voltage of S1/S2	S1/S2 OPEN	S1/S2 SEL
$0.8V \leq DC$	0	1
$1.3V \leq DC \leq 3.5V$	0	0
$DC \leq 4.5V$	1	0

[about power on reset]

MM1492 is provided with a power on reset function to reset each control register to 0 when power supply is turned on.

The power on reset threshold has the hysteresis as shown in following figure.



Switch Control Table

(1) Video output 1

b6	b5	b4	b3	V _{OUT1}	Y _{OUT1}	C _{OUT1}
0	0	0	0	Mute	Mute	Mute
0	0	0	1	MTV-V	Y _{IN1}	C _{IN1}
0	0	1	0	V1-V	Y _{IN1}	C _{IN1}
0	0	1	1	V2-V	Y _{IN1}	C _{IN1}
0	1	0	0	V3-V	Y _{IN1}	C _{IN1}
0	1	0	1	STV-V	Y _{IN1}	C _{IN1}
0	1	1	0	Mute	Mute	Mute
0	1	1	1			
1	0	0	0	Mute	Mute	Mute
1	0	0	1	MTV-V	Y _{IN1}	C _{IN1}
1	0	1	0	V1-(Y+C)	V1-Y	V1-C
1	0	1	1	V2-(Y+C)	V2-Y	V2-C
1	1	0	0	V3-V	Y _{IN1}	C _{IN1}
1	1	0	1	STV-V	Y _{IN1}	C _{IN1}
1	1	1	0	Mute	Mute	Mute
1	1	1	1			

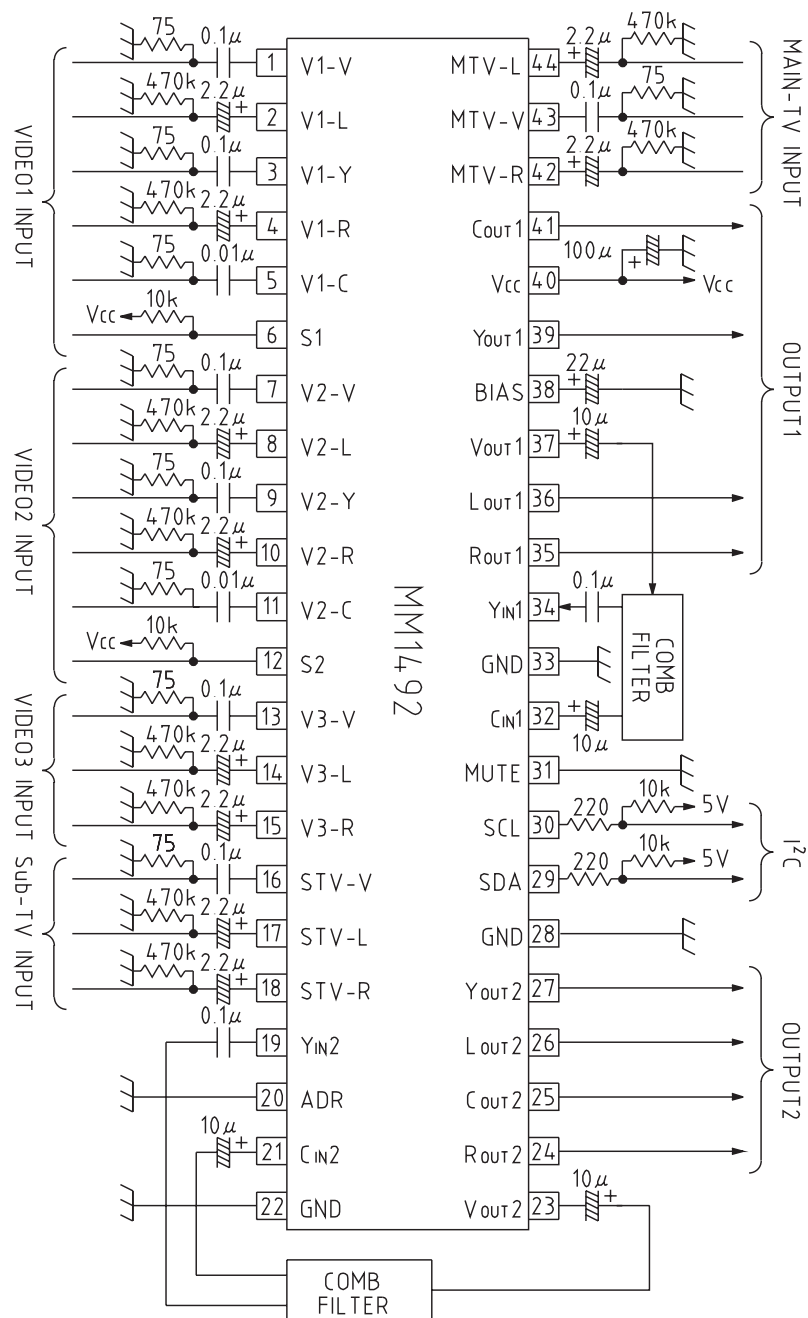
(2) Audio output 1

Mute terminal	b2	b1	b0	L _{OUT1}	R _{OUT1}
≤1.5V (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV-L	MTV-R
	0	1	0	V1-L	V1-R
	0	1	1	V2-L	V2-R
	1	0	0	V3-L	V3-R
	1	0	1	STV-L	STV-R
	1	1	0	Mute	Mute
	1	1	1		
≥3.0V				Mute	Mute

(3) Audio gain

b7	L _{OUT1}	R _{OUT1}
0	-6dB	-6dB
1	0dB	0dB

Application Circuit



Note.

(1) V_{OUT} is set to 4.2V, While C_{IN} is set to 4.9V.

Be careful since the capacity polarity may differ according to the comb filter bias.

(2) Each audio output can be set to myte by setting pin 31 to high. The mute is turned off in when pin 19 is open or low.