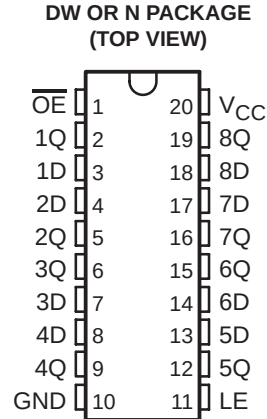


SN64BCT373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- High-Impedance State During Power Up and Power Down
- 3-State True Outputs Drive Bus Lines or Buffer-Memory Address Registers
- Full Parallel Access for Loading
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)



description

This 8-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the SN64BCT373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the enable is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

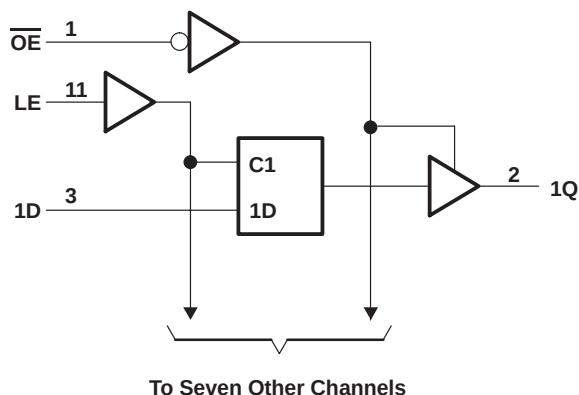
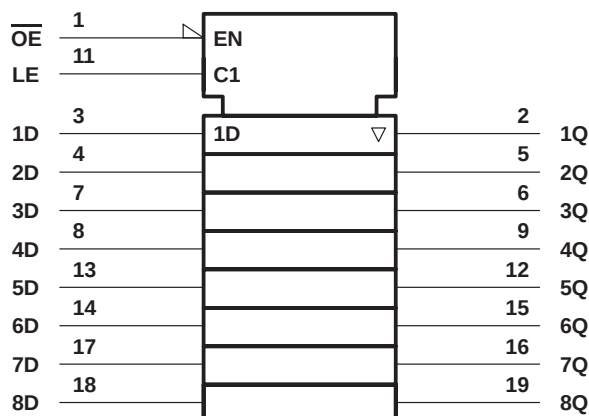
The SN64BCT373 is characterized for operation from -40°C to 85°C and 0°C to 70°C .

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	−0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	−0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$)	−30 mA
Current into any output in the low state, I_O	128 mA
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			−18	mA
I _{OH}	High-level output current			−15	mA
I _{OL}	Low-level output current			64	mA
Δt/ΔV _{CC}	Power-up ramp rate	2			μs/V
T _A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

SN64BCT373
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3		V
		$I_{OH} = -15\text{ mA}$	2	3.1		
V_{OL}	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 64\text{ mA}$		0.42	0.55	V
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$			0.4	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			-0.6	mA
$I_{OS}^\ddagger$	$V_{CC} = 5.5\text{ V}$,	$V_O = 0$	-100		-225	mA
I_{OZ}	$V_{CC} = 0\text{ to }2.3\text{ V}$ (power up)	$V_O = 2.7\text{ V or }0.5\text{ V}$, $\overline{OE} = 0.8\text{ V}$			± 50	μA
	$V_{CC} = 1.8\text{ V to }0$ (power down)				± 50	
I_{OZH}	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$			50	μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.5\text{ V}$			-50	μA
I_{CCL}	$V_{CC} = 5.5\text{ V}$,	Outputs open		37	60	mA
I_{CCH}	$V_{CC} = 5.5\text{ V}$,	Outputs open		2	5	mA
I_{CCZ}	$V_{CC} = 5.5\text{ V}$,	Outputs open		5	8	mA
C_i	$V_{CC} = 5\text{ V}$,	$V_I = 2.5\text{ V or }0.5\text{ V}$		6		pF
C_o	$V_{CC} = 5\text{ V}$,	$V_O = 2.5\text{ V or }0.5\text{ V}$		11		pF

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended range of supply voltage (unless otherwise noted)

		V _{CC} = 5 V, T _A = 25°C		V _{CC} = 4.5 V to 5.5 V				UNIT
				T _A = -40°C to 85°C		T _A = 0°C to 70°C		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high	7.5		7.5		7.5		ns
t _{su}	Setup time, data before LE↓	2		2		2		ns
t _h	Hold time, data after LE↓	5.5		5.5		5.5		ns

switching characteristics over recommended range of supply voltage, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		$T_A = 0^\circ\text{C}$ to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	5.9	7.7	1.5	10.1	2	9.3	ns
t_{PHL}			2	6.7	8.5	1	10.3	1.5	9.5	
t_{PLH}	LE	Q	2	6.2	8.2	2	10.1	2	9.3	ns
t_{PHL}			2	5.9	7.8	2	9.2	2	8.8	
t_{PZH}	$\overline{OE}$	Q	1	7.8	9.6	1	12.3	1	11.8	ns
t_{PZL}			1	8.2	10.2	1	12.5	1	12	
t_{PHZ}	$\overline{OE}$	Q	1	4.9	6.6	1	7.4	1	7	ns
t_{PLZ}			1	5	6.7	1	8.1	1	7.4	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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