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FAIRCHILD SEMICONDUCTOR®

August 2009

FSA2367 — Low R_{ON} (0.75Ω) Triple-SPDT, Negative-Swing Audio Source Switch

Features

- 10µA Maximum I_{CCT} Current Over Expanded Control Voltage Range (V_{IN}=2.6V, V_{CC}=4.3V)
- On Capacitance 55pF Typical (C_{ON})
- 0.75Ω Typical On Resistance (R_{ON})
- Common Ports 1A, 2A, 3A with Negative Swing Audio to -2V
- -3db Bandwidth: >150 MHz
- Low Power Consumption (1µA Maximum)
- Power-Off Feature for 1A/2A/3A Pin (I_{IN} < 2µA)
- Packaged in Pb-Free 14-Pin TSSOP and DQFN

Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Description

The FSA2367 is a triple Single-Pole Double-Throw (SPDT) switch that multiplexes three sources of data or audio under independent control pins. The FSA2367 has special circuitry on the 1A, 2A, 3A pins that allows a power-off feature. With the V_{CC} supply removed and a voltage on the 1A/2A/3A pins, there is minimal leakage current into the 1A/2A/3A data pins. In addition, the FSA2367 also features very low quiescent current to extend battery life. The low quiescent current allows mobile handset applications direct interface with the baseband processor general-purpose I/Os. Typical applications involve switching in portables and consumer applications such as cell phones, digital cameras, and notebooks with hubs or controllers.

IMPORTANT NOTE:

For additional information, please contact analogswitch@fairchildsemi.com.

Ordering Information

Part Number	Top Mark	Eco Status	Package
FSA2367BQX	2367	Green	14-Terminal Depopulated very thin Quad Flat-pack No leads (DQFN) 2.5 x 3.0mm, JEDEC MO-241
FSA2367MTCX	FSA2367	RoHS	14-Lead Thin Shrink Small Outline Package (TSSOP), 4.4mm Wide, JEDEC MO-153

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Analog Symbol

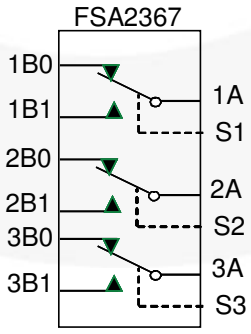


Figure 1. Analog Symbol

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Pin Assignments

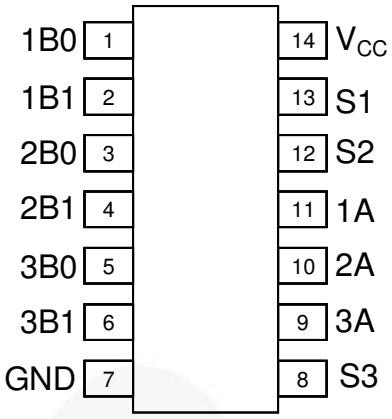


Figure 2. Pin Assignment TSSOP-14 (Top View)

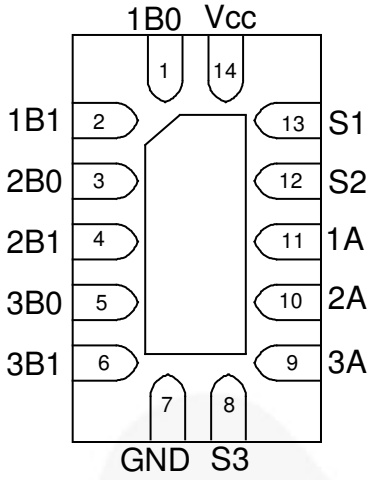


Figure 3. Pad Assignment DQFN-14 (Top View)

Pin Descriptions

Pin Name	Description
S1, S2, S3	Switch Control Selects
1A, 2A, 3A	A Data Bus (Common)
1Bn, 2Bn, 3Bn	Multiplexed Source inputs

Truth Table

S1, S2, S3	Function
LOW	1B0=1A; 2B0=2A; 3B0=3A
HIGH	1B1=1A; 2B1=2A; 3B1=3A

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltages		-0.5	6.0	V
V_{SW}	Switch I/O Voltage[1]	1Bn, 2Bn Pins	V_{CC}-5.5V	V_{CC}-0.3V	V
		1A, 2A Pins	V_{CC}-5.5V	V_{CC}-0.3V	V
V_{CNTRL}	Control Input Voltage[1]	S0, S1	-0.5	6.0	V
	Input Clamp Diode Current		-50		mA
	Switch I/O Current	Continuous		350	mA
	Peak Switch Current	Pulsed at 1ms duration, <10% Duty Cycle		500	mA
P_D	Power Dissipation at 85ºC	DQFN14 package		2.5	µW
		TSSOP14 package		2.5	µW
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature	Soldering, 10 seconds		+260	°C
ESD	Human Body Model (JEDEC: JESD22-A114)	All Pins		5500	kV
		I/O to GND		8000	
		VCC to GND		8000	
	Charged Device Model (JEDEC-JESD22-C101)			2000	kV

Note:

1. Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltages	2.7	4.3	V
$V_{S0:S1}$	Control Input Voltage	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	V_{CC} -5.5	V_{CC}-0.3	V
T_A	Operating Temperature	-40	+85	ºC
θ_{JA}	Thermal Resistance (free air)		145	ºC/W

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DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Vcc (V)	T_A=- 40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
	Analog Signal Range			Vcc-5.5		Vcc	V
V_{IK}	Clamp Diode Voltage	I_{IN}=-18mA	3.0			-1.2	V
V_{IH}	Input Voltage High		2.7 to 3.6	1.2			V
			3.6 to 4.3	1.5			
V_{IL}	Input Voltage Low		2.7 to 3.6			0.5	V
			3.6 to 4.3			0.7	
I_{IN}	Control Input Leakage	V_{IN}=0 to V_{cc}	4.3			±1	µA
I_{OFF}	Power-Off Leakage Current (Common Port Only 1A, 2A)	Common Port (1A, 2A), $V_{SW=}$0 to 4.3V, V_{CC}=0V	0V			±10	µA
$I_{NO(0FF)}$	Off-Leakage Current of Port 1Bn, 2Bn	1Bn, 2Bn=0.5V, V_{CC} - 0.5V or Floating 1A, 2A=0.5V, V_{CC} – 0.5V Figure 8	4.3	-250	10	250	nA
$I_{NC(0N)}$	On-Leakage Current of Port 1Bn, 2Bn	1Bn, 2Bn=Floating 1A, 2A=0.5V, V_{CC} – 0.5V Figure 10	4.3	-250	10	250	nA
R_{ON}	Switch On Resistance[2]	1Bn or 2Bn=0V, 0.7V, 2.0V,2.7V, $I_{ON=}$-100m Figure 9	2.7		0.75	2.00	Ω
ΔR_{ON}	Delta R_{ON}[3]	1Bn or 2Bn=0.7V , $I_{ON=}$-100mA	2.7		0.5		Ω
$R_{FLAT(ON)}$	On Resistance Flatness[4]	1Bn or 2Bn=0V, 0.7V, 2.0V,2.7V, $I_{ON=}$-100mA	2.7 to 4.3		0.23	0.40	Ω
I_{CC}	Quiescent Supply Current	$V_{SW=}$0 or V_{CC}, I_{OUT}=0	4.3			500	nA
I_{CCT}	Increase in I_{CC} Current per Control Voltage and V_{CC}	$V_{CNTRL=}$2.6V	4.3		2.2	10.0	µA
		$V_{CNTRL=}$1.8V	4.3		6.5	15.0	

Notes:

2. Measured by the voltage drop between the 1Bn (2Bn, 3Bn) and 1A (2A, 3A) pins at the indicated current through the switch. On resistance is determined by the lower voltage on the two.
3. Guaranteed by characterization; not tested in production.
4. Flatness is defined as the difference between minimum and maximum on resistance over the specified range.

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AC Electrical Characteristics

All typical values are for V_{CC}=3.3V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Vcc (V)	T_A=- 40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time, S to Output	V_{Bn}=1.5V, R_L=50Ω, C_L=35pF Figure 10, Figure 12	2.7 to 4.3		45	60	ns
t_{OFF}	Turn-Off Time, S to Output	V_{Bn}=1.5V, R_L=50Ω, C_L=35pF Figure 10, Figure 12	2.7 to 4.3		25	45	ns
t_{PD}	Propagation Delay(5)	R_L=50Ω, C_L=5pF Figure 10, Figure 13	3.3		0.25		ns
t_{BBM}	Break-Before-Make(5)	R_L=50Ω, C_L=35pF $V_{IN1=}V_{IN2=}V_{IN3=}$1.5V Figure 11	2.7 to 4.3	1	6		ns
Q	Charge Injection	$R_{GEN=}$0Ω, C_L=100pF, R_L=OPEN; $V_{GEN=}$0V Figure 14	2.7 to 4.3		9		pC
O_{IRR}	Off-Isolation	f=100 kHz, R_L=50Ω Figure 4, Figure 16	2.7 to 4.3		-70		dB
Xtalk	Non-Adjacent Channel Crosstalk	f=100 kHz, R_L=50Ω Figure 5, Figure 17	2.7 to 4.3		-100		dB
THD	Total Harmonic Distortion	R_L=600Ω, $V_{SW=}$0.5V_{pp}, f=20 Hz to 20kHz Figure 20	2.7 to 4.3		0.01		%
BW	-3db bandwidth	R_L=50Ω, C_L=0, 5pF Figure 6, Figure 15	2.7 to 4.3		150		MHz

Note:

5. Guaranteed by characterization; not tested in production.

Capacitance

Symbol	Parameter	Conditions	T_A=- 40ºC to +85ºC			Unit
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance	V_{CC}=0V		2.5		pF
C_{ON}	A/B On Capacitance	V_{CC}=3.3, f=1MHz Figure 19			55	
C_{OFFB}	Port 1Bn, 2Bn,3Bn Off Capacitance	V_{CC}=3.3, f=1MHz Figure 18			16	
C_{OFFA}	Port 1A, 2A,3A Off Capacitance	V_{CC}=3.3, f=1MHz Figure 18			20	

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Typical Performance Characteristics

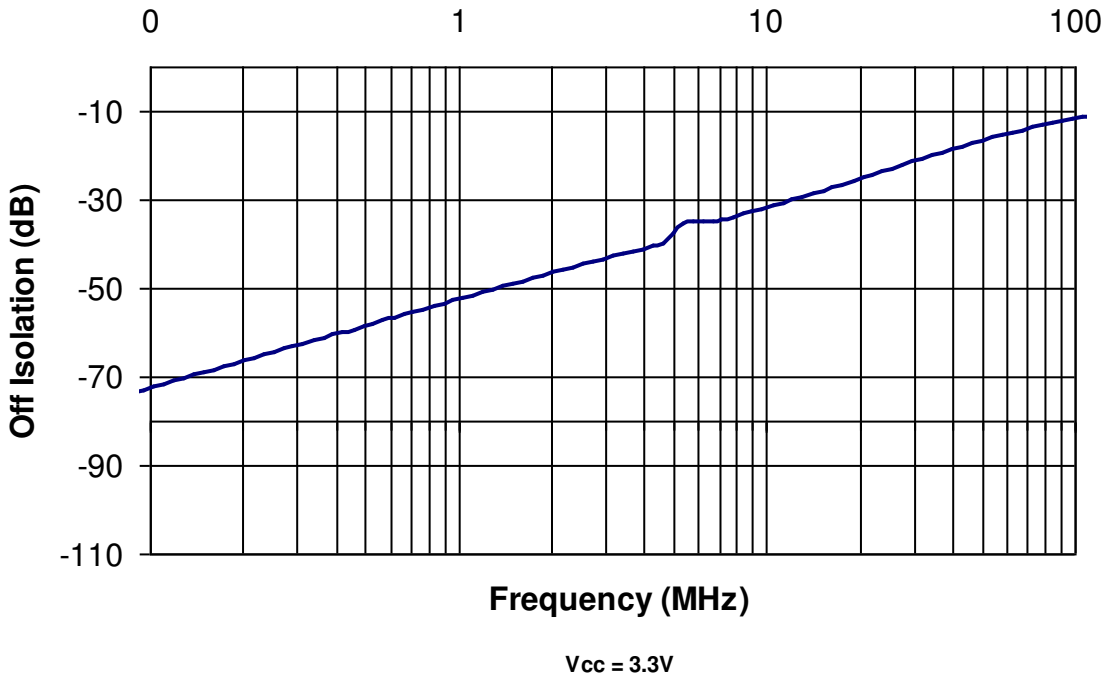


Figure 4. Off Isolation V_{CC}=3.3V, C_L=0pF

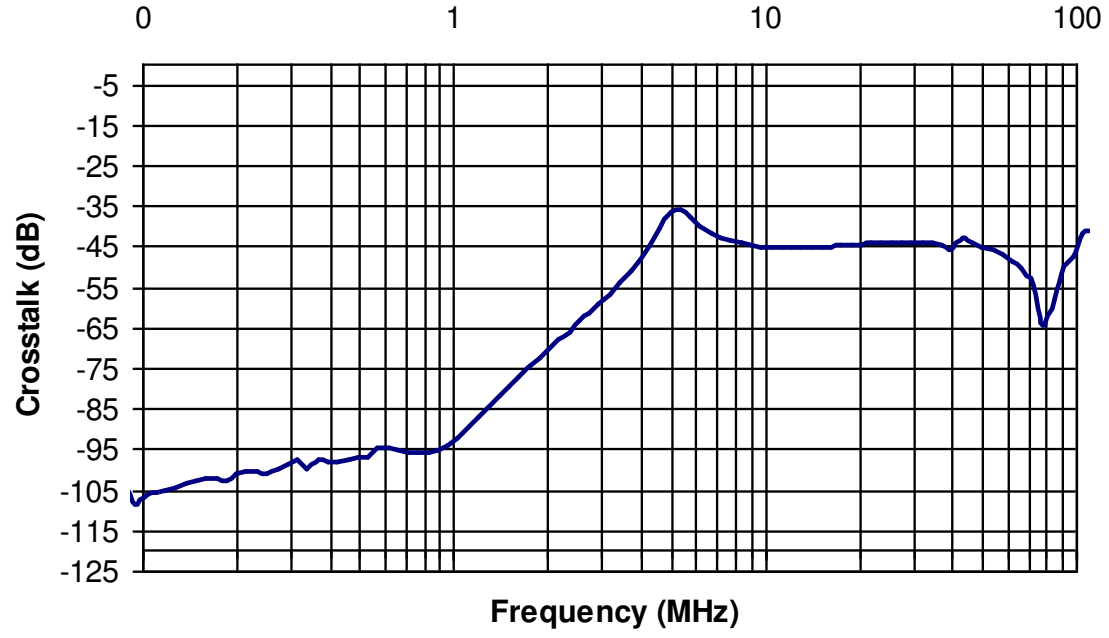


Figure 5. Non-Adjacent Crosstalk V_{CC}=3.3, C_L=0pF

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Typical Performance Characteristics (Continued)

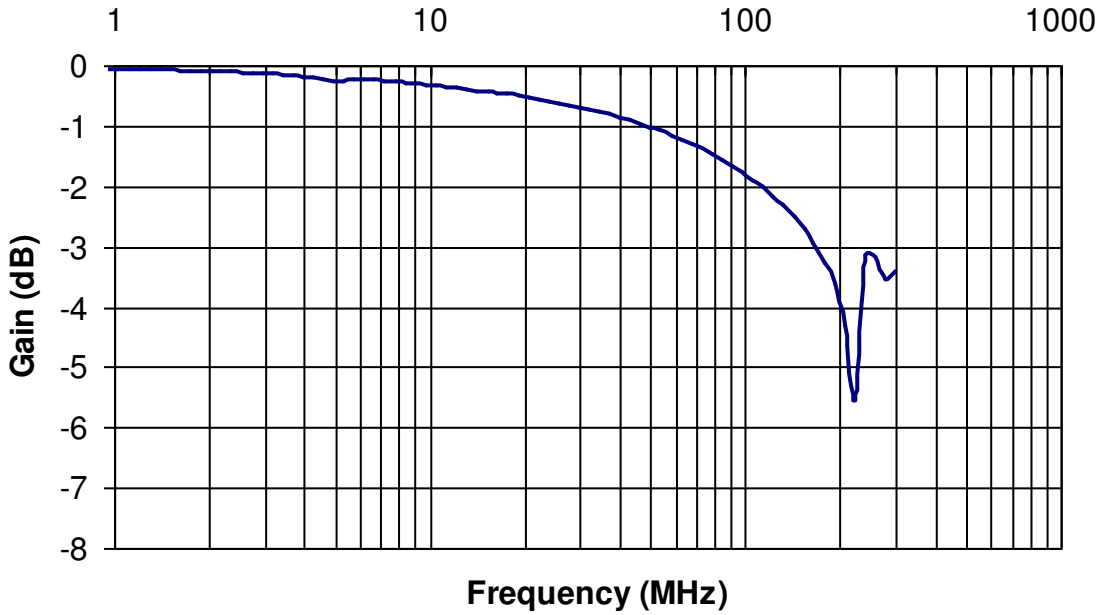


Figure 6. Bandwidth Characterization, Frequency Response at V_{CC}=3.3V, C_L=0pF

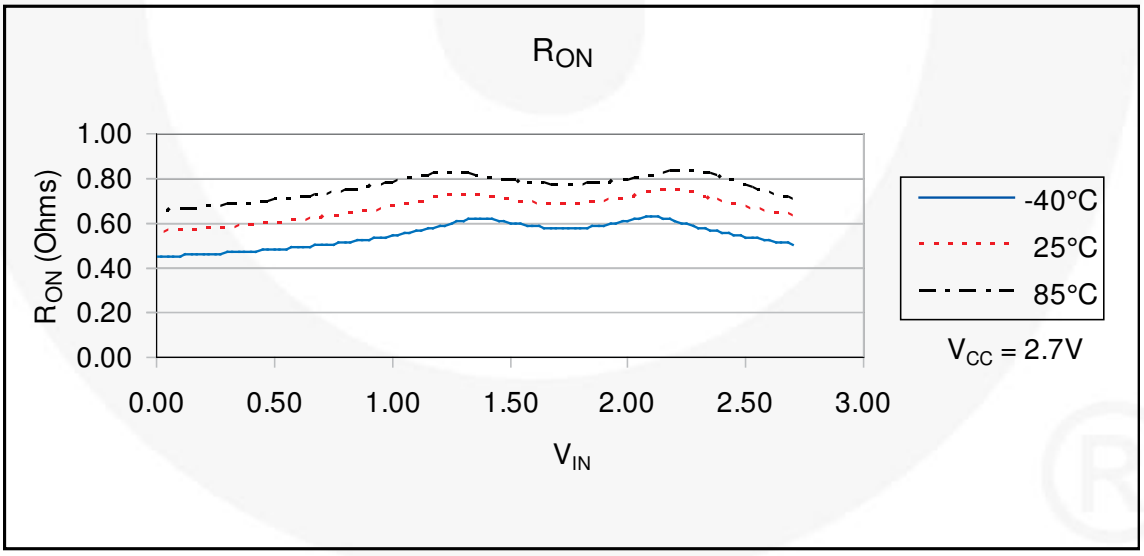
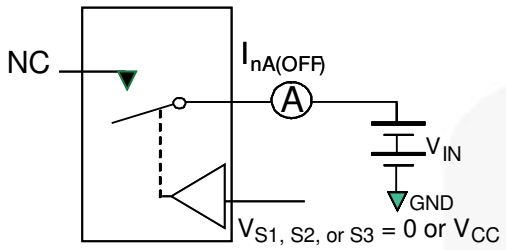


Figure 7. On Resistance

Test Diagrams



**Each switch port is tested separately

Figure 8. Off Leakage

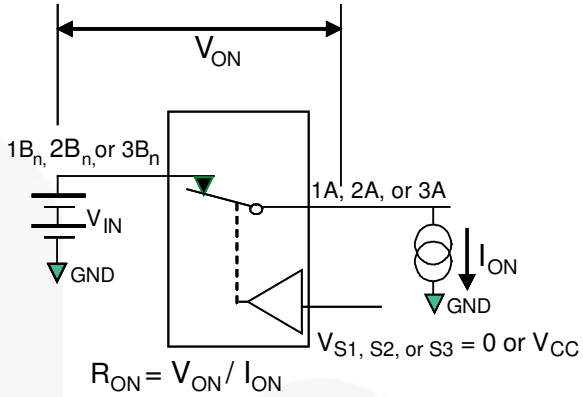
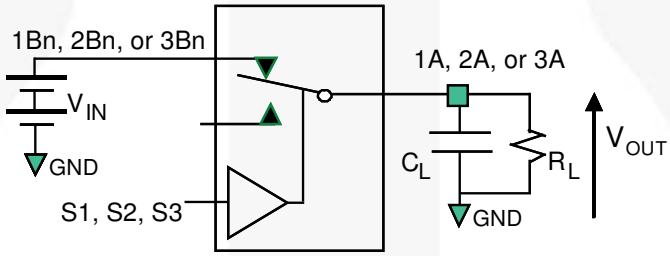
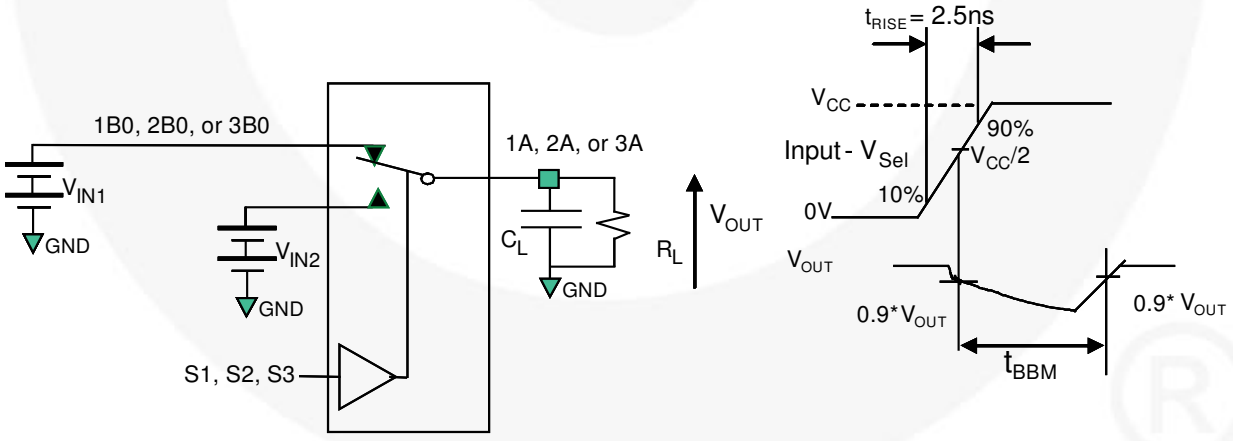


Figure 9. On Resistance



R_L and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance

Figure 10. AC Test Circuit Load



R_L and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance

Figure 11. Break-Before-Make Interval Timing

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Test Diagrams (Continued)

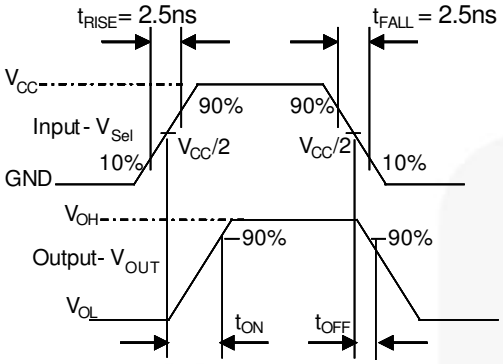


Figure 12. Turn-On / Turn-Off Waveforms

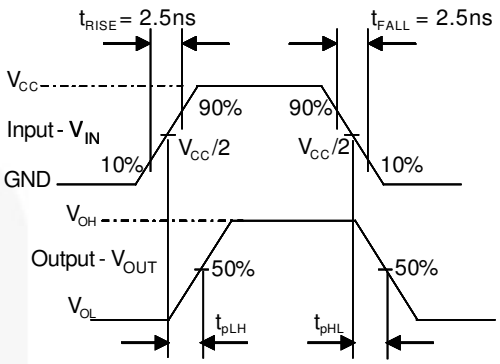


Figure 13. Switch Propagation Delay Waveforms

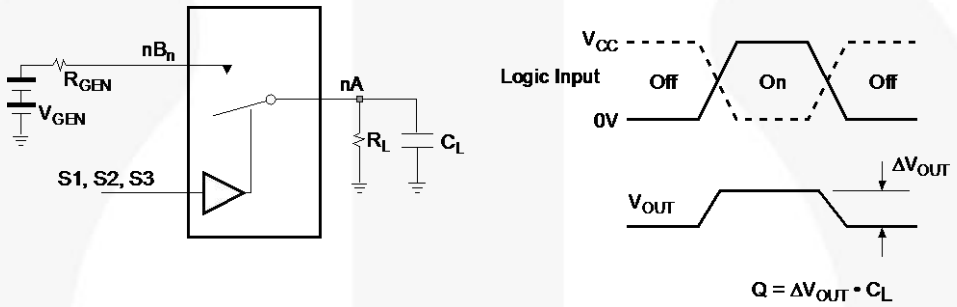
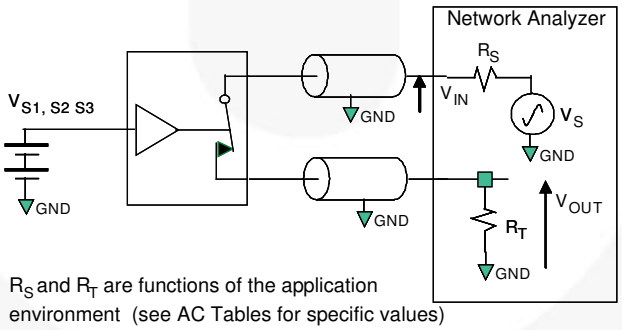
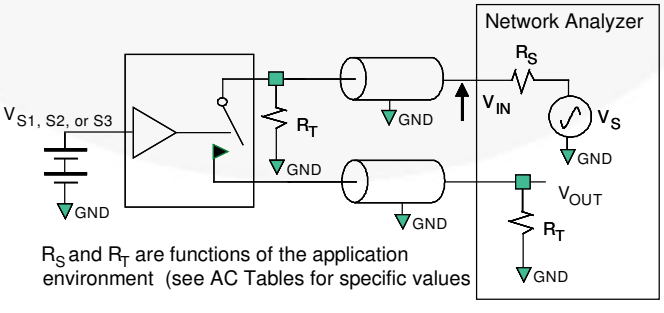


Figure 14. Charge Injection Test ($Q=\Delta V_{OUT} * C_L$)



R_S and R_T are functions of the application environment (see AC Tables for specific values)

Figure 15. Bandwidth



R_S and R_T are functions of the application environment (see AC Tables for specific values

Off -Isolation = 20 Log (V_{OUT} / V_{IN})

Figure 16. Channel Off Isolation

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Test Diagrams (Continued)

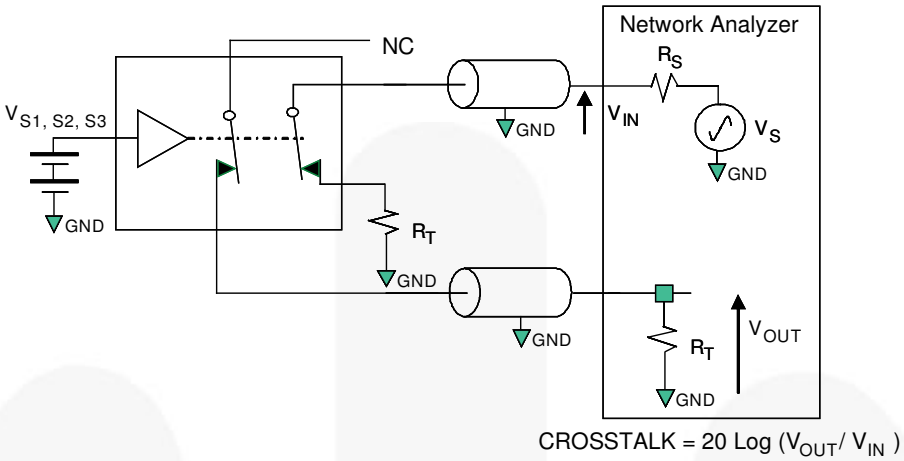


Figure 17. Non-Adjacent Channel-to-Channel Crosstalk

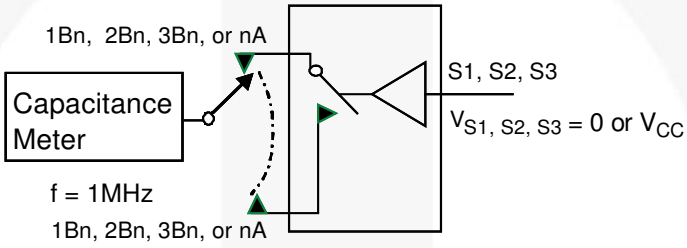


Figure 18. Channel Off Capacitance

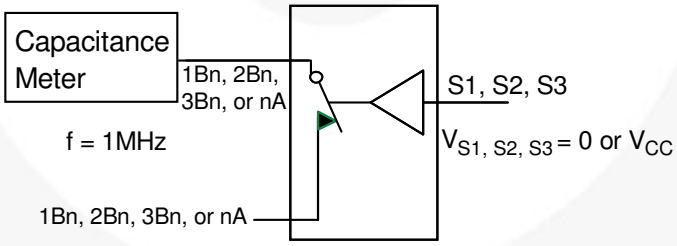


Figure 19. Channel On Capacitance

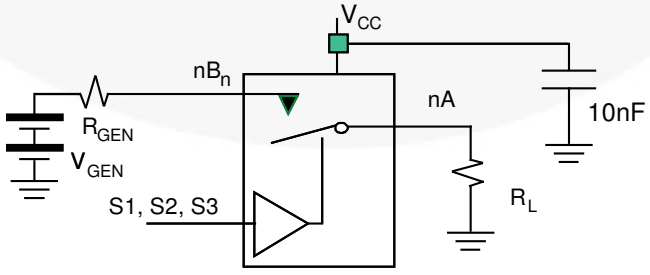
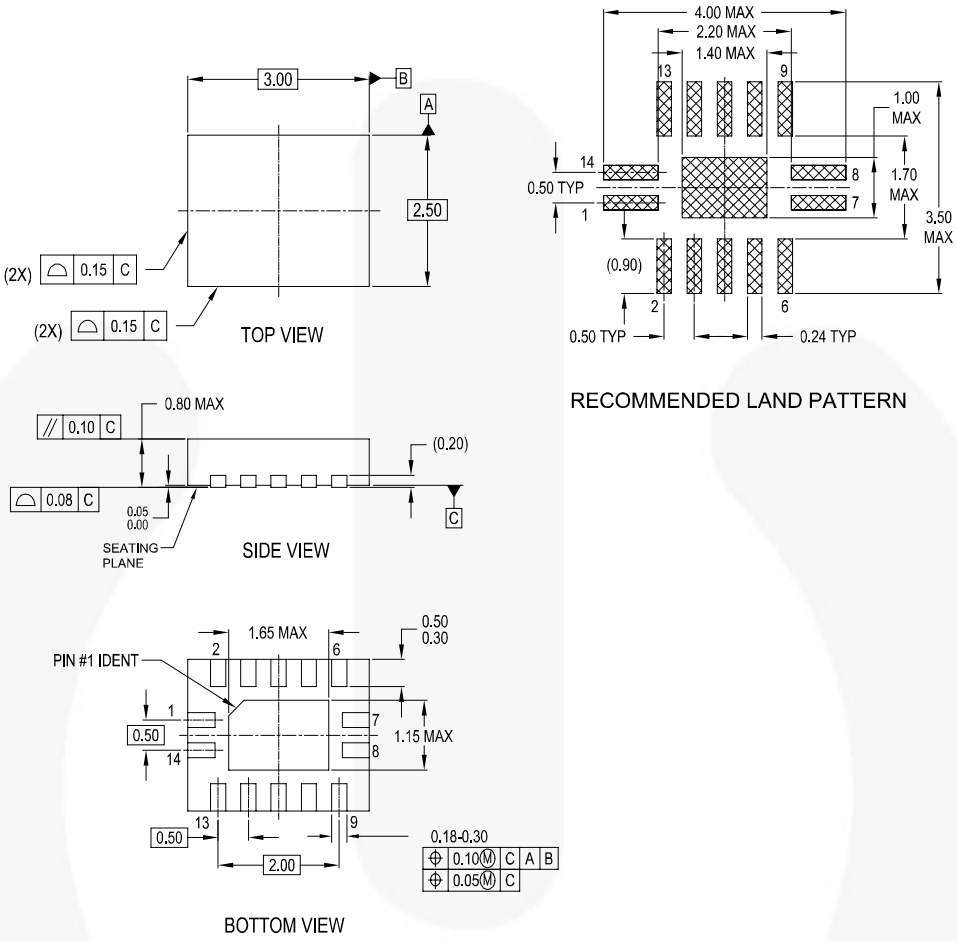


Figure 20. Total Harmonic Distortion

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Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP14ArevA

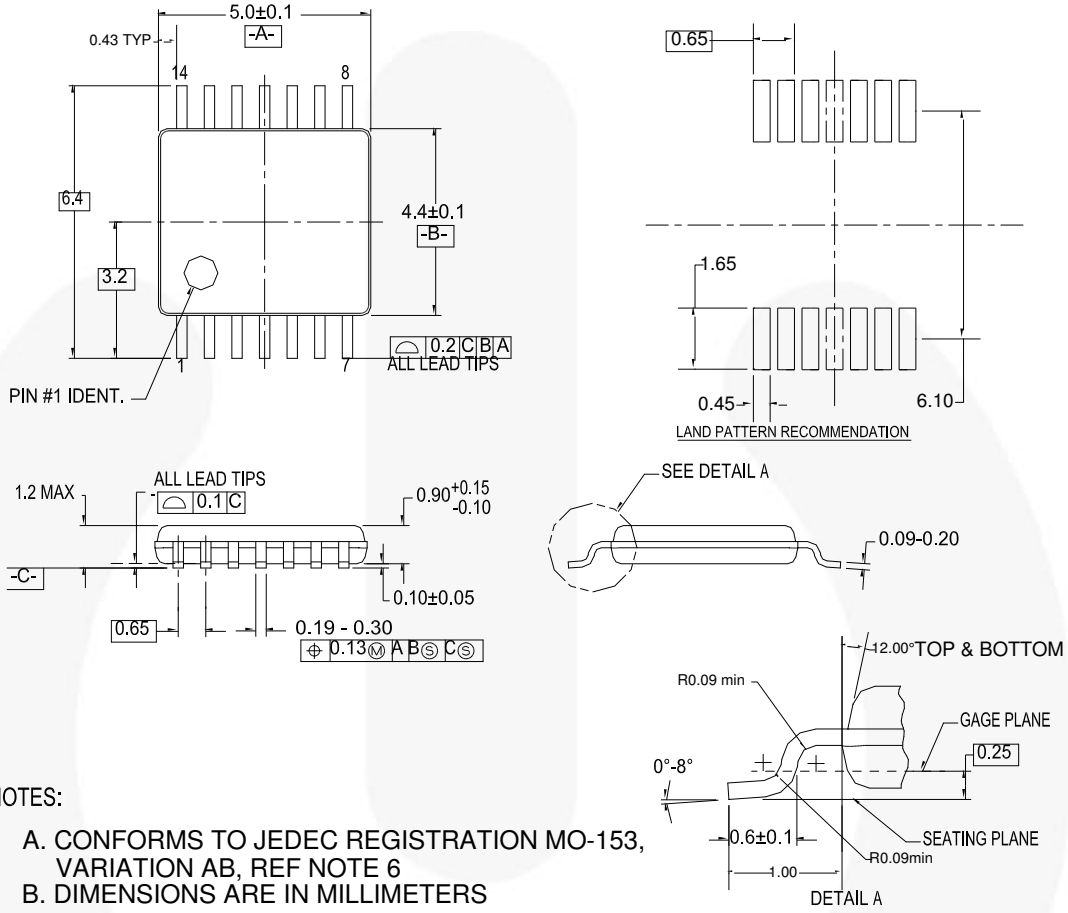
Figure 21. 14-Terminal Depopulated very thin Quad Flat-pack No leads (DQFN)

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Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6

Figure 22. 4-Lead Thin Shrink Small Outline Package (TSSOP)

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FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
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