Supertex inc.

IRF531
R531

Preliminary

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
60V	0.18Ω	12.0A	IRF531	R531

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

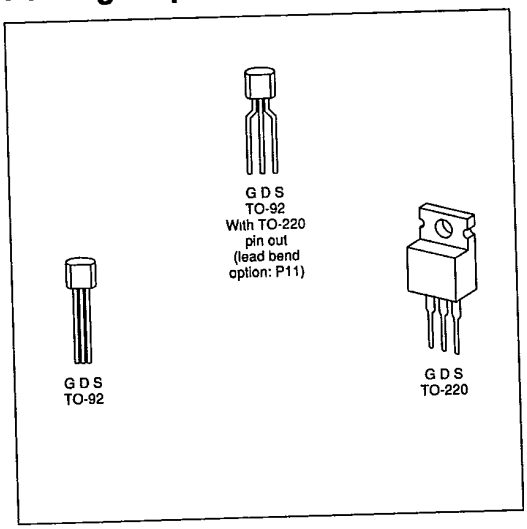
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

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Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options



Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
IRF531	14.0A	56.0A	75W	80	3.12	14.0A	56.0A
R531	1.5A	15.0A	1W	170	125	1.5A	15.0A

*I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	V_{GS} = 0, I_D = 250µA
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	V_{GS} = V_{DS}, I_D = 250µA
I_{GSS}	Gate Body Leakage			500	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			250	µA	V_{GS} = 0, V_{DS} = Max Rating
				1000		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	12.0			A	V_{GS} = 10V, V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max Rating
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.18	Ω	V_{GS} = 10V, I_D = 8.0A
G_{FS}	Forward Transconductance	4.0			℧	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max Rating, I_D = 8.0A
C_{ISS}	Input Capacitance			800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			500		
C_{RSS}	Reverse Transfer Capacitance			150		
$t_{d(ON)}$	Turn-ON Delay Time			30	ns	V_{DD} = 0.5BV_{DSS}, I_D = 4.0A, V_{DS} = 0.8 Max Rating
t_r	Rise Time			75		
$t_{d(OFF)}$	Turn-OFF Delay Time			40		
t_f	Fall Time			45		
V_{SD}	Diode Forward Voltage Drop			2.5	V	V_{GS} = 0V, I_{SD} = 1A
				2.3		V_{GS} = 0V, I_{SD} = 8A
t_{rr}	Reverse Recovery Time		360		ns	T_j = 150°C, I_F = 8.0A, $dI_{F/dt}$ = 100A/µS

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

