

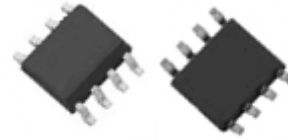
## Description

SSC4S701 is a single channel low-side gate driver, and drives a power transistor such as an IGBT and a power MOSFET. The IC has the undervoltage lockout for power supply and the overcurrent protection. When these protections are activated, the IC outputs the fault signal whose width is adjustable by an external capacitor.

The IC is provided in the compact and low profile SOIC8 package.

## Package

SOIC8



Not to scale

## Features

- Single Input and Output
- Fault Signal Output at Abnormal Condition
- Adjustable Fault Signal Output Time
- Protections
  - Undervoltage Lockout for Power Supply
  - Overcurrent Protection

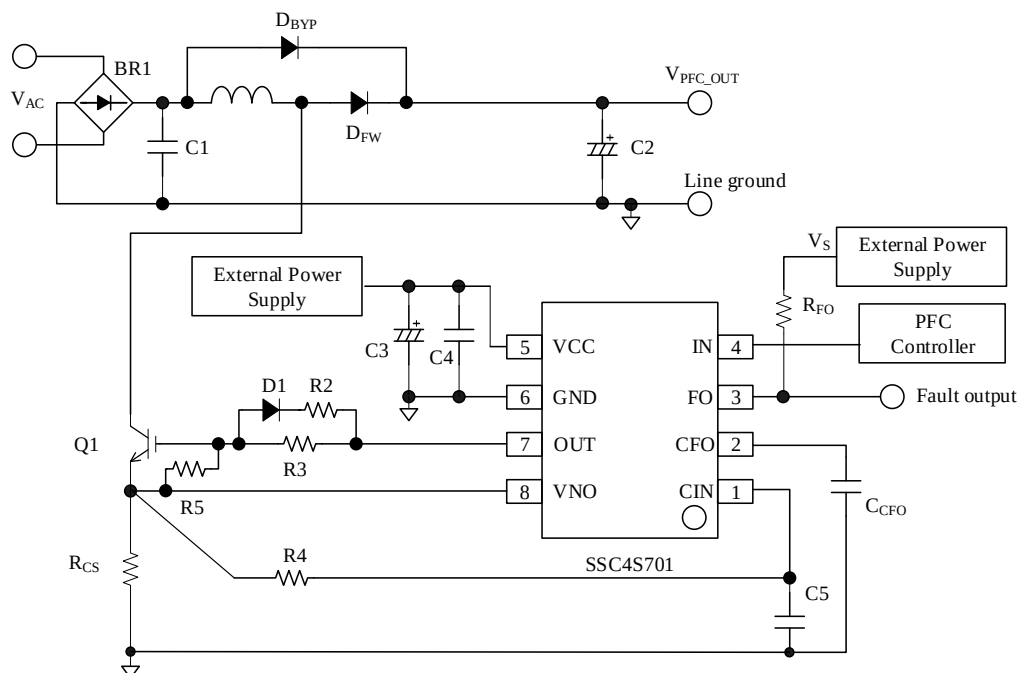
## Specifications

- Power Supply Voltage,  $V_{CC}$ : 24 V  
(Recommended Value is 15 V)
- OUT Pin Peak Source Current:  $-0.8\text{ A}$
- OUT Pin Peak Sink Current:  $1.75\text{ A}$

## Applications

- Inverter Air Conditioners
- Refrigerators
- Industrial Equipment
- Server, etc.

## Typical Application



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**1. Absolute Maximum Ratings**

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (–).

Unless otherwise specified,  $T_A = 25\text{ }^{\circ}\text{C}$ .

| Parameter                     | Symbol                | Conditions | Pins  | Rating                                         | Unit               |
|-------------------------------|-----------------------|------------|-------|------------------------------------------------|--------------------|
| CIN Pin Voltage               | $V_{\text{CIN}}$      |            | 1 – 6 | –0.3 to 7                                      | V                  |
| CFO Pin Voltage               | $V_{\text{CFO}}$      |            | 2 – 6 | –0.3 to 7                                      | V                  |
| FO Pin Voltage                | $V_{\text{FO}}$       |            | 3 – 6 | –0.3 to 7                                      | V                  |
| FO Pin Current                | $I_{\text{FO}}$       |            | 3 – 6 | 1.0                                            | mA                 |
| IN Pin Voltage                | $V_{\text{IN}}$       |            | 4 – 6 | –0.3 to 7                                      | V                  |
| VCC Pin Voltage               | $V_{\text{CC}}$       |            | 5 – 6 | –0.3 to 24                                     | V                  |
| OUT Pin Voltage               | $V_{\text{OUT}}$      |            | 7 – 6 | $V_{\text{NO}} - 0.3$ to $V_{\text{CC}} + 0.3$ | V                  |
| OUT Pin Peak Source Current   | $I_{\text{OUT(SRC)}}$ |            | 7 – 6 | –0.8                                           | A                  |
| OUT Pin Peak Sink Current     | $I_{\text{OUT(SNK)}}$ |            | 7 – 6 | 1.75                                           | A                  |
| VNO Pin Voltage               | $V_{\text{NO}}$       |            | 8 – 6 | –5 to $V_{\text{CC}} + 0.3$                    | V                  |
| Power Dissipation             | $P_D$                 |            | —     | 0.78                                           | W                  |
| Operating Ambient Temperature | $T_{\text{OP}}$       |            | —     | –40 to 100                                     | $^{\circ}\text{C}$ |
| Storage Temperature           | $T_{\text{STG}}$      |            | —     | –40 to 150                                     | $^{\circ}\text{C}$ |
| Junction Temperature          | $T_J$                 |            | —     | 150                                            | $^{\circ}\text{C}$ |

**2. Recommended Operating Range**

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (–).

Unless otherwise specified,  $T_A = 25\text{ }^{\circ}\text{C}$ .

| Parameter       | Symbol          | Conditions                    | Min. | Max. | Unit |
|-----------------|-----------------|-------------------------------|------|------|------|
| IN Pin Voltage  | $V_{\text{IN}}$ | $V_{\text{CC}} = 15\text{ V}$ | 0    | 5    | V    |
| VCC Pin Voltage | $V_{\text{CC}}$ |                               | 13.5 | 16.5 | V    |
| VNO Pin Voltage | $V_{\text{NO}}$ | $V_{\text{CC}} = 15\text{ V}$ | –5   | 5    | V    |

### 3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified,  $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 15\text{ V}$  and  $V_{NO} = 0\text{ V}$ .

| Parameter                           | Symbol        | Conditions                                                                                                                     | Pins  | Min.  | Typ.  | Max.  | Unit          |
|-------------------------------------|---------------|--------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|-------|---------------|
| <b>Power Supply Operation</b>       |               |                                                                                                                                |       |       |       |       |               |
| Operation Start Voltage             | $V_{CC(ON)}$  | The FO pin increases low- to high- level, or decreases high- to low-level.<br>$R_{FO} = 5\text{ k}\Omega$ , $V_S = 5\text{ V}$ | 5 – 6 | 11.20 | 11.90 | 12.70 | V             |
| Operation Stop Voltage              | $V_{CC(OFF)}$ |                                                                                                                                | 5 – 6 | —     | 11.40 | —     | V             |
| Operation Start Stop Hysteresis     | $V_{CC(HYS)}$ |                                                                                                                                | 5 – 6 | —     | 0.50  | —     | V             |
| Circuit Current in Operation        | $I_{CC(ON)}$  | $V_{IN} = 0\text{ V}$                                                                                                          | 5 – 6 | —     | 0.40  | 1.70  | mA            |
| Filtering Time                      | $t_{VCC\_UV}$ | $V_{CC}$ decreases 15 V to 10 V.                                                                                               | 5 – 6 | —     | 10    | —     | $\mu\text{s}$ |
| <b>CIN Pin Operation</b>            |               |                                                                                                                                |       |       |       |       |               |
| CIN Trip Voltage                    | $V_{CIN}$     | The FO pin increases low- to high- level, or decreases high- to low-level.                                                     | 1 – 6 | 0.45  | 0.50  | 0.55  | V             |
| CIN Voltage Delay Time              | $t_{CIN\_1}$  | See Figure 3-1.                                                                                                                | 1 – 6 | —     | —     | 500   | ns            |
| CIN Filtering Time                  | $t_{CIN\_2}$  | The CIN pin maximum pulse width that the FO pin does not response.<br>See Figure 3-1.                                          | 1 – 6 | 80    | 180   | 240   | ns            |
| <b>CFO Pin Operation</b>            |               |                                                                                                                                |       |       |       |       |               |
| Fault Output Time                   | $t_{WFOP}$    | $C_{CFO} = 1\text{ nF}$                                                                                                        | 2 – 6 | 75    | 110   | 180   | $\mu\text{s}$ |
| CFO Threshold Voltage               | $V_{CFH}$     | The FO pin increases low- to high- level.                                                                                      | 2 – 6 | 2.4   | 2.7   | 3.0   | V             |
| CFO Pin Source Current              | $I_{CFO}$     | $V_{CFO} = 0\text{ V}$                                                                                                         | 2 – 6 | −40   | −25   | −15   | $\mu\text{A}$ |
| <b>FO Pin Operation</b>             |               |                                                                                                                                |       |       |       |       |               |
| FO Pin High Level Output Voltage    | $V_{FOH}$     | $V_{CIN} = 0\text{ V}$ , $R_{FO} = 5\text{ k}\Omega$ ,<br>$V_S = 5\text{ V}$                                                   | 3 – 6 | 4.50  | 5.00  | —     | V             |
| FO Pin Low Level Output Voltage     | $V_{FOL}$     | $V_{CIN} = 1\text{ V}$ , $I_{FO} = 1\text{ mA}$                                                                                | 3 – 6 | —     | —     | 0.95  | V             |
| FO Pin Leakage Current              | $I_{FO}$      | $V_{CIN} = 0\text{ V}$ , $V_{FO} = 5\text{ V}$                                                                                 | 3 – 6 | —     | —     | 1.0   | $\mu\text{A}$ |
| <b>IN Pin Operation</b>             |               |                                                                                                                                |       |       |       |       |               |
| High Level Input Threshold Voltage  | $V_{INH}$     | The OUT pin increases low- to high- level.                                                                                     | 4 – 6 | —     | 2.10  | 2.60  | V             |
| Low Level Input Threshold Voltage   | $V_{INL}$     | The OUT pin decreases high- to low-level.                                                                                      | 4 – 6 | —     | 1.30  | —     | V             |
| Input Hysteresis Voltage            | $V_{INHYS}$   |                                                                                                                                | 4 – 6 | 0.35  | 0.80  | —     | V             |
| Input Pull-down Current             | $I_{IN}$      | $V_{IN} = 5\text{ V}$                                                                                                          | 4 – 6 | 0.24  | 0.33  | 0.50  | mA            |
| <b>OUT Pin Operation</b>            |               |                                                                                                                                |       |       |       |       |               |
| High Level Output Threshold Voltage | $V_{OUTH}$    | $I_{OUT} = 0\text{ mA}$                                                                                                        | 7 – 6 | 14.50 | 15.00 | —     | V             |
| Low Level Output Threshold Voltage  | $V_{OUTL}$    | $I_{OUT} = 0\text{ mA}$                                                                                                        | 7 – 6 | —     | 0.00  | 0.10  | V             |
| Turn-on Delay Matching              | $t_{dLH}$     | $C_{OUT} = 1000\text{ pF}$ ,<br>see Figure 3-2                                                                                 | 7 – 6 | —     | —     | 300   | ns            |

| Parameter                | Symbol     | Conditions                                        | Pins  | Min. | Typ. | Max. | Unit          |
|--------------------------|------------|---------------------------------------------------|-------|------|------|------|---------------|
| Turn-off Delay Matching  | $t_{dHL}$  | $C_{OUT} = 1000 \text{ pF}$ ,<br>see Figure 3-2   | 7 – 6 | —    | —    | 300  | ns            |
| Output Rise Time         | $t_r$      | $C_{OUT} = 1000 \text{ pF}$ ,<br>see Figure 3-2   | 7 – 6 | —    | —    | 150  | ns            |
| Output Fall Time         | $t_f$      | $C_{OUT} = 1000 \text{ pF}$ ,<br>see Figure 3-2   | 7 – 6 | —    | —    | 75   | ns            |
| <b>VNO Pin Operation</b> |            |                                                   |       |      |      |      |               |
| VNO Pin Current 1        | $I_{VNO1}$ | $V_{NO} = -5 \text{ V}$                           | 8 – 6 | -7.0 | -5.0 | -3.0 | mA            |
| VNO Pin Current 2        | $I_{VNO2}$ | $V_{CC} = 24 \text{ V}$ , $V_{NO} = 15 \text{ V}$ | 8 – 6 | —    | 15   | —    | $\mu\text{A}$ |

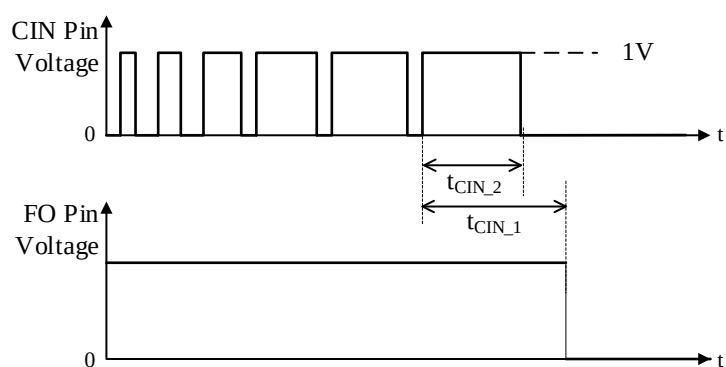


Figure 3-1. CIN Voltage Delay Time and CIN Filtering Time

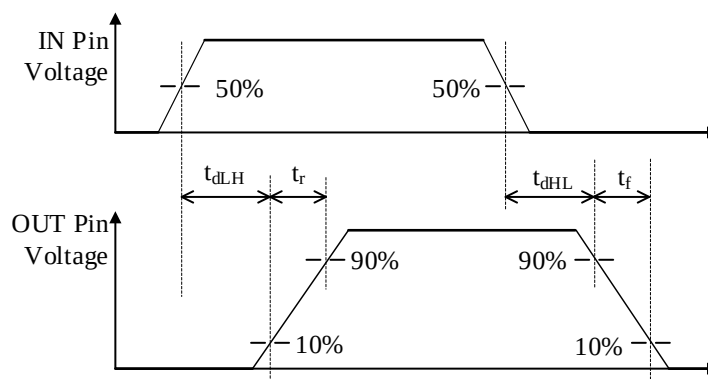


Figure 3-2. Input and Output Waveforms

## 4. Performance Curves

### 4.1. Thermal Derating Curve

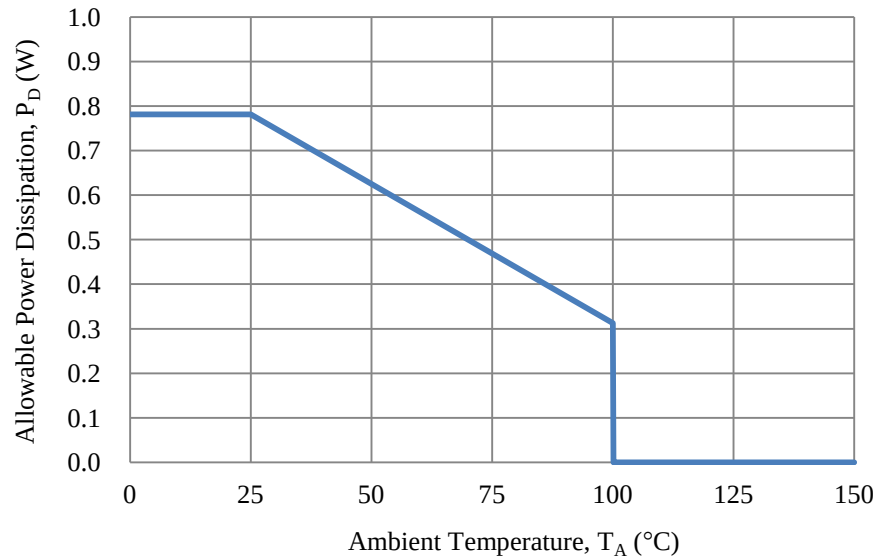
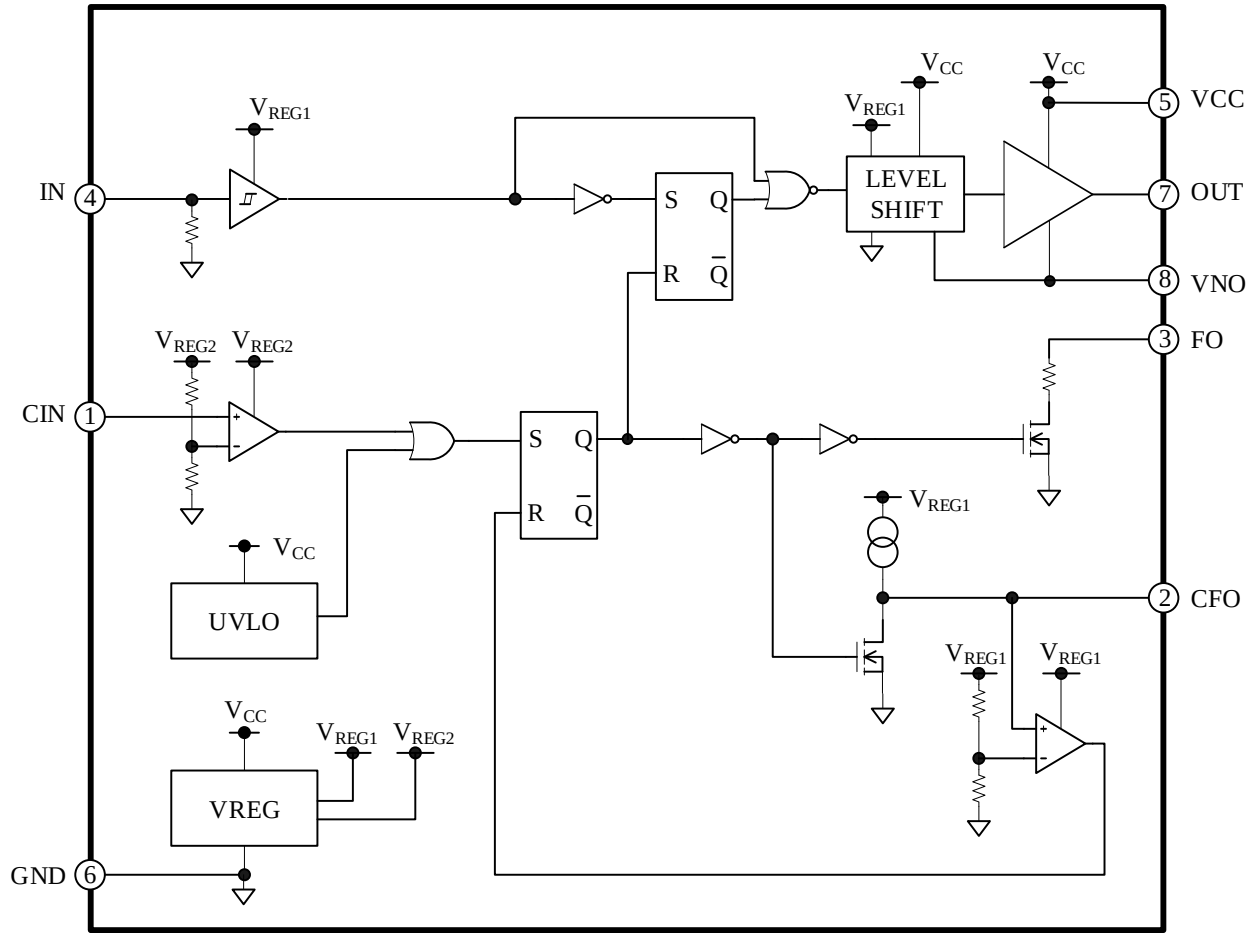
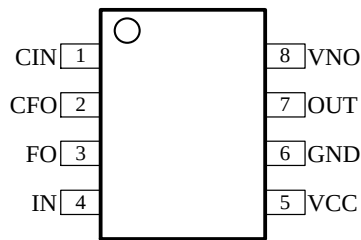


Figure 4-1. Thermal Derating Curve

5. Block Diagram



6. Pin Configuration Definitions



| Pin Number | Pin Name | Description                                                          |
|------------|----------|----------------------------------------------------------------------|
| 1          | CIN      | Input for overcurrent protection                                     |
| 2          | CFO      | Capacitor connection for setting a fault signal output time          |
| 3          | FO       | Fault signal output                                                  |
| 4          | IN       | Signal input                                                         |
| 5          | VCC      | Power supply input                                                   |
| 6          | GND      | Ground                                                               |
| 7          | OUT      | Gate drive signal output                                             |
| 8          | VNO      | Drive current return pin<br>(For example, IGBT emitter is connected) |

## 7. Typical Application

Figure 7-1 shows the PFC circuit example using the SSC4S701.

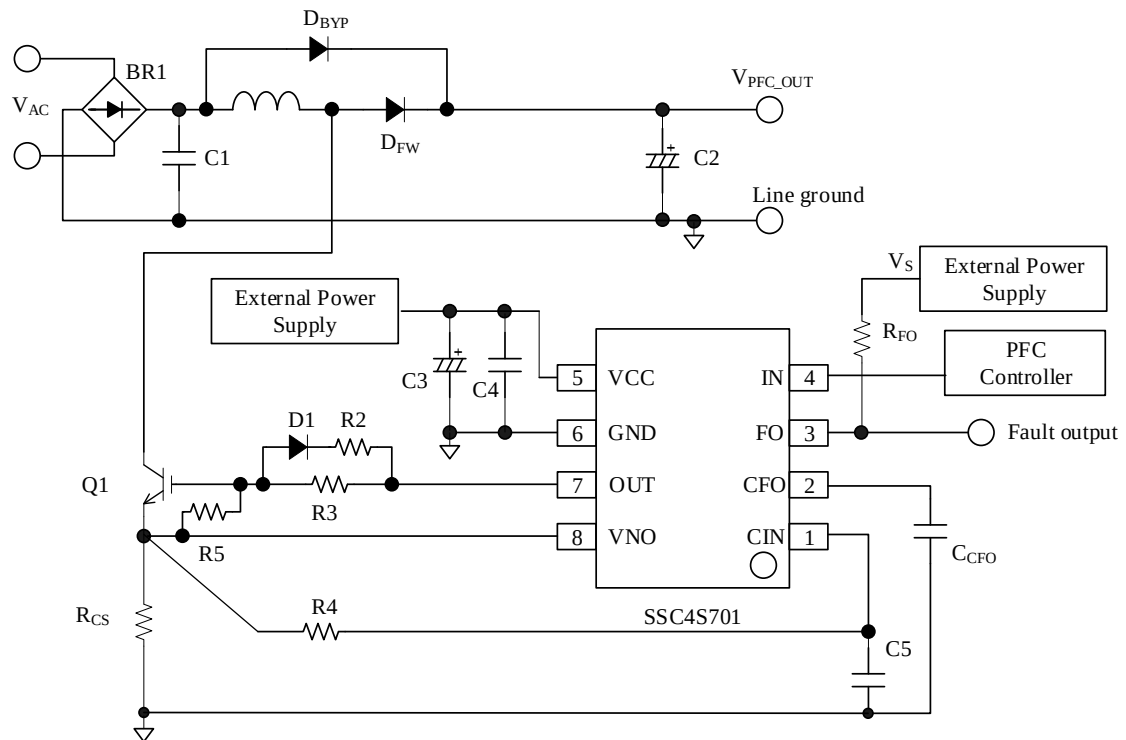
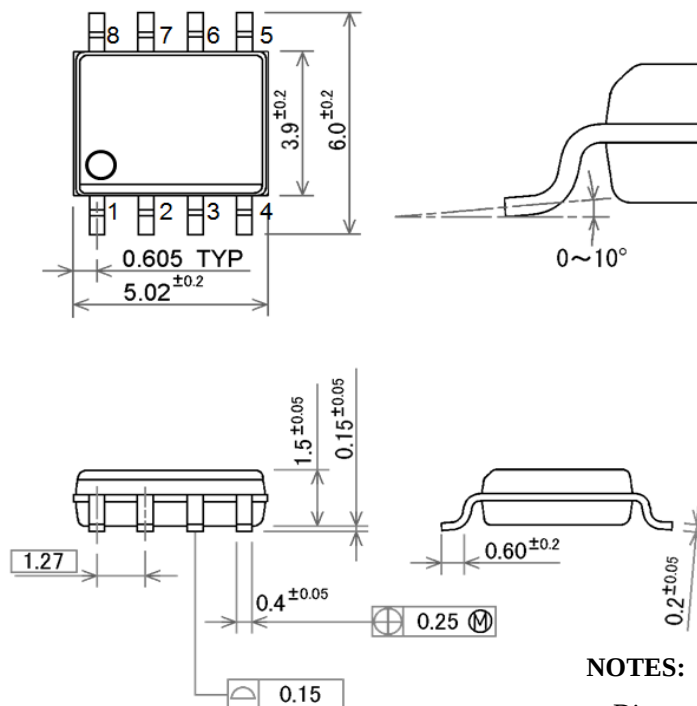


Figure 7-1. PFC Circuit Example Using SSC4S701



## 8. Physical Dimensions

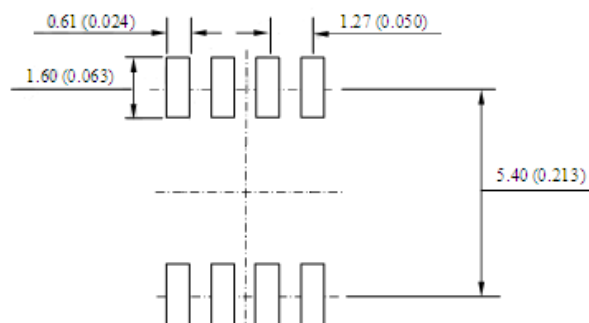
### • SOIC8 Package



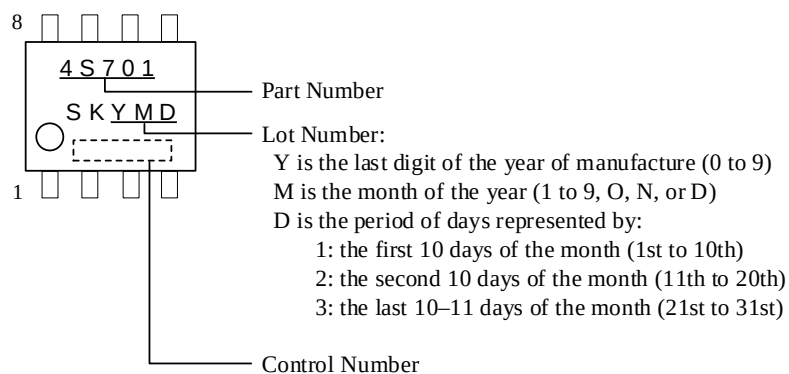
#### NOTES:

- Dimensions in millimeters
- Pb-free

### • SOIC8 Land Pattern Example



## 9. Marking Diagram



## 10. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (-).

Figure 10-1 shows the SSC4S701 peripheral circuit and the meaning of the symbols used in Section 10.

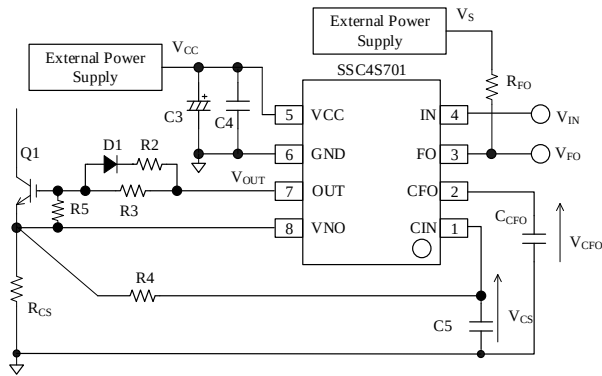


Figure 10-1. SSC4S701 Peripheral Circuit

### 10.1. Fault Signal Output

When the undervoltage lockout for power supply or the overcurrent protection is activated, the FO pin outputs the fault signal that is low level. Then, the capacitor,  $C_{CFO}$ , connected to the CFO pin is charged by the CFO Pin Source Current,  $I_{CFO}$ . When a CFO pin voltage,  $V_{CFO}$ , increases to the CFO Threshold Voltage,  $V_{CFH}$ ,  $C_{CFO}$  is discharged. If the fault condition is removed during the fault output time,  $t_{WFOP}$ , the FO pin becomes high level. Then, a OUT pin signal,  $V_{OUT}$ , operates according to an input signal,  $V_{IN}$ .

The fault output time,  $t_{WFOP}$ , is determined by the value of  $C_{CFO}$ . The approximate value of  $t_{WFOP}$  is calculated by the following equation.

$$t_{WFOP} = \frac{C_{CFO} \times V_{CFH}}{|I_{CFO}|}, \quad (1)$$

where:

$C_{CFO}$  is the CFO pin capacitor value,

$V_{CFH}$  is the CFO Threshold Voltage (= 2.7 V), and

$I_{CFO}$  is the CFO Pin Source Current (= -25  $\mu$ A).

The FO pin should be connected to an external power supply by the pull-up resistor,  $R_{FO}$ . If the external power supply voltage is 5 V,  $R_{FO}$  is about 5 k $\Omega$ .

### 10.2. Startup Operation

Figure 10-2 and Figure 10-3 show the startup waveforms. The VCC pin voltage,  $V_{CC}$ , is added from an external power supply.

While  $V_{CC}$  increases to the internal circuit start voltage from 0 V (period A described in Figure 10-2 and Figure 10-3), the FO pin voltage becomes  $V_F + V_{CC}$  (where  $V_F$  is a forward voltage of an internal protection diode). When the internal circuit operates, the FO pin becomes low level and outputs the fault signal. If  $V_{CC}$  is the Operation Start Voltage,  $V_{CC(ON)}$ , or more for the fault output time,  $t_{WFOP}$ , the IC discharges  $C_{CFO}$ , and turns the FO pin status into high (see Figure 10-2).

The approximate value of the fault output time,  $t_{WFOP}$ , is calculated by Equation (1) (see Section 10.1).

On the other hand, when  $V_{CC}$  is less than  $V_{CC(ON)}$  for the fault output time,  $t_{WFOP}$ , the IC keeps to charge  $C_{CFO}$  until  $V_{CC}$  increases to  $\geq V_{CC(ON)}$  (see Figure 10-3). When  $V_{CC}$  becomes  $\geq V_{CC(ON)}$ , the IC discharges  $C_{CFO}$ , and turns the FO pin status into high. Then, the OUT pin outputs the signals according to the IN pin signal after the next rising edge of an IN pin signal.

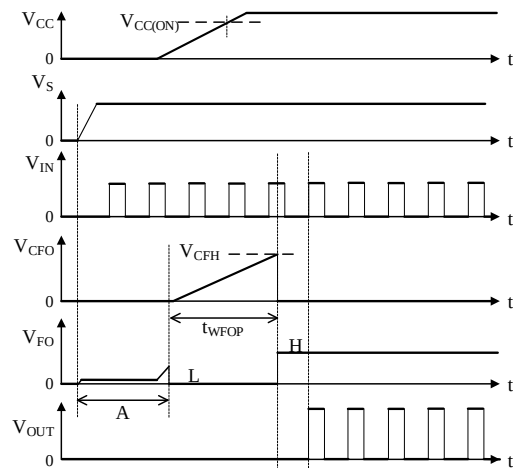


Figure 10-2. Startup Waveforms 1

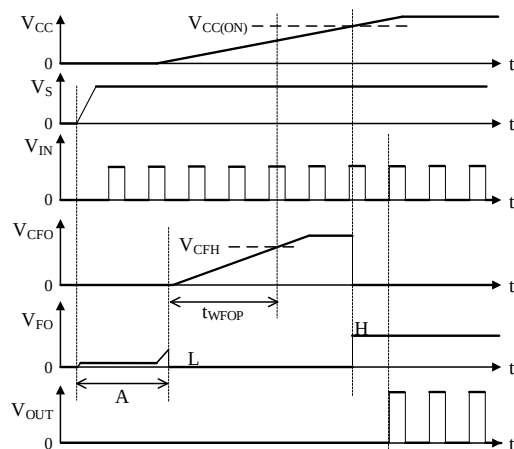


Figure 10-3. Startup Waveforms 2

### 10.3. Undervoltage Lockout for Power Supply

The undervoltage lockout (UVLO) circuit for power supply has a filter circuit to prevent the malfunction caused by the rapid decrease of the power supply, which is caused by noise, etc. The Filtering Time,  $t_{VCC\_UV}$ , is 10  $\mu$ s.

Figure 10-4 shows the UVLO operational waveforms. The UVLO is activated when all the following conditions are fulfilled.

- The VCC pin voltage,  $V_{CC}$ , decreases to the Operation Stop Voltage,  $V_{CC(OFF)}$ , or less after the IC operates.
- Then,  $V_{CC}$  remains less than the Operation Start Voltage,  $V_{CC(ON)}$  for  $t_{VCC\_UV}$ .

While the UVLO is activated, the IC turns the FO pin status into low, and stops the output of the OUT pin signal. The subsequent operations are explained in Section 10.1.

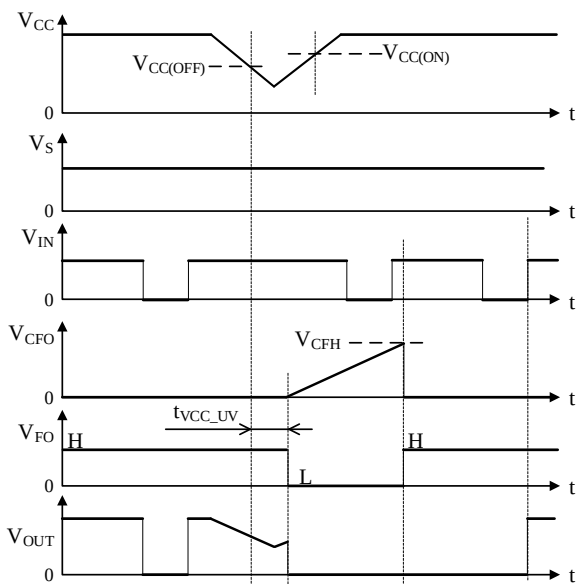


Figure 10-4. Undervoltage Lockout for Power Supply Operational Waveforms

### 10.4. Overcurrent Protection

The CIN pin is the input of overcurrent signals. When the CIN pin detects the voltage of  $\geq V_{CIN}$  for  $\geq t_{CIN\_2}$ , the overcurrent protection is activated after  $t_{CIN\_1}$ . Where:  $V_{CIN}$  is the CIN Trip Voltage of 0.50 V,  $t_{CIN\_2}$  is the CIN Filtering Time of 180 ns, and  $t_{CIN\_1}$  is the CIN Voltage Delay Time of 500 ns (max.).

While the overcurrent protection is activated, the IC turns the FO pin status into low, and stops the output of the OUT pin signal. When the CIN pin voltage decreases to  $< V_{CIN}$  for the fault output time,  $t_{WFOP}$ , from overcurrent protection activation, the IC discharges  $C_{CFO}$ ,

and turns the FO pin status into high (see Figure 10-5). The approximate value of  $t_{WFOP}$  is calculated by Equation (1) (see Section 10.1).

On the other hand, when the CIN pin voltage is more than  $V_{CIN}$  for  $t_{WFOP}$ , the IC keeps to charge  $C_{CFO}$  until the CIN pin voltage decreases to  $< V_{CIN}$  (see Figure 10-6). When the CIN pin voltage becomes  $< V_{CIN}$ , the IC discharges  $C_{CFO}$ , and turns the FO pin status into high. Then, the OUT pin outputs the signals according to the IN pin signal after the next rising edge of an IN pin signal.

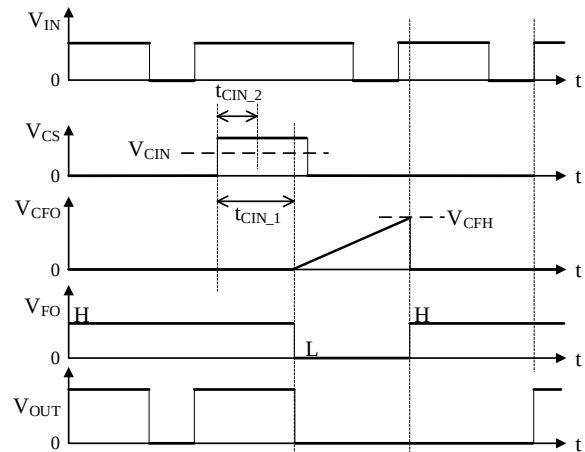


Figure 10-5. Overcurrent Protection Operational Waveforms 1

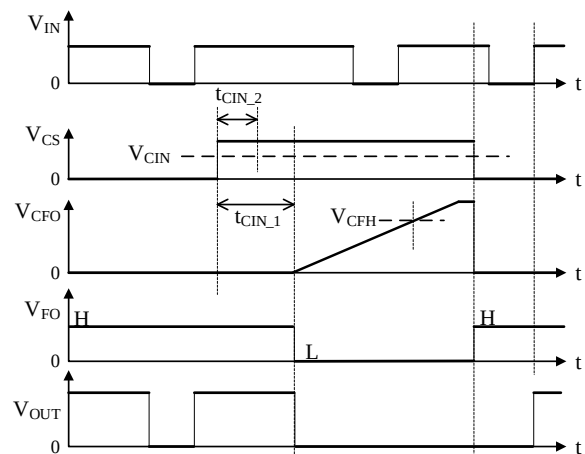


Figure 10-6. Overcurrent Protection Operational Waveforms 2

## Important Notes

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