SYNCHRONOUS BURST SRAM PIPELINED OUTPUT

128K x 32 SRAM

+3.3V SUPPLY, PIPELINED, SINGLE CYCLE DESELECT, BURST COUNTER

FEATURES

- Fast access times: 4.8, 5, 6, and 7ns
- Fast clock speed: 100, 83, and 66MHz
- Provide high performance 3-1-1-1 access rate
- Fast OE# access times: 5, 6, and 7ns
- Optimal for depth expansion (one cycle chip deselect to eliminate bus contention)
- Single +3.3V -5% and +10%power supply
- Support +2.5V I/O
- 5V tolerant inputs except I/O's
- Clamp diodes to VSSQ at all outputs
- Common data inputs and data outputs
- BYTE WRITE ENABLE and GLOBAL WRITE control
- Three chip enables for depth expansion and address pipeline
- Address, control, input, and output pipeline registers
- Internally self-timed WRITE CYCLE
- Burst control pins (interleaved or linear burst sequence)
- Automatic power-down for portable applications
- High density, high speed packages
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS / MARKING

• Timing		
4.8ns access/10ns cycle	-4	
5ns access/10ns cycle	-5	
6ns access/12ns cycle	-6	
7ns access/15ns cycle	-7	
• Packages		
100-pin TQFP	T	
• Temperature		
Commercial	None	(0°C to 70°C)
Industrial	I	(-40°C to 85°C)

GENERAL DESCRIPTION

The Galvantech Synchronous Burst SRAM family employs high-speed, low power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

The GVT71128D32 SRAM integrates 131,072x32 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable (CE#), depth-expansion chip enables (CE2# and CE2), burst control inputs (ADSC#, ADSP#, and ADV#), write enables (BW1#, BW2#, BW3#, BW4#,and BWE#), and global write (GW#).

Asynchronous inputs include the output enable (OE#) and burst mode control (MODE). The data outputs (Q), enabled by OE#, are also asynchronous.

Addresses and chip enables are registered with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Address, data inputs, and write controls are registered on-chip to initiate self-timed WRITE cycle. WRITE cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. BW1# controls DQ1-DQ8. BW2# controls DQ9-DQ16. BW3# controls DQ17-DQ24. BW4# controls DQ25-DQ32. BW1#, BW2# BW3#, and BW4# can be active only with BWE# being LOW. GW# being LOW causes all bytes to be written. This device also incorporates pipelined enable circuit for easy depth expansion without penalizing system performance.

The GVT71128D32 operates from a +3.3V power supply. All inputs and outputs are TTL-compatible. The device is ideally suited for 486, Pentium™, 680x0, and PowerPC™ systems and for systems that are benefited from a wide synchronous data bus.

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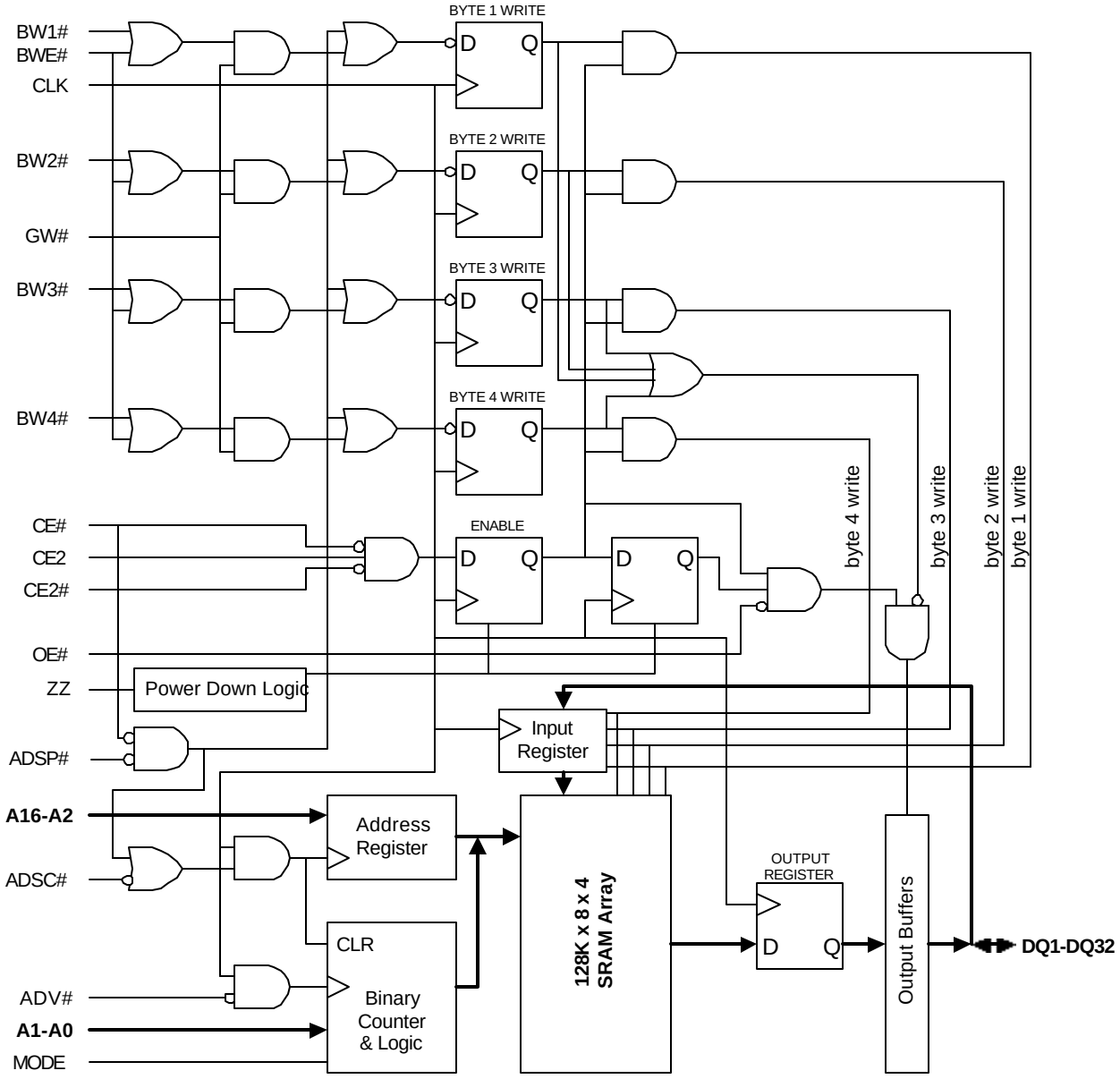
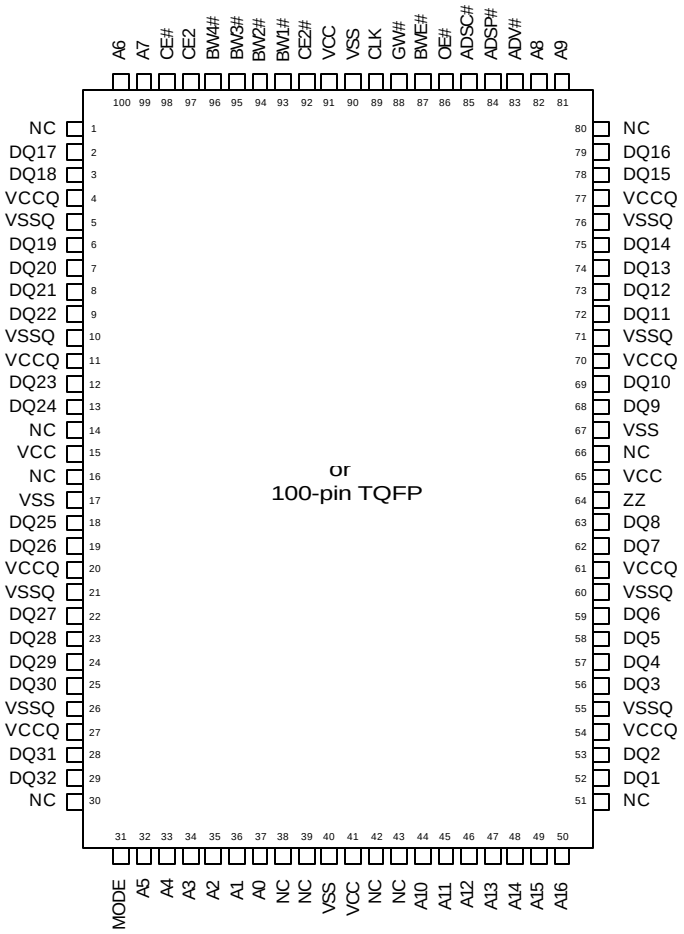
Rev. 11/99

FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN ASSIGNMENT (Top View)



PIN DESCRIPTIONS

QFP PINS	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50	A0-A16	Input-Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
93,94,95,96	BW1#, BW2#, BW3#, BW4#	Input-Synchronous	Byte Write: A byte write is LOW for a WRITE cycle and HIGH for a READ cycle. BW1# controls DQ1-DQ8. BW2# controls DQ9-DQ16. BW3# controls DQ17-DQ24. BW4# controls DQ25-DQ32. Data I/O are high impedance if either of these inputs are LOW, conditioned by BWE# being LOW.
87	BWE#	Input-Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the setup and hold times around the rising edge of CLK.
88	GW#	Input-Synchronous	Global Write: This active LOW input allows a full 32-bit WRITE to occur independent of the BWE# and BWn# lines and must meet the setup and hold times around the rising edge of CLK.
89	CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	CE#	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device and to gate ADSP#.
92	CE2#	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device.

PIN DESCRIPTIONS (continued)

QFP PINS	SYMBOL	TYPE	DESCRIPTION
97	CE2	input-Synchronous	Chip enable: This active HIGH input is used to enable the device.
86	OE#	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
83	ADV#	Input-Synchronous	Address Advance: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
84	ADSP#	Input-Synchronous	Address Status Processor: This active LOW input, along with CE# being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
85	ADSC#	Input-Synchronous	Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
31	MODE	Input-Static	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST.
64	ZZ	Input-Asynchro-nous	Snooze: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (No Connect).
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72-75, 78, 79, 2, 3, 6-9, 12, 13, 18, 19, 22-25, 28, 29	DQ1-DQ32	Input/ Output	Data Inputs/Outputs: First Byte is DQ1-DQ8. Second Byte is DQ9-DQ16. Third Byte is DQ17-DQ24. Fourth Byte is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
15, 41, 65, 91	VCC	Supply	Power Supply: +3.3V -5% to +10%. Pin 14 does not have to be connected directly to VCCas long as it is greater than VIH.
17, 40, 67, 90	VSS	Ground	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	VCCQ	I/O Supply	Output Buffer Supply: +3.3V -5% to +10%. For 2.5V I/O: 2.375V to VCC.
5, 10, 21, 26, 55, 60, 71, 76	VSSQ	I/O Ground	Output Buffer Ground: GND
1, 14, 16, 30, 38, 39, 42, 43, 50, 51, 66, 80	NC	-	No Connect: These signals are not internally connected.

BURST ADDRESS TABLE (MODE = NC/VCC)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

BURST ADDRESS TABLE (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

PARTIAL TRUTH TABLE FOR READ/WRITE

FUNCTION	GW#	BWE#	BW1#	BW2#	BW3#	BW4#
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE one byte	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

TRUTH TABLE

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ADSP#	ADSC#	ADV#	WRITE#	OE#	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Note:
1. X means “don’t care.” H means logic HIGH. L means logic LOW. WRITE# = L means [BWE# + BW1#*BW2#*BW3#*BW4#]*GW# equals LOW. WRITE# = H means [BWE# + BW1#*BW2#*BW3#*BW4#]*GW# equals HIGH.
2. BW1# enables write to DQ1-DQ8. BW2# enables write to DQ9-DQ16. BW3# enables write to DQ17-DQ24. BW4# enables write to DQ25-DQ32.
3. All inputs except OE# must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Suspending burst generates wait cycle.
5. For a write operation following a read operation, OE# must be HIGH before the input data required setup time plus High-Z time for OE# and staying HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. ADSP# LOW along with chip being selected always initiates an READ cycle at the L-H edge of CLK. A WRITE cycle can be performed by setting WRITE# LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.....-0.5V to +4.6V
V_{IN} .....-0.5V to VCC+0.5V
Storage Temperature (plastic) .....-55°C to +150°
Junction Temperature .....+150°
Power Dissipation 1.0W
Short Circuit Output Current 50mA

*Stresses greater than those listed uunder "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(All Temperature Ranges; VCC = 3.3V -5 to +10% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data Inputs (DQxx)	V_{IHD}	2.0	VCCQ+0.3	V	1,2
	All Other Inputs	V_{IH}	2.0	4.6	V	1,2
Input Low (Logic 0) Voltage		V_{Il}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq VCC$	IL_I	-2	2	uA	14
Output Leakage Current	Output(s) disabled, $0V \leq V_{OUT} \leq VCC$	IL_O	-2	2	uA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1, 11
Supply Voltage		VCC	3.1	3.6	V	1
I/O Supply Voltage (3.3V I/O)		VCCQ	3.1	3.6	V	1
I/O Supply Voltage (2.5V I/O)		VCCQ	2.375	VCC	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	-4	-5	-6	-7	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; cycle time $\geq {}^tKC$ MIN; VCC =MAX; outputs open	Icc	80	225	225	185	120	mA	3, 12, 13
CMOS Standby	Device deselected; VCC = MAX; all inputs $\leq$ VSS +0.2 or $\geq$VCC -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	12,13
TTL Standby	Device deselected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; all inputs static; VCC = MAX; CLK frequency = 0	I_{SB3}	8	18	18	18	18	mA	12,13
Clock Running	Device deselected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; VCC = MAX; CLK cycle time $\geq {}^tKC$ MIN	I_{SB4}	12	30	30	25	20	mA	12,13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz VCC = 3.3V	C_I	3	4	pF	4
Input/Output Capacitance (DQ)		C_O	6	7	pF	4

THERMAL CONSIDERATION

DESCRIPTION	CONDITIONS	SYMBOL	TQFP TYP	UNITS	NOTES
Thermal Resistance - Junction to Ambient	Still air, soldered on 4.25 x 1.125 inch 4-layer PCB	Θ_{JA}	20	°C/W	
Thermal Resistance - Junction to Case		Θ_{JC}	1	°C/W	

AC ELECTRICAL CHARACTERISTICS

(Note 5) (All Temperature Ranges; VCC = 3.3V -5 to +10%)

DESCRIPTION		-4		-5		-6		-7			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock											
Clock cycle time	^tKC	10		10		12		15		ns	
Clock HIGH time	^tKH	4		4		4		5		ns	
Clock LOW time	^tKL	4		4		4		5		ns	
Output Times											
Clock to output valid	^tKQ		4.8		5		6		7	ns	
Clock to output invalid	^tKQX	2		2		2		2		ns	
Clock to output in Low-Z	^tKQLZ	3		3		3		3		ns	6,7
Clock to output in High-Z	^tKQHZ		5		5		5		6	ns	6,7
OE to output valid	^tOEQ		5		5		6		7	ns	9
OE to output in Low-Z	^tOELZ	0		0		0		0		ns	6,7
OE to output in High-Z	^tOEHZ		4		4		5		6	ns	6,7
Setup Times											
Address, Controls and Data In	^tS	2.0		2.5		2.5		2.5		ns	10
Hold Times											
Address, Controls and Data In	^tH	0.5		0.5		0.5		0.5		ns	10

CAPACITANCE DERATING

DESCRIPTION	SYMBOL	TYP	MAX	UNITS	NOTES
Clock to output valid	$\Delta\ ^tKQ$	0.016		ns / pF	15

AC TEST CONDITIONS FOR 3.3V I/O

Input pulse levels	0V to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

AC TEST CONDITIONS FOR 2.5V I/O

Input pulse levels	0V to 2.5V
Input slew rate	1.0V/ns
Output rise and fall times(max)	1.8ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Output load	See Figures 3

OUTPUT LOADS FOR 3.3V I/O

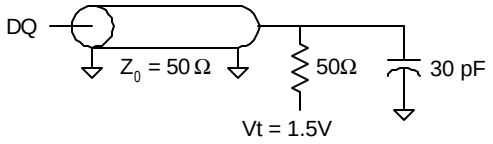


Fig. 1 OUTPUT LOAD EQUIVALENT

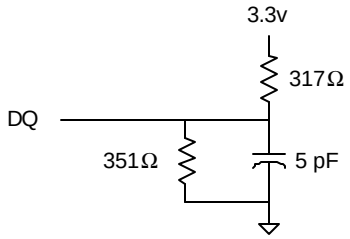


Fig. 2 OUTPUT LOAD EQUIVALENT

OUTPUT LOADS FOR 2.5V I/O

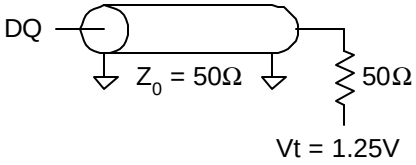
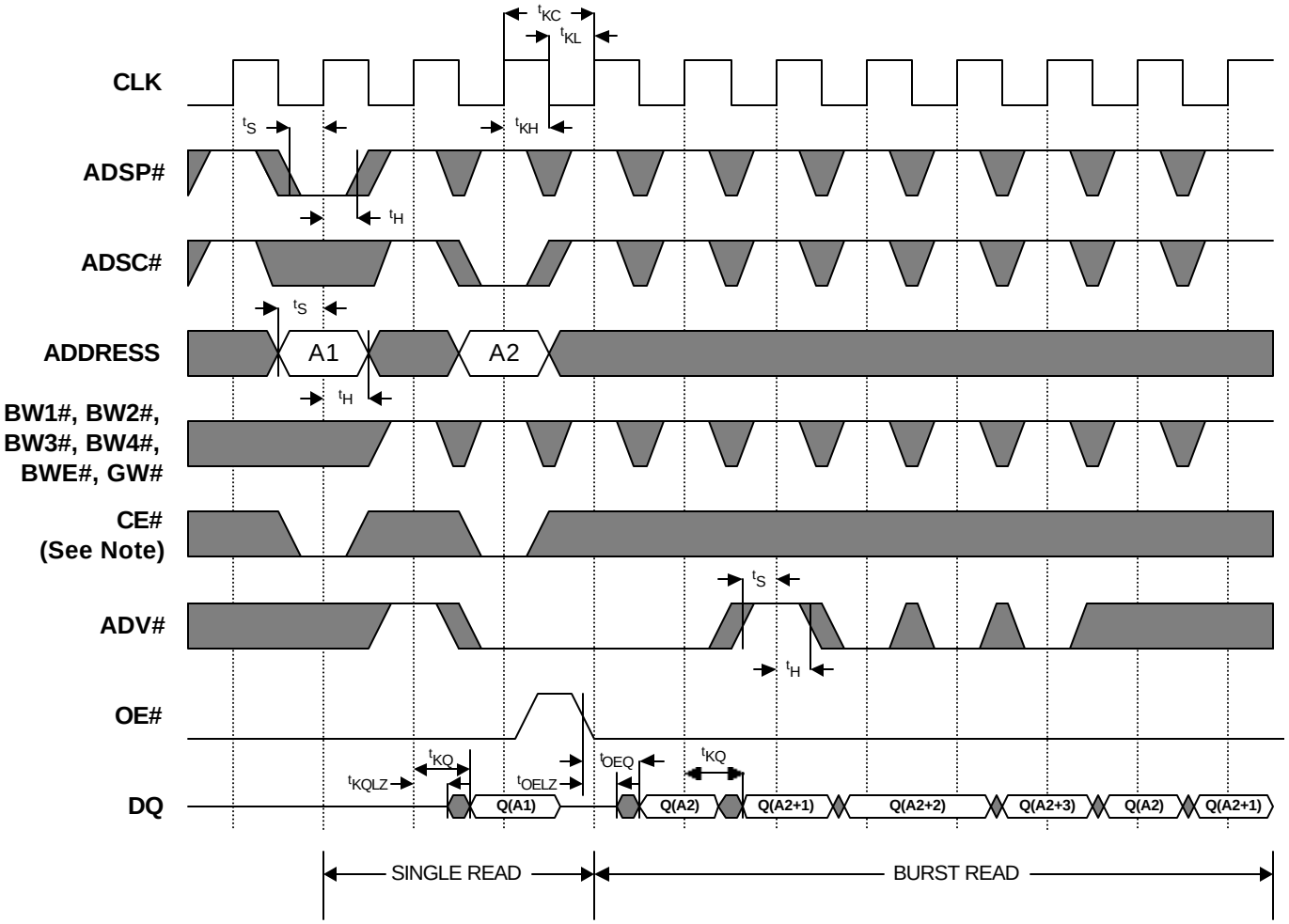


Fig. 3 OUTPUT LOAD EQUIVALENT

NOTES

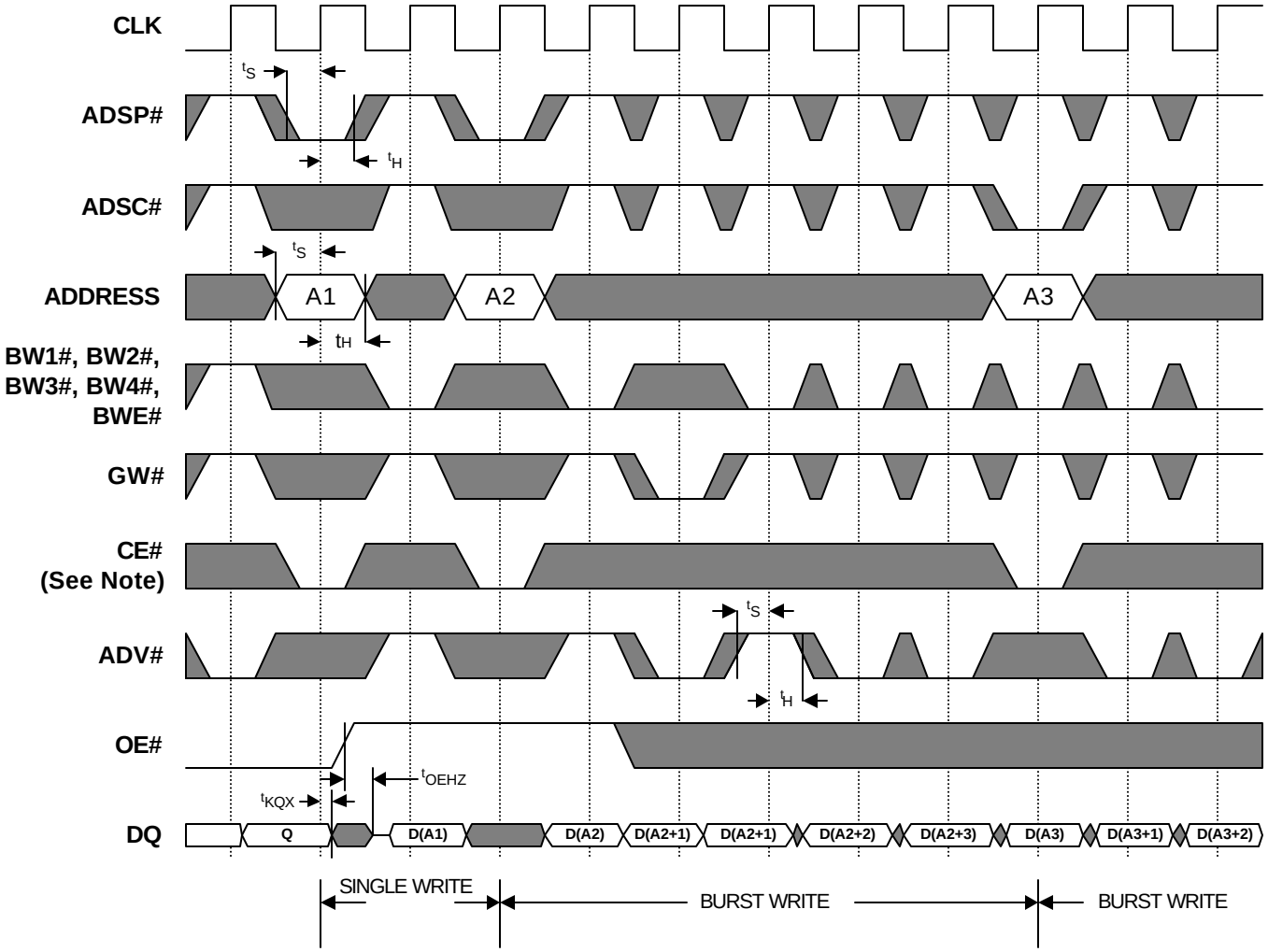
1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tKC/2$
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL=5pF as in Fig. 2.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or ADSP# LOW along with chip enables being active for the required setup and hold times. A WRITE cycle is defined by at one byte or all byte WRITE per READ/WRITE TRUTH TABLE.
9. OE# is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for "don't care" as defined in the truth table.
11. AC I/O curves are available upon request.
12. "Device Deselected" means the device is in POWER -DOWN mode as defined in the truth table. "Device Selected" means the device is active.
13. Typical values are measured at 3.3V, 25ºC and 20ns cycle time.
14. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±30 µA.
15. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1 or Fig. 3, for 3.3V or 2.5V I/O respectively

READ TIMING



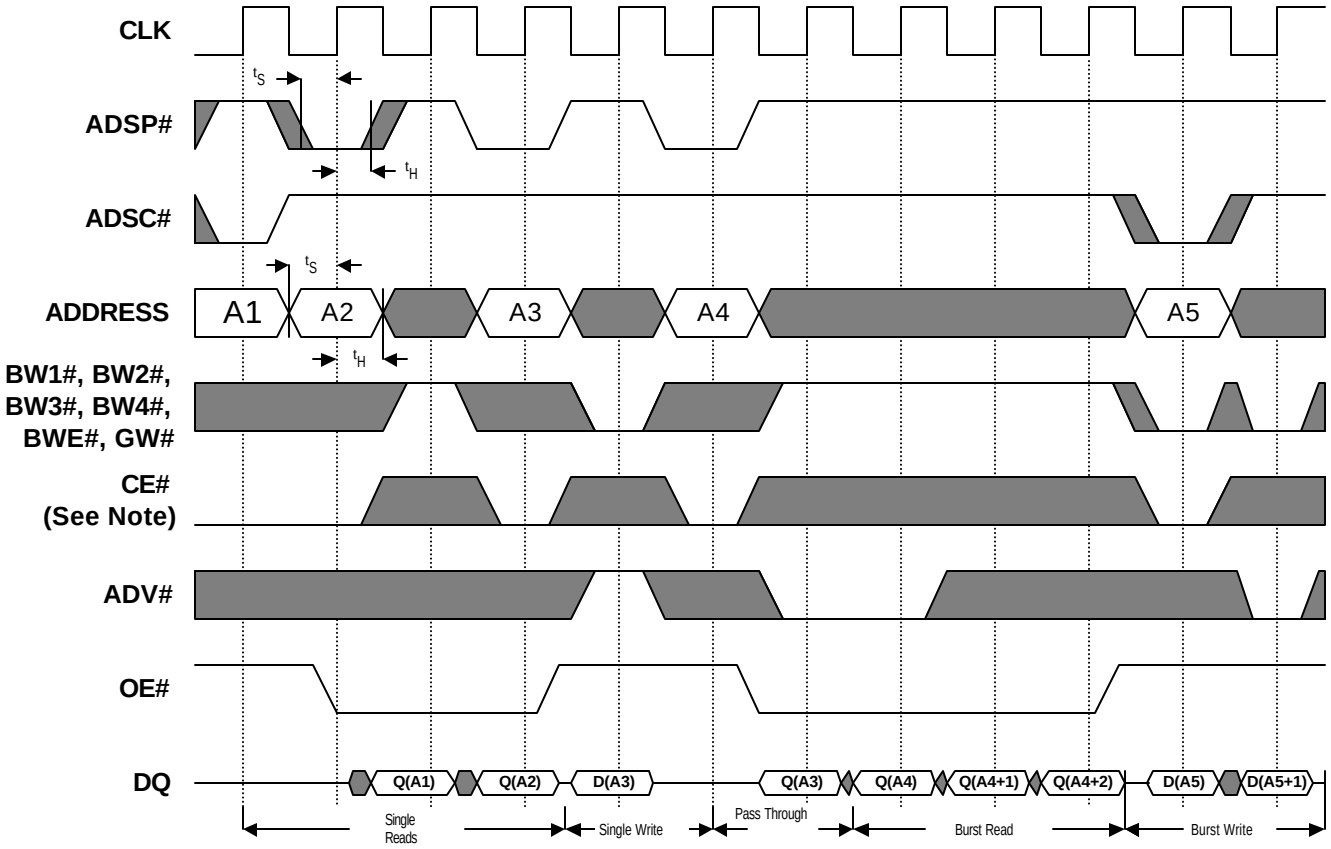
Note: CE# active in this timing diagram means that all chip enables CE#, CE2, and CE2# are active.

WRITE TIMING



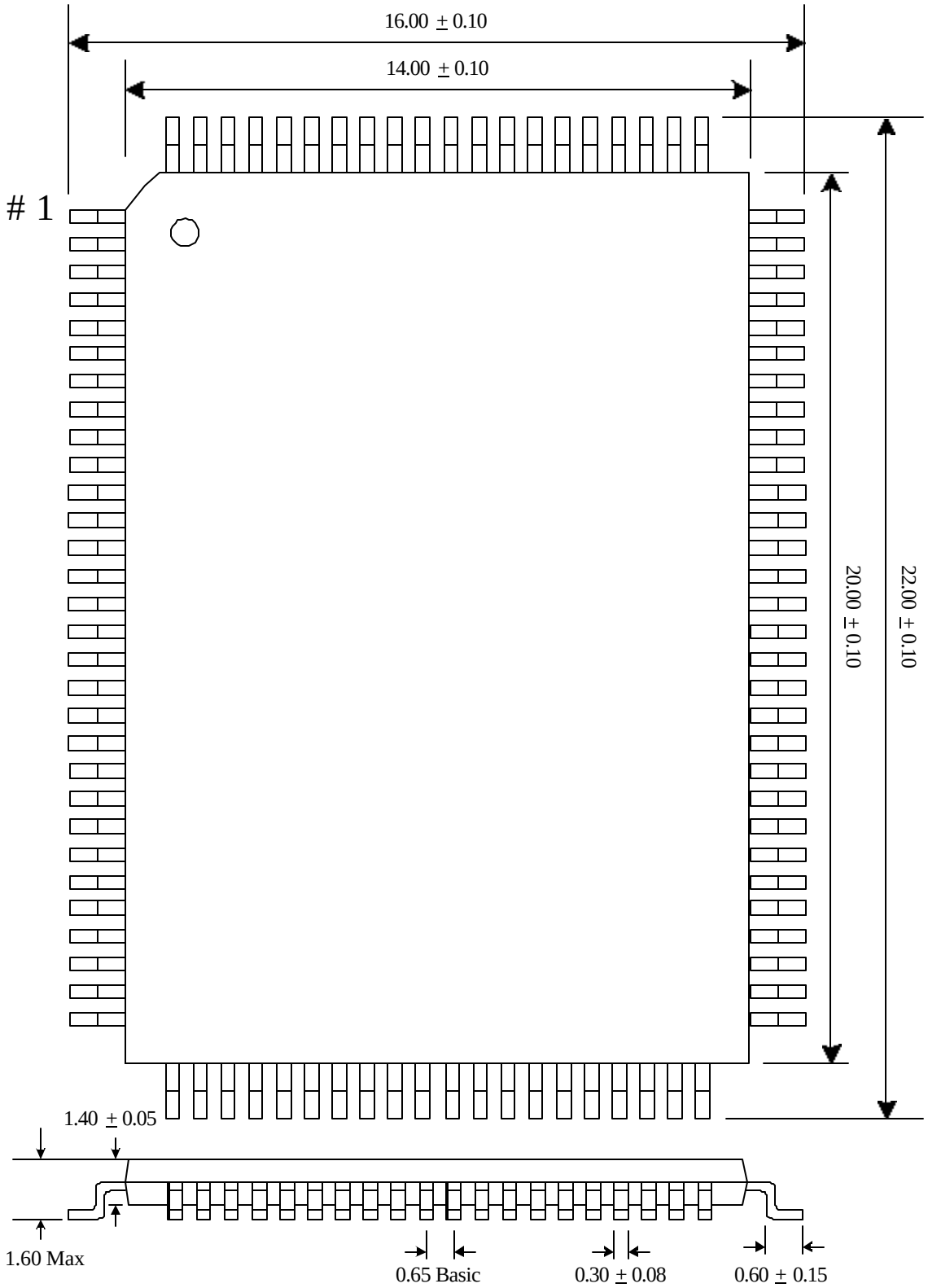
Note: CE# active in this timing diagram means that all chip enables CE#, CE2, and CE2# are active.

READ/WRITE TIMING



Note: CE# active in this timing diagram means that all chip enables CE#, CE2, and CE2# are active.

100 Pin TQFP Package Dimensions



Note: All dimensions in Millimeters

Ordering Information