

N-Channel Enhancement Mode Power MOSFET

Description

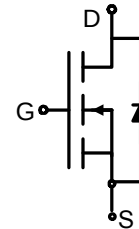
The TF30115 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V.

General Features

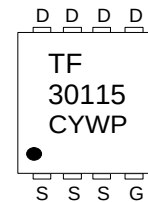
- $V_{DS} = 30V$, $I_D = 115A$
 $R_{DS(ON)} < 6.0m\Omega$ @ $V_{GS}=4.5V$
 $R_{DS(ON)} < 4.0m\Omega$ @ $V_{GS}=10V$
- High power and current handling capability
- Lead free product is acquired
- Surface mount package

Application

- Battery Switch
- Load switch
- Power management



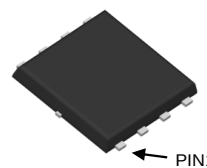
Schematic diagram



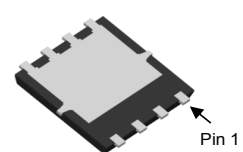
Y : year code W : week code

Pin assignment

Top View



Bottom View



PDFN5X6-8L

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ($T_J=150^\circ C$)	$T_A=25^\circ C$	I_D	115	A
	$T_A=70^\circ C$		25	
Drain Current-Pulsed (Note 1)		I_{DM}	180	A
Maximum Power Dissipation		P_D	60	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	2.0	$^\circ C/W$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.7	2.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	2.8	4.0	mΩ
		V _{GS} =5V, I _D =20A	-	4.7	6.0	
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =20A	20	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	2225	-	PF
Output Capacitance	C _{oss}		-	986	-	PF
Reverse Transfer Capacitance	C _{rss}		-	100	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V, I _D =20A V _{GS} =10V, R _{GEN} =3.0Ω	-	15	-	nS
Turn-on Rise Time	t _r		-	5	-	nS
Turn-Off Delay Time	t _{d(off)}		-	35	-	nS
Turn-Off Fall Time	t _f		-	9	-	nS
Total Gate Charge	Q _g	V _{DS} =10V, I _D =20A, V _{GS} =10V	-	6.0	-	nC
Gate-Source Charge	Q _{gs}		-	5.5	-	nC
Gate-Drain Charge	Q _{gd}		-	29.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	115	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 20A di/dt = 100A/μs ^(Note3)	-	24	-	nS
Reverse Recovery Charge	Q _{rr}		-	30	-	uC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=15V, V_G=10V, L=0.5mH, R_g=25\Omega$

Figure 1 Output Characteristics

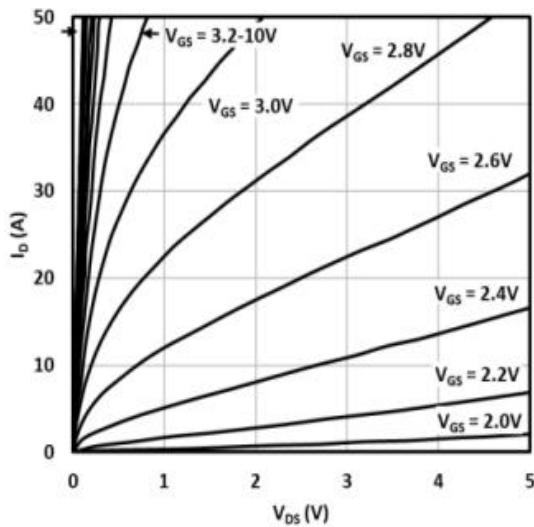


Figure 2 Transfer Characteristics

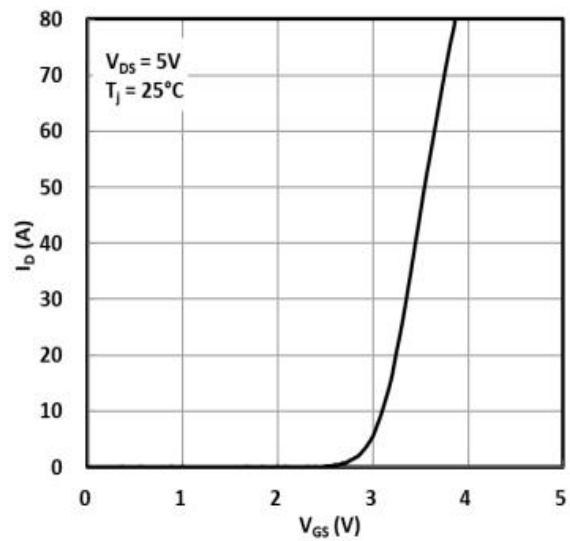


Figure 3 On-resistance vs.gate voltage

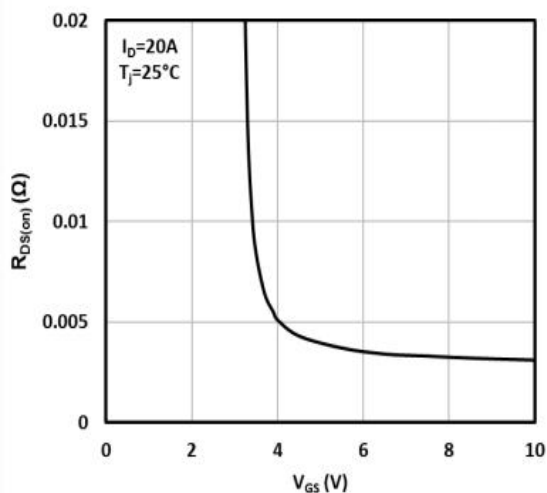


Figure 4 On-resistance vs.drain current

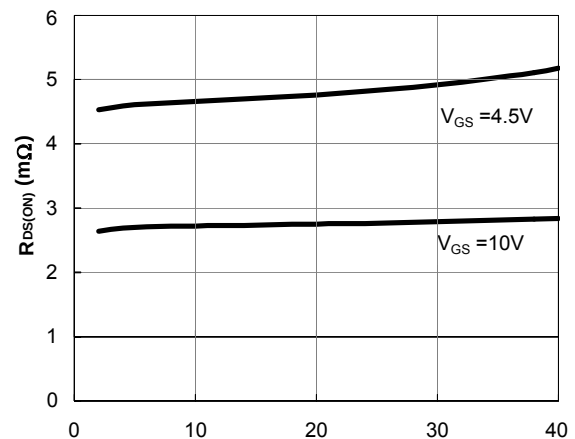


Figure 5 Source-to-drain diode forward characteristics

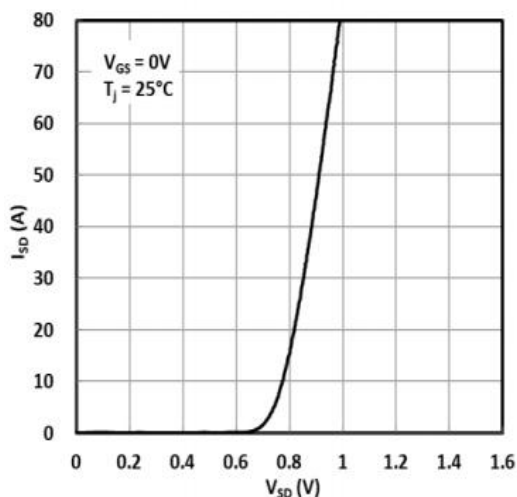


Figure 6 Capacitance vs drain-to-source Voltage

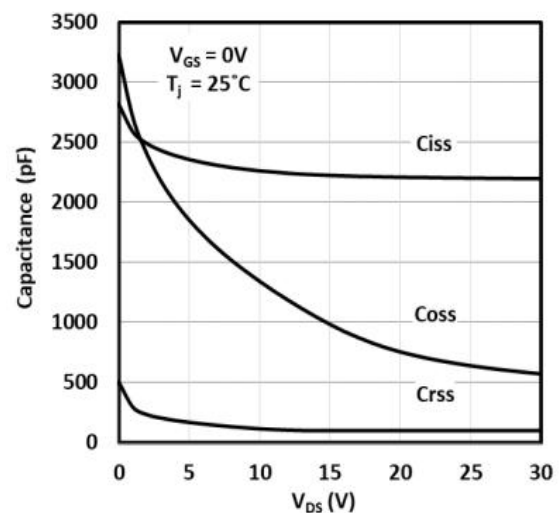


Figure 7 Gate-to-source voltage vs.gate charge

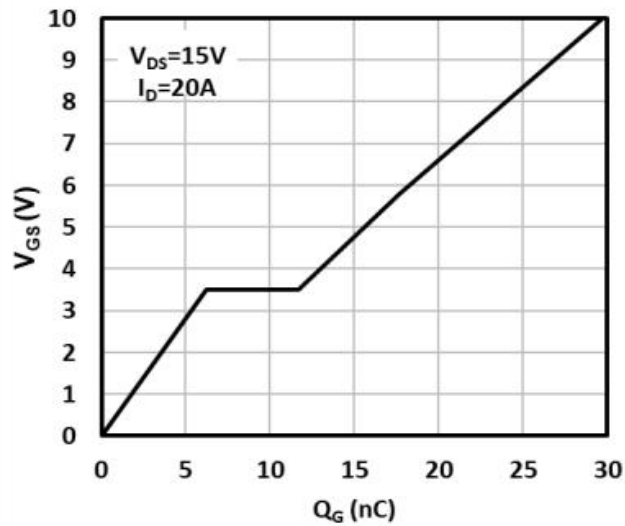


Figure 8 Maximum drain current vs.case temperature

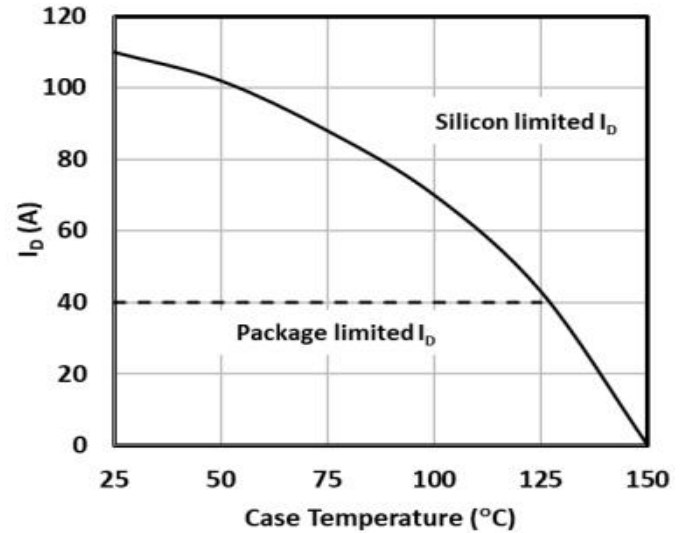
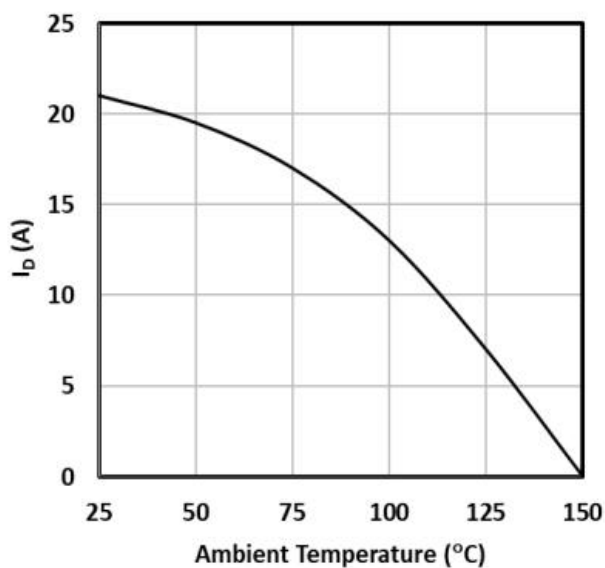
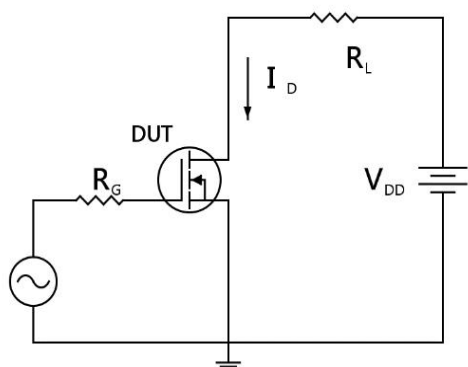
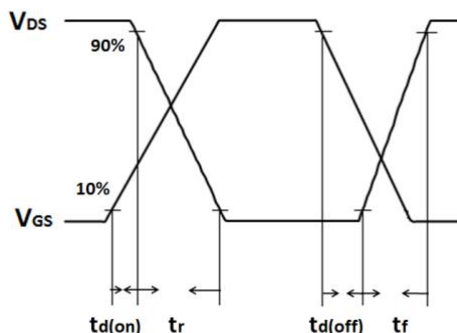


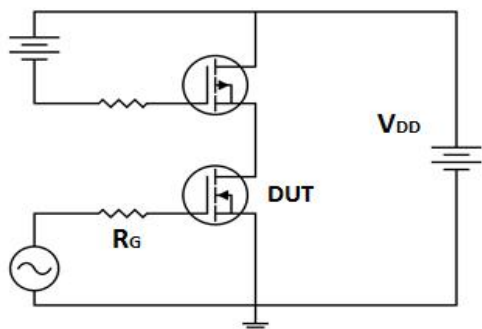
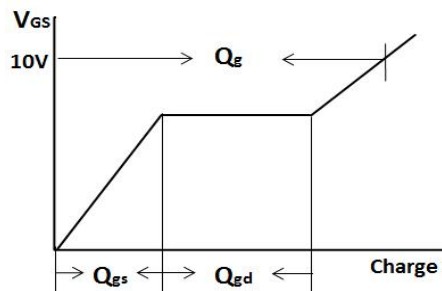
Figure 9 Maximum drain current vs. ambient temperature



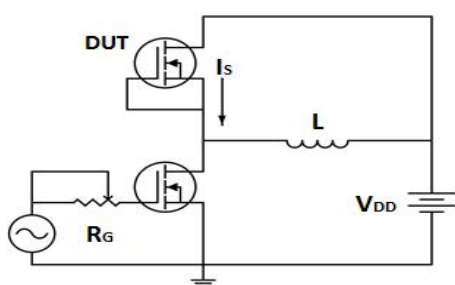
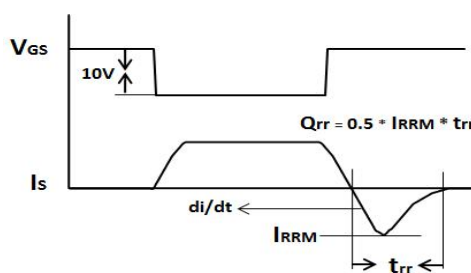
Resistive switching time test circuit & waveforms



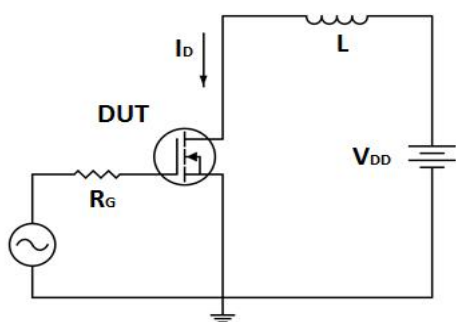
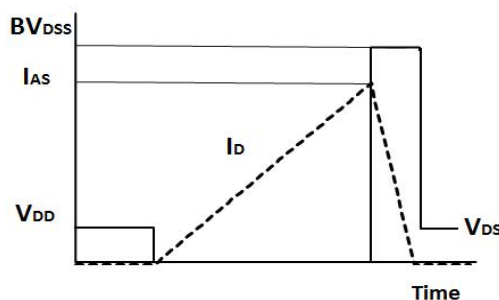
Gate charge test circuit & waveforms



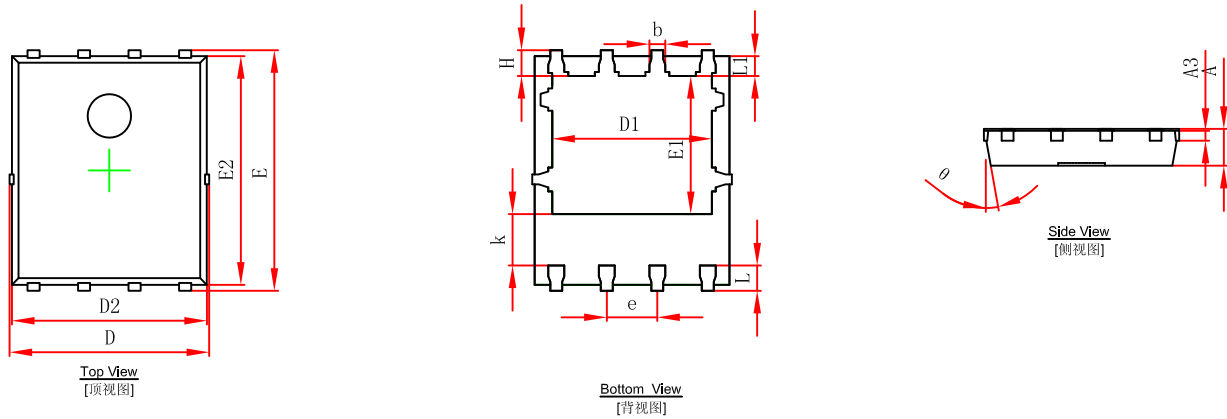
Peak diode recovery dv/dt circuit & waveforms



Unclamped inductive switching test circuit & waveforms

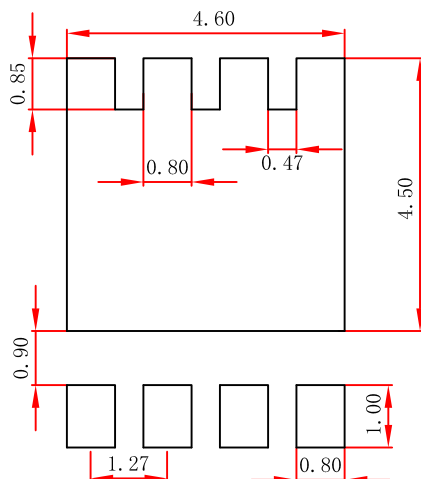


PDFNWB5x6-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.