

CERAMIC SMD CRYSTAL CLOCK OSCILLATOR WITH VOLTAGE CONTROL



ABNM SERIES

: PRELIMINARY

5.0 x 7.0 x 1.8mm

FEATURES:

- Low Jitter (<20pS P-P typ.)
- Low Phase Noise (<0.5pS typ, 12kHz to 20MHz)
- Low Power (2.5V to 3.3V)
- CMOS, LVPECL or LVDS output

APPLICATIONS:

- SONET, PCI Express, SERDES, Video
- Anywhere Low Jitter is required

STANDARD SPECIFICATIONS:

PARAMETERS	
Frequency Range	32.5 MHz to 130 MHz
Operating Temperature	0°C to + 70°C (see options)
Storage Temperature	-55°C to +125°C
Overall Frequency Stability	± 50 ppm max. (see options)
Supply Voltage (Vdd)	2.25V to 3.63
Jitter (12KHz-20MHz)	RMS phase jitter 0.5pS typ. < 1pS max.
Period Jitter	< 30pS peak to peak typ., 40pS max.
Phase Noise (77.76MHz)	-75 dBc/Hz @ 10Hz; -95 dBc/Hz @ 100Hz; -125 dBc/Hz @ 1kHz
	-145 dBc/Hz @ 10kHz; -155 dBc/Hz @ 100kHz
Tri-State Function	"1" (VIH ³ 0.7* Vdd) or open: Oscillation; "0" (VIL < 0.3* Vdd): No oscillation/Hi Z
Optional PECL OE	"0" (Vih < 0.3* Vdd) or Open: Oscillation; "1" (VIH > 0.7* Vdd): No Oscillation/Hi Z
PECL	
Supply Current (IDD)	100mA max
Symmetry (Duty Cycle)	45% min, 50% typical, 55% max.
Output Logic High	VDD -1.025V min, VDD -0.880V max.
Output Logic Low	VDD -1.810V min, VDD -1.620V max.
Rise time	850pS max, 500pS typ.
Fall time	850pS max, 500pS typ.
LVDS	
Supply Current (IDD)	80mA max
Output Clock Duty Cycle @ 1.25V	45% min, 50% typical, 55% max
Output Differential Voltage (VOD)	247mV min, 355mV typical, 454mV max
VDD Magnitude Change (ΔVOD)	-50mV min, 50mV max
Output High Voltage	VOH = 1.6V max, 1.4V typical
Output Low Voltage	VOL = 0.9V min, 1.1V typical
Offset Voltage [RL = 100Ω]	VOS = 1.125V min, 1.2V typical, 1.375V max
Offset Magnitude Voltage[RL = 100Ω]	ΔVOS = 0mV min, 3mV typical, 25mV max
Power-off Leakage (IOXD) [Vout=VDD or GND, VDD=0V]	±10μA max, ±1μA typical
Differential Clock Rise Time (tr) [RL=100Ω, CL=10pF]	0.2ns min, 0.7ns typical, 1.0ns max
Differential Clock Fall Time (tf) [RL=100Ω, CL=10pF]	0.2ns min, 0.7ns typical, 1.0ns max



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STANDARD SPECIFICATIONS (cont'd):

CMOS

Supply Current (I_{DD})	40mA max
Output Clock Duty Cycle @ 50% V_{DD}	45% min, 50% typical, 55% max
Output High Voltage (V_{OH}) [$I_{OH}=8.5mA$]	2.4V max
Output Low Voltage (V_{OL}) [$I_{OL}=8.5mA$]	0.4V max
Output Drive Current - Standard Drive (I_{OSD}) [$V_{OL}=0.4V$, $V_{OH}=2.4V$]	10mA Min
Output Drive Current - High Drive (I_{OSD}) [$V_{OL}=0.4V$, $V_{OH}=2.4V$]	30mA Min
Output Clock Rise/Fall Time - Standard Drive [10%~90% V_{DD} with 15pF load]	2.4nS typical
Output Clock Rise/Fall Time - High Drive [10%~90% V_{DD} with 10pF load]	1.2nS typical
Output Clock Duty Cycle [Measured @ 50% V_{DD}]	45% min, 50% typical, 55% max

PIN ASSIGNMENTS:

PIN #	NAME	DESCRIPTION
1	Tri-state	Tri-state
2	NC	No Connect
3	GND	Ground
4	$\overline{Q}$	PECL, LVDS, or CMOS Output
5	$\overline{Q}$	Complimentary PECL, LVDS, or NC
6	V_{DD}	V_{DD} Connection

TRI-STATE PIN OPERATION:

OUTPUT TYPE OPTION		PIN 1 LOGIC LEVEL*	OUTPUT STATE
P	PECL	0 (Default)	Enabled
		1	Tri-state
P1	PECL1	1	Enabled
		0	Tri-state
V, C, & CH	LVDS, CMOS, Hi-Drive CMOS	0	Tri-state
		1 (Default)	Enabled

*Connect to V_{DD} from logic level "1", connect to ground for logic level "0".

MARKING:

- HTU.th (Frequency: H=First "100" digit of frequency (if applicable), T=First "10" digit of frequency, U=First "unit" of frequency, t=First "tenth" digit of freq, h=First "hundredth" digit of freq.
Ex: 156.25 for 156.25MHz; 14.31 for 14.31818 MHz)
- ABNM ZYX (Z: Month, A to L; Y: Year, 5 for 2005; X: Traceability Code)

OPTIONS AND PART IDENTIFICATION (Left blank if standard):

ABNM - Frequency - Temperature - Frequency Stability - Output - Packaging

Temperature:

D for -10°C to +60°C
E for -20°C to +70°C
F for -30°C to +70°C
N for -30°C to +85°C
L for -40°C to +85°C

Stability options:

R for ± 25 ppm max
K for ± 30 ppm max
H for ± 35 ppm max

Output options:

P = PECL
P1 = PECL1
V = LVDS
C = CMOS
CH = CMOS High Drive

Packaging option: T for Tape and Reel (1,000pcs/reel)

OUTLINE DRAWING:

