1.4-W MONO FILTER-FREE CLASS-D AUDIO POWER AMPLIFIER

Check for Samples: TPA2005D1-Q1

FEATURES

- **Qualified for Automotive Applications**
- **1.4 W Into 8 Ω From a 5-V Supply at THD = 10% (Typ)**
- **Maximum Battery Life and Minimum Heat**
  - **Efficiency With an 8-Ω Speaker:**
    - **84% at 400 mW**
    - **79% at 100 mW**
  - **2.8-mA Quiescent Current**
  - **0.5-μA Shutdown Current**
- **Only Three External Components**
  - **Optimized PWM Output Stage Eliminates LC Output Filter**
  - **Internally Generated 250-kHz Switching Frequency Eliminates Capacitor and Resistor**
  - **Improved PSRR (–71 dB at 217 Hz) and Wide Supply Voltage (2.5 V to 5.5 V) Eliminates Need for a Voltage Regulator**
  - **Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor**
  - **Improved CMRR Eliminates Two Input Coupling Capacitors**
- **Space-Saving Packages**
  - **3 mm x 3 mm QFN package (DRB)**
  - **3 mm x 5 mm MSOP PowerPAD™ Package (DGN)**

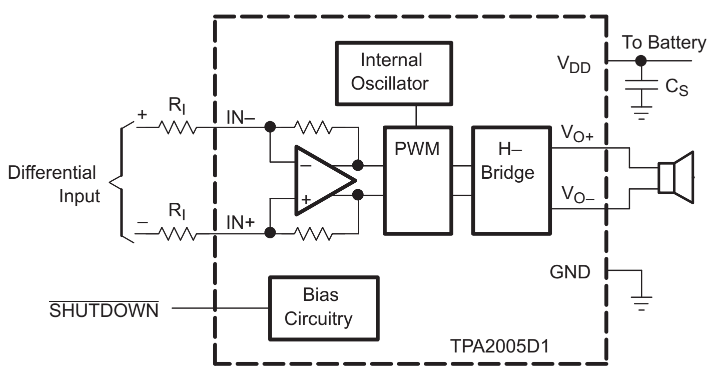
DESCRIPTION

The TPA2005D1 is a 1.4-W high-efficiency filter-free class-D audio power amplifier in a QFN or MSOP package that requires only three external components.

Features like 84% efficiency, –71-dB PSRR at 217 Hz, improved RF-rectification immunity, and 15-mm^2 total PCB area make the TPA2005D1 ideal for cellular handsets. A fast start-up time of 9 ms with minimal pop makes the TPA2005D1 ideal for PDA applications.

In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the TPA2005D1. The device allows independent gain control by summing the signals from each function, while minimizing noise to only 48 μV_{RMS}.

APPLICATION CIRCUIT



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – DRB	Reel of 3000	TPA2005D1DRBRQ1	BIQ
	MSOP – DGN	Reel of 2500	TPA2005D1DGNRQ1	2005I
–40°C to 105°C	MSOP – DGN	Reel of 2500	TPA2005D1TDGNRQ1	2005T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

V_{DD}	Supply voltage range(2)	In active mode	–0.3 V to 6 V
		In SHUTDOWN mode	–0.3 V to 7 V
V_I	Input voltage range		–0.3 V to (V_{DD} + 0.3 V)
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature range	Industrial range	–40°C to 85°C
		T-suffix range	–40°C to 105°C
T_J	Operating junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 85°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For the MSOP (DGN) package option, the maximum V_{DD} should be limited to 5 V if short-circuit protection is desired.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage		2.5	5.5	V
V_{IH}	High-level input voltage	SHUTDOWN	2	V_{DD}	V
V_{IL}	Low-level input voltage	SHUTDOWN	0	0.7	V
R_I	Input resistor	Gain ≤ 20 V/V (26 dB)	15		kΩ
V_{IC}	Common-mode input voltage range	V_{DD} = 2.5 V, 5.5 V, CMRR ≤ –49 dB	0.5	V_{DD} – 0.8	V
T_A	Operating free-air temperature		–40	85	°C

DISSIPATION RATINGS

PACKAGE	DERATING FACTOR	T_A ≤ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DRB	21.8 mW/°C	2.7 W	1.7 W	1.4 W
DGN	17.1 mW/°C	2.13 W	1.36 W	1.11 W

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS}\rvert$	Output offset voltage (measured differentially)	V_I = 0 V, A_V = 2 V/V, V_{DD} = 2.5 V to 5.5 V				25	mV
PSRR	Power-supply rejection ratio	V_{DD} = 2.5 V to 5.5 V			–75	–55	dB
CMRR	Common-mode rejection ratio	V_{DD} = 2.5 V to 5.5 V, V_{IC} = V_{DD}/2 to 0.5 V, V_{IC} = V_{DD}/2 to V_{DD} – 0.8 V	T_A = 25°C		–68	–49	dB
			T_A = –40°C to 85°C			–35	
$\lvert I_{IH}\rvert$	High-level input current	V_{DD} = 5.5 V, V_I = 5.8 V				50	μA
$\lvert I_{IL}\rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0.3 V	T_A = –40°C to 85°C			4	μA
			T_A = –40°C to 105°C			12	
$I_{(Q)}$	Quiescent current	V_{DD} = 5.5 V, no load			3.4	4.5	mA
		V_{DD} = 3.6 V, no load			2.8		
		V_{DD} = 2.5 V, no load			2.2	3.2	
$I_{(SD)}$	Shutdown current	$V_{\overline{(SHUTDOWN)}}$ = 0.8 V, V_{DD} = 2.5 V to 5.5 V	T_A = –40°C to 85°C		0.5	2	μA
			T_A = –40°C to 105°C			2.5	
$r_{DS(on)}$	Static drain-source on-state resistance	V_{DD} = 2.5 V			770		mΩ
		V_{DD} = 3.6 V			590		
		V_{DD} = 5.5 V			500		
	Output impedance in $\overline{\text{SHUTDOWN}}$	$V_{\overline{(SHUTDOWN)}}$ = 0.8 V			>1		kΩ
$f_{(sw)}$	Switching frequency	V_{DD} = 2.5 V to 5.5 V		200	250	300	kHz
	Gain			$2 \times \frac{142\ k\Omega}{R_I}$	$2 \times \frac{150\ k\Omega}{R_I}$	$2 \times \frac{158\ k\Omega}{R_I}$	$\frac{V}{V}$

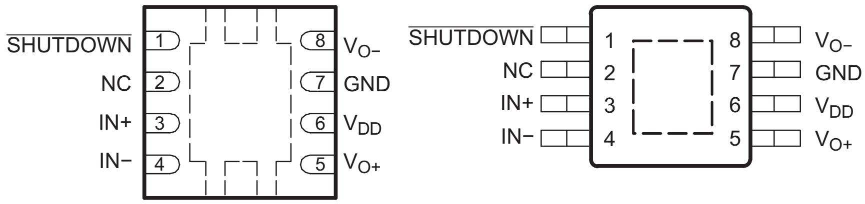
OPERATING CHARACTERISTICS

T_A = 25°C, Gain = 2 V/V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD + N= 1%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.18		W
			V_{DD} = 3.6 V		0.58		
			V_{DD} = 2.5 V		0.26		
		THD + N= 10%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.45		W
			V_{DD} = 3.6 V		0.75		
			V_{DD} = 2.5 V		0.35		
THD+N	Total harmonic distortion plus noise	P_O = 1 W, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		0.18%		
		P_O = 0.5 W, f = 1 kHz, R_L = 8 Ω	V_{DD} = 3.6 V		0.19%		
		P_O = 200 mW, f = 1 kHz, R_L = 8 Ω	V_{DD} = 2.5 V		0.20%		
k_{SVR}	Supply ripple rejection ratio	f = 217 Hz, $V_{(RIPPLE)}$ = 200 mV_{pp}, Inputs ac-grounded with C_i = 2 μF	V_{DD} = 3.6 V		–71		dB
SNR	Signal-to-noise ratio	P_O= 1 W, R_L = 8 Ω	V_{DD} = 5 V		97		dB
V_n	Output voltage noise	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, Inputs ac-grounded with C_i = 2 μF	No weighting		48		μV_{RMS}
			A weighting		36		
CMRR	Common-mode rejection ratio	V_{IC} = 1 V_{pp} , f = 217 Hz	V_{DD} = 3.6 V		–63		dB
Z_I	Input impedance			142	150	158	kΩ
	Start-up time from shutdown		V_{DD} = 3.6 V		9		ms

PIN ASSIGNMENTS

8-PIN QFN (DRB) PACKAGE (TOP VIEW) 8-PIN MSOP (DGN) PACKAGE (TOP VIEW)



NC − No internal connection

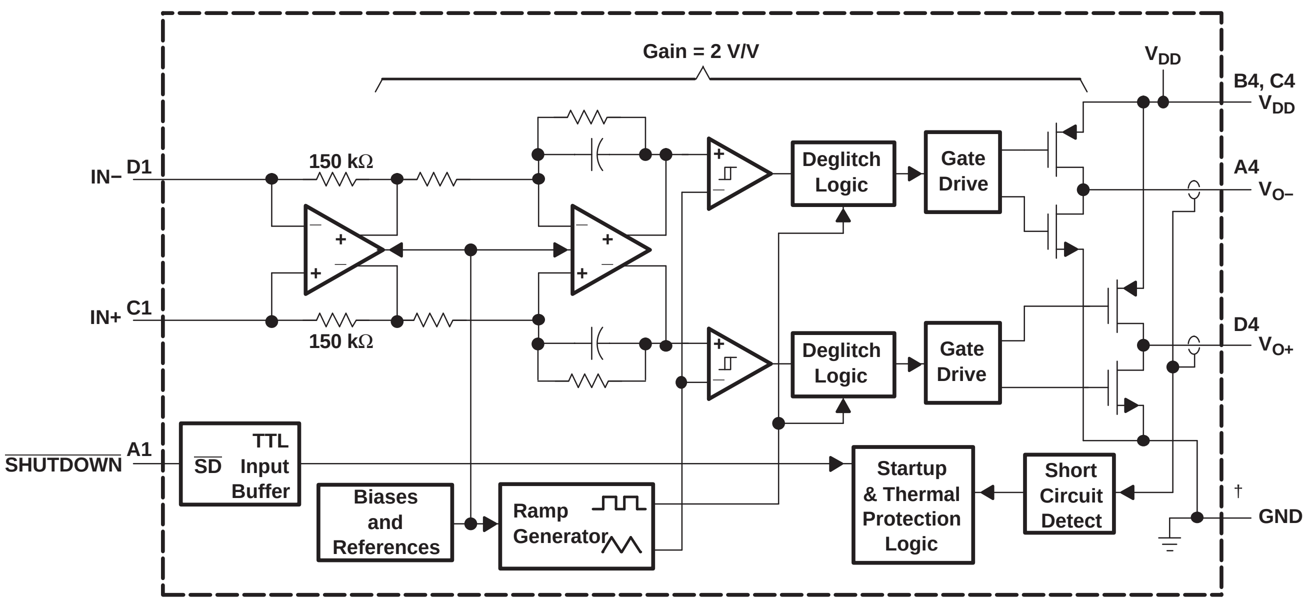
A. The shaded terminals are used for electrical and thermal connections to the ground plane. All of the shaded terminals must be electrically connected to ground. No connect (NC) terminals still need a pad and trace.

B. The thermal pad of the DRB and DGN packages must be electrically and thermally connected to a ground plane.

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
IN–	4	I	Negative differential input
IN+	3	I	Positive differential input
V_{DD}	6	I	Power supply
V_{O+}	5	O	Positive BTL output
GND	7	I	High-current ground
V_{O-}	8	O	Negative BTL output
$\overline{\text{SHUTDOWN}}$	1	I	Shutdown terminal (active low logic)
NC	2		No internal connection
Thermal Pad			Must be soldered to a grounded pad on the PCB.

FUNCTIONAL BLOCK DIAGRAM



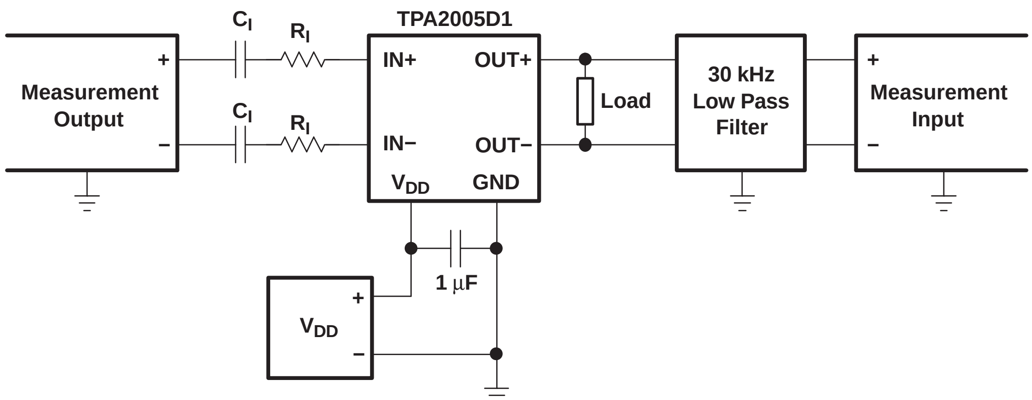
† A2, A3, B3, C2, C3, D2, D3 (terminal labels for MicroStar Junior™ package)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Efficiency	vs Output power	1, 2
P_D	Power dissipation	vs Output power	3
	Supply current	vs Output power	4, 5
$I_{(Q)}$	Quiescent current	vs Supply voltage	6
$I_{(SD)}$	Shutdown current	vs Shutdown voltage	7
P_O	Output power	vs Supply voltage	8
		vs Load resistance	9, 10
THD+N	Total harmonic distortion plus noise	vs Output power	11, 12
		vs Frequency	13, 14, 15, 16
		vs Common-mode input voltage	17
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	18, 19, 20
		vs Common-mode input voltage	21
	GSM power-supply rejection	vs Time	22
		vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency	24
		vs Common-mode input voltage	25

TEST SETUP FOR GRAPHS



A. C_I was shorted for any common-mode input voltage measurement.

B. A 33-µH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.

C. The 30-kHz low-pass filter is required, even if the analyzer has a low-pass filter. An RC filter (100 Ω, 47 nF) is used on each output for the data sheet graphs.

EFFICIENCY vs OUTPUT POWER

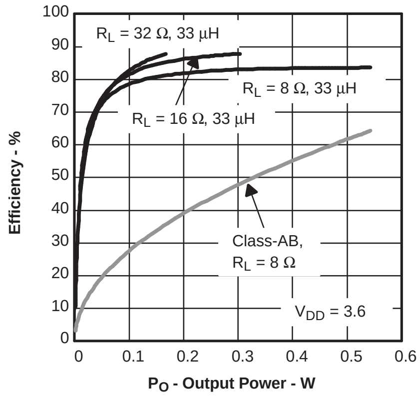


Figure 1.

EFFICIENCY vs OUTPUT POWER

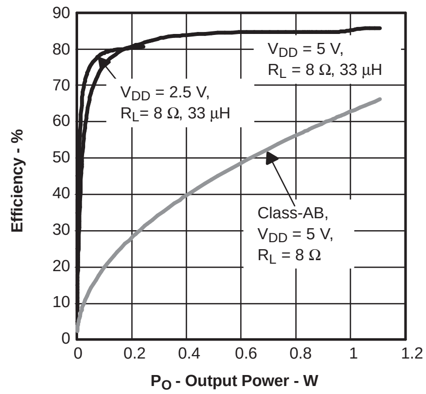


Figure 2.

POWER DISSIPATION vs OUTPUT POWER

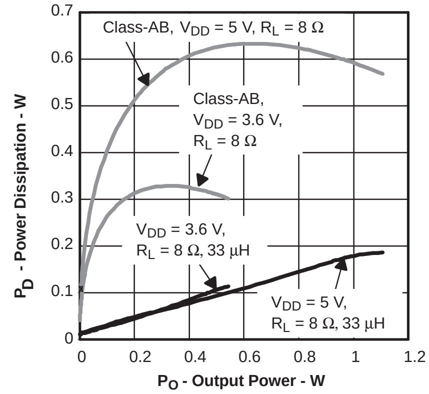


Figure 3.

SUPPLY CURRENT vs OUTPUT POWER

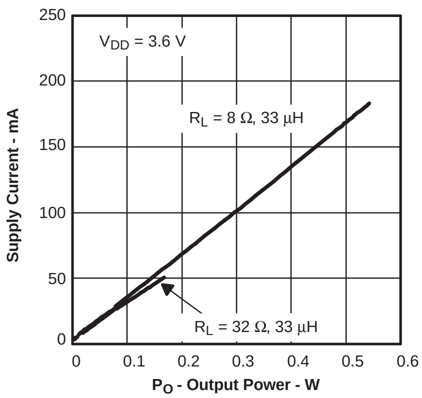


Figure 4.

SUPPLY CURRENT vs OUTPUT POWER

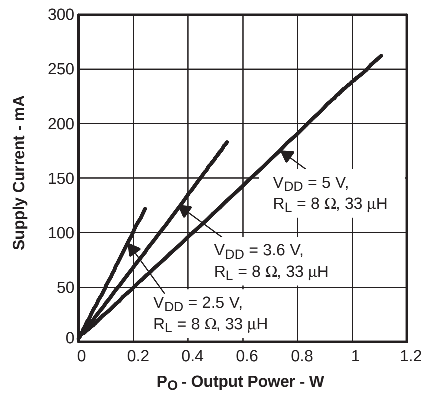


Figure 5.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

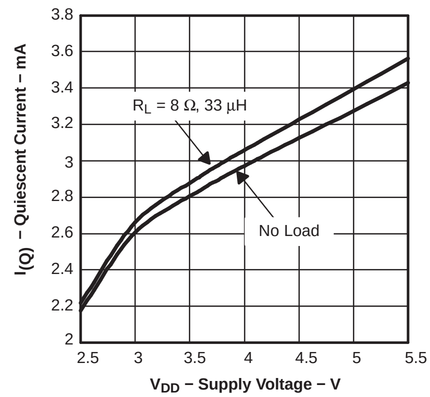


Figure 6.

SHUTDOWN CURRENT vs SHUTDOWN VOLTAGE

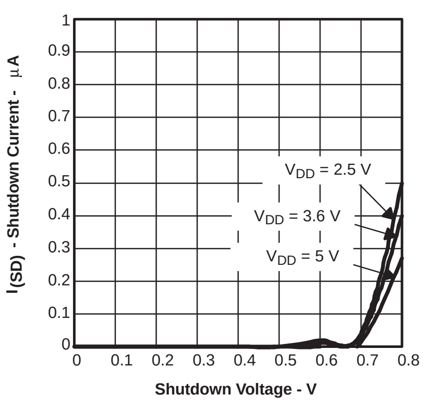


Figure 7.

OUTPUT POWER vs SUPPLY VOLTAGE

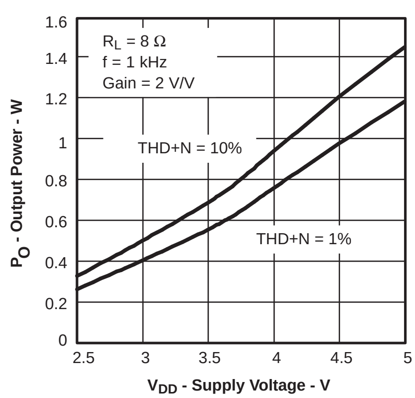


Figure 8.

OUTPUT POWER vs LOAD RESISTANCE

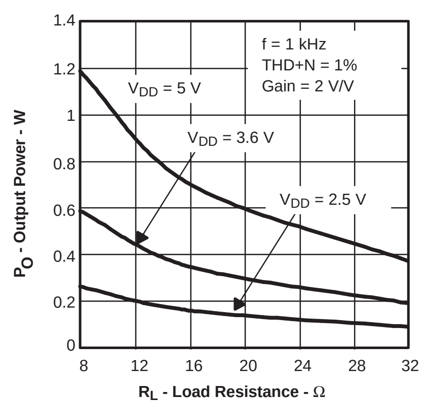


Figure 9.

OUTPUT POWER vs LOAD RESISTANCE

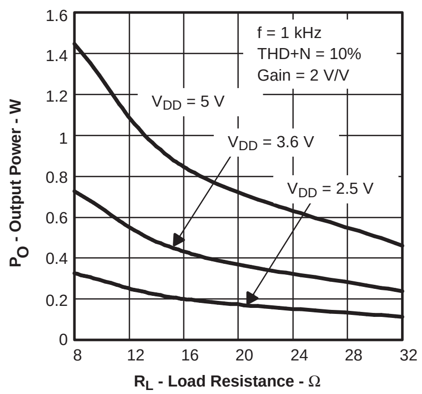


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

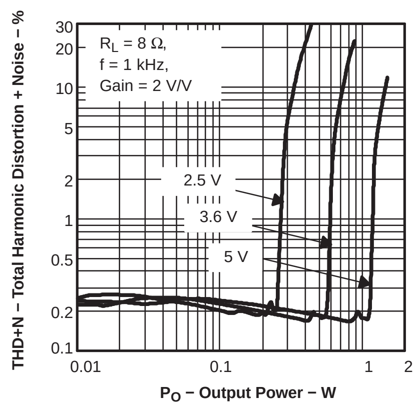


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

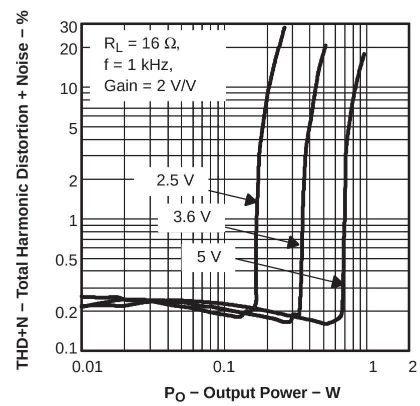


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

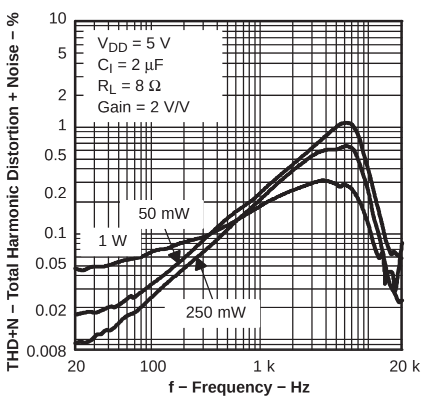


Figure 13.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

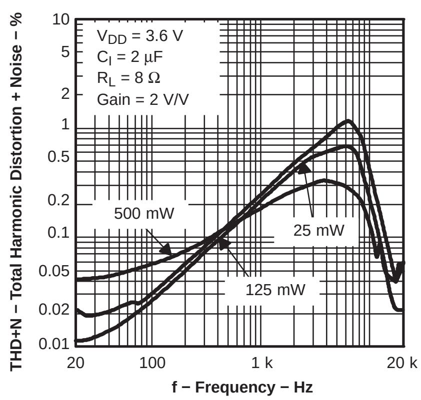


Figure 14.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

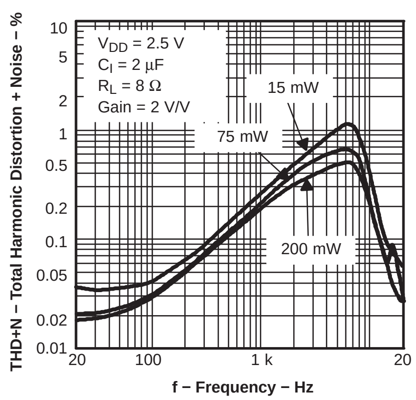


Figure 15.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

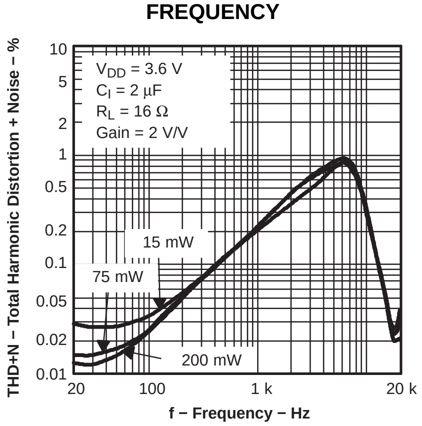


Figure 16.

TOTAL HARMONIC DISTORTION + NOISE vs COMMON MODE INPUT VOLTAGE

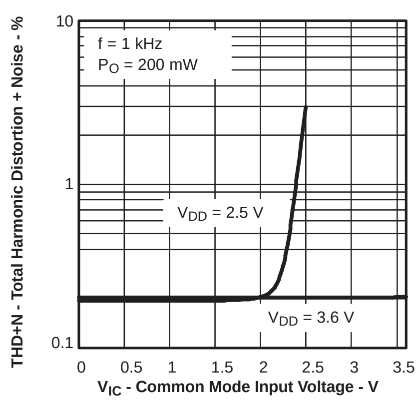


Figure 17.

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

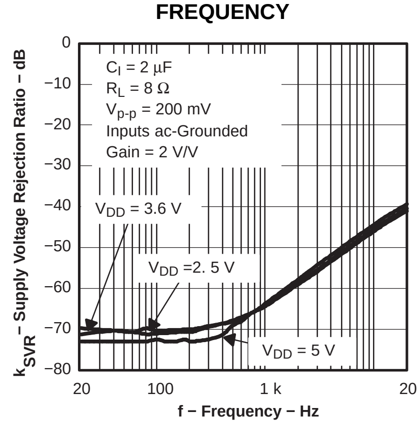


Figure 18.

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

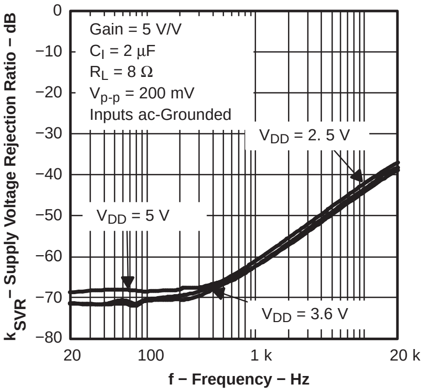


Figure 19.

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

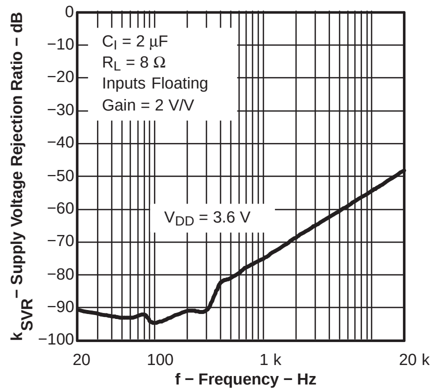


Figure 20.

SUPPLY-VOLTAGE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE

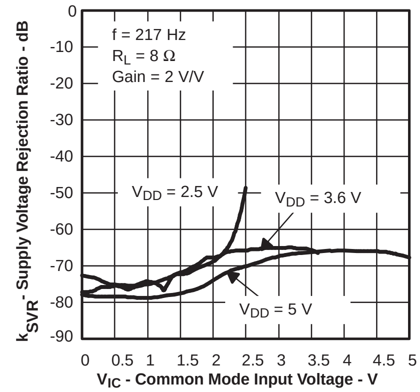


Figure 21.

GSM POWER-SUPPLY REJECTION vs TIME

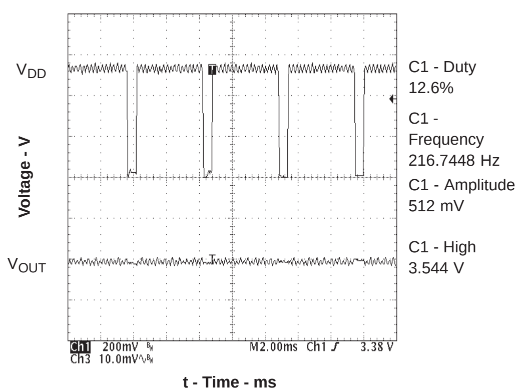


Figure 22.

GSM POWER-SUPPLY REJECTION vs FREQUENCY

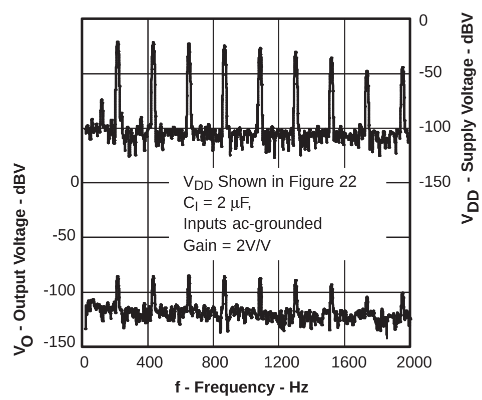


Figure 23.

COMMON-MODE REJECTION RATIO vs FREQUENCY

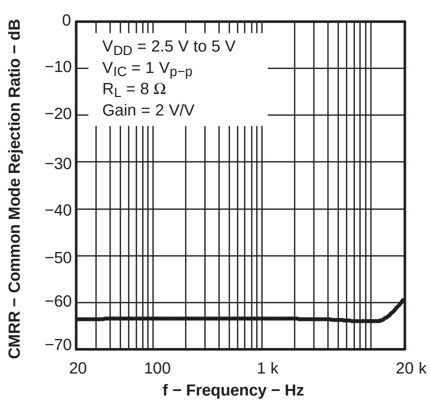


Figure 24.

COMMON-MODE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE

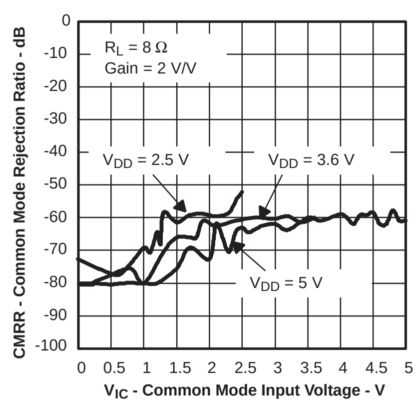


Figure 25.

APPLICATION INFORMATION

FULLY DIFFERENTIAL AMPLIFIER

The TPA2005D1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$, regardless of the common-mode voltage at the input. The fully differential TPA2005D1 can still be used with a single-ended input; however, the TPA2005D1 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

- Input-coupling capacitors not required:
  - The fully differential amplifier allows the inputs to be biased at a voltage other than mid-supply. For example, if a codec has a mid-supply lower than the mid-supply of the TPA2005D1, the common-mode feedback circuit adjusts, and the TPA2005D1 outputs still is biased at mid-supply of the TPA2005D1. The inputs of the TPA2005D1 can be biased from 0.5 V to V_{DD} – 0.8 V. If the inputs are biased outside of that range, input-coupling capacitors are required.
- Mid-supply bypass capacitor, $C_{(BYPASS)}$, not required:
  - The fully differential amplifier does not require a bypass capacitor. This is because any shift in the mid-supply affects both positive and negative channels equally and cancels at the differential output.
- Better RF immunity:
  - GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

COMPONENT SELECTION

Figure 26 shows the TPA2005D1 typical schematic with differential inputs, and Figure 27 shows the TPA2005D1 with differential inputs and input capacitors, and Figure 28 shows the TPA2005D1 with single-ended inputs. Differential inputs should be used whenever possible, because the single-ended inputs are much more susceptible to noise.

Table 1. Typical Component Values

REF DES	VALUE	EIA SIZE	MANUFACTURER	PART NUMBER
R_I	150 kΩ (±0.5%)	0402	Panasonic	ERJ2RHD154V
C_S	1 µF (+22%, –80%)	0402	Murata	GRP155F50J105Z
C_I (1)	3.3 nF (±10%)	0201	Murata	GRP033B10J332K

(1) C_I is needed only for single-ended input or if V_{ICM} is not between 0.5 V and V_{DD} – 0.8 V. C_I = 3.3 nF (with R_I = 150 kΩ) gives a high-pass corner frequency of 321 Hz.

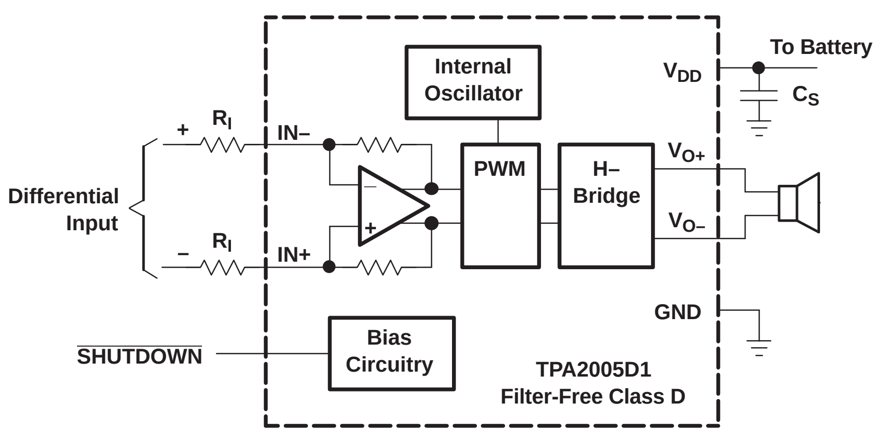


Figure 26. Typical TPA2005D1 Application Schematic With Differential Input for a Wireless Phone

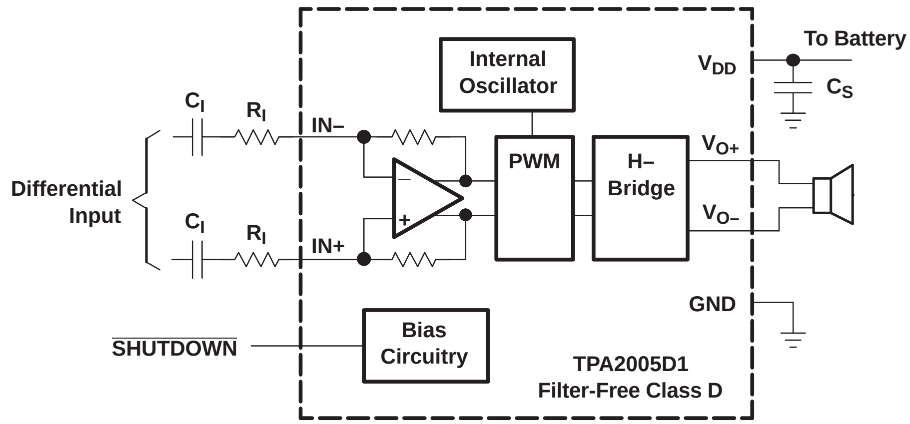


Figure 27. TPA2005D1 Application Schematic With Differential Input and Input Capacitors

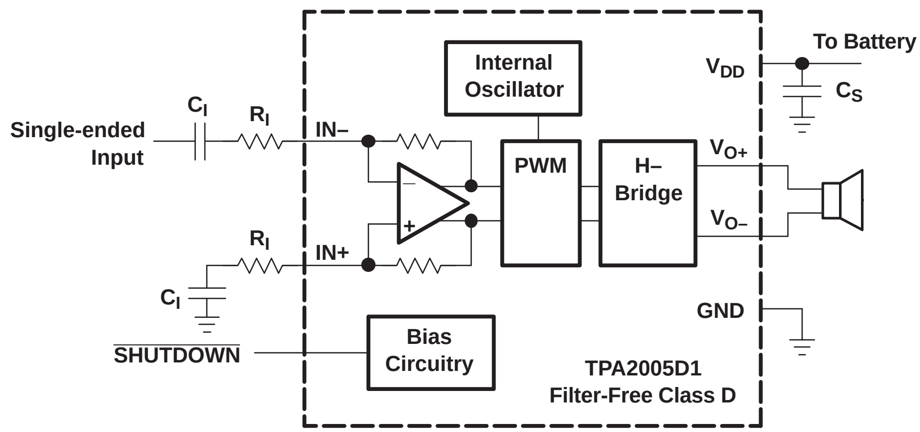


Figure 28. TPA2005D1 Application Schematic With Single-Ended Input

Input Resistors (R_I)

The input resistors (R_I) set the gain of the amplifier according to equation Equation 1.

$$\text{Gain} = 2 \times \frac{150\ k\Omega}{R_I} \tag{1}$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors, or better, to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the TPA2005D1 to limit noise injection on the high-impedance nodes.

For optimal performance, the gain should be set to 2 V/V or lower. Lower gain allows the TPA2005D1 to operate at its best and keeps a high voltage at the input, making the inputs less susceptible to noise.

Decoupling Capacitor (C_S)

The TPA2005D1 is a high-performance class-D audio amplifier that requires adequate power-supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μF, placed as close as possible to the device V_{DD} lead, works best. Placing this decoupling capacitor close to the TPA2005D1 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10-μF, or greater, capacitor placed near the audio power amplifier also helps, but it is not required in most applications because of the high PSRR of this device.

Input Capacitors (C_I)

The TPA2005D1 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to V_{DD} – 0.8 V (shown in Figure 26). If the input signal is not biased within the recommended common-mode input range, if needing to use the input as a high pass filter (shown in Figure 27), or if using a single-ended source (shown in Figure 28), input coupling capacitors are required.

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_c, determined in Equation 2.

$$f_C = \frac{1}{\left(2\pi R_I C_I\right)} \tag{2}$$

The value of the input capacitor is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones usually cannot respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

Equation 3 is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{\left(2\pi R_I f_C\right)} \tag{3}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low-frequency response, use large input coupling capacitors (1 μF). However, in a GSM phone the ground signal is fluctuating at 217 Hz, but the signal from the codec does not have the same 217-Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217-Hz hum.

SUMMING INPUT SIGNALS WITH THE TPA2005D1

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The TPA2005D1 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

Summing Two Differential Input Signals

Two extra resistors are needed for summing differential signals (a total of 5 components). The gain for each input source can be set independently (see Equation 4 and Equation 5 and Figure 29).

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = 2 \times \frac{150\ \text{k}\Omega}{R_{I1}} \quad \left(\frac{V}{V}\right) \tag{4}$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = 2 \times \frac{150\ \text{k}\Omega}{R_{I2}} \quad \left(\frac{V}{V}\right) \tag{5}$$

If summing left and right inputs with a gain of 1 V/V, use R_{I1}= R_{I2}= 300 kΩ.

If summing a ring tone and a phone signal, set the ring-tone gain to gain 2 = 2 V/V, and the phone gain to gain 1 = 0.1 V/V. The resistor values are:

- R_{I1} = 3 MΩ and R_{I2} = 150 kΩ.

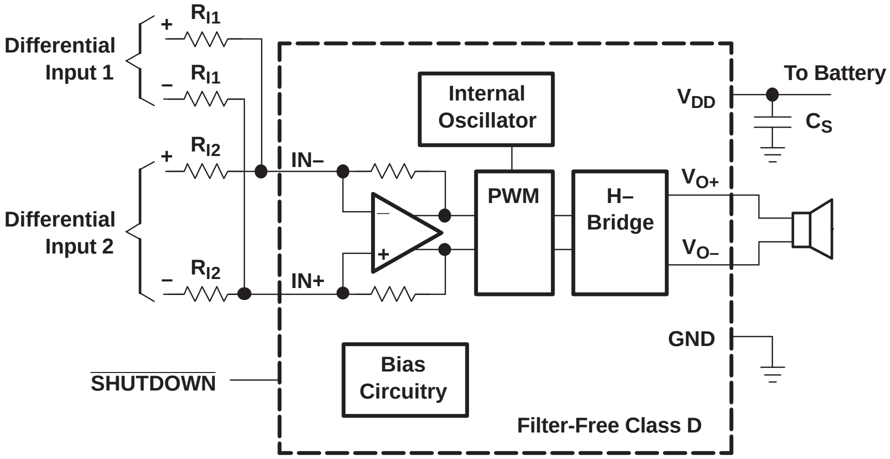


Figure 29. Application Schematic With TPA2005D1 Summing Two Differential Inputs

Summing a Differential Input Signal and a Single-Ended Input Signal

Figure 30 shows how to sum a differential input signal and a single-ended input signal. Ground noise can couple in through IN+ with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by C_{I2}, shown in Equation 8. To ensure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use.

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = 2 \times \frac{150\ \text{k}\Omega}{R_{I1}} \quad \left(\frac{V}{V}\right) \tag{6}$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = 2 \times \frac{150\ \text{k}\Omega}{R_{I2}} \quad \left(\frac{V}{V}\right) \tag{7}$$

$$C_{I2} = \frac{1}{\left(2\pi R_{I2} f_{c2}\right)} \tag{8}$$

If summing a ring tone and a phone signal, the phone signal should use a differential input signal while the ring tone might be limited to a single-ended signal. If phone gain is set at gain 1 = 0.1 V/V, and the ring-tone gain is set to gain 2 = 2 V/V, the resistor values are:

- R_{I1} = 3 MΩ and R_{I2} = 150 kΩ.

The high-pass corner frequency of the single-ended input is set by C_{I2}. If the desired corner frequency is less than 20 Hz, then:

$$C_{I2} > \frac{1}{(2\pi\ 150k\Omega\ 20Hz)} \quad (9)$$

$$C_{I2} > 53pF \quad (10)$$

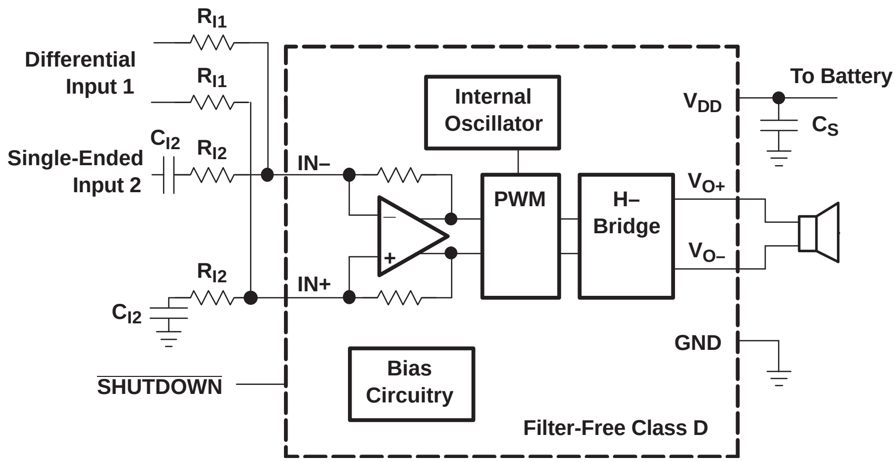


Figure 30. Application Schematic With TPA2005D1 Summing Differential Input and Single-Ended Input Signals

Summing Two Single-Ended Input Signals

Four resistors and three capacitors are needed for summing single-ended input signals. The gain and corner frequencies (f_{c1} and f_{c2}) for each input source can be set independently (see Equation 11 through Equation 14 and Figure 31). Resistor, R_P, and capacitor, C_P, are needed on the IN+ terminal to match the impedance on the IN– terminal. The single-ended inputs must be driven by low-impedance sources, even if one of the inputs is not outputting an ac signal.

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = 2 \times \frac{150\ k\Omega}{R_{I1}} \left(\frac{V}{V}\right) \quad (11)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = 2 \times \frac{150\ k\Omega}{R_{I2}} \left(\frac{V}{V}\right) \quad (12)$$

$$C_{I1} = \frac{1}{\left(2\pi\ R_{I1}\ f_{c1}\right)} \quad (13)$$

$$C_{I2} = \frac{1}{\left(2\pi\ R_{I2}\ f_{c2}\right)} \quad (14)$$

$$C_P = C_{I1} + C_{I2} \quad (15)$$

$$R_P = \frac{R_{I1} \times R_{I2}}{\left(R_{I1} + R_{I2}\right)} \quad (16)$$

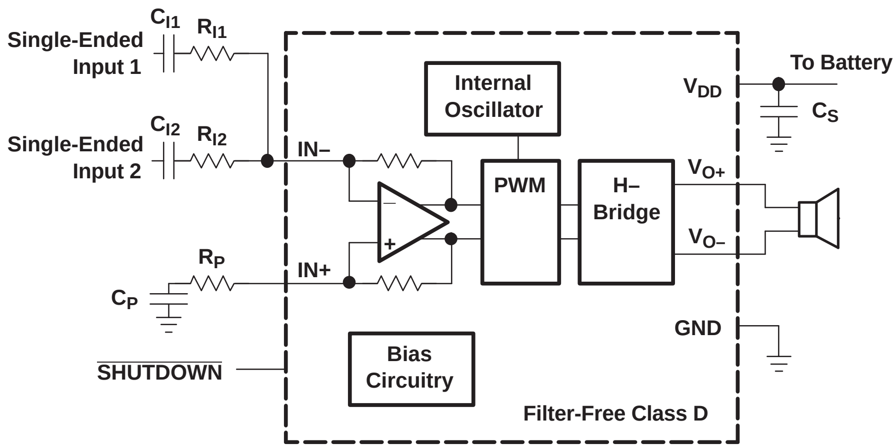


Figure 31. Application Schematic With TPA2005D1 Summing Two Single-Ended Inputs

EFFICIENCY AND THERMAL INFORMATION

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the 2,5-mm x 2,5-mm MicroStar Junior package is shown in the dissipation rating table. Converting this to θ_{JA}:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.016} = 62.5°\text{C/W} \quad (17)$$

Given θ_{JA} of 62.5°C/W, the maximum allowable junction temperature of 150°C, and the maximum internal dissipation of 0.2 W (worst case 5-V supply), the maximum ambient temperature can be calculated with equation Equation 18.

$$T_A\text{Max} = T_J\text{Max} - \theta_{JA}P_{Dmax} = 150 - 62.5\,(0.2) = 137.5°\text{C} \quad (18)$$

Equation 18 shows that the calculated maximum ambient temperature is 137.5°C at maximum power dissipation with a 5-V supply; however, the maximum ambient temperature of the package is limited to 85°C. Because of the efficiency of the TPA2005D1, it can be operated under all conditions to an ambient temperature of 85°C. The TPA2005D1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using speakers more resistive than 8 Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

BOARD LAYOUT

Component Location

Place all the external components very close to the TPA2005D1. The input resistors need to be very close to the TPA2005D1 input pins so noise does not couple on the high-impedance nodes between the input resistors and the input amplifier of the TPA2005D1. Placing the decoupling capacitor, C_S, close to the TPA2005D1 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Trace Width

Make the high current traces going to pins VDD, GND, V_{O+} and V_{O-} of the TPA2005D1 have a minimum width of 0,7 mm. If these traces are too thin, the TPA2005D1 performance and output power will decrease. The input traces do not need to be wide, but do need to run side-by-side to enable common-mode noise cancellation.

8-Pin QFN (DRB) Layout

Use the following land pattern for board layout with the 8-pin QFN (DRB) package. Note that the solder paste should use a hatch pattern to fill solder paste at 50% to ensure that there is not too much solder paste under the package.

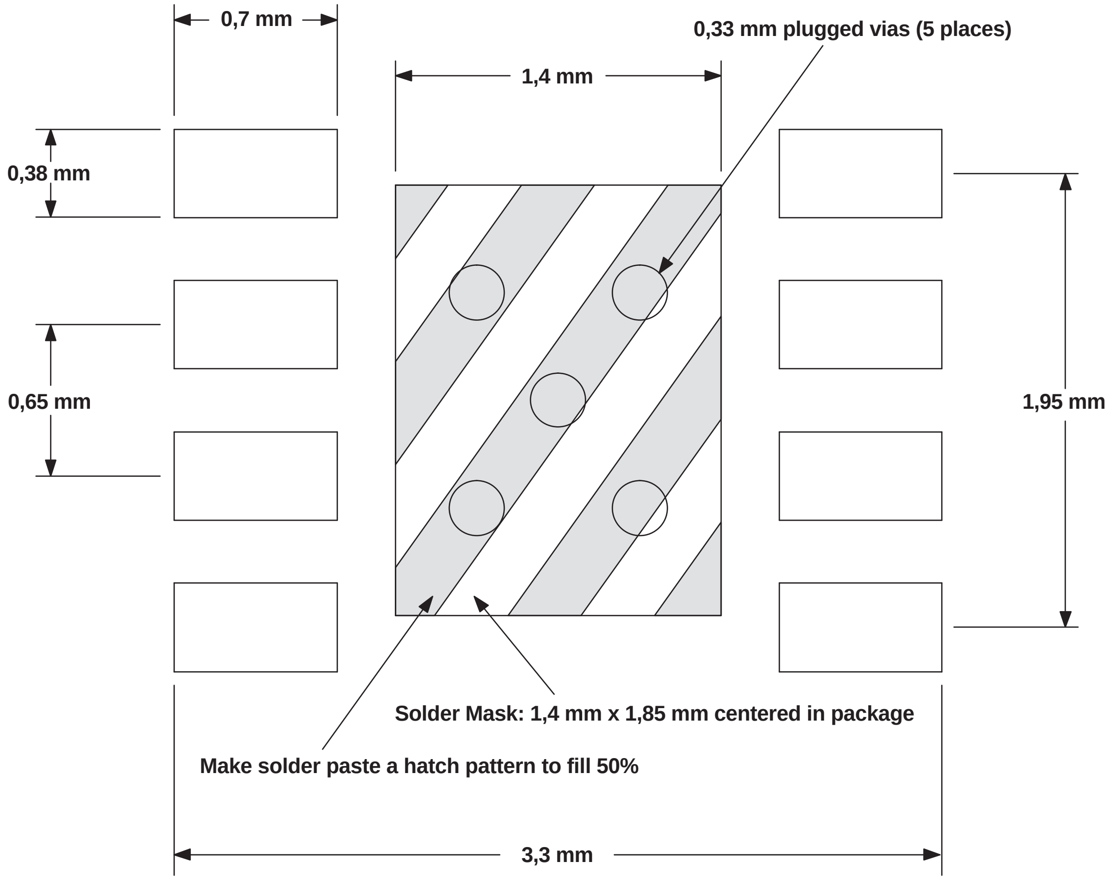


Figure 32. TPA2005D1 8-Pin QFN (DRB) Board Layout (Top View)

ELIMINATING THE OUTPUT FILTER WITH THE TPA2005D1

This section focuses on why the user can eliminate the output filter with the TPA2005D1.

Effect on Audio

The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

Traditional Class-D Modulation Scheme

The traditional class-D modulation scheme, which is used in the TPA005Dxx family, has a differential output in which each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{DD}. Therefore, the differential pre-filtered output varies between positive and negative V_{DD}, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 33. Note that, even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing a high loss and thus causing a high supply current.

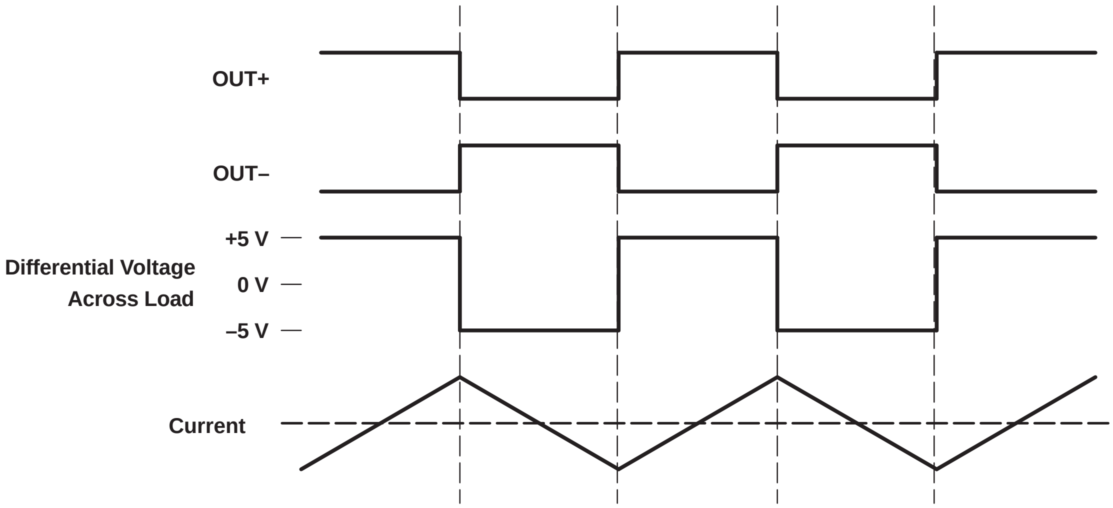


Figure 33. Traditional Class-D Modulation Scheme Output Voltage and Current Waveforms Into an Inductive Load With No Input

TPA2005D1 Modulation Scheme

The TPA2005D1 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUT+ and OUT– are now in phase with each other, with no input. The duty cycle of OUT+ is greater than 50% and OUT– is less than 50% for positive voltages. The duty cycle of OUT+ is less than 50% and OUT– is greater than 50% for negative voltages. The voltage across the load remains at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load.

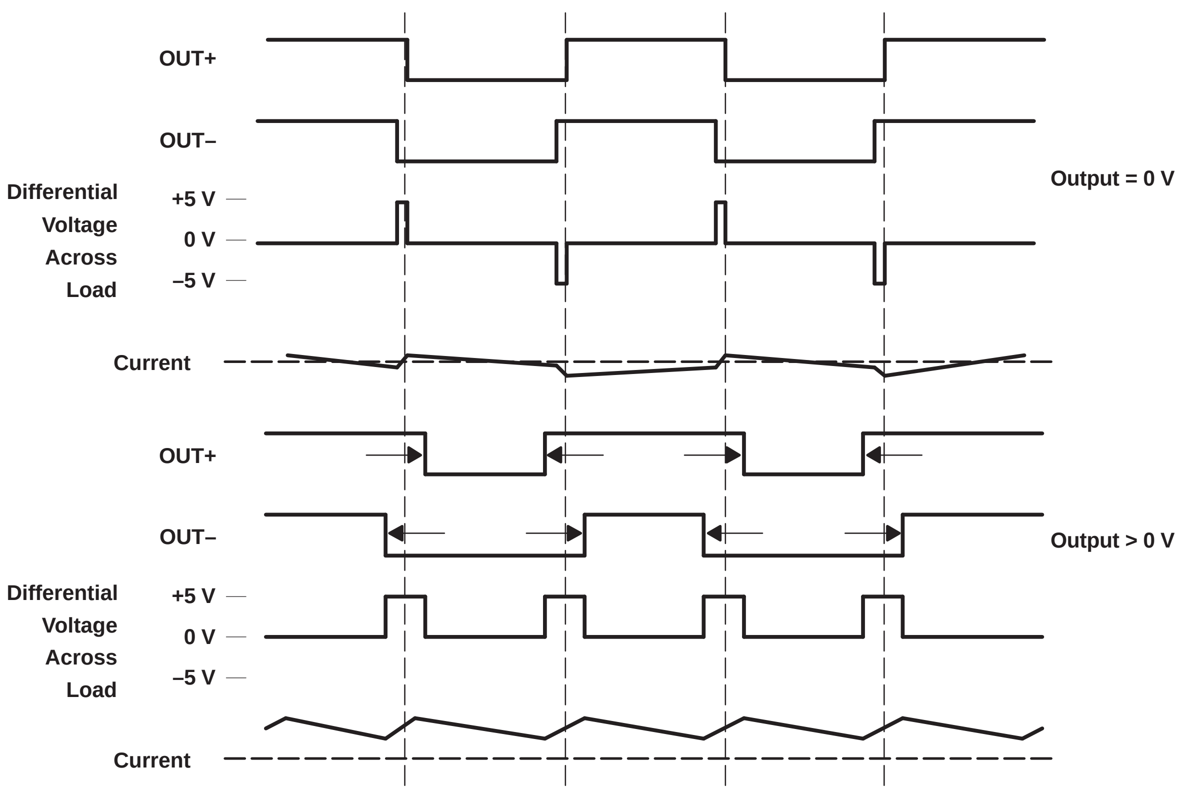


Figure 34. The TPA2005D1 Output Voltage and Current Waveforms Into an Inductive Load

Efficiency: Why You Must Use a Filter With the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × V_{DD}, and the time at each voltage is one-half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half-cycle for the next half-cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA2005D1 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is V_{DD} instead of 2 × V_{DD}. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker, resulting in less power dissipation, which increases efficiency.

Effects of Applying a Square Wave Into a Speaker

If the amplitude of a square wave is high enough and the frequency of the square wave is within the bandwidth of the speaker, a square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, is not significant because the speaker cone movement is proportional to $1/f^2$ for frequencies beyond the audio band. Therefore, the amount of cone movement at the switching frequency is very small. However, damage could occur to the speaker if the voice coil is not designed to handle the additional power. To size the speaker for added power, the ripple current dissipated in the load must be calculated by subtracting the theoretical supplied power, $P_{SUP\ THEORETICAL}$, from the actual supply power, P_{SUP}, at maximum output power, P_{OUT}. The switching power dissipated in the speaker is the inverse of the measured efficiency,$\eta_{MEASURED}$, minus the theoretical efficiency,$\eta_{THEORETICAL}$.

$$P_{SPKR} = P_{SUP} – P_{SUP\ THEORETICAL} \text{ (at max output power)} \tag{19}$$

$$P_{SPKR} = \frac{P_{SUP}}{P_{OUT}} – \frac{P_{SUP\ THEORETICAL}}{P_{OUT}} \text{ (at max output power)} \tag{20}$$

$$P_{SPKR} = P_{OUT}\left(\frac{1}{\eta_{MEASURED}} – \frac{1}{\eta_{THEORETICAL}}\right) \text{ (at max output power)} \tag{21}$$

$$\eta THEORETICAL = \frac{R_L}{R_L + 2r_{DS(on)}} \text{ (at max output power)} \tag{22}$$

The maximum efficiency of the TPA2005D1 with a 3.6-V supply and an 8-Ω load is 86% from Equation 22. Using Equation 21 with the efficiency at maximum power (84%), we see that there is an additional 17 mW dissipated in the speaker. The added power dissipated in the speaker is not an issue as long as it is taken into account when choosing the speaker.

When to Use an Output Filter

Design the TPA2005D1 without an output filter if the traces from amplifier to speaker are short. The TPA2005D1 passed FCC and CE radiated emissions with no shielding and with speaker trace wires 100 mm long or less. Wireless handsets and PDAs are great applications for class-D without a filter.

A ferrite bead filter often can be used if the design is failing radiated emissions without an LC filter, and the frequency-sensitive circuit is greater than 1 MHz. This is good for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use an LC output filter if there are low-frequency (<1 MHz) EMI-sensitive circuits and/or there are long leads from amplifier to speaker.

Figure 35 and Figure 36 show typical ferrite bead and LC output filters.

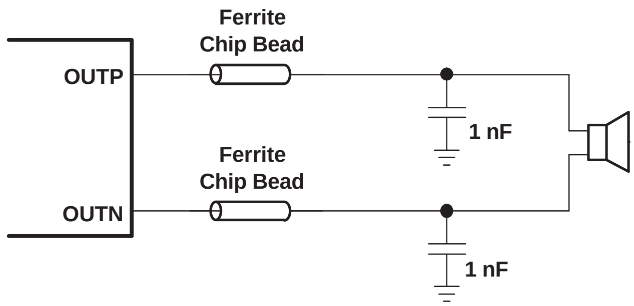


Figure 35. Typical Ferrite Chip Bead Filter (Chip bead example: NEC/Tokin: N2012ZPS121)

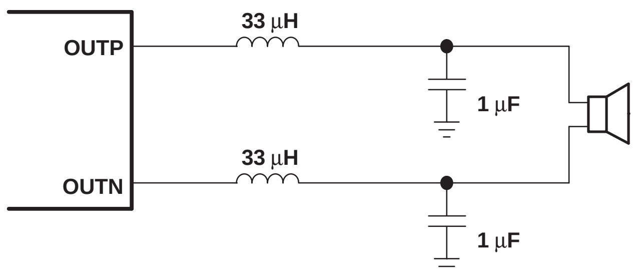


Figure 36. Typical LC Output Filter, Cut-Off Frequency of 27 kHz

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPA2005D1DGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2005I	Samples
TPA2005D1DRBQ1	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIQ	Samples
TPA2005D1TDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2005T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPA2005D1-Q1 :

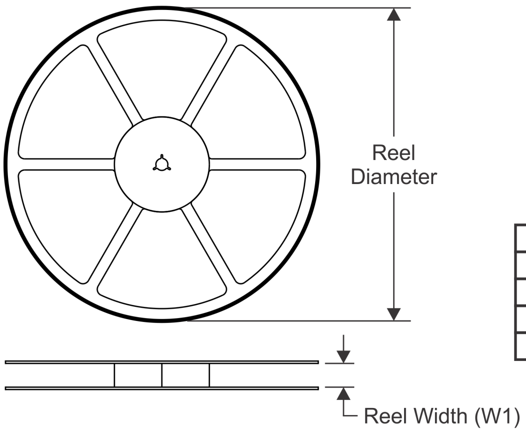
- Catalog: TPA2005D1

NOTE: Qualified Version Definitions:

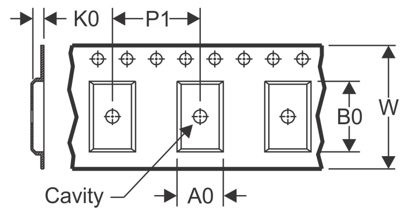
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

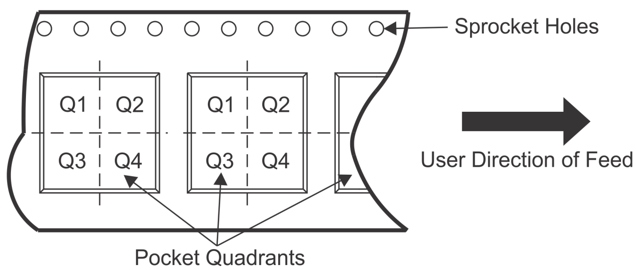


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

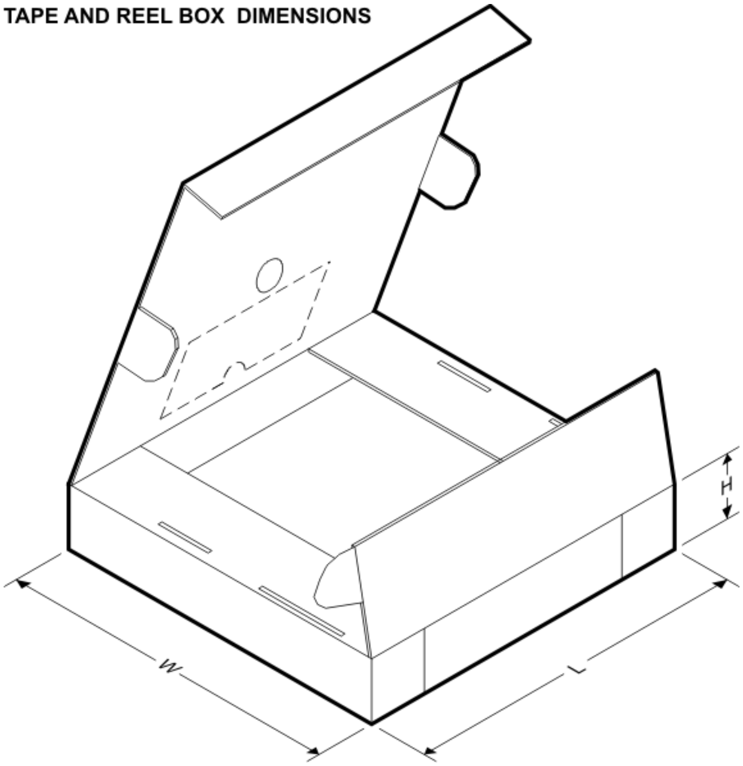
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2005D1DGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA2005D1DRBQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA2005D1TDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

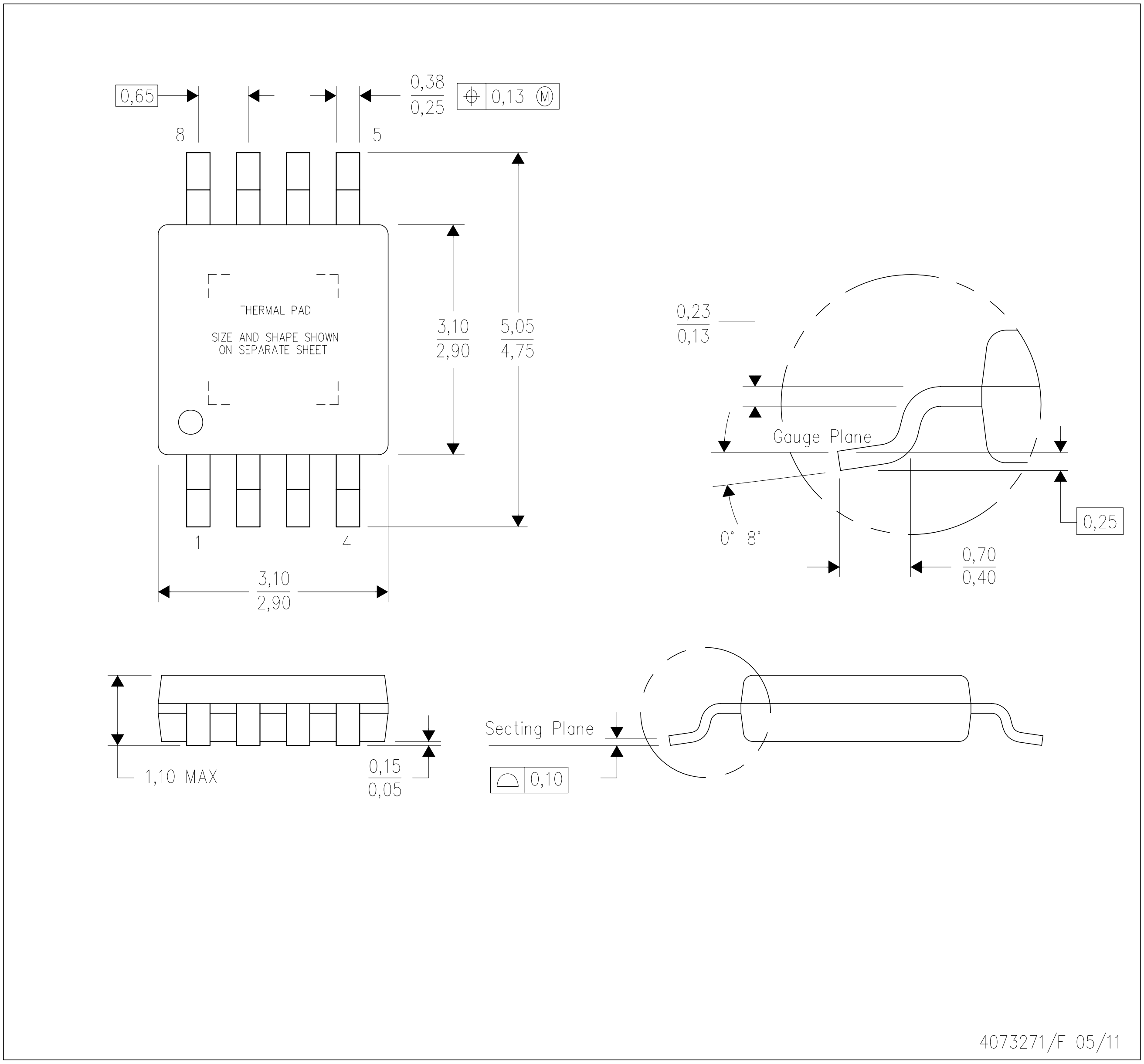
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2005D1DGNRQ1	MSOP-PowerPAD	DGN	8	2500	367.0	367.0	35.0
TPA2005D1DRBQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPA2005D1TDGNRQ1	MSOP-PowerPAD	DGN	8	2500	367.0	367.0	35.0

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–187 variation AA–T

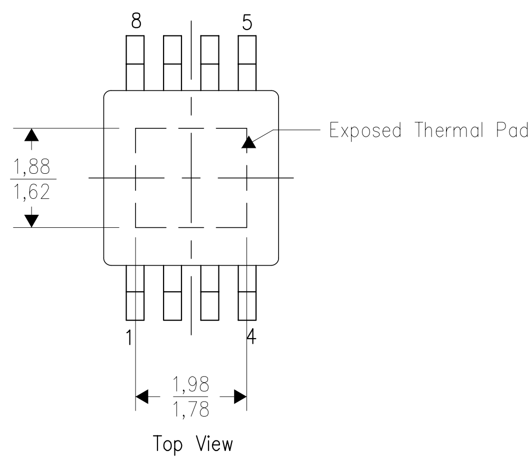
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

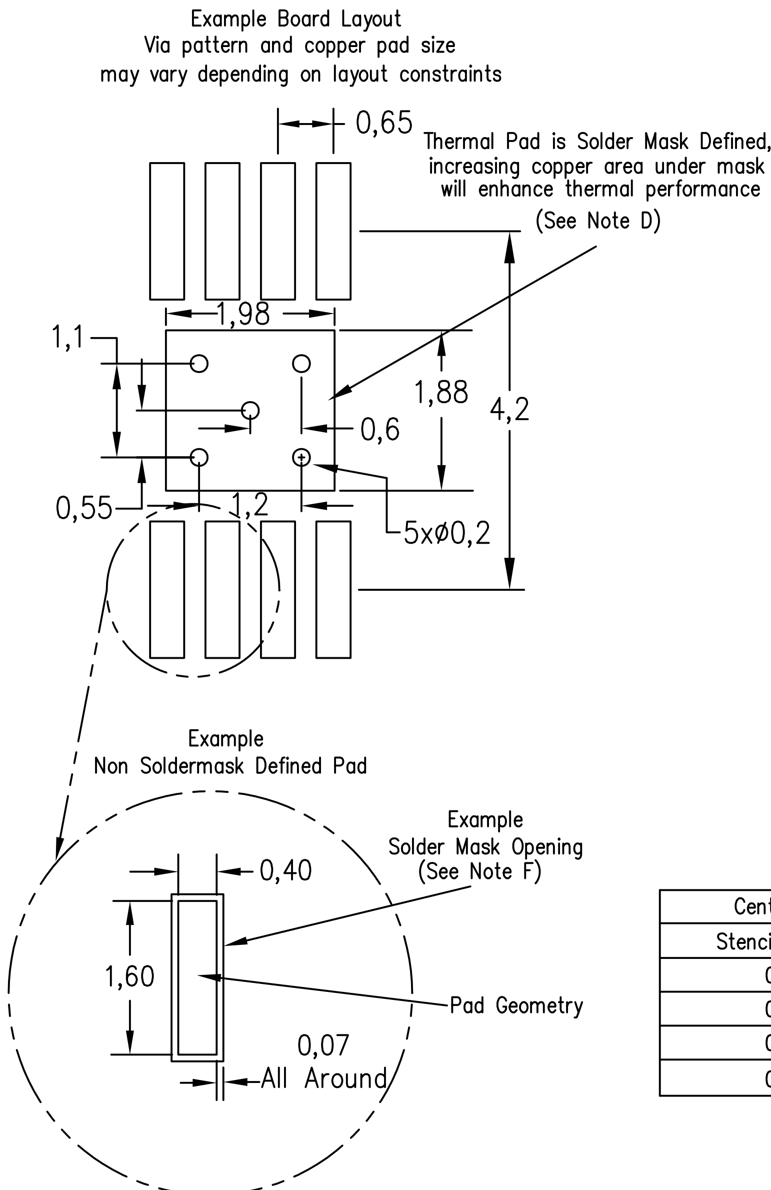


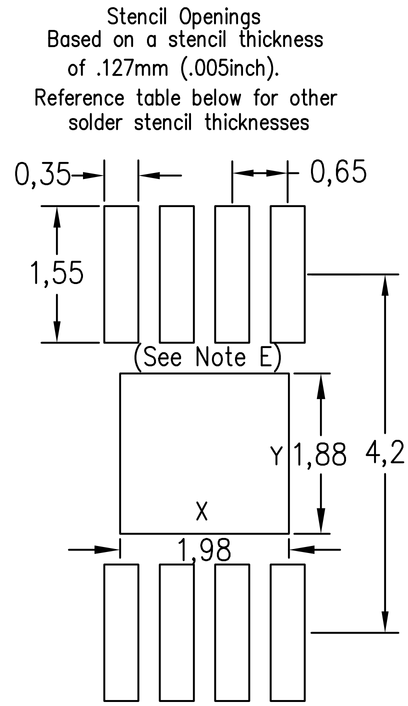
Exposed Thermal Pad Dimensions

4206323-3/I 12/11

NOTE: All linear dimensions are in millimeters

DGN (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



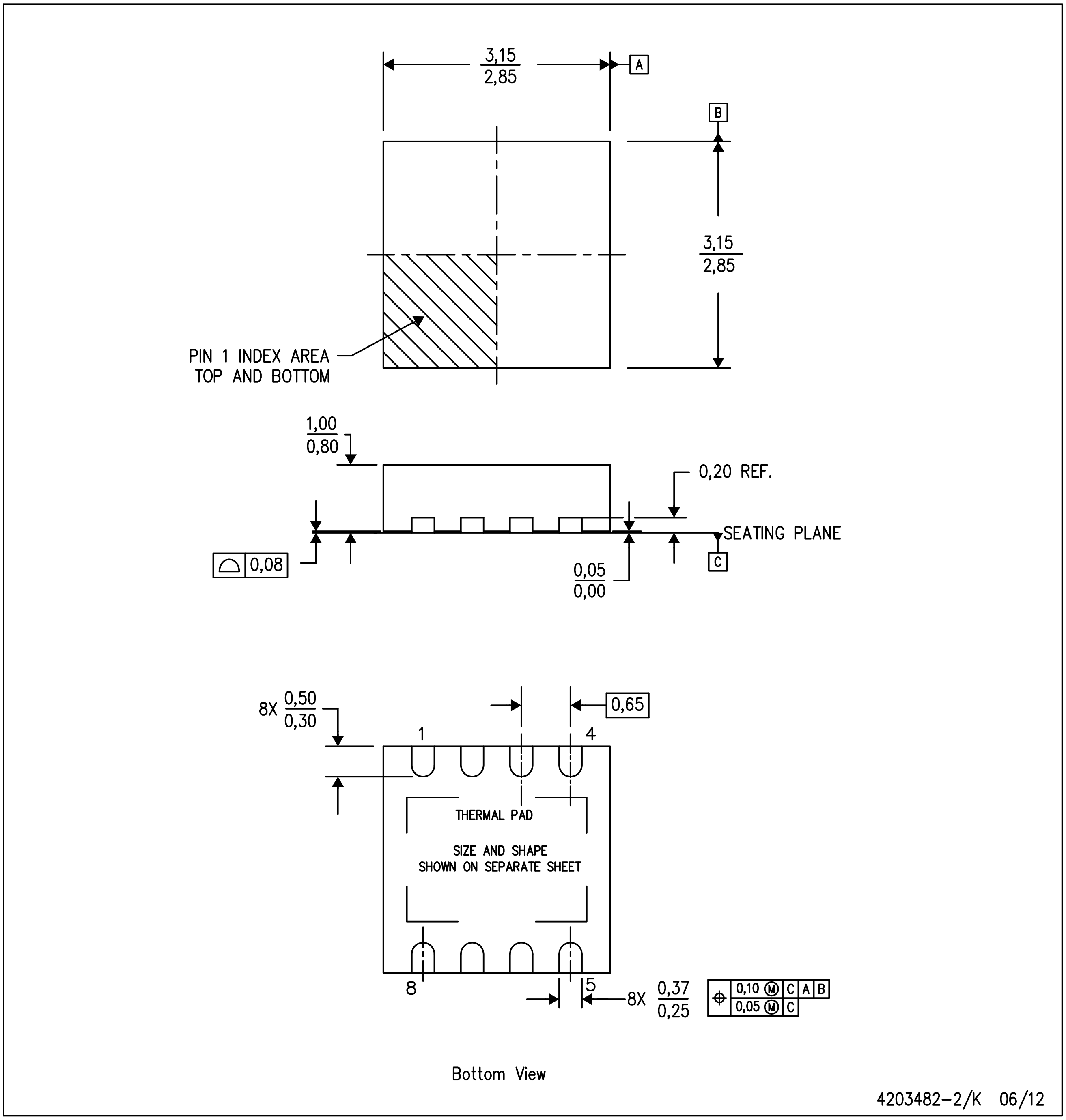


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.2	2.1
0.127mm	1.98	1.88
0.152mm	1.85	1.75
0.178mm	1.75	1.60

4207737-3/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

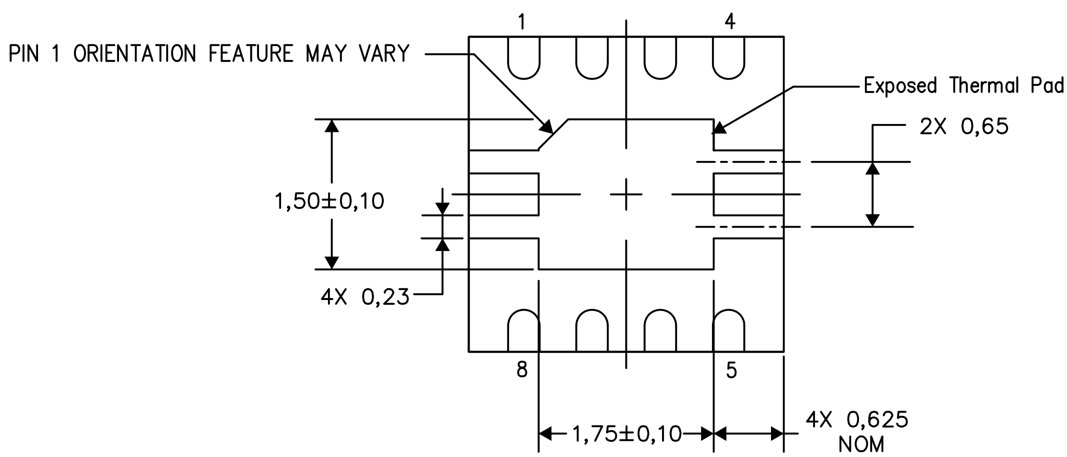
DRB (S-PVSON-N8) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



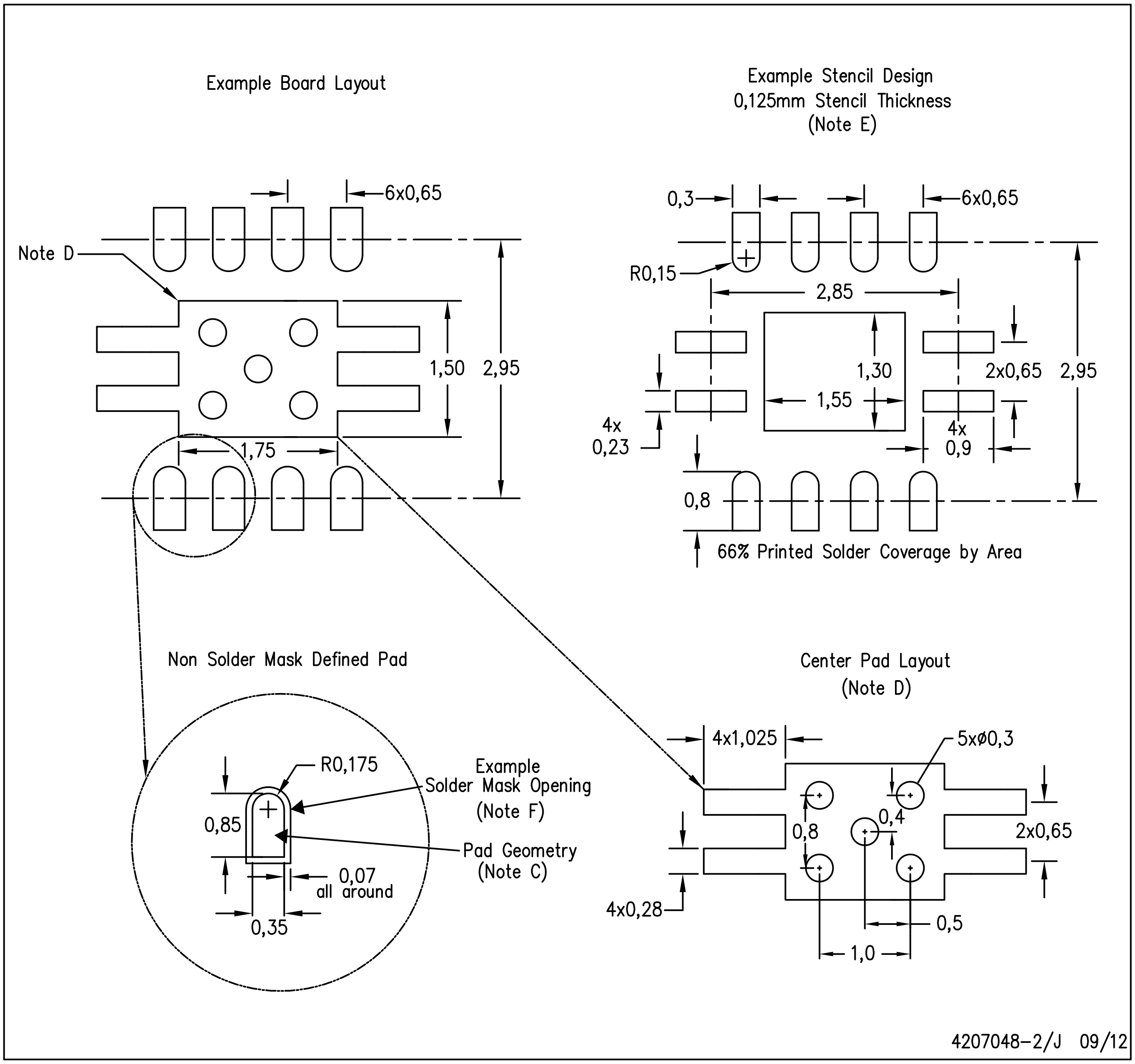
Bottom View

Exposed Thermal Pad Dimensions

4206340-2/N 09/12

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

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