OKI Semiconductor

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MSM5299C

80-DOT LCD SEGMENT DRIVER

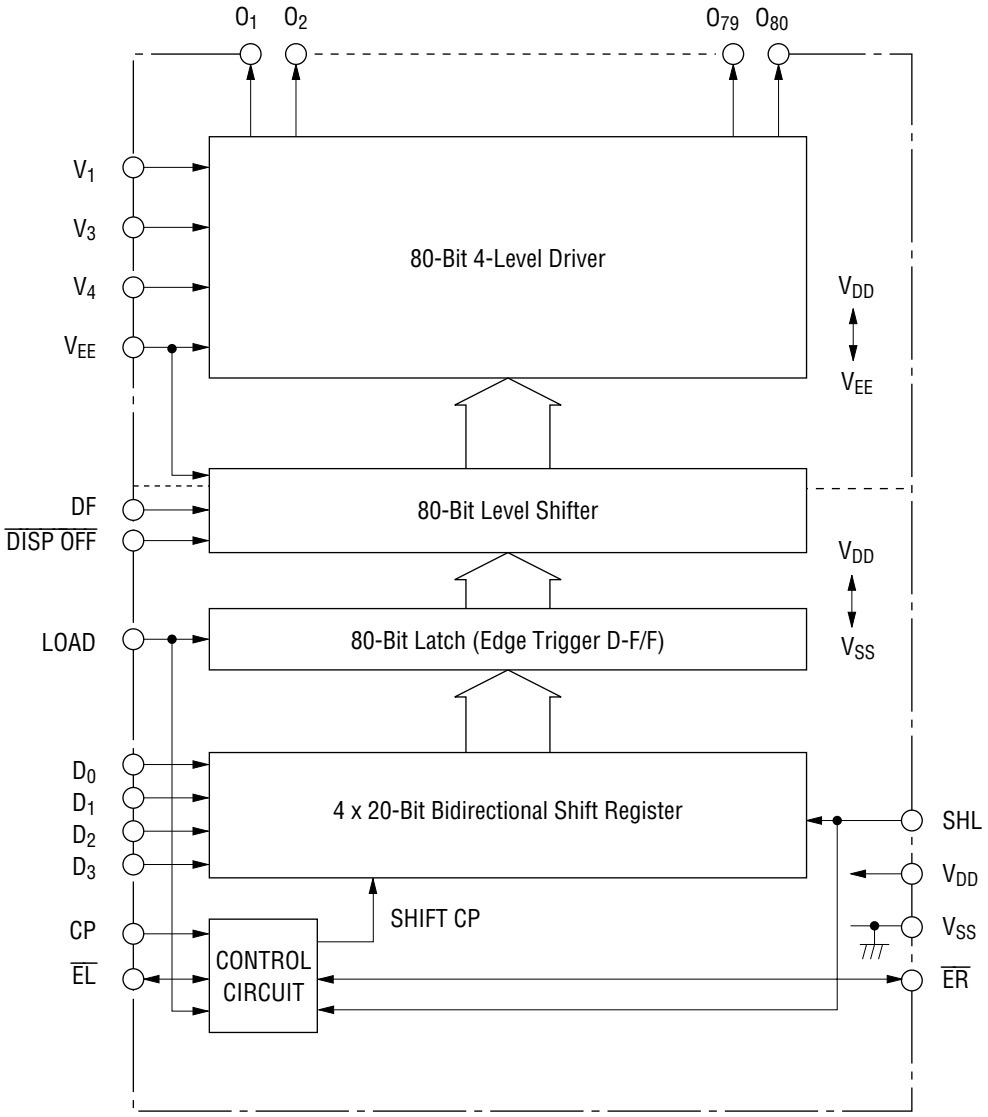
GENERAL DESCRIPTION

The MSM5299C is a dot matrix LCD segment driver LSI which is fabricated using CMOS low power metal gate technology. This LSI consists of an 80-bit bidirectional shift register, 80-bit latch, 80-bit level shifter, and 80-bit 4-level driver.
It receives the 4-bit parallel display data transferred from a microcomputer or an LCD controller LSI such as MSM6255, then outputs the LCD driving waveform to the LCD.
This LSI is improved with respect to timing between load and clock in the switching characteristics of MSM5299A. (t_{LC} = 200ns → 63ns)
However, note that the timing regulations for the load signal leading edge are added.

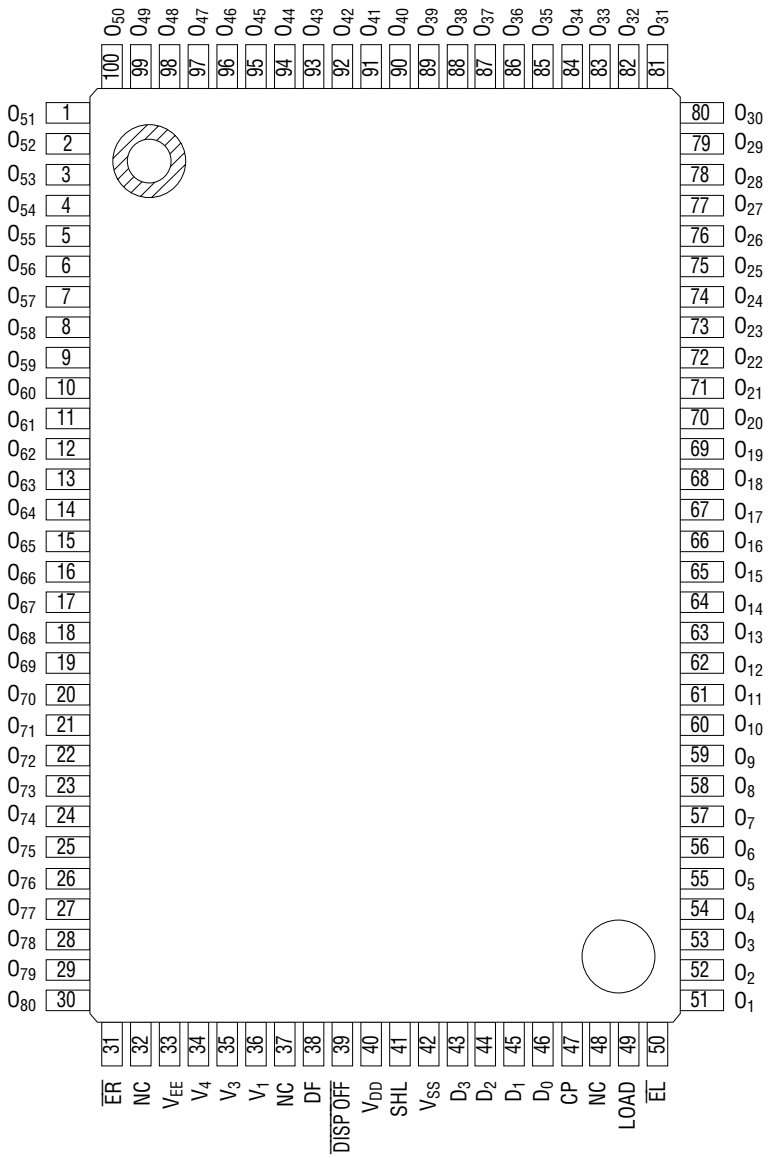
FEATURES

- Logic supply voltage : 4.5 to 5.5V
- LCD driving voltage : 8 to 28V
- Applicable LCD duty : 1/64 to 1/256
- LCD Output : 80
- 4-bit parallel data processing has improved the transfer speed to 1/4 that of the conventional serial transfer, thereby achieving low power consumption
- Can be interfaced with the LCD controller LSI MSM6255
- Applicable common driver : MSM5298A (68 outputs)
- Package options :
  100-pin plastic QFP (QFP100-P-1420-0.65-K) (Product name : MSM5299CGS-K)
  100-pin plastic QFP (QFP100-P-1420-0.65-BK) (Product name : MSM5299CGS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No connection

100-Pin Plastic QFP

Note : The abbreviated part number "M5299C" is imprinted on the package surface.

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	Ta = 25°C	–0.3 to +6	V
Supply Voltage (2)	V_{LCD}	Ta = 25°C, V_{DD}–V_{EE} *1	0 to 30	V
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

*1 $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Supply Voltage (1)	V_{DD}	—	4.5 to 5.5	V
Supply Voltage (2)	V_{LCD}	V_{DD}–V_{EE} *1	8 to 28	V
Operating Temperature	T_{op}	—	–20 to +85	°C

*1 $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5V ± 10%, Ta = –20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH} *1	—	$0.8V_{DD}$	—	V_{DD}	V
"L" Input Voltage	V_{IL} *1	—	V_{SS}	—	$0.2V_{DD}$	V
"H" Input Current	I_{IH} *1	$V_{IH} = V_{DD}$, V_{DD} = 5.5V	—	—	1	µA
L" Input Current	I_{IL} *1	V_{IL} = 0V, V_{DD} = 5.5V	—	—	–1	µA
"H" Output Voltage	V_{OH} *2	I_O = –0.2mA, V_{DD} = 4.5V	V_{DD} – 0.4	—	—	V
"L" Output Voltage	V_{OL} *2	I_O = 0.2mA, V_{DD} = 4.5V	—	—	0.4	V
ON Resistance	R_{ON} *4	$V_{DD} - V_{EE}$ = 23V *3 $\lvert V_N - V_O \rvert$ = 0.25V, V_{DD} = 4.5V	—	—	4	kΩ
Stand-by Current	I_{DDSBY}	f_{CP} = 1MHz, V_{DD} = 5.5V *5 $V_{DD} - V_{EE}$ = 26V, no load	—	—	200	µA
Supply Current (1)	I_{DD1}	f_{CP} = 1MHz, V_{DD} = 5.5V *6 $V_{DD} - V_{EE}$ = 26V, no load	—	—	3	mA
Supply Current (2)	I_V	f_{CP} = 1MHz, V_{DD} = 5.5V *7 $V_{DD} - V_{EE}$ = 26V, no load	—	—	±100	µA
Input Capacitance	C_I	f = 1MHz	—	5	—	pF

*1 Applicable to LOAD, CP, D_0 to D_3, $\overline{EL}$, $\overline{ER}$, SHL, DF, $\overline{DISP\ OFF}$ pins

*2 Applicable to $\overline{EL}$, $\overline{ER}$ pins.

*3 $V_N = V_{DD}$ to V_{EE}, $V_4 = \frac{13}{15}(V_{DD} - V_{EE})$, $V_3 = \frac{2}{15}(V_{DD} - V_{EE})$, $V_{DD} = V_1$

*4 Applicable to O_1 to O_{80} pins.

*5 Display data 1010, f_{DF} = 40 Hz, current that flows from V_{DD} to V_{SS} when the display data is not clocked in.

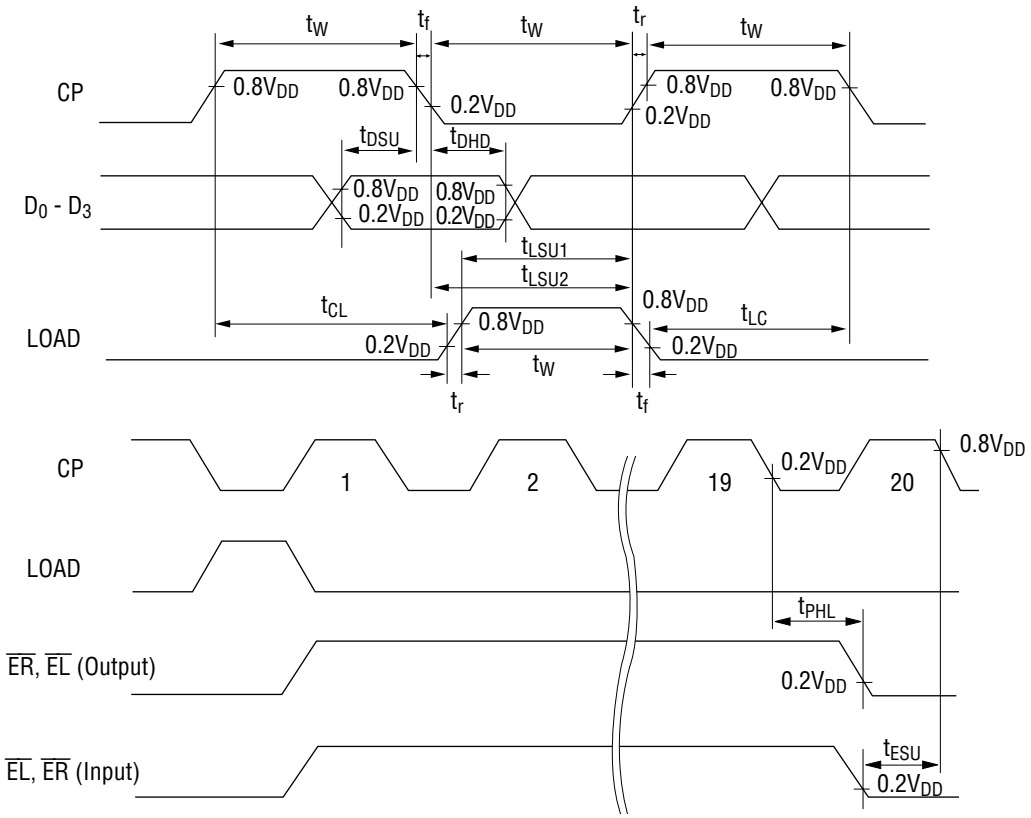
*6 Display data 1010, f_{DF} = 40 Hz, current that flows from V_{DD} to V_{SS} when the display data is clocked in.

*7 Display data 1010, f_{DF} = 40 Hz, current that flows to each of the V_1, V_3 and V_4 pins.

Switching Characteristics

(V_{DD} = 5V ± 10%, Ta = –20 to +75°C, C_L = 15pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	f_{CP}	DUTY=50%	—	—	3.4	MHz
Clock, Load Pulse Width	t_W	—	100	—	—	ns
Clock Pulse Rise/Fall Time	t_r, t_f	—	—	—	50	ns
Data Setup Time	t_{DSU}	—	50	—	—	ns
Data Hold Time	t_{DHD}	—	80	—	—	ns
Clock → Load Time	t_{CL}	—	63	—	—	ns
Load Setup Time	t_{LSU1}	—	90	—	—	ns
Load Setup Time	t_{LSU2}	—	90	—	—	ns
Load → Clock Time	t_{LC}	—	63	—	—	ns
Propagation Delay Time	t_{PHL}	—	—	—	224	ns
$\overline{ER}$, $\overline{EL}$ Setup Time	t_{ESU}	—	70	—	—	ns



FUNCTIONAL DESCRIPTION

Pin Functional Description

- **$\overline{ER}$, $\overline{EL}$**

Pin	Input/Output	SHL	Description
$\overline{ER}$	Input	L	Input pin to ENABLE F/F of MSM5299C.
$\overline{EL}$	Output		Output pin of ENABLE F/F. $\overline{EL}$ is connected to next MSM5299C's $\overline{ER}$ when MSM5299Cs are connected in series (cascade connection).
$\overline{EL}$	Input	H	Input pin to ENABLE F/F of MSM5299C.
$\overline{ER}$	Output		Output pin of ENABLE F/F. $\overline{ER}$ is connected to next MSM5299C's $\overline{EL}$ when MSM5299Cs are connected in series (cascade connection).

When a single MSM5299C device is used, $\overline{ER}$ ($\overline{EL}$) should be set at "L" level.

When a cascade connection is required, set the first MSM5299C's $\overline{ER}$ ($\overline{EL}$) pin at "L" level and connect the next MSM5299C's $\overline{EL}$ ($\overline{ER}$) pin to the further next MSM5299C's $\overline{ER}$ ($\overline{EL}$) pin.

- **CP**
  Clock pulse input pin for the 4-bit parallel shift register. The data is shifted to the 4-bit parallel shift register at the falling edge of the clock pulse.

- **SHL**
  $\overline{ER}$ and $\overline{EL}$ can be used as either an input pin or an output pin based on the H/L condition of SHL. The shift direction of each data (D_0 to D_3), the Input/Output condition of $\overline{ER}$ and $\overline{EL}$ and the H/L condition of SHL are described in the table below.

SHL	$\overline{ER}$	$\overline{EL}$	Shift direction
L	Input	Output	$D_0 \rightarrow O_1 \rightarrow O_5 \cdots\cdots\rightarrow O_{77}$ $D_1 \rightarrow O_2 \rightarrow O_6 \cdots\cdots\rightarrow O_{78}$ $D_2 \rightarrow O_3 \rightarrow O_7 \cdots\cdots\rightarrow O_{79}$ $D_3 \rightarrow O_4 \rightarrow O_8 \cdots\cdots\rightarrow O_{80}$
H	Output	Input	$D_0 \rightarrow O_{80} \rightarrow O_{76} \cdots\cdots\rightarrow O_4$ $D_1 \rightarrow O_{79} \rightarrow O_{75} \cdots\cdots\rightarrow O_3$ $D_2 \rightarrow O_{78} \rightarrow O_{74} \cdots\cdots\rightarrow O_2$ $D_3 \rightarrow O_{77} \rightarrow O_{73} \cdots\cdots\rightarrow O_1$ ↑ end data ↑ start data

- **D_0, D_1, D_2, D_3**
  Display data input pins for 4×20-bit shift register. The display data is clocked into these pins. The combinations of D_0 to D_3, DF signal level, display data output level and the display on the LCD panel are described in the table below.

D_0 - D_3	DF	Liquid crystal drive output	Liquid crystal dispaly
L	L	Non-select level (V_3)	OFF
H	L	Select level (V_1)	ON
L	H	Non-select level (V_4)	OFF
H	H	Select level (V_{EE})	ON

- **LOAD**
  The signal for latching the shift register contents is input to this pin. The display data stored in the shift register is latched at the falling edge of the LOAD pulse.

- **DF**
  Alternate signal input pin for LCD driving. Frame inversion signal is input to this pin.

- **V_{DD}, V_{SS}**
  Supply voltage pins. V_{DD} should be 4.5 to 5.5V. V_{SS} is a ground pin (V_{SS} = 0V).

- **V_1, V_3, V_4, V_{EE}**
  Bias supply voltage pin to drive the LCD. Bias voltage to drive the LCD is supplied from an external source.

- **O_1 to O_{80}**
  Display data output pins which correspond to the respective latch contents. One of V_1, V_3, V_4 and V_{EE} is selected as a display driving voltage source based on the combination of the latched data level and DF signal. (Refer to the Truth Table).
  The outputs O_1 to O_{80} are connected to the segment side of the LCD panel.

- **$\overline{\text{DISP OFF}}$**
  Input pin for controlling the outputs of O_1 to O_{80}. V_1 level is output from O_1 to O_{80} pins during "L" level input. Refer to the Truth Table.

Truth Table

DF	Latched data	$\overline{\text{DISP OFF}}$	Driver output level (O_1-O_{80})
L	L	H	V_3
L	H	H	V_1
H	L	H	V_4
H	H	H	V_{EE}
X	X	L	V_1

NOTES ON USE

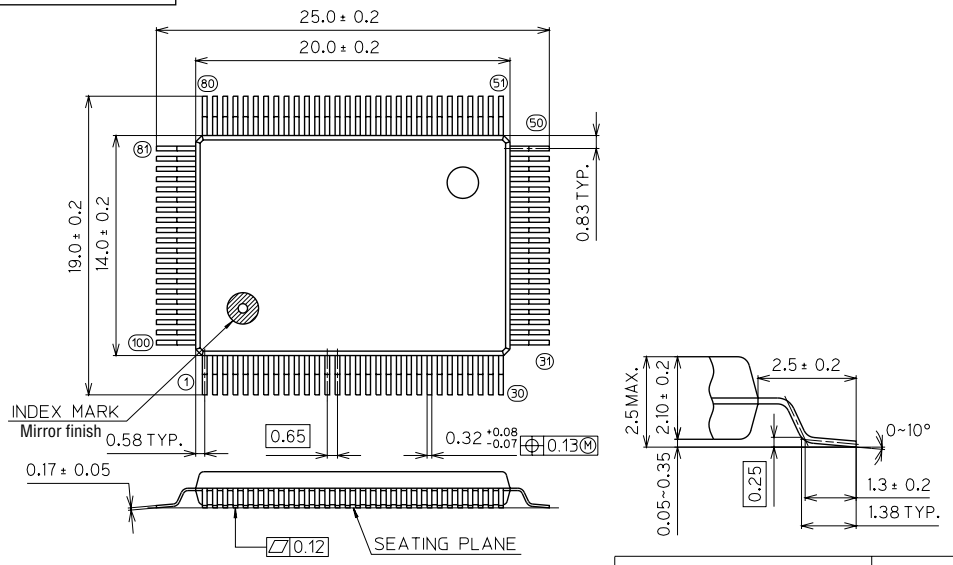
Note the following when turning power on and off :
The LCD drivers of this IC require a high voltage. For this reason, if a high voltage is applied to the LCD drivers with the logic power supply floating, excess current flows. This may damage the IC. Be sure to carry out the follwing power-on and power-off sequences :

When turning power on :
First V_{DD} ON, next V_{EE}, V_4, V_3, V_1 ON. Or both ON at the same time.
When turning power off :
First V_{EE}, V_4, V_3, V_1 OFF, next V_{DD} OFF. Or both OFF at the same time.

PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-K



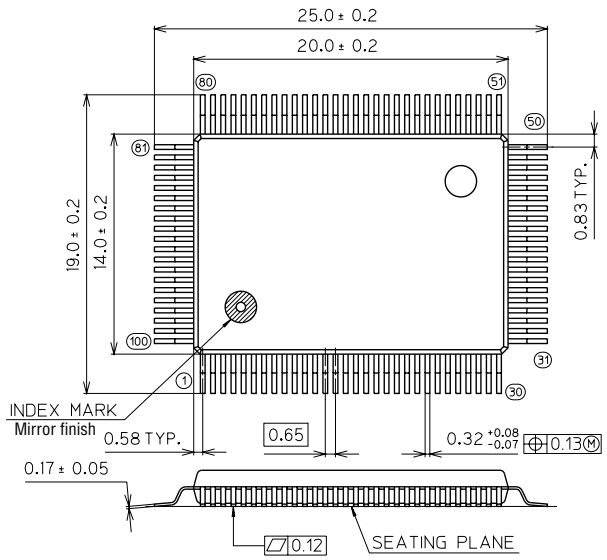
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.29 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP100-P-1420-0.65-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.29 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
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