HANBit

SRAM MODULE 2Mbyte (512K x 32-Bit), LOW POWER, 72-Pin SIMM 5V **Part No. HMS51232M4L**

GENERAL DESCRIPTION

The HMS51232M4L is a static random access memory (SRAM) module containing 524,288 words organized in a x32-bit configuration. The module consists of four 512K x 8 SRAMs mounted on a 72-pin, single-sided, FR4-printed circuit board.

The HMS51232M4L also support low data retention voltage for battery back-up operations with low data retention current. Four chip enable inputs, (/CE_UU1, /CE_UM1, /CE_LM1 and /CE_LL1) are used to enable the module's 4 bytes independently. Output enable (/OE) and write enable (/WE) can set the memory input and output.

Data is written into the SRAM memory when write enable (/WE) and chip enable (/CE) inputs are both LOW.

Reading is accomplished when /WE remains HIGH and /CE and output enable (/OE) are LOW.

For reliability, this SRAM module is designed as multiple power and ground pin. All module components may be powered from a single +5V DC power supply and all inputs and outputs are fully TTL-compatible.

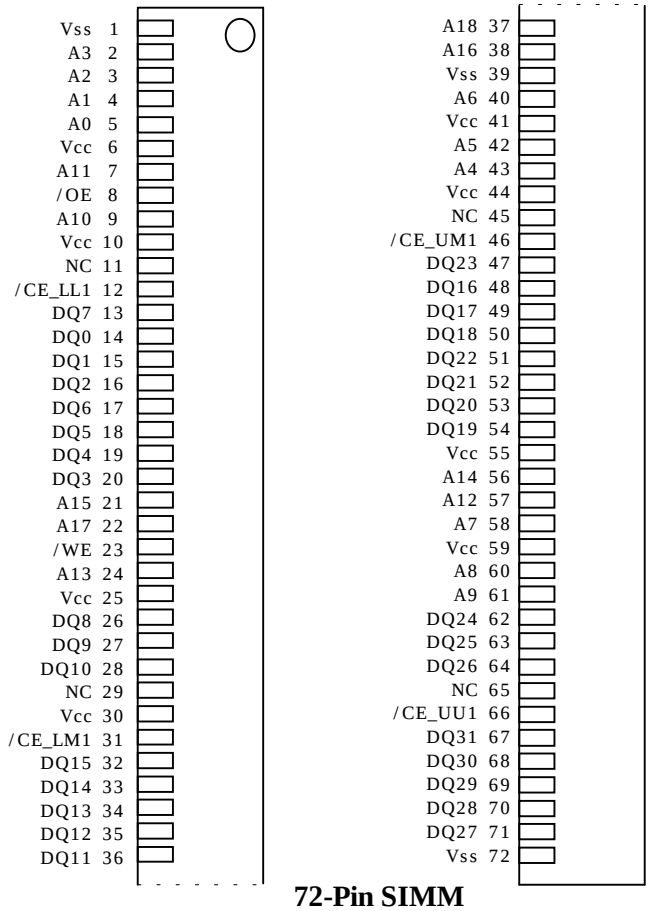
FEATURES

- Access time : 55, 70ns
- High-density 2MByte design
- High-reliability, low-power design
- Single +5V ±0.5V power supply
- Low data retention voltage : 2V(min)
- Three state output and TTL-compatible
- FR4-PCB design
- Low profile 72-Pin SIMM

OPTIONS MARKING

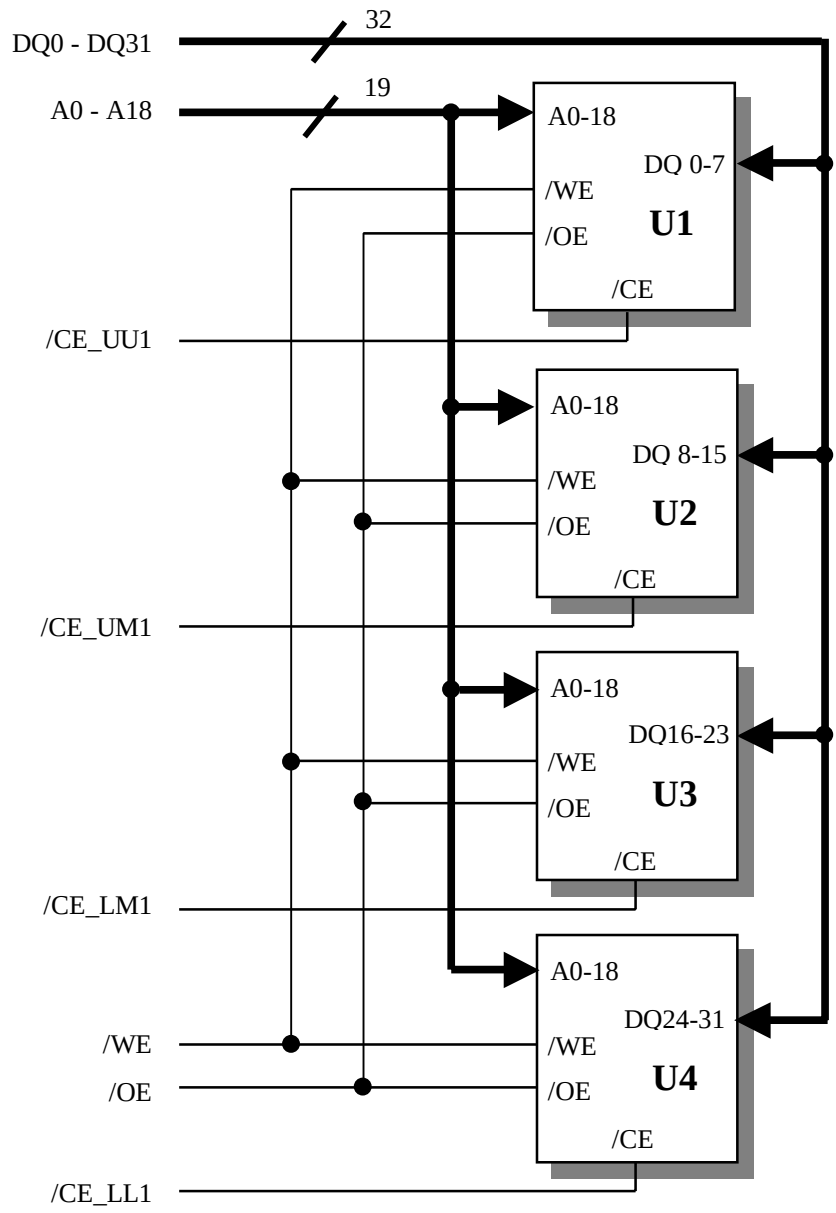
- Timing
  - 55ns access -55
  - 70ns access -70
- Packages
  - 72-pin SIMM M

PIN ASSIGNMENT



72-Pin SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Dout	ACTIVE
WRITE	X	L	L	Din	ACTIVE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5V to +7.0V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5V to +7.0V
Power Dissipation	P_D	4W
Storage Temperature	T_{STG}	-65°C to +150°C
Operating Temperature	T_A	0°C to +70°C

- Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V_{CC}	4.5V	5.0V	5.5V
Ground	V_{SS}	0	0	0
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5V**
Input Low Voltage	V_{IL}	-0.5*	-	0.8V

* V_{IL}(Min.) = -2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

****** V_{IH}(Min.) = Vcc+2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

DC AND OPERATING CHARACTERISTICS (1)(0°C ≤ T_A ≤ 70 °C ; Vcc = 5V ± 0.5V)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V_{IN} = Vss to Vcc	IL_I	-4	4	µA
Output Leakage Current	/CE=V_{IH} or /OE =V_{IH} or /WE=V_{IL} V_{OUT}=Vss to V_{CC}	IL_0	-4	4	µA
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V

* Vcc=5.0V, Temp=25 °C

DC AND OPERATING CHARACTERISTICS (2)

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX -55	MAX -70	UNIT
Power Supply Current:Operating	I_{IO}=0mA,/CE=V_{IL}, V_{IN}=V_{IL} or V_{IH}, Read	l_{CC}	60	60	mA
Power Supply Current:Standby	/CE=V_{IH}, Other inputs=V_{IL} or V_{IH}	l_{SB}	12	12	mA
	/CE≥Vcc-0.2V, Other inputs=0~Vcc	l_{SB1}	400	400	μA

CAPACITANCE

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX	UNIT
Input /Output Capacitance	$V_{I/O}$=0V	$C_{I/O}$	32	pF
Input Capacitance	V_{IN}=0V	C_{IN}	40	pF

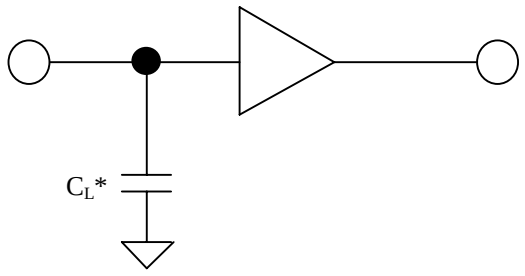
* **NOTE** : Capacitance is sampled and not 100% tested

AC CHARACTERISTICS ($0^{o}C \le T_A \le 70\ ^{o}C$; Vcc = 5V ± 0.5V, unless otherwise specified)

TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=100pF + 1TTL

* See test condition of DC and Operating characteristics



* Including scope and jig capacitance

READ CYCLE

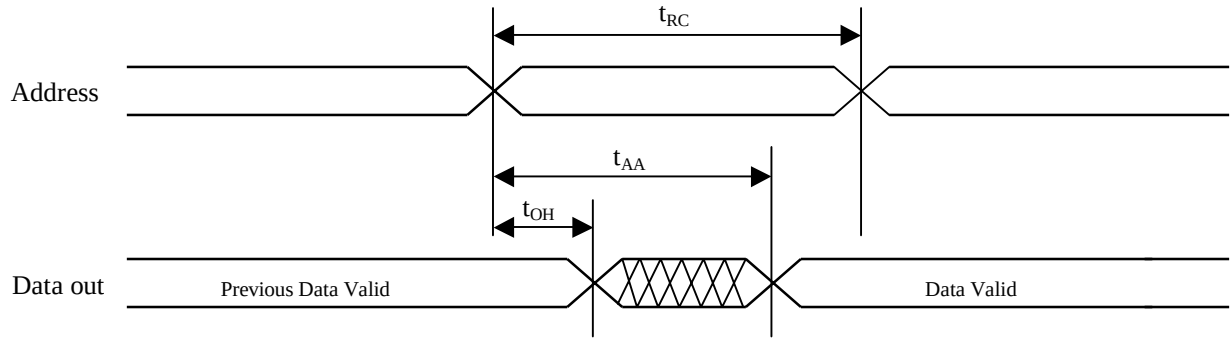
PARAMETER	SYMBOL	-55		-70		UNIT
		MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	55		70		ns
Address Access Time	t_{AA}		55		70	ns
Chip Select to Output	t_{CO}		55		70	ns
Output Enable to Output	t_{OE}		25		35	ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Enable to Low-Z Output	t_{LZ}	10		10		ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	25	ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	25	ns
Output Hold from Address Change	t_{OH}	10		10		ns

WRITE CYCLE

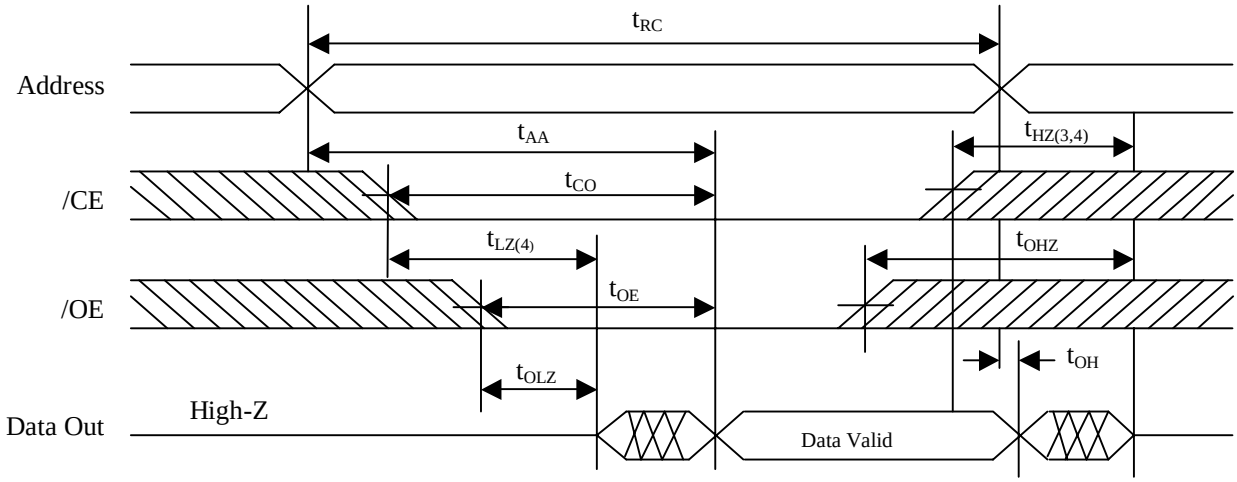
PARAMETER	SYMBOL	-55		-70		UNIT
		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	55		70		ns
Chip Select to End of Write	t_{CW}	45		60		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	45		60		ns
Write Pulse Width	t_{WP}	40		50		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	20	0	25	ns
Data to Write Time Overlap	t_{DW}	25		30		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(Address Controlled) (/CE = /OE = V_{IL} , /WE = V_{IH})



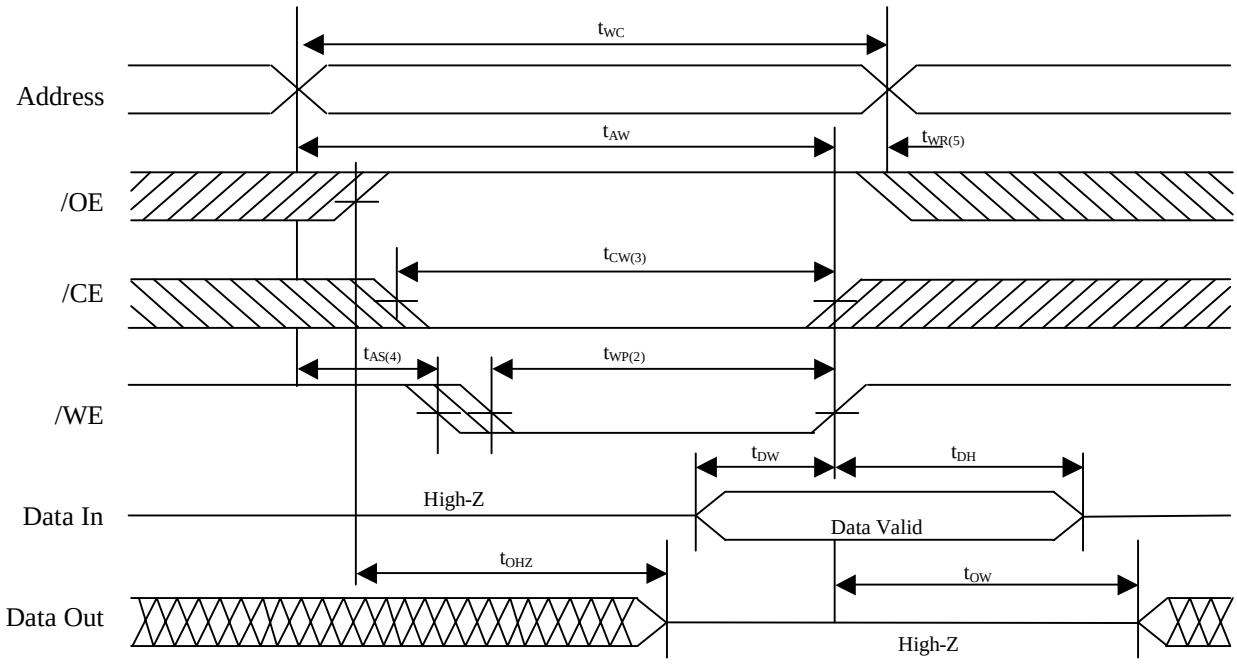
TIMING WAVEFORM OF READ CYCLE (/WE = V_{IH})



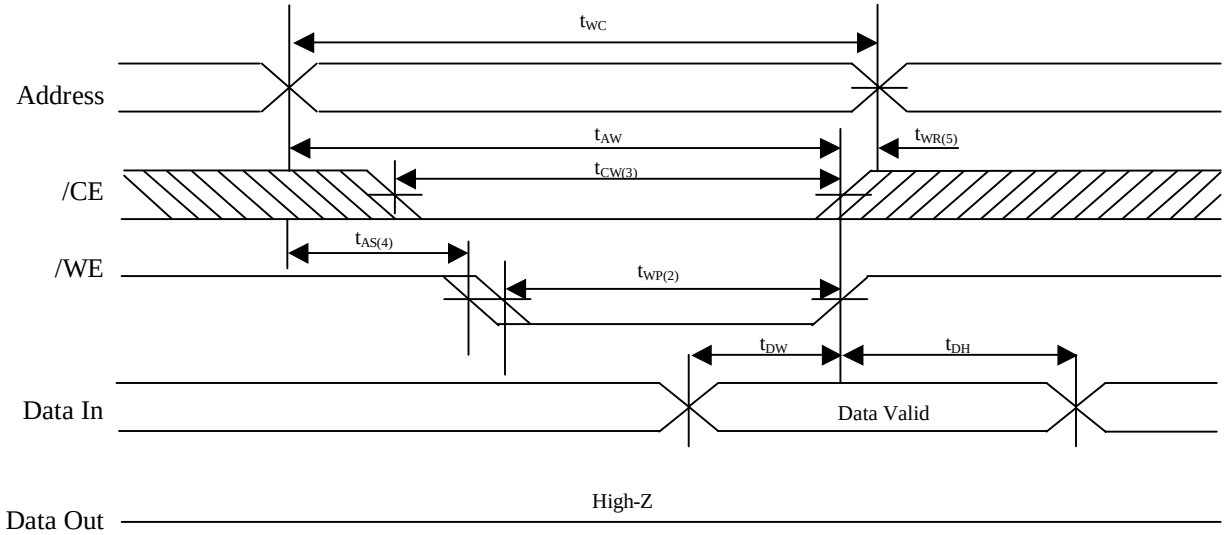
Notes (Read Cycle)

1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/CE Controlled)



Notes(Write Cycle)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CE and a low /WE. A write begins at the latest transition among /CE going low and /WE going low : A write ends at the earliest transition among /CE going high and/WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CE going low to the end of write.

4. t_{AS} is measured from the address valid to the beginning of wirte.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as/CE, or /WE going high.

FUNCTIONAL DESCRIPTION

/CE	/WE	/OE	MODE	I/O PIN	SUPPLY CURRENT
H	X*	X	Not Select	High-Z	l_{SB}, l_{SB1}
L	H	H	Output Disable	High-Z	l_{CC}
L	H	L	Read	D_{OUT}	l_{CC}
L	L	X	Write	D_{IN}	l_{CC}

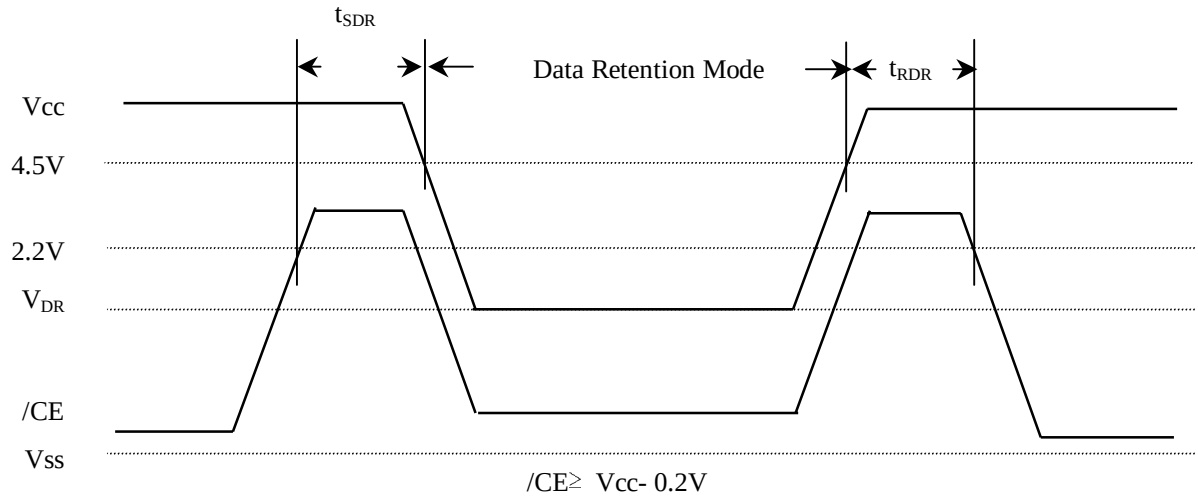
Note: X means Don't Care

DATA RETENTION CHARACTERISTICS* (TA = 0 to 70 ℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
V_{CC} for Data Retention	V_{DR}	/CE≥ V_{CC}-0.2V	2	5.5	V
Data Retention Current	I_{DR}	V_{CC}=3.0V, /CE≥ V_{CC}-0.2V V_{IN}≥ V_{CC}-0.2V or V_{IN}≤ 0.2V	-	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention	0	-	ns
Recovery Time	t_{RDR}	Wave forms(below)	5	-	ns

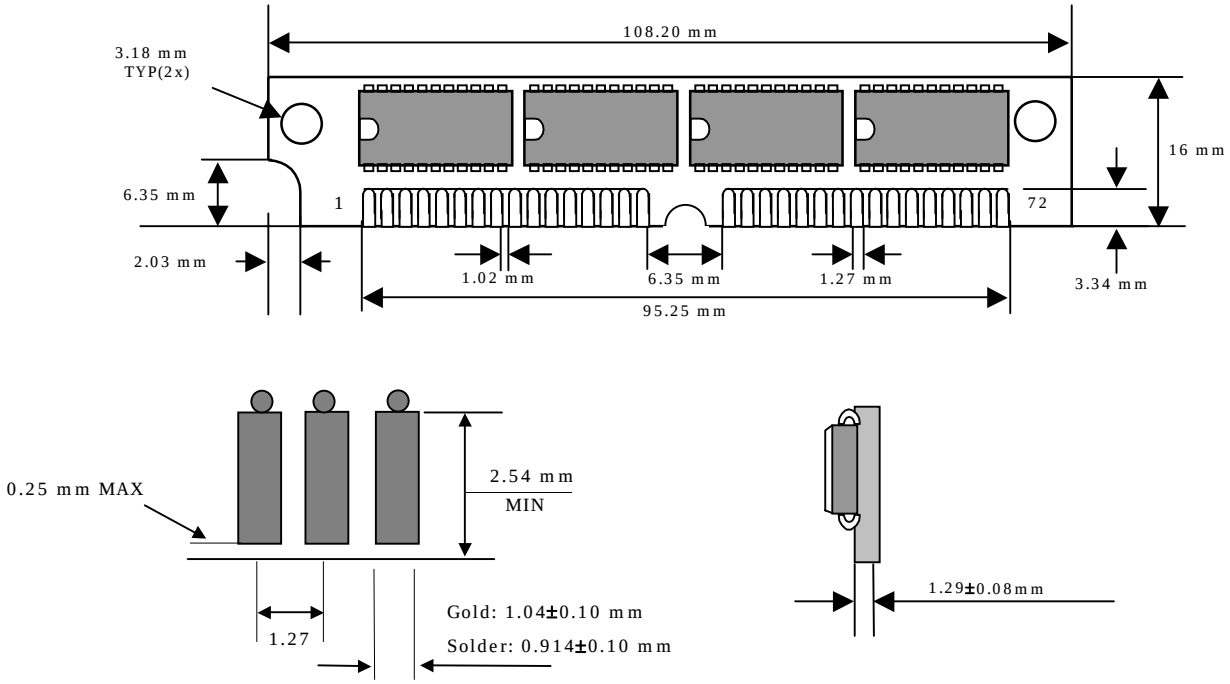
* L-Version Only

DATA RETENTION WAVEFORM 1 (/CE Controlled)



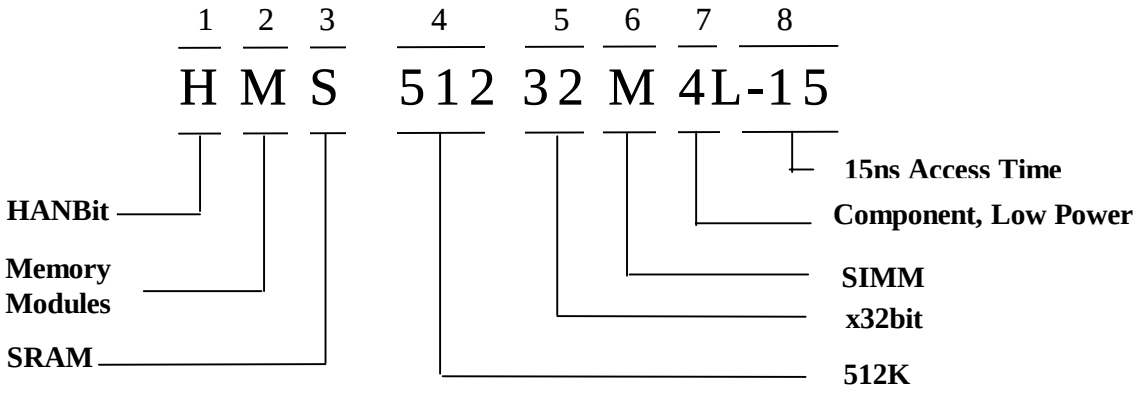
PACKAGING INFORMATION

SIMM Design



(Solder & Gold Plating Lead)

ORDERING INFORMATION



1. - Product Line Identifier
HANBit ---------- H
2. - Memory Modules
3. - SRAM
4. - Depth : 512K
5. - Width : x 32bit
6. - Package Code
SIMM ---------- M
ZIP ---------- Z

7. - Number of Memory Components, Low Power -------L
8. - Access time
10 ---------- 10ns
12 ---------- 12ns
15 ---------- 15ns
17 ---------- 17ns
20 ---------- 20ns