EVALUATION KIT AVAILABLE

MAX34460

PMBus 12-Channel Voltage Monitor and Sequencer

General Description

The MAX34460 is a system monitor that is capable of managing up to 12 power supplies. The power-supply manager monitors the power-supply output voltages and constantly checks for user-programmable overvoltage and undervoltage thresholds. If a fault is detected, the device automatically shuts down the system in an orderly fashion. The device can sequence the supplies in any order at both power-up and power-down. With the addition of external current DACs, the device has the ability to close-loop margin the power-supply output voltages up or down to a user-programmable level. The device contains an internal temperature sensor and can support up to four external remote temperature sensors. Once configured, the device can operate autonomously without any host intervention.

Applications

Network Switches/Routers

Base Stations

Servers

Smart Grid Network Systems

Ordering Information and Typical Operating Circuit appear at end of data sheet.

Features

- **12 Channels of Power-Supply Management**
- **Power-Supply Voltage Measurement and Monitoring**
- **Fast Minimum/Maximum Threshold Excursion Detection**
- **Remote Ground Sensing Improves Measurement Accuracy**
- **Automatic Closed-Loop Margining**
- **Programmable Up and Down Time-Based or Event-Based Sequencing**
- **Supports Dual-Sequencing Groups**
- **Supports Up to Five Temperature Sensors (One Internal/Four Remote)**
- **Fault Detection on All Temperature Sensors**
- **Programmable Alarm Outputs**
- **Reports Peak and Average Levels for a Number of Parameters**
- **Watchdog Timer Function**
- **PMBus™-Compliant Command Interface**
- **I²C/SMBus-Compatible Serial Bus with Bus Timeout Function**
- **On-Board Nonvolatile Black Box Fault Logging and Default Configuration Setting**
- **Expandable Channel Operation with Parallel Devices**
- **Up to 20 GPOs**
- **No External Clocking Required**
- **3.0V to 3.6V Supply Voltage**

PMBus is a trademark of SMIF, Inc.

For related parts and recommended products to use with this part, refer to: www.maximintegrated.com/MAX34460.related

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6486; Rev 0; 9/12

PMBus 12-Channel Voltage Monitor and Sequencer

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ABSOLUTE MAXIMUM RATINGS

V_{DD} and V_{DDA} to V_{SS} ..... -0.3V to +4.0V
RSG0 and RSG1 to V_{SS} ..... -0.3V to +0.3V
All Other Pins Except REG18
Relative to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)*
REG18 to V_{SS} ..... -0.3V to +2.0V

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 26.3mW/°C above +70°C) 2105.3mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10s) ..... +260°C
Soldering Temperature (reflow) ..... +260°C

**Subject to not exceeding +4.0V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Operating Voltage Range	V_{DD}	(Note 1)	3.0		3.6	V
Input Logic 1 (Except I²C Pins)	V_{IH1}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Logic 0 (Except I²C Pins)	V_{IL1}		-0.3		+0.3 x V_{DD}	V
Input Logic 1: SCL, SDA, MSCL, MSDA	V_{IH2}		2.1		V_{DD} + 0.3	V
Input Logic 0: SCL, SDA, MSCL, MSDA	V_{IL2}		-0.3		+0.8	V
Source Impedance to RS		ADC_TIME[1:0] = 00			1	kΩ
		ADC_TIME[1:0] = 01			5	
		ADC_TIME[1:0] = 10			10	
		ADC_TIME[1:0] = 11			20	

ELECTRICAL CHARACTERISTICS

(V_{DD} and V_{DDA} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD}/V_{DDA} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Supply Current	I_{CPU}	(Note 2)		12		mA
	$I_{PROGRAM}$			18		
System Clock Error	$f_{ERR:MOSC}$	+25°C < T_A < +85°C	-3		+3	%
		-40°C < T_A < +25°C	-4		+4	
Output Logic-Low (Except I²C Pins)	V_{OL1}	I_{OL} = 4mA (Note 1)			0.4	V
Output Logic-High (Except I²C Pins)	V_{OH1}	I_{OH} = -2mA (Note 1)	V_{DD} - 0.5			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} and V_{DDA} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD}/V_{DDA} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic-Low SCL, SDA, MSCL, MSDA	V_{OL2}	I_{OL} = 4mA (Note 1)			0.4	V
SCL, SDA, MSCL, MSDA Leakage	IL_{I2C}	V_{DD} = 0V or unconnected			±5	µA
CONTROL Threshold				2.048		V
CONTROL Hysteresis				50		mV
ADC						
ADC Bit Resolution				12		Bits
ADC Conversion Time		ADC_TIME[1:0] = 00		1000		ns
ADC Full Scale	V_{FS}	T_A = 0°C to +85°C	2.032	2.048	2.064	V
ADC Measurement Resolution	V_{LSB}			500		µV
RS Input Capacitance	C_{RS}			15		pF
RS Input Leakage	IL_{RS}			±0.25		µA
ADC Integral Nonlinearity	INL			±1		LSB
ADC Differential Nonlinearity	DNL			±1		LSB
TEMPERATURE SENSOR						
Internal Temperature-Measurement Error		T_A = -40°C to +85°C		±2		°C
FLASH						
Flash Endurance	N_{FLASH}		20,000			Write Cycles
Data Retention		T_A = +50°C	100			Years
STORE_DEFAULT_ALL Write Time				70		ms
MFR_STORE_SINGLE Write Time				310		µs
RESTORE_DEFAULT_All Time				70		ms
MFR_NV_FAULT_LOG Write Time		Writing 1 fault log		11		ms
MFR_NV_FAULT_LOG Delete Time		Deleting all fault logs		200		ms
MFR_NV_FAULT_LOG Overwrite Time				40		ms
TIMING OPERATING CHARACTERISTICS						
Voltage Sample Rate		Threshold excursion (Note 3)		48		µs
		Data collection		5		ms
Temperature Sample Rate				1000		ms
Device Startup Time				135		ms

I²C/SMBus INTERFACE ELECTRICAL SPECIFICATIONS

(V_{DD} and V_{DDA} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD}/V_{DDA} = 3.3V, T_A = +25°C.)

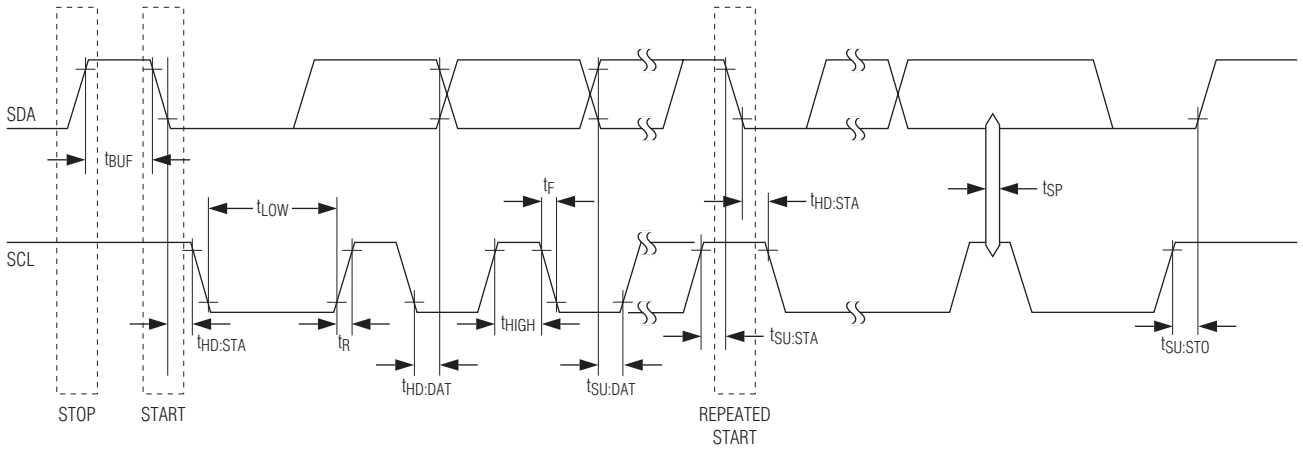
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		10		400	kHz
MSCL Clock Frequency	f_{MSCL}			100		kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$	Receive	0			ns
		Transmit	300			ns
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R				300	ns
SDA and SCL Fall Time	t_F				300	ns
Stop Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Time Out	t_{TO}		25	27	35	ms

Note 1: All voltages are referenced to ground. Current entering the device are specified as positive and currents exiting the device are negative.

Note 2: This does not include pin input/output currents.

Note 3: The round-robin threshold excursion rate can be changed with the ADC_AVERAGE and ADC_TIME bits in MFR_MODE from 12µs (no averaging and 1µs conversion) to 768µs (8x averaging and 8µs conversion).

I²C/SMBus Timing

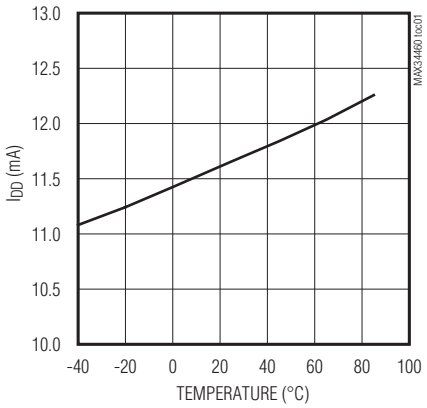


NOTE: TIMING IS REFERENCED TO $V_{IL(MAX)}$ AND $V_{IH(MIN)}$.

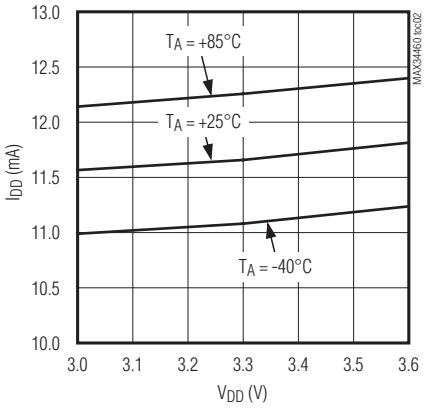
Typical Operating Characteristics

(V_{DD} = 3.3V and T_A = +25°C, unless otherwise noted.)

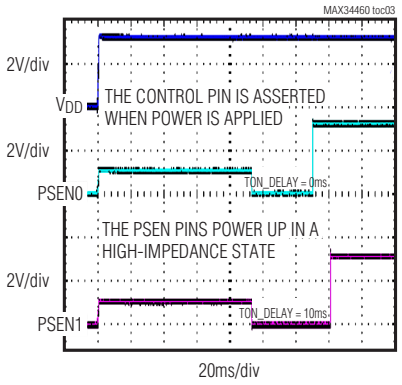
SUPPLY CURRENT vs. TEMPERATURE



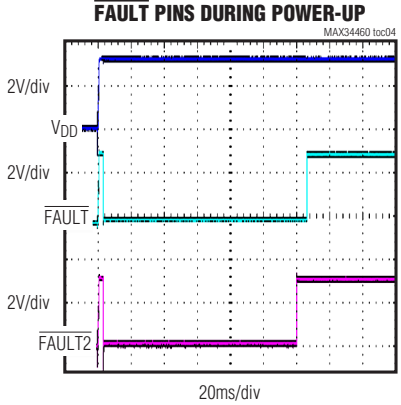
SUPPLY CURRENT vs. SUPPLY VOLTAGE



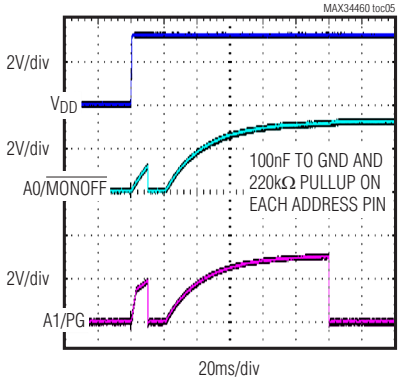
PSEN OUTPUTS DURING POWER-UP



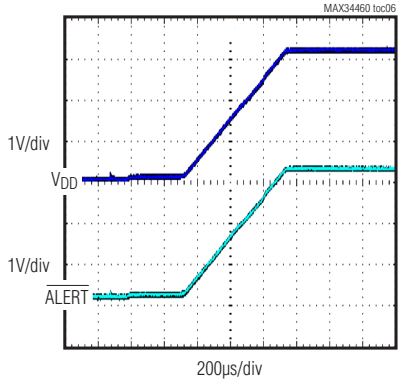
$\overline{\text{FAULT}}$ PINS DURING POWER-UP



ADDRESS PINS DURING POWER-UP



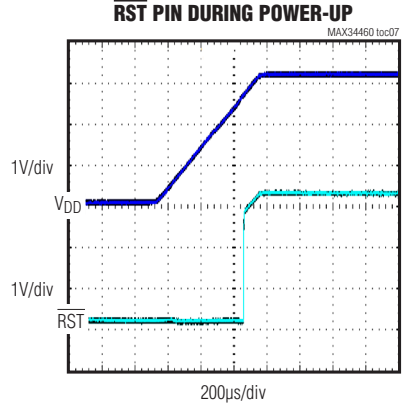
$\overline{\text{ALERT}}$ PIN DURING POWER-UP



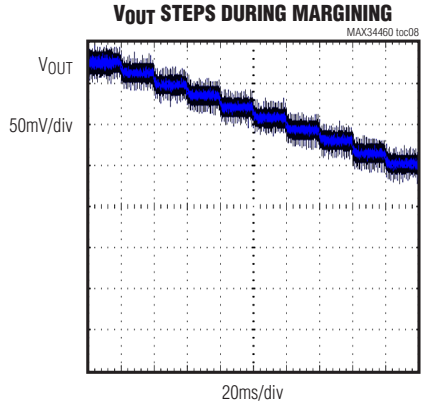
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V and T_A = +25°C, unless otherwise noted.)

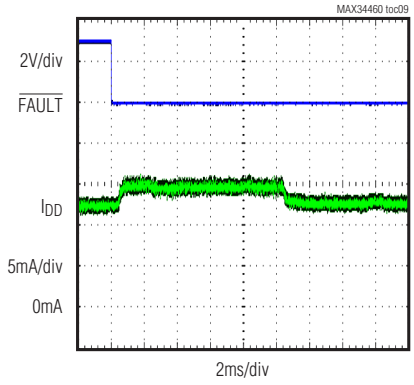
$\overline{RST}$ PIN DURING POWER-UP



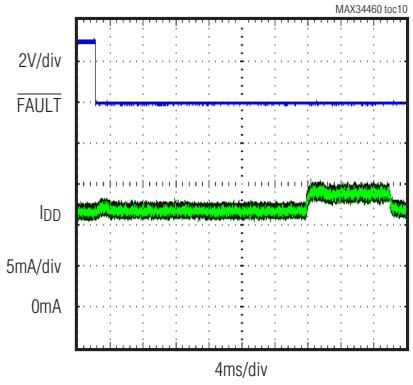
V_{OUT} STEPS DURING MARGINING



I_{DD} vs. TIME DURING A NONVOLATILE LOG WRITE

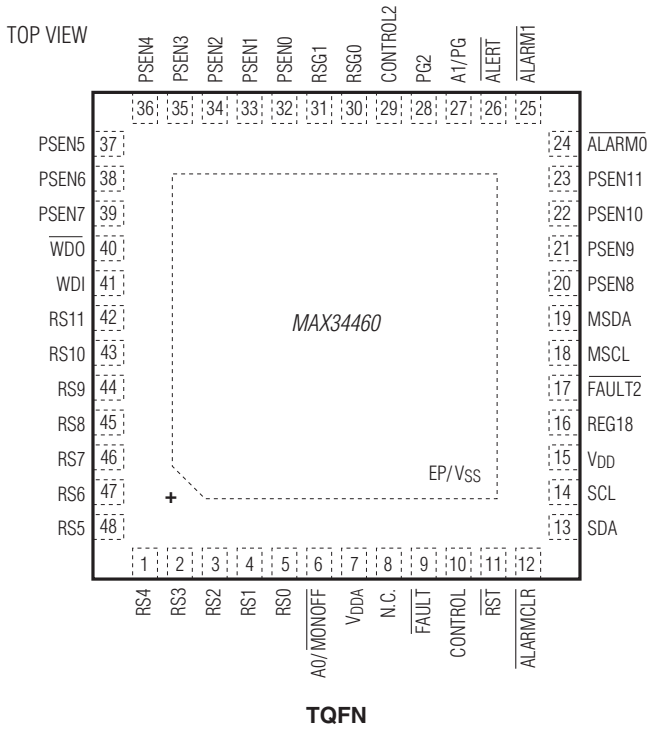


I_{DD} vs. TIME DURING A NONVOLATILE LOG WRITE WITH OVERWRITE ENABLED



PMBus 12-Channel Voltage Monitor and Sequencer

Pin Configuration



TQFN

Pin Description

PIN*	NAME	TYPE**	FUNCTION
1	RS4	AI	ADC Voltage-Sense Input 4. Connect to V_{SS} if unused.
2	RS3	AI	ADC Voltage-Sense Input 3. Connect to V_{SS} if unused.
3	RS2	AI	ADC Voltage-Sense Input 2. Connect to V_{SS} if unused.
4	RS1	AI	ADC Voltage-Sense Input 1. Connect to V_{SS} if unused.
5	RS0	AI	ADC Voltage-Sense Input 0. Connect to V_{SS} if unused.
6	A0/$\overline{\text{MONOFF}}$	DI	SMBus Address 0 Input/Active-Low Monitoring Off Input. This dual-function pin is sampled on device power-up to determine the SMBus address. After device power-up, this pin becomes an input, with an internal pullup, that when pulled low defeats the overvoltage and undervoltage monitoring to allow an external device to margin the power supplies.
7	V_{DDA}	Power	Analog Supply Voltage. Bypass V_{DDA} to V_{SS} with 0.1µF. Connect to V_{DD}.
8	N.C.	—	No Connection. Do not connect any signal to this pin.
9	$\overline{\text{FAULT}}$	DIO	Active-Low Fault Input/Output for the Primary Sequence. See the *Expanded Pin Description* section for more details.

Pin Description (continued)

PIN*	NAME	TYPE**	FUNCTION
10	CONTROL	AI	Power-Supply Master On/Off Control for the Primary Sequence. Active low or active high based on the ON_OFF_CONFIG command.
11	$\overline{RST}$	DIO	Active-Low Reset Input/Output. Contains an internal pullup.
12	$\overline{ALARMCLR}$	DI	Active-Low Alarm Clear Input with a Weak Pullup. Toggle low to clear the $\overline{ALARM0}$/$\overline{ALARM1}$ outputs. Leave open circuit or connect high if not used.
13	SDA	DIO	I²C/SMBus-Compatible Input/Open-Drain Output
14	SCL	DIO	I²C/SMBus-Compatible Clock Input/Open-Drain Output
15	V_{DD}	Power	Digital Supply Voltage. Bypass V_{DD} to V_{SS} with 0.1µF. Connect to V_{DDA}.
16	REG18	Power	Regulator for Digital Circuitry. Bypass to V_{SS} with 1µF and 10nF (500mΩ maximum ESR). Do not connect other circuitry to this pin.
17	$\overline{FAULT2}$	DIO	Active-Low Fault Input/Output for the Secondary Sequence. See the *Expanded Pin Description* section for more details.
18	MSCL	DIO	Master I²C Clock Input/Open-Drain Output
19	MSDA	DIO	Master I²C Data Input/Open-Drain Output
20	PSEN8	DO	Power-Supply Enable Output 8. See the *Expanded Pin Description* section for more details.
21	PSEN9	DO	Power-Supply Enable Output 9. See the *Expanded Pin Description* section for more details.
22	PSEN10	DO	Power-Supply Enable Output 10. See the *Expanded Pin Description* section for more details.
23	PSEN11	DO	Power-Supply Enable Output 11. See the *Expanded Pin Description* section for more details.
24	$\overline{ALARM0}$	DO	Active-Low Alarm Output 0. See the *Expanded Pin Description* section for more details.
25	$\overline{ALARM1}$	DO	Active-Low Alarm Output 1. See the *Expanded Pin Description* section for more details.
26	$\overline{ALERT}$	DO	Active-Low, Open-Drain Alert Output
27	A1/PG	DIO	SMBus Address 1 Input/Power-Good Output for the Primary Sequence. This dual-function pin is sampled on device power-up to determine the SMBus address. After device power-up, this pin becomes an output that transitions high when all the enabled power supplies are above their associated POWER_GOOD_ON thresholds. This pin is forced low immediately when the CONTROL pin goes inactive or the OPERATION off command is received. This pin contains a weak pullup during device reset.
28	PG2	DO	Power Good for the Secondary Sequence
29	CONTROL2	DI	Power-Supply Master On/Off Control for the Secondary Sequence. Active low or active high based on the ON_OFF_CONFIG command.
30	RSG0	AI	Remote-Sense Ground for RS0–RS3.
31	RSG1	AI	Remote-Sense Ground for RS4–RS11.
32	PSEN0	DO	Power-Supply Enable Output 0. See the *Expanded Pin Description* section for more details.
33	PSEN1	DO	Power-Supply Enable Output 1. See the *Expanded Pin Description* section for more details.
34	PSEN2	DO	Power-Supply Enable Output 2. See the *Expanded Pin Description* section for more details.
35	PSEN3	DO	Power-Supply Enable Output 3. See the *Expanded Pin Description* section for more details.
36	PSEN4	DO	Power-Supply Enable Output 4. See the *Expanded Pin Description* section for more details.
37	PSEN5	DO	Power-Supply Enable Output 5. See the *Expanded Pin Description* section for more details.

Pin Description (continued)

PIN*	NAME	TYPE**	FUNCTION
38	PSEN6	DO	Power-Supply Enable Output 6. See the *Expanded Pin Description* section for more details.
39	PSEN7	DO	Power-Supply Enable Output 7. See the *Expanded Pin Description* section for more details.
40	$\overline{WDO}$	DIO	Open-Drain, Active-Low Watchdog Input/Output. Can be configured with MFR_WATCHDOG_CONFIG as a manual reset input.
41	WDI	DI	Watchdog Input. Rising edge triggered.
42	RS11	AI	ADC Voltage-Sense Input 11. Connect to V_{SS} if unused.
43	RS10	AI	ADC Voltage-Sense Input 10. Connect to V_{SS} if unused.
44	RS9	AI	ADC Voltage-Sense Input 9. Connect to V_{SS} if unused.
45	RS8	AI	ADC Voltage-Sense Input 8. Connect to V_{SS} if unused.
46	RS7	AI	ADC Voltage-Sense Input 7. Connect to V_{SS} if unused.
47	RS6	AI	ADC Voltage-Sense Input 6. Connect to V_{SS} if unused.
48	RS5	AI	ADC Voltage-Sense Input 5. Connect to V_{SS} if unused.
—	EP/V_{SS}	Power	Exposed Pad (Bottom Side of Package). Must be connected to local ground. The exposed pad is the ground reference (V_{SS}) for the entire device.

**All pins except V_{DD}, EP/V_{SS}, $\overline{ALERT}$, A1/PG, and REG18 are high impedance during device power-up and reset.*

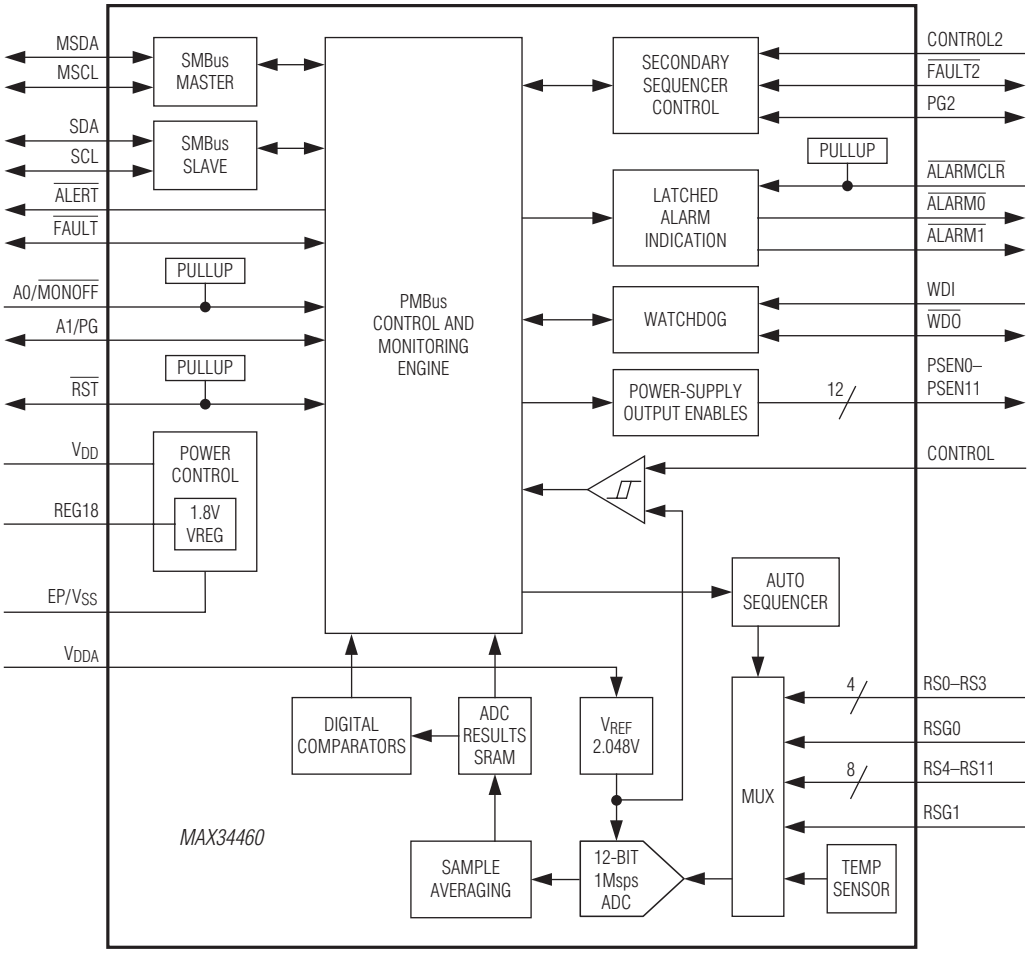
***AI = Analog input, AO = Analog output; DI = Digital input; DIO = Digital input/output; DO = Digital output*

Expanded Pin Description

NAME	FUNCTION
PSEN0–PSEN11	The PSEN0–PSEN11 outputs are programmable with the MFR_PSEN_CONFIG command for either active-high or active-low operation and can be either open-drain or push-pull. If not used for power-supply enables, these outputs can be repurposed as general-purpose outputs using the MFR_PSEN_CONFIG command. If these pins are used to enable power supplies, it is **highly recommended** that these pins have external pullups or pulldowns to force the supplies into an off state when the device is not active.
$\overline{FAULT}$	Open-Drain, Active-Low Fault Input/Output. This pin is asserted when one or more of the power supplies in a global group are being shut down due to a fault condition. Also, this pin is monitored and when it is asserted, all power supplies in a global group are shut down. This pin is used to provide hardware control for power supplies in a global group across multiple devices. This output is unconditionally deasserted when $\overline{RST}$ is asserted or the device is power cycled. Upon reset, this output is pulled low until monitoring starts.
$\overline{ALARM}$	Open-Drain, Active-Low Alarm Output. The outputs can be configured with the MFR_FAULT_RESPONSE command to go active in any combination of channels for undervoltage or overvoltage, or sequencing faults or warnings. These outputs are latched until cleared with the $\overline{ALARMCLR}$ pin or the ALARM_CLR bit in MFR_MODE.

PMBus 12-Channel Voltage Monitor and Sequencer

Block Diagram



Detailed Description

The MAX34460 is a highly integrated system monitor with functionality to monitor up to 12 power supplies. The device provides power-supply voltage monitoring and sequencing. It can also provide closed-loop margining control and local/remote thermal-sensing facilities.

The power-supply manager monitors the power-supply output voltage and constantly checks for user programmable overvoltage and undervoltage thresholds. It also has the ability to margin the power-supply output voltage up or down by a user-programmable level. The margining is performed in a closed-loop arrangement, whereby the device automatically adjusts an external-current DAC

output and then measures the resultant output voltage. The power-supply manager can also sequence the supplies in any order at both power-up and power-down.

Thermal monitoring can be accomplished using up to five temperature sensors including an on-chip temperature sensor and up to four external remote DS75LV digital temperature sensors. Communications with the DS75LV temperature sensors is conducted through a dedicated I2C/SMBus interface.

The device provides $\overline{\text{ALERT}}$ and $\overline{\text{FAULT}}$ output signals. Host communications are conducted through a PMBus-compatible communications port.

Table 1. PMBus Command Codes

CODE	COMMAND NAME	TYPE	PAGE 0–11	PAGE 13–17	PAGE 255	NO. OF BYTES	FLASH STORED/ LOCKED (NOTE 2)	DEFAULT VALUE (NOTE 2)
			(NOTE 1)					
00h	PAGE	R/W byte	R/W	R/W	R/W	1	N/N	00h
01h	OPERATION	R/W byte	R/W		W	1	N/N	00h
02h	ON_OFF_CONFIG	R/W byte	R/W	R/W	R/W	1	Y/Y	1Ah
03h	CLEAR_FAULTS	Send byte	W	W	W	0	N/N	—
10h	WRITE_PROTECT	R/W byte	R/W	R/W	R/W	1	N/Y	00h
11h	STORE_DEFAULT_ALL	Send byte	W	W	W	0	N/Y	—
12h	RESTORE_DEFAULT_ALL	Send byte	W	W	W	0	N/Y	—
19h	CAPABILITY	Read byte	R	R	R	1	N/N	20h/30h
20h	VOUT_MODE	Read byte	R	R	R	1	FIXED/N	40h
25h	VOUT_MARGIN_HIGH	R/W word	R/W	—	—	2	Y/Y	0000h
26h	VOUT_MARGIN_LOW	R/W word	R/W	—	—	2	Y/Y	0000h
2Ah	VOUT_SCALE_MONITOR	R/W word	R/W	—	—	2	Y/Y	7FFFh
40h	VOUT_OV_FAULT_LIMIT	R/W word	R/W	—	—	2	Y/Y	7FFFh
42h	VOUT_OV_WARN_LIMIT	R/W word	R/W	—	—	2	Y/Y	7FFFh
43h	VOUT_UV_WARN_LIMIT	R/W word	R/W	—	—	2	Y/Y	0000h
44h	VOUT_UV_FAULT_LIMIT	R/W word	R/W	—	—	2	Y/Y	0000h
4Fh	OT_FAULT_LIMIT	R/W word	—	R/W	—	2	Y/Y	7FFFh
51h	OT_WARN_LIMIT	R/W word	—	R/W	—	2	Y/Y	7FFFh
5Eh	POWER_GOOD_ON	R/W word	R/W	—	—	2	Y/Y	0000h
5Fh	POWER_GOOD_OFF	R/W word	R/W	—	—	2	Y/Y	0000h
60h	TON_DELAY	R/W word	R/W	—	—	2	Y/Y	0000h
62h	TON_MAX_FAULT_LIMIT	R/W word	R/W	—	—	2	Y/Y	FFFFh
64h	TOFF_DELAY	R/W word	R/W	—	—	2	Y/Y	0000h
79h	STATUS_WORD	Read word	R	R	R	2	N/N	0000h
7Ah	STATUS_VOUT	Read byte	R	—	—	1	N/N	00h
7Dh	STATUS_TEMPERATURE	Read byte	—	R	—	1	N/N	00h
7Eh	STATUS_CML	Read byte	R	R	R	1	N/N	00h
80h	STATUS_MFR_SPECIFIC	Read byte	R	—	R	1	N/N	00h
8Bh	READ_VOUT	Read word	R	—	—	2	N/N	0000h
8Dh	READ_TEMPERATURE_1	Read word	—	R	—	2	N/N	0000h
98h	PMBUS_REVISION	Read byte	R	R	R	1	FIXED/N	11h

Table 1. PMBus Command Codes (continued)

CODE	COMMAND NAME	TYPE	PAGE 0–11	PAGE 13–17	PAGE 255	NO. OF BYTES	FLASH STORED/ LOCKED (NOTE 2)	DEFAULT VALUE (NOTE 2)
			(NOTE 1)					
99h	MFR_ID	Read byte	R	R	R	1	FIXED/N	4Dh
9Ah	MFR_MODEL	Read byte	R	R	R	1	FIXED/N	57h
9Bh	MFR_REVISION	Read word	R	R	R	2	FIXED/N	(Note 3)
9Ch	MFR_LOCATION	Block R/W	R/W	R/W	R/W	8	Y/Y	(Note 4)
9Dh	MFR_DATE	Block R/W	R/W	R/W	R/W	8	Y/Y	(Note 4)
9Eh	MFR_SERIAL	Block R/W	R/W	R/W	R/W	8	Y/Y	(Note 4)
D1h	MFR_MODE	R/W word	R/W	R/W	R/W	2	Y/Y	0008h
D2h	MFR_PSEN_CONFIG	R/W byte	R/W	—	—	1	Y/Y	00h
D3h	MFR_SEQ_TIMESLOT	R/W byte	R/W	—	—	1	Y/Y	00h
D4h	MFR_VOUT_PEAK	R/W word	R/W	—	—	2	N/Y	0000h
D6h	MFR_TEMPERATURE_PEAK	R/W word	—	R/W	—	2	N/Y	8000h
D7h	MFR_VOUT_MIN	R/W word	R/W	—	—	2	N/Y	7FFFh
D8h	MFR_NV_LOG_CONFIG	R/W word	R/W	R/W	R/W	2	Y/Y	0000h
D9h	MFR_FAULT_RESPONSE	R/W word	R/W	—	—	2	Y/Y	0000h
DAh	MFR_FAULT_RETRY	R/W word	R/W	R/W	R/W	2	Y/Y	0000h
DBh	MFR_PG_DELAY	R/W word	R/W	R/W	R/W	2	Y/Y	0000h
DCh	MFR_NV_FAULT_LOG	Block read	R	R	R	255	Y/Y	(Note 5)
DDh	MFR_TIME_COUNT	Block read	R/W	R/W	R/W	4	N/Y	(Note 6)
DFh	MFR_MARGIN_CONFIG	R/W word	R/W	—	—	2	Y/Y	0000h
E3h	MFR_TEMPERATURE_AVG	R/W word	—	R/W	—	2	N/Y	0000h
F0h	MFR_TEMP_SENSOR_CONFIG	R/W word	—	R/W	—	2	Y/Y	0000h
FBh	MFR_GPO_CONFIG	R/W word	R/W	R/W	R/W	2	Y/Y	0000h
FCh	MFR_STORE_SINGLE	R/W word	R/W	R/W	R/W	2	N/Y	0000h
FDh	MFR_WATCHDOG_CONFIG	R/W word	R/W	R/W	R/W	2	Y/Y	0000h

Note 1: Common commands are shaded. Access through any page results in the same device response.

Note 2: In the **Flash Stored/Locked** column, the “N” on the left indicates that this parameter is not stored in flash memory when the STORE_DEFAULT_ALL command is executed; the value shown in the **Default Value** column is automatically loaded upon power-on reset or when the $\overline{RST}$ pin is asserted. In the **Flash Stored/Locked** column, the “Y” on the left side indicates that the currently loaded value in this parameter is stored in flash memory when the STORE_DEFAULT_ALL command is executed and is automatically loaded upon power-on reset, or when the $\overline{RST}$ pin is asserted and the value shown in the **Default Value** column is the value when shipped from the factory. “FIXED” in the **Flash Stored/Locked** column means that the value is fixed at the factory and cannot be changed. The value shown in the **Default Value** column is automatically loaded upon power-on reset, or when the $\overline{RST}$ pin is asserted. The right-side Y/N indicates that when the device is locked, only the commands listed with “N” can be accessed. All other commands are ignored if written and return FFh if read. Only the PAGE, CLEAR_FAULTS, OPERATION, and MFR_SERIAL commands can be written to. The device unlocks if the upper 4 bytes of MFR_SERIAL match the data written to the device.

Note 3: The factory-set value is dependent on the device hardware and firmware revision.

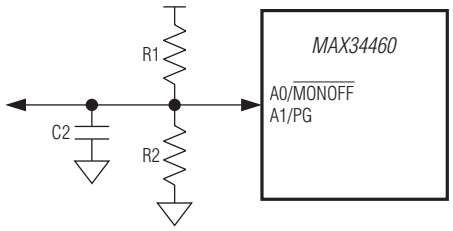
Note 4: The factory-set default value for this 8-byte block is 3130313031303130h.

Note 5: The factory-set default value for the complete block of the MFR_NV_FAULT_LOG is FFh.

Note 6: The factory-set default value for this 4-byte block is 00000000h.

Address Select

On device power-up, the device samples the A0 and A1 pins to determine the PMBus/SMBus serial-port address. The combination of the components shown below determines the serial-port address (see also Table 2).



SMBus/PMBus Operation

The device implements the PMBus command structure using the SMBus format. The structure of the data flow between the host and the slave is shown below for several different types of transactions. All transactions begin with a host sending a command code that is immediately preceded with a 7-bit slave address (R/$\overline{W}$ = 0). Data is sent MSB first.

Table 2. PMBus/SMBus Serial-Port Address

A1			A0			7-BIT SLAVE ADDRESS
R1	R2	C2	R1	R2	C2	
	220kΩ			220kΩ		1110 100 (E8h)
	220kΩ		220kΩ			1110 101 (EAh)
	220kΩ		220kΩ		100nF	0001 010 (24h)
	220kΩ		22kΩ		100nF	0001 011 (26h)
220kΩ				220kΩ		1110 110 (ECh)
220kΩ			220kΩ			1110 111 (EEh)
220kΩ			220kΩ		100nF	0001 100 (28h)
220kΩ			22kΩ		100nF	0001 101 (2Ah)
220kΩ		100nF		220kΩ		1001 100 (98h)
220kΩ		100nF	220kΩ			1001 101 (9Ah)
220kΩ		100nF	220kΩ		100nF	1011 000 (B0h)
220kΩ		100nF	22kΩ		100nF	1011 001 (B2h)
22kΩ		100nF		220kΩ		1001 110 (9Ch)
22kΩ		100nF	220kΩ			1001 111 (9Eh)
22kΩ		100nF	220kΩ		100nF	1011 110 (BCh)
22kΩ		100nF	22kΩ		100nF	1011 111 (BEh)

Note: *The device also responds to a slave address of 34h (this is the factory programming address) and the device should not share the same I²C bus with other devices that use this slave address.*

SMBus/PMBus Communication Examples

READ WORD FORMAT

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	R	A	DATA BYTE LOW	A	DATA BYTE HIGH	NA	P

READ BYTE FORMAT

1	7	1	1	8	1	1	7	1	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	R	A	DATA BYTE	NA	P

WRITE WORD FORMAT

1	7	1	1	8	1	8	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	P

WRITE BYTE FORMAT

1	7	1	1	8	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA BYTE	A	P

SEND BYTE FORMAT

1	7	1	1	8	1	1
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	P

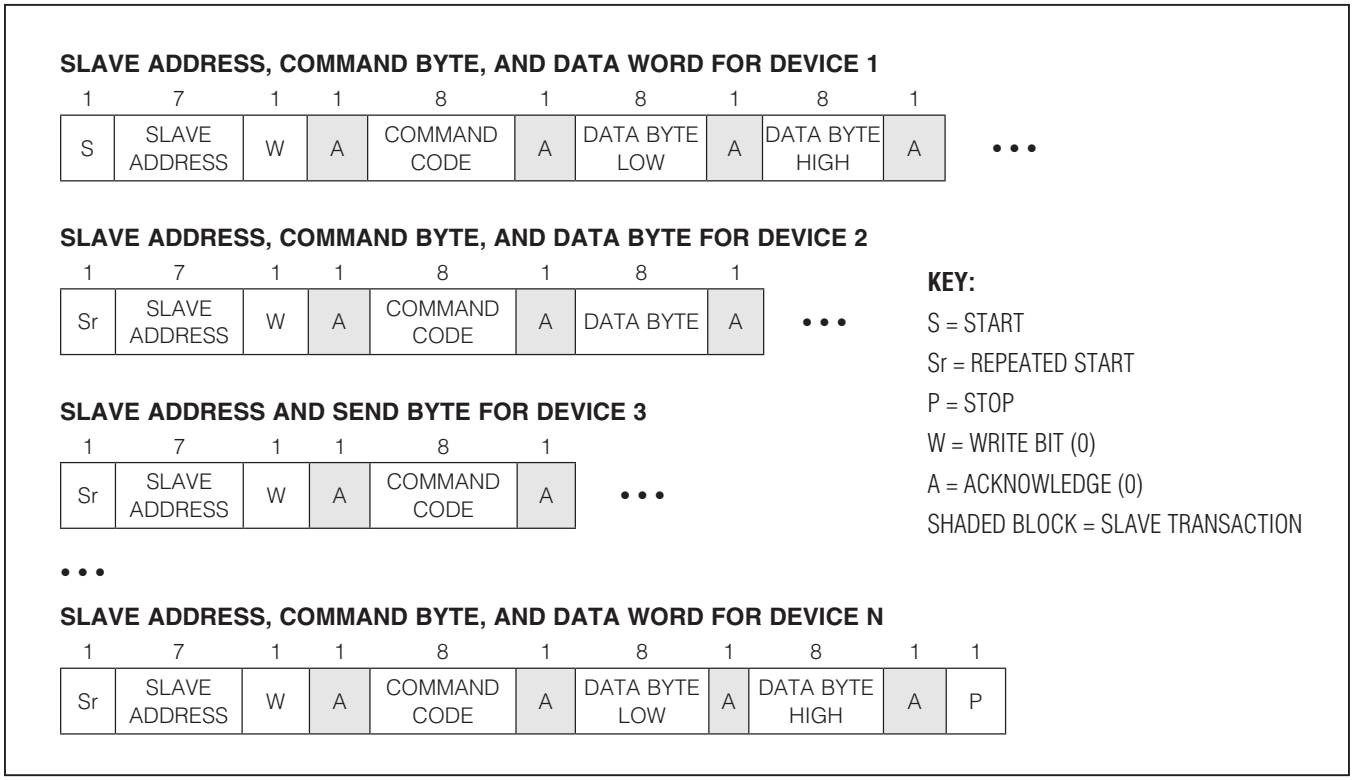
KEY:

S = START
Sr = REPEATED START
P = STOP
W = WRITE BIT (0)
R = READ BIT (1)
A = ACKNOWLEDGE (0)
NA = NOT ACKNOWLEDGE (1)
SHADED BLOCK = SLAVE TRANSACTION

Group Command

The device supports the group command. With the group command, a host can write different data to multiple devices on the same serial bus with one long continuous data stream. All the devices addressed during this transaction wait for the host to issue a STOP before beginning to respond to the command.

Group Command Write Format



Addressing

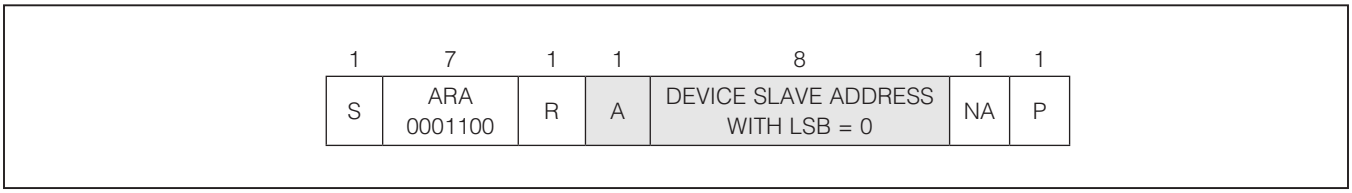
The device responds to receiving its fixed slave address by asserting an acknowledge (ACK) on the bus. The device does not respond to a general call address; it only responds when it receives its fixed slave address or the alert response address (ARA). See the *ALERT and Alert Response Address (ARA)* section for more details.

ALERT and Alert Response Address (ARA)

If the $\overline{\text{ALERT}}$ output is enabled (ALERT bit = 1 in MFR_MODE), when a fault occurs the device asserts the $\overline{\text{ALERT}}$ signal and then waits for the host to send an ARA, as shown in the *Alert Response Address (ARA) Byte Format* section.

When the ARA is received and the device is asserting $\overline{\text{ALERT}}$, the device ACKs it and then attempts to place its fixed slave address on the bus by arbitrating the bus, since another device could also try to respond to the ARA. The rules of arbitration state that the lowest address device wins. If the device wins the arbitration, it deasserts $\overline{\text{ALERT}}$. If the device loses arbitration, it keeps $\overline{\text{ALERT}}$ asserted and waits for the host to once again send the ARA.

Alert Response Address (ARA) Byte Format



Host Sends or Reads Too Few Bits

If, for any reason, the host does not complete writing a full byte or reading a full byte from the device before a START or STOP is received, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_WORD.
3) Sets the DATA_FAULT bit in STATUS_CML.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Sends or Reads Too Few Bytes

For each supported command, the device expects a fixed number of bytes to be written or read from the device. If, for any reason, less than the expected number of bytes is written to or read from the device, the device completely ignores the command and takes no action.

Host Sends Too Many Bytes or Bits

For each supported command, the device expects a fixed number of bytes to be written to the device. If, for any reason, more than the expected number of bytes or bits are written to the device, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_WORD.
3) Sets the DATA_FAULT bit in STATUS_CML.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Reads Too Many Bytes or Bits

For each supported command, the device expects a fixed number of bytes to be read from the device. If, for any reason, more than the expected number of bytes or bits are read from the device, the device does the following:

1) Sends all ones (FFh) as long as the host keeps acknowledging.
2) Sets the CML bit in STATUS_WORD.
3) Sets the DATA_FAULT bit in STATUS_CML.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Sends Improperly Set Read Bit in the Slave Address Byte

If the device receives the R/$\overline{\text{W}}$ bit in the slave address set to a one immediately preceding the command code, the device does the following (this does not apply to the ARA):

1) ACKs the address byte.
2) Sends all ones (FFh) as long as the host keeps acknowledging.
3) Sets the CML bit in STATUS_WORD.
4) Sets the DATA_FAULT bit in STATUS_CML.
5) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Unsupported Command Code Received/ Host Writes to a Read-Only Command

If the host sends the device a command code that it does not support, or if the host sends a command code that is not supported by the current PAGE setting, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_WORD.
3) Sets the COMM_FAULT bit in STATUS_CML.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Invalid Data Received

The device checks the PAGE, OPERATION, and WRITE_ PROTECT command codes for valid data. If the host writes a data value that is invalid, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_WORD.
3) Sets the DATA_FAULT bit in STATUS_CML.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Reads from a Write-Only Command

When a read request is issued to a write-only command (CLEAR_FAULTS, STORE_DEFAULT_ALL, RESTORE_DEFAULT_ALL, OPERATION with PAGE = 255), the device does the following:

1) ACKs the address byte.
2) Ignores the command.
3) Sends all ones (FFh), as long as the host keeps acknowledging.
4) Sets the CML bit in STATUS_WORD.
5) Sets the DATA_FAULT bit in STATUS_CML.
6) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

Host Writes to a Read-Only Command

When a write request is issued to a read-only command, the device does the following:

1) Ignores the command.
2) Sets the CML bit in STATUS_WORD.
3) Sets the COMM_FAULT bit in STATUS_SML.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled).

SMBus Timeout

If during an active SMBus communication sequence the SCL signal is held low for greater than the timeout duration (nominally 27ms), the device terminates the sequence and resets the serial bus. It takes no other action. No status bits are set.

PMBus Operation

From a software perspective, the device appears as a PMBus device capable of executing a subset of PMBus commands. A PMBus 1.1-compliant device uses the SMBus version 1.1 for transport protocol and responds to the SMBus slave address. In this data sheet, the term SMBus is used to refer to the electrical characteristics of the PMBus communication using the SMBus physical layer. The term PMBus is used to refer to the PMBus command protocol. The device employs a number of standard SMBus protocols (e.g., Write Word, Read Word, Write Byte, Read Byte, Send Byte, etc.) to program output voltage and warning/fault thresholds, read monitored data, and provide access to all manufacturer-specific commands.

The device supports the group command. The group command is used to send commands to more than one PMBus device. It is not required that all the devices receive the same command. However, no more than one command can be sent to any one device in one group command packet. The group command must not be used with commands that require receiving devices to respond with data, such as the STATUS_WORD command. When the device receives a command through this protocol, it immediately begins execution of the received command after detecting the STOP condition.

The device supports the PAGE command and uses it to select which individual channel to access. When a data word is transmitted, the lower order byte is sent first and the higher order byte is sent last. Within any byte, the (MSB is sent first and the LSB is sent last.

PMBus Protocol Support

The device supports a subset of the commands defined in the PMBus Power System Management Protocol Specification Part II - Command Language Revision 1.1. For detailed specifications and the complete list of PMBus commands, refer to Part II of the PMBus specification available at www.PMBus.org. The supported PMBus commands and the corresponding device behavior are described in this document. All data values are represented in DIRECT format, unless otherwise stated. Whenever the PMBus specification refers to the PMBus device, it is referring to the device operating in conjunction with a power supply. While the command can call for turning on or off the PMBus device, the device always remains on to continue communicating with the PMBus master and the device transfers the command to the power supply accordingly.

Data Format

Voltage data for commanding or reading the output voltage or related parameters (such as the overvoltage threshold) are presented in DIRECT format. DIRECT format data is a 2-byte, two's complement binary value. DIRECT format data can be used with any command that sends or reads a parametric value. The DIRECT format uses an equation and defined coefficients to calculate the desired values. Table 3 lists coefficients used by the device.

Interpreting Received DIRECT Format Values

The host system uses the following equation to convert the value received from the PMBus device—in this case, the MAX34460—into a reading of volts, degrees Celsius, or other units as appropriate:

$$X = (1/m) \times (Y \times 10^{-R} - b)$$

where X is the calculated, real-world value in the appropriate units (i.e., V, °C, etc.); m is the slope coefficient; Y is the 2-byte, two's complement integer received from the PMBus device; b is the offset; and R is the exponent.

Table 3. PMBus Command Code Coefficients

PARAMETER	COMMANDS	UNITS	RESOLUTION	MAXIMUM	m	b	R
Voltage	VOUT_MARGIN_HIGH VOUT_MARGIN_LOW VOUT_OV_FAULT_LIMIT VOUT_OV_WARN_LIMIT VOUT_UV_WARN_LIMIT VOUT_UV_FAULT_LIMIT POWER_GOOD_ON POWER_GOOD_OFF READ_VOUT MFR_VOUT_PEAK MFR_VOUT_MIN	mV	1	32,767	1	0	0
Voltage Scaling	VOUT_SCALE_MONITOR	—	1/32,767	1	32,767	0	0
Temperature	OT_FAULT_LIMIT OT_WARN_LIMIT READ_TEMPERATURE_1 MFR_TEMPERATURE_PEAK MFR_TEMPERATURE_AVG	°C	0.01	327.67	1	0	2
Timing	TON_DELAY TON_MAX_FAULT_LIMIT TOFF_DELAY MFR_FAULT_RETRY MFR_PG_DELAY	ms	0.2	6553.4	5	0	0

Table 4. Coefficients for DIRECT Format Value

COMMAND CODE	COMMAND NAME	m	b	R
25h	VOUT_MARGIN_HIGH	1	0	0
8Bh	READ_VOUT	1	0	0

Sending a DIRECT Format Value

To send a value, the host must use the following equation to solve for Y:

$$Y = (mX + b) \times 10^{R}$$

where Y is the 2-byte, two's complement integer to be sent to the unit; m is the slope coefficient; X is the real-world value, in units such as volts, to be converted for transmission; b is the offset; and R is the exponent.

The following example demonstrates how the host can send and retrieve values from the device. Table 4 lists the coefficients used in the following parameters.

If a host wants to set the device to change the power-supply output voltage to 3.465V (or 3465mV), the corresponding VOUT_MARGIN_HIGH value is:

$Y = (1 \times 3465 + 0) \times 10^{0} = 3465$ (decimal) = 0D89h (hex)

Conversely, if the host received a value of 0D89h on a READ_VOUT command, this is equivalent to:

$X = (1/1) \times (0D89h \times 10^{-(-0)} - 0) = 3465mV = 3.465V$

Power supplies and power converters generally have no way of knowing how their outputs are connected to ground. Within the power supply, all output voltages are most commonly treated as positive. Accordingly, all output voltages and output voltage-related parameters of PMBus devices are commanded and reported as positive values. It is up to the system to know that a particular output is negative if that is of interest to the system. All output-voltage-related commands use 2 data bytes.

Fault Management and Reporting

For reporting faults/warnings to the host on a real-time basis, the device asserts the open-drain $\overline{ALERT}$ pin (if enabled in MFR_MODE) and sets the appropriate bit in the various status registers. On recognition of the $\overline{ALERT}$ assertion, the host or system manager is expected to poll the I^2C bus to determine the device asserting $\overline{ALERT}$. The host sends the SMBus ARA (0001 100). The device ACKs the SMBus ARA, transmits its slave address, and deasserts $\overline{ALERT}$. The system controller then communicates with PMBus commands to retrieve the fault/warning status information from the device.

See the individual command sections for more details. Faults and warnings that are latched in the status registers are cleared when any one of the following conditions occurs:

- A CLEAR_FAULTS command is received.
- The $\overline{RST}$ pin is toggled or a soft-reset is issued.
- Bias power to the device is removed and then reapplied.

One or more latched-off power supplies are only restarted when one of the following conditions occurs:

- The OPERATION commands are received that turn off and on the power supplies or the CONTROL pin is toggled to turn off and then turn on the power supplies.
- The $\overline{RST}$ pin is toggled or a soft-reset is issued.
- Bias power to the device is removed and then reapplied.

A power supply is not allowed to turn on if any faults the supply responds to are detected. Only after the faults clear is the power supply allowed to turn on. When GLOBAL supplies are being sequenced on, a fault on any of the supplies keeps all GLOBAL supplies from being turned on.

Upon a system-wide power-up (OPERATION command is received to turn the supplies on when PAGE is 255 or the CONTROL pin is toggled to turn on the supplies), all enabled GLOBAL power supplies with their overvoltage- or overtemperature-fault responses enabled with the MFR_FAULT_RESPONSE command are only allowed to power up if neither the overvoltage or overtemperature fault exists.

The device responds to fault conditions according to the manufacturer fault response command (MFR_FAULT_RESPONSE). This command byte determines how the device should respond to each particular fault.

Password Protection

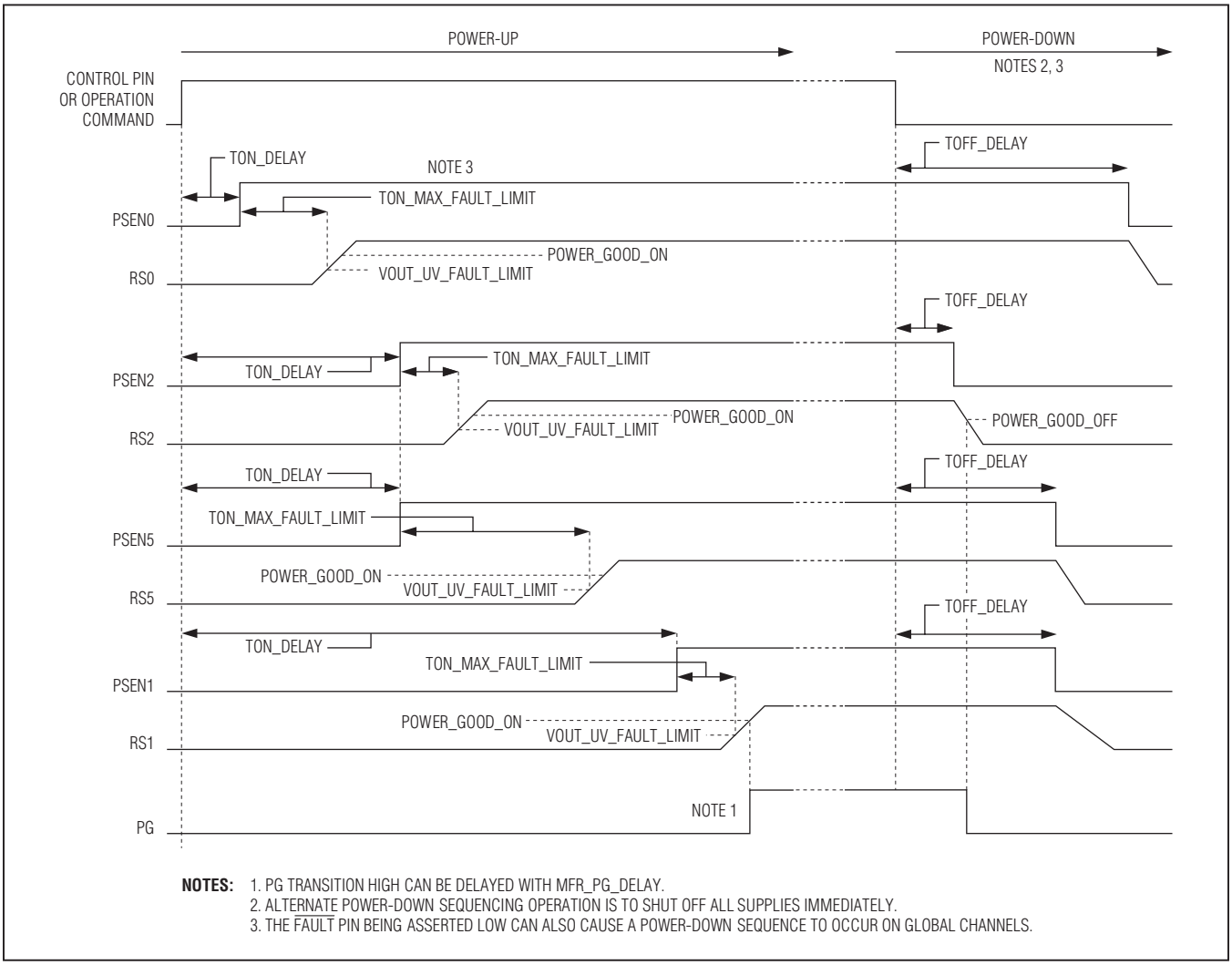
The device can be password protected by using the LOCK bit in the MFR_MODE command. Once the device is locked, only certain PMBus commands can be accessed with the serial port. See Table 1 for a complete list. Commands that have password protection return all ones (FFh), with the proper number of data bytes when read. When the device is locked, only the PAGE, OPERATION, CLEAR_FAULTS, and MFR_SERIAL commands can be written; all other written commands are ignored. When MFR_SERIAL is written and the upper 4 bytes match the internally flash-stored value, the device unlocks and remains unlocked until the LOCK bit in MFR_MODE is activated once again. The LOCK status bit in STATUS_MFR_SPECIFIC is always available to indicate whether the device is locked or unlocked.

Sequencing

The device implements both PMBus-defined time-based sequencing and timeslot-defined event-based sequencing. The SEQ bit in MFR_MODE determines which sequencing profile is used. With PMBus-defined sequencing, the activation of all power-supply channels (even across multiple devices) is timed from a common START signal that can be either the CONTROL pin or the OPERATION command. With timeslot sequencing, each power-supply channel is assigned to a particular timeslot and each power supply waits until the preceding power supply is active before it is turned on. The power-down sequencing of both the PMBus and the timeslot arrangements is the same. When the power supplies are instructed to turn off, all supplies can be switched off immediately, or they can be shut down in any order according to the TOFF_DELAY command setting.

PMBus-Defined Time-Based Sequencing

Figure 1 details a simple sequencing scheme using four power supplies. When either the CONTROL pin goes active or the OPERATION command is received (as defined by the ON_OFF_CONFIG command), each enabled PSENn output goes active (can be active high or low, as defined in MFR_PSEN_CONFIG) after the associated delay time programmed in TON_DELAY. The power supplies can be sequenced on in any order. The output voltage of each power supply is monitored to ensure that the supply crosses the undervoltage fault limit (as configured in VOUT_UV_FAULT_LIMIT) within a programmable time limit (as configured in TON_MAX_FAULT_LIMIT). After all enabled supplies are turned on and above their respective power-good-on levels (as configured in POWER_GOOD_ON), the PG output transitions high. The PG output transition can be delayed with the MFR_PG_DELAY command. When either the CONTROL pin goes inactive or the OPERATION off command is received (or the $\overline{\text{FAULT}}$ pin goes low for GLOBAL channels), the power supplies are sequenced off. The order in which the supplies are disabled is determined with the TOFF_DELAY configuration. Alternatively, all of the power supplies can be switched off immediately, as configured in the ON_OFF_CONFIG command or with the OPERATION command.



NOTES: 1. PG TRANSITION HIGH CAN BE DELAYED WITH MFR_PG_DELAY.
2. ALTERNATE POWER-DOWN SEQUENCING OPERATION IS TO SHUT OFF ALL SUPPLIES IMMEDIATELY.
3. THE $\overline{\text{FAULT}}$ PIN BEING ASSERTED LOW CAN ALSO CAUSE A POWER-DOWN SEQUENCE TO OCCUR ON GLOBAL CHANNELS.

Figure 1. PMBus-Defined Time-Based Sequencing Example

Timeslot-Defined Event-Based Sequencing

As an example of timeslot sequencing, Figure 2 details a simple sequencing scheme using four power supplies. When either the CONTROL pin goes active or the OPERATION command is received (as defined by the ON_OFF_CONFIG command), PSEN0, which has been assigned to timeslot 0 (with the MFR_SEQ_TIMESLOT command), goes active (can be active high or low, as defined in MFR_PSEN_CONFIG) after the associated delay time programmed in TON_DELAY. RS0 is monitored to make sure that the PSEN0 supply crosses the undervoltage-fault limit (as configured in VOUT_UV_FAULT_LIMIT) within a programmable time limit (as configured in TON_MAX_FAULT_LIMIT). When RS0 crosses the undervoltage-fault limit, timeslot 1 begins. PSEN2 and PSEN5 have been assigned to timeslot 1 and each has their own unique TON_DELAY and TON_MAX_FAULT_LIMIT values. Since two power supplies have been assigned to timeslot 1, the last power supply to cross its associated undervoltage-fault-limit level defines when

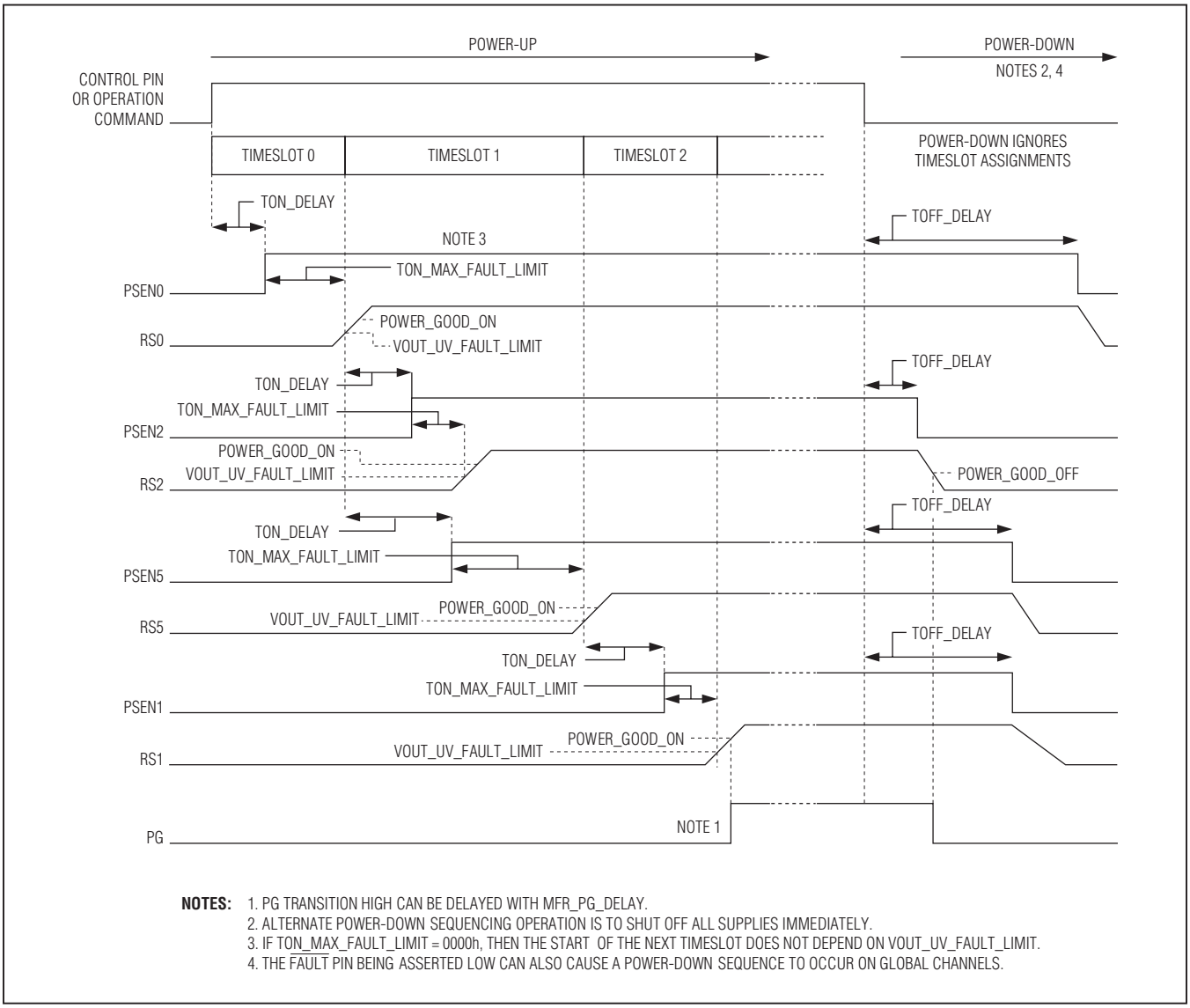


Figure 2. Timeslot-Defined Event-Based Sequencing Example

timeslot 2 begins. The power supplies can be sequenced on in any order. Since multiple power supplies can be assigned to a single timeslot, not all timeslots may be needed. However, timeslot assignment must be sequential. GLOBAL channels must start in timeslot 0, whereas local channels can be assigned to any timeslot. After all enabled supplies are turned on and above their respective power-good-on levels, the PG output transitions high. The PG output transition can be delayed with the MFR_PG_DELAY command. When either the CONTROL pin goes inactive or the OPERATION command is received (or the $\overline{\text{FAULT}}$ pin goes low for GLOBAL channels), the power supplies are sequenced off. The order in which the supplies are disabled is determined with the TOFF_DELAY configuration. Alternatively, all the power supplies can be switched off immediately, as configured in ON_OFF_CONFIG or with the OPERATION command.

Dual-Sequencing Groups

If enabled with the DUAL_SEQ bit in MFR_MODE, the device implements two independent sequencing groups. Each group has its own CONTROL, $\overline{\text{FAULT}}$, and PG pins, as shown in Table 5.

Which power supplies are assigned to which sequencing group is different depending on the selected sequencing profile. Each power-supply channel is assigned to either the primary or the secondary group with the GROUP bit in MFR_SEQ_TIMESLOT. There are special OPERATION commands to allow a host to independently control the two sequencing groups. The watchdog timer function only uses the primary group to time the beginning of the watchdog startup when the watchdog is operated in the dependent mode.

Multiple Device Connections

Multiple MAX34460 devices (or even other MAX3445x and MAX3446x PMBus system managers from the Maxim Integrated family) can be connected together to increase the system channel count. Figure 3 details the two possible connection schemes. The MULTI_SEQ bits in the MFR_MODE command are used to select the sequencing configuration.

With the Common Control or Common OPERATION command sequencing arrangement, all the paralleled devices share the same CONTROL, $\overline{\text{FAULT}}$, and SMBus signals. All the devices use a common signal (either the CONTROL pin or the OPERATION command) to enable and disable all of the power supplies. Any of the monitored power supplies can be configured with the MFR_FAULT_RESPONSE command to be tagged as GLOBAL supplies and hence activate the $\overline{\text{FAULT}}$ signal and shut down all the other supplies tagged as GLOBAL.

With the Cascaded sequencing arrangement, the PG output from upstream device is connected to the CONTROL input on the downstream device. The CONTROL input on the downstream device must be enabled with the ON_OFF_CONFIG command. All the power supplies in the upstream device must be

Table 5. Dual-Sequencing Groups

SEQUENCING GROUP	ASSIGNED SIGNALS	ALTERNATE FUNCTIONALITY
Primary	CONTROL	Not available
	$\overline{\text{FAULT}}$	
	PG	
Secondary	CONTROL2	GPO4
	$\overline{\text{FAULT2}}$	GPO3
	PG2	GPO5

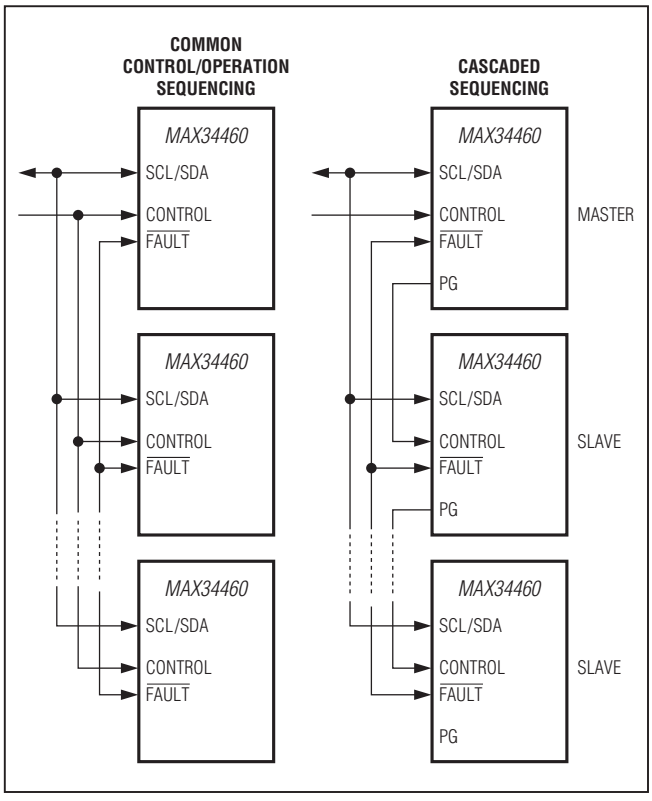


Figure 3. Multiple Device Hardware Connections

Table 6. Device Configuration Quick Reference

ACTION	CONFIGURATION
Enable a channel	Configure TON_MAX_FAULT_LIMIT = 0000h to 7FFFh.
Disable a channel	Configure TON_MAX_FAULT_LIMIT = 8000h to FFFFh.

Table 7. GPO Pins

PIN	DEFAULT FUNCTIONALITY	ALTERNATE GPO
24	$\overline{\text{ALARM0}}$	GPO0
25	$\overline{\text{ALARM1}}$	GPO1
12	$\overline{\text{ALARMCLR}}$	GPO2
17	$\overline{\text{FAULT2}}$	GPO3
29	CONTROL2	GPO4
28	PG2	GPO5
40	$\overline{\text{WDO}}$	GPO6
41	WDI	GPO7

above the POWER_GOOD_ON level before the power supplies in the downstream device are sequenced on. When the CONTROL line is inactivated or the OPERATION off command turns the supplies off in the master device, the PG output is pulled low when the first power supply falls below the POWER_GOOD_OFF level, which in turn initiates the shutdown of the channels in the first downstream device. A detected fault on any GLOBAL power supply can also initiate the shutdown of the rest of the GLOBAL power supply channels by pulling the $\overline{\text{FAULT}}$ signal low. Only channels in the primary sequencing group should be arranged in a cascaded sequence.

USER NOTE: In Cascaded Sequencing, the master and slave devices must be powered up at the same time. Also, all devices must be configured for the same latch off or retry configuration.

System Watchdog Timer

The device uses an internal watchdog timer that is internally reset every 5ms. In the event the device is locked up and this watchdog reset does not occur after 210ms, the device automatically resets. After the reset occurs, the device reloads all configuration values that were stored to flash and begins normal operation. After the reset, the device also does the following:

1) Sets the MFR bit in STATUS_WORD.
2) Sets the WATCHDOG_INT bit in STATUS_MFR_SPECIFIC (for PAGE 255).
3) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled in MFR_MODE).

CRC Memory Check

Upon reset, the device runs an internal algorithm to check the integrity of the key internal nonvolatile memory. If the CRC check fails, the device does not power up and remains in a null state with all pins high impedance, but asserts the $\overline{\text{FAULT}}$ and $\overline{\text{FAULT2}}$ outputs.

Alarm Outputs

The $\overline{\text{ALARM0}}$ and $\overline{\text{ALARM1}}$ pins are active-low, open-drain outputs that can be configured with the MFR_FAULT_RESPONSE command to assert under any combination of undervoltage, overvoltage, or sequencing faults or warnings. If more than one channel is configured to assert either alarm output, the multiple channels are logically ORed such that any enabled channel asserts the output. Once asserted, the outputs remain asserted until they are cleared either by toggling the $\overline{\text{ALARMCLR}}$ input low or by setting the ALARM_CLR bit in MFR_MODE. The current real-time status of the alarm outputs is reported in STATUS_MFR_SPECIFIC (PAGE = 255).

$\overline{\text{FAULT}}$ and $\overline{\text{FAULT2}}$ Input/Output Pins

$\overline{\text{FAULT}}$ and $\overline{\text{FAULT2}}$ are open-drain, active-low input/output pins. The primary purpose of the fault pins is to provide sequencing control across multiple devices in fault situations. Within the device, any power supply tagged as a GLOBAL power supply (with the MFR_FAULT_RESPONSE command) asserts the associated fault pin to indicate to other GLOBAL power supplies in other devices that action should be taken. The fault pins are also inputs that can be configured with the FAULT_IGNORE and FAULT2_IGNORE bits in the MFR_MODE command to cause all GLOBAL power supplies within the device to shut down and retry when $\overline{\text{FAULT}}$ is released. The input status of the fault pins is available in the STATUS_MFR_SPECIFIC command when the PAGE is set to 255. The fault pins are pulled low when the device is reset until monitoring begins.

$\overline{\text{MONOFF}}$ Disable Monitoring Control Input

The $\overline{\text{MONOFF}}$ control (which is shared with the A0 I^2C slave address-select function) is an active-low input with an internal weak pullup. To allow the device to properly set the I^2C address, this pin should be high impedance upon power-up or device reset (it is recommended that a small-signal MOSFET be used to pull this pin low). See the *Typical Operating Circuit* for an example. After power-up, when this pin is pulled low, the device stops monitoring for overvoltage/undervoltage and temperature faults/warnings and freezes the current state of the power-good and fault signals. The $\overline{\text{MONOFF}}$ input is useful in systems that do not use the external DS4424 current DACs to margin the power supplies and instead use some other technique such as a bed-of-nails tester. Asserting this pin lets the system be margin tested without causing any voltage faults or warnings. The $\overline{\text{MONOFF}}$ input is ignored when faults are active and when the power-good signals are not asserted. No sequencing should be performed while $\overline{\text{MONOFF}}$ is active.

External Signal Watchdog

The external signal watchdog function is configured using the MFR_WATCHDOG_CONFIG command. The startup sequence for the watchdog depends on whether the device is configured for dependent or independent mode operation. In the dependent mode, the PG output must be asserted before the watchdog startup timer begins. If dual sequencing is enabled, PG2 has no effect on the watchdog. In dependent mode, the watchdog function stops each time the PG output deasserts and $\overline{\text{WDO}}$ is deasserted; the device waits for PG to assert before once again starting the watchdog. In independent mode, the watchdog startup time begins after device startup. The watchdog startup time is defined with the WD_STARTUP bits in MFR_WATCHDOG_CONFIG.

After the first rising edge is detected at the WDI input during the startup time, the watchdog begins expecting a rising edge to occur before the watchdog timeout period expires. Each rising edge at WDI resets the watchdog timeout counter. The watchdog timeout period is defined with the WD_TIMEOUT bits in MFR_WATCHDOG_CONFIG. As an alternative to using the WDI input to reset the watchdog timeout counter, the WD_TOGGLE bit in MFR_WATCHDOG_CONFIG can be used.

The $\overline{\text{WDO}}$ output can be used in conjunction with the power-good outputs to create a system reset or can also be used to shut down the supplies or restart them, depending on how the device is configured.

In both dependent and independent modes, the $\overline{\text{WDO}}$ pin can also be configured to act as a manual-reset (MR) input. When the WD_WDO_MR bit is set in MFR_WATCHDOG_CONFIG, the $\overline{\text{WDO}}$ pin becomes a digital input/output pin that detects a falling edge, debounces the falling edge for a 200ms period, and then once the manual reset has been qualified, the device asserts the $\overline{\text{WDO}}$ output low for the time configured in MFR_PG_DELAY before releasing the pin and restarting the watchdog function. To prevent glitches from occurring in the reset signal, the device seizes the reset signal as soon as it qualifies the manual reset and holds the $\overline{\text{WDO}}$ output low for the MFR_PG_DELAY time. The MFR_PG_DELAY time should be configured for a time longer than the manual-reset pulse length. When the time configured in MFR_PG_DELAY expires, the device releases the reset signal and restarts the watchdog as long as the pin is high. If the pin is low when the $\overline{\text{WDO}}$ pin is released, the device waits for the pin to go high (debounced by 20ms) before restarting the watchdog function. See Figure 4.

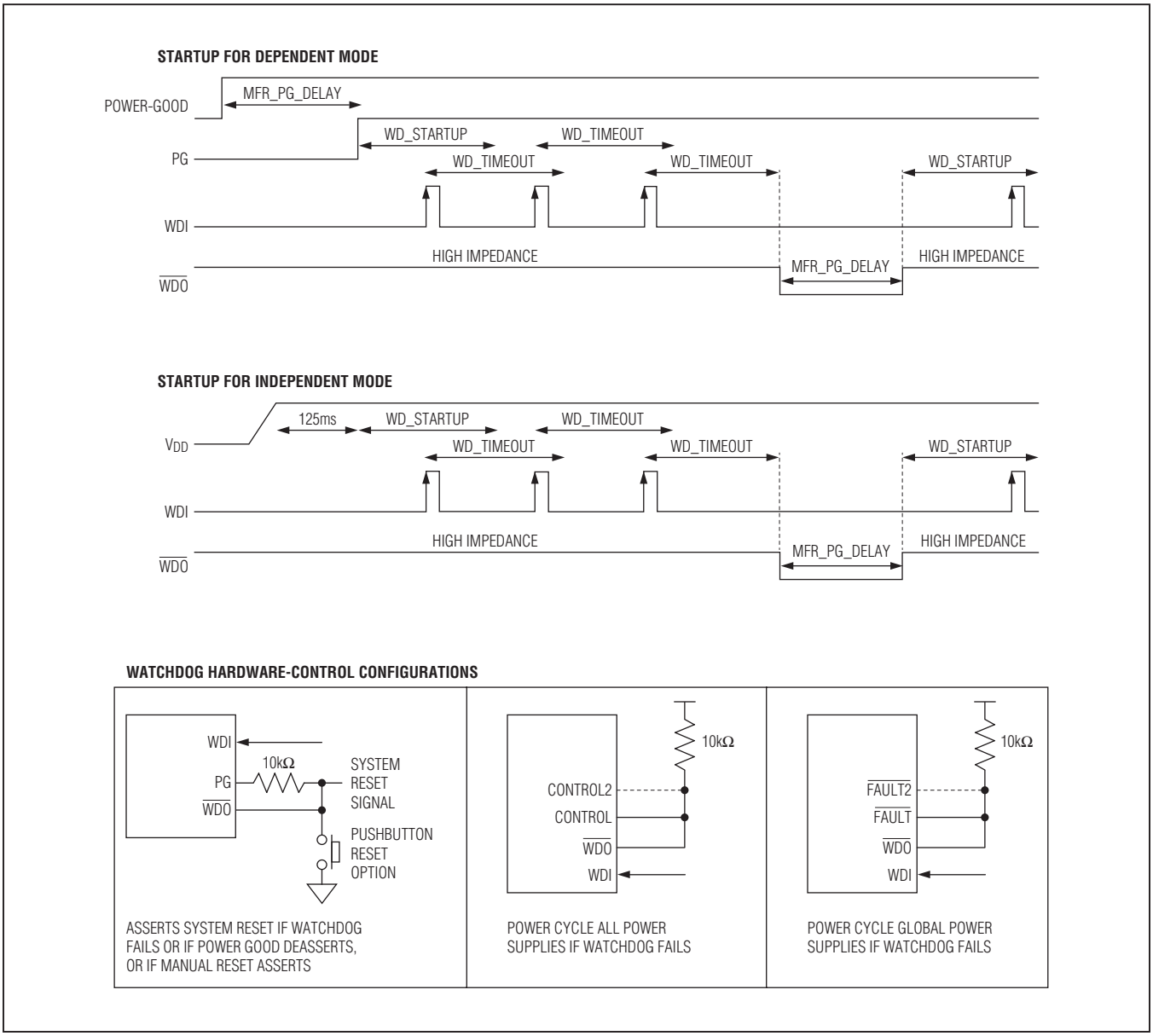


Figure 4. External Watchdog Operation

PMBus Commands

A summary of the PMBus commands supported by the device are described in the following sections.

PAGE (00h)

The device can monitor up to 12 voltages, sequence up to 12 power supplies, and margin up to 12 power supplies using three external current DACs (DS4424). The device can monitor up to five temperature sensors, one internal local temperature sensor, plus four external remote temperature sensors (DS75LV). All the monitoring and control is accomplished using one PMBus (I^2C) address. Send the PAGE command with data 0–11 and 13–17 (decimal) to select which power supply or temperature sensor is affected by all the following PMBus commands. Not all commands are supported within each page. If an unsupported command is received, the CML status bit is set. Some commands are common, which means that any selected page has the same effect on and the same response from the device. See Table 8 for PAGE commands.

Table 8. PAGE Commands

PAGE	ASSOCIATED CONTROL
0	Power supply monitored by RS0 and controlled by PSEN0 and optionally margined by OUT0 of the external DS4424 at I^2C address 20h.
1	Power supply monitored by RS1 and controlled by PSEN1 and optionally margined by OUT1 of the external DS4424 at I^2C address 20h.
2	Power supply monitored by RS2 and controlled by PSEN2 and optionally margined by OUT2 of the external DS4424 at I^2C address 20h.
3	Power supply monitored by RS3 and controlled by PSEN3 and optionally margined by OUT3 of the external DS4424 at I^2C address 20h.
4	Power supply monitored by RS4 and controlled by PSEN4 and optionally margined by OUT0 of the external DS4424 at I^2C address 60h.
5	Power supply monitored by RS5 and controlled by PSEN5 and optionally margined by OUT1 of the external DS4424 at I^2C address 60h.
6	Power supply monitored by RS6 and controlled by PSEN6 and optionally margined by OUT2 of the external DS4424 at I^2C address 60h.
7	Power supply monitored by RS7 and controlled by PSEN7 and optionally margined by OUT3 of the external DS4424 at I^2C address 60h.
8	Power supply monitored by RS8 and controlled by PSEN8 and optionally margined by OUT0 of the external DS4424 at I^2C address A0h.
9	Power supply monitored by RS9 and controlled by PSEN9 and optionally margined by OUT1 of the external DS4424 at I^2C address A0h.
10	Power supply monitored by RS10 and controlled by PSEN10 and optionally margined by OUT2 of the external DS4424 at I^2C address A0h.
11	Power supply monitored by RS11 and controlled by PSEN11 and optionally margined by OUT3 of the external DS4424 at I^2C address A0h.
12	Reserved.
13	Internal temperature sensor.
14	External DS75LV temperature sensor with I^2C address 90h.
15	External DS75LV temperature sensor with I^2C address 92h.
16	External DS75LV temperature sensor with I^2C address 94h.
17	External DS75LV temperature sensor with I^2C address 96h.
18–254	Reserved.
255	Applies to all pages.

Set the PAGE command to 255 when the following PMBus commands should apply to all pages at the same time. There are only a few commands (OPERATION, CLEAR_FAULTS) where this function has a real application.

OPERATION (01h)

The OPERATION command is used to turn the power supply on and off in conjunction with the CONTROL input pin. The OPERATION command is also used to cause the power supply to set the output voltage to the upper or lower margin voltages. The power supply stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CONTROL pin (if enabled) instructs the power supply to change to another state. The valid OPERATION command byte values are shown in Table 9. The OPERATION command controls how the device responds when commanded to change the output. When the command byte is 00h, the device immediately turns the power supply off and ignores any programmed turn-off delay. When the command byte is set to 40h, the device powers down according to the programmed turn-off delay. In Table 9 and Table 10, "act on any fault" means that if any warning or fault on the selected power supply is detected when the output is margined, the device treats this as a warning or fault and responds as programmed. "Ignore all faults" means that all warnings and faults on the selected power supply are ignored. Any command value not shown in Table 9 is an invalid command. If the device receives a data byte that is not listed in Table 9, then it treats this as invalid data, declares a data fault (set CML bit and assert $\overline{\text{ALERT}}$), and responds, as described in the *Fault Management and Reporting* section.

USER NOTE: All power supplies tagged as GLOBAL supplies (see MFR_FAULT_RESPONSE) should be turned on and off at the same time by setting the PAGE to 255. If supplies are turned on and off independently by setting the PAGE from 0–11, then the supplies are not sequenced and only use their associated TON_DELAY and TOFF_DELAY settings, without any regard to the other supplies. For timeslot-defined sequencing, GLOBAL channels must start in timeslot 0; LOCAL channels can be assigned to any timeslot.

Table 9. OPERATION Command Byte (When Bit 3 of ON_OFF_CONFIG = 1)

COMMAND BYTE	POWER SUPPLY ON/OFF	MARGIN STATE
00h	Immediate off (no sequencing)	—
40h	Soft off (with sequencing)	—
80h	On	Margin off
94h	On	Margin low (ignore all faults)
98h	On	Margin low (act on any fault)
A4h	On	Margin high (ignore all faults)
A8h	On	Margin high (act on any fault)

Note: *Active margining begins once power good has been exceeded for all channels.*

Table 10. OPERATION Command Byte (When Bit 3 of ON_OFF_CONFIG = 0)

COMMAND BYTE	POWER SUPPLY ON/OFF	MARGIN STATE
00h	Command has no effect	Margin off
40h	Command has no effect	Margin off
80h	Command has no effect	Margin off
94h	Command has no effect	Margin low (ignore all faults)
98h	Command has no effect	Margin low (act on any fault)
A4h	Command has no effect	Margin high (ignore all faults)
A8h	Command has no effect	Margin high (act on any fault)

Note: *The device only takes action if the supply is enabled. The V_{OUT} of all channels must exceed POWER_GOOD_ON for margining to begin, or power good must be forced good through the test mode.*

Table 11. Special OPERATION Command Bytes for Primary Sequence

COMMAND BYTE	POWER SUPPLY ON/OFF	MARGIN STATE
01h	Immediate off (no sequencing)	—
41h	Soft-off (with sequencing)	—
81h	On	Margin off

Table 12. Special OPERATION Command Bytes for Secondary Sequence

COMMAND BYTE	POWER SUPPLY ON/OFF	MARGIN STATE
02h	Immediate off (no sequencing)	—
42h	Soft-off (with sequencing)	—
82h	On	Margin off

Special OPERATION Commands for Dual-Sequencing Mode

When the device is configured to operate in dual-sequencing mode (the DUAL_SEQ bit in MFR_MODE is set), the OPERATION command (described in Table 10) applies to both the primary and secondary sequences. There are several special OPERATION commands for individual control of the primary and secondary sequences (see Table 11 and Table 12). In dual-sequencing mode, when the OPERATION command is read, the channels always respond with the standard OPERATION commands, not the special command bytes (01h, 41h, 81h, 02h, 42h, 82h). These special OPERATION commands can only be used with the PAGE set to 255.

ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of CONTROL input and PMBus OPERATION commands needed to turn the power supply on and off. This indicates how the power supply is commanded when power is applied. Table 13 describes the ON_OFF_CONFIG message content. The host should not modify ON_OFF_CONFIG while the power supplies are active.

When the device is configured to operate in dual-sequencing mode (the DUAL_SEQ bit in MFR_MODE is set), the ON_OFF_CONFIG command applies to both the primary and secondary sequences.

Table 13. ON_OFF_CONFIG (02h) Command Byte

BIT	PURPOSE	BIT VALUE	MEANING
7:5	Reserved	—	Always returns 000.
4	Turn on supplies when bias is present, or use the CONTROL pin and/or OPERATION command.	0	Turn on the supplies (with sequencing if so configured) as soon as bias is supplied to the device regardless of the CONTROL pin.
		1	Use CONTROL pin (if enabled) and/or OPERATION command (if enabled). See note below.
3	OPERATION command enable.	0	Ignore the on/off portion of the OPERATION command.
		1	OPERATION command enabled and required for action.
2	CONTROL pin enable.	0	Ignore the CONTROL pin.
		1	CONTROL pin enabled and required for action.
1	CONTROL pin polarity.	0	Active low (drive low to turn on the power supplies).
		1	Active high (drive high to turn on the power supplies).
0	CONTROL pin turn-off action.	0	Use the programmed turn-off delay (soft-off).
		1	Turn off the power supplies immediately.

Note: *If both bits 2 and 3 are set, both the CONTROL pin and the OPERATION command are required to turn the supplies on, and either one can turn the supplies off.*

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any latched fault or warning bits in the status registers that have been set and also unconditionally deasserts the $\overline{ALERT}$ output. This command clears all bits simultaneously. The CLEAR_FAULTS command does not cause a power supply that has latched off for a fault condition to restart. The state of the PSENn outputs under fault conditions is not affected by this command and changes only if commanded through the OPERATION command or CONTROL pin. If a fault is still present after the CLEAR_FAULTS command is executed, the fault status bit is immediately set again, but $\overline{ALERT}$ is not reasserted. $\overline{ALERT}$ is only asserted again when a new fault or warning is detected that occurs after the CLEAR_FAULTS command is executed. This command is write-only. There is no data byte for this command.

WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to provide protection against accidental changes to the device's operating memory. All supported commands can have their parameters read, regardless of the WRITE_PROTECT settings. The WRITE_PROTECT message content is described in Table 14.

STORE_DEFAULT_ALL (11h)

The STORE_DEFAULT_ALL command instructs the device to transfer the complete device configuration information to the internal flash memory array. Not all information is stored; only configuration data is stored, not any status or operational data. If an error occurs during the transfer, $\overline{ALERT}$ asserts if enabled and the CML bit in and STATUS_WORD is set to 1. No bits are set in STATUS_CML. This command is write-only. There is no data byte for this command. **Note:** It is not recommended to use the STORE_DEFAULT_ALL command while the device is operating power supplies. The device is unresponsive to PMBus commands and does not monitor power supplies while transferring the configuration. If the device configuration needs to be stored to flash while the device is operating the power supplies, it should be done one configuration parameter at a time using the MFR_STORE_SINGLE command.

USER NOTE: V_{DD} must be above 2.9V for the device to perform the STORE_DEFAULT_ALL command.

MFR_STORE_SINGLE (FCh)

MFR_STORE_SINGLE is a read/write word command that instructs the device to transfer a single configuration parameter to the internal flash memory array. The upper byte contains the PAGE and the lower byte contains the PMBus command that should be stored. For example, if the TON_DELAY parameter for the power supply controlled by PAGE 4 needs to be stored to flash, 0460h would be written with this command. When read, this command reports the last single PAGE/command written to flash. This command can be used while the device is operating the power supplies. If an error occurs during the transfer, $\overline{ALERT}$ asserts if enabled and the CML bit in STATUS_WORD is set to 1. No bits are set in STATUS_CML. **Note:** The MFR_STORE_SINGLE command should only be invoked a maximum of 85 times before either a device reset is issued or a device power cycle occurs, or the RESTORE_DEFAULT_ALL command is invoked. Also, MFR_STORE_SINGLE should not be used for commands that are not stored in flash. See Table 1 for a list of commands that are stored in flash.

USER NOTE: V_{DD} must be above 2.9V for the device to perform the MFR_STORE_SINGLE command.

Table 14. WRITE_PROTECT Command Byte

COMMAND BYTE	MEANING
80h	Disables all writes except the WRITE_PROTECT command.
40h	Disables all writes except the WRITE_PROTECT, OPERATION, and PAGE commands.
20h	Disables all writes except the WRITE_PROTECT, OPERATION, PAGE, and ON_OFF_CONFIG commands.
00h	Enables writes for all commands (default).

Note: *No fault or error is generated if the host attempts to write to a protected area.*

RESTORE_DEFAULT_ALL (12h)

The RESTORE_DEFAULT_ALL command transfers the default configuration information from the internal flash memory array to the user memory registers in the device. The RESTORE_DEFAULT_ALL command should only be executed when the device is not operating the power supplies. Upon a device power-on reset or any device reset, this command is automatically executed by the device without PMBus action required. This command is write-only. There is no data byte for this command.

CAPABILITY (19h)

The CAPABILITY command is used to determine some key capabilities of the device. The CAPABILITY command is read-only. The message content is described in Table 15.

VOUT_MODE (20h)

The VOUT_MODE command is used to report the data format of the device. The device uses the DIRECT format for all the voltage-related commands. The value returned is 40h, indicating DIRECT data format. This command is read-only. If a host attempts to write this command, the CML status bit is asserted. See Table 3 for the m, b, and R values for the various commands.

VOUT_MARGIN_HIGH (25h)

The VOUT_MARGIN_HIGH command loads the device with the voltage to which the power-supply output is to be changed when the OPERATION command is set to margin high. If the power supply is already operating at margin high, changing VOUT_MARGIN_HIGH has no effect on the output voltage. The device only adjusts the power supply to the new VOUT_MARGIN_HIGH voltage after receiving a new margin-high OPERATION command. The 2 data bytes are in DIRECT format. If the device cannot successfully close-loop margin the power supply, the device keeps attempting to margin the supply and does the following:

1) Sets the MARGIN bit in STATUS_WORD.
2) Sets the MARGIN_FAULT bit in STATUS_MFR_SPECIFIC (PAGE 0–11).
3) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled in MFR_MODE).

VOUT_MARGIN_LOW (26h)

The VOUT_MARGIN_LOW command loads the device with the voltage to which the power-supply output is to be changed when the OPERATION command is set to margin low. If the power supply is already operating at margin low, changing VOUT_MARGIN_LOW has no effect on the output voltage. The device only adjusts the power supply to the new VOUT_MARGIN_LOW voltage after receiving a new margin-low OPERATION command. The 2 data bytes are in DIRECT format. If the device cannot successfully close-loop margin the power supply, the device keeps attempting to margin the supply and does the following:

1) Sets the MARGIN bit in STATUS_WORD.
2) Sets the MARGIN_FAULT bit in STATUS_MFR_SPECIFIC (PAGE 0–11).
3) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled in MFR_MODE).

Table 15. CAPABILITY Command Byte

BIT	DESCRIPTION	MEANING
7	Packet-error checking	0 = PEC not supported.
6:5	PMBus speed	01 = Maximum supported bus speed is 400kHz.
4	ALERT	1 = Device supports an ALERT output (if ALERT is enabled in MFR_MODE). 0 = Device does not support ALERT output (ALERT is disabled in MFR_MODE).
3:0	Reserved	Always returns 0000.

VOUT_SCALE_MONITOR (2Ah)

In applications where the measured power-supply voltage is not equal to the voltage at the ADC input, VOUT_SCALE_MONITOR is used. For example, if the ADC input expects a 1.8V input for a 12V output, VOUT_SCALE_MONITOR = 1.8V/12V = 0.15. In applications where the power-supply output voltage is greater than the device's 2.048V input range, the output voltage of the power supply is sensed through a resistive voltage-divider. The resistive voltage-divider reduces or scales the output voltage. The PMBus commands specify the actual power-supply output voltages and not the input voltage to the ADC. To allow the device to map between the high power-supply voltages (such as 12V) and the voltage at the ADC input, the VOUT_SCALE_MONITOR command is used. The 2 data bytes are in DIRECT format. This value is dimensionless. For example, if the required scaling factor is 0.15, then VOUT_SCALE_MONITOR should be set to 1333h (4915/32767 = 0.15). See Table 16 for more examples.

Table 16. VOUT_SCALE_MONITOR Examples

NOMINAL VOLTAGE LEVEL MONITORED (V)	NOMINAL ADC INPUT VOLTAGE LEVEL (V)*	RESISTIVE VOLTGE-DIVIDER RATIO	VOUT_SCALE_MONITOR VALUE (hex)
1.8 or less	1.8	1.0	7FFFh
2.5	1.8	0.72	5C28h
3.3	1.8	0.545454	45D1h
5	1.8	0.36	2E14h
12	1.8	0.15	1333h

**The full-scale ADC voltage on the device is 2.048V. A scaling factor where a 1.8V ADC input represents a nominal 100% voltage level is recommended to allow headroom for margining. Resistor-dividers with a maximum source impedance of 1kΩ must be used to measure voltage greater than 1.8V.*

Table 17. Parametric Monitoring States

PARAMETER	REQUIRED CONDITIONS FOR ACTIVE MONITORING	ACTION DURING A FAULT
Overvoltage	• Power supply enabled (TON_MAX_FAULT_LIMIT ≠ 8000h to FFFFh)	Stop monitoring while PSENn is inactive and resume monitoring before channel is restarted.
Undervoltage	• Power supply enabled (TON_MAX_FAULT_LIMIT ≠ 8000h to FFFFh) • PSENn output is active • Channel's VOUT must have exceeded VOUT_UV_FAULT during channel power-up	Stop monitoring while the power supply is off.
Power-up time	• Power supply enabled (TON_MAX_FAULT_LIMIT ≠ 8000h to FFFFh or 0000h) • PSENn output is active	Monitor only during power-on.
Overtemperature	• Temp sensor enabled (ENABLE in MFR_TEMP_SENSOR_CONFIG = 1)	Continue monitoring.

VOUT_OV_FAULT_LIMIT (40h)

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage that causes an output overvoltage fault. The monitored voltage must drop by at least 2% below the limit before the fault is allowed to clear. This fault is masked until the output voltage is below this limit for the first time. The 2 data bytes are in DIRECT format. In response to the VOUT_OV_FAULT_LIMIT being exceeded, the device does the following:

1) Sets the VOUT_OV bit and the VOUT bit in STATUS_WORD.
2) Sets the VOUT_OV_FAULT bit in STATUS_VOUT.
3) Responds as specified in the MFR_FAULT_RESPONSE.
4) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled in MFR_MODE).

VOUT_OV_WARN_LIMIT (42h)

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage that causes an output voltage high warning. The monitored voltage must drop by at least 2% below the limit before the warning is allowed to clear. This warning is masked until the output voltage is below this limit for the first time. This value is typically less than the output overvoltage threshold in VOUT_OV_FAULT_LIMIT. The 2 data bytes are in DIRECT format. In response to the VOUT_OV_WARN_LIMIT being exceeded, the device does the following:

1) Sets the VOUT bit in STATUS_WORD.
2) Sets the VOUT_OV_WARN bit in STATUS_VOUT.
3) Notifies the host using $\overline{\text{ALERT}}$ assertion (if enabled in MFR_MODE).

VOUT_UV_WARN_LIMIT (43h)

The VOUT_UV_WARN_LIMIT command sets the value of the output voltage that causes an output-voltage low warning. The monitored voltage must increase by at least 2% above the limit before the warning is allowed to clear. This value is typically greater than the output undervoltage fault threshold in VOUT_UV_FAULT_LIMIT. This warning is masked until the output voltage reaches the programmed VOUT_UV_WARN_LIMIT for the first time and also during turn-off when the power supply is disabled. The 2 data bytes are in DIRECT format. In response to violation of the VOUT_UV_WARN_LIMIT, the device does the following:

1) Sets the VOUT bit in STATUS_WORD.
2) Sets the VOUT_UV_WARN bit in STATUS_VOUT.
3) Notifies the host using $\overline{\text{ALERT}}$ assertion (if enabled in MFR_MODE).

VOUT_UV_FAULT_LIMIT (44h)

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage, which causes an output undervoltage fault. The monitored voltage must increase by at least 2% above the limit before the fault is allowed to clear. This fault is masked until the output voltage reaches the programmed VOUT_UV_FAULT_LIMIT for the first time and also during turn-off when the power supply is disabled. The VOUT_UV_FAULT_LIMIT threshold is also used to determine if TON_MAX_FAULT_LIMIT is exceeded. The 2 data bytes are in DIRECT format. In response to violation of the VOUT_UV_FAULT_LIMIT, the device does the following:

1) Sets the VOUT bit in STATUS_WORD.
2) Sets the VOUT_UV_FAULT bit in STATUS_VOUT.
3) Responds as specified in MFR_FAULT_RESPONSE.
4) Notifies the host using $\overline{\text{ALERT}}$ assertion (if enabled in MFR_MODE).

OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command sets the temperature, in degrees Celsius, of the selected temperature sensor at which an overtemperature fault is detected. The monitored temperature must drop by at least 4°C below the limit before the fault is allowed to clear. The 2 data bytes are in DIRECT format. In response to the OT_FAULT_LIMIT being exceeded, the device does the following:

1) Sets the TEMPERATURE bit in STATUS_WORD.
2) Sets the OT_FAULT bit in STATUS_TEMPERATURE register.
3) Responds as specified in the MFR_FAULT_RESPONSE.
4) Notifies the host using $\overline{\text{ALERT}}$ assertion (if enabled in MFR_MODE).

OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT command sets the temperature, in degrees Celsius, of the selected temperature sensor at which an overtemperature warning is detected. The monitored temperature must drop by at least 4°C below the limit before the warning is allowed to clear. The 2 data bytes are in DIRECT format. In response to the OT_WARN_LIMIT being exceeded, the device does the following:

1) Sets the TEMPERATURE bit in STATUS_WORD.
2) Sets the OT_WARN bit in STATUS_TEMPERATURE register.
3) Notifies the host through $\overline{ALERT}$ assertion (if enabled in MFR_MODE).

POWER_GOOD_ON (5Eh)

The POWER_GOOD_ON command sets the value of the output voltage, which causes the PG output (and the PG2 output in dual-sequencing mode) to assert. All power supplies must be above their associated POWER_GOOD_ON thresholds before the PG output is asserted. Unused channels or disabled power supplies can use the test mode described in the user note below to force power good on the associated channel. All power supplies must also be above POWER_GOOD_ON for power-supply margining to begin. The POWER_GOOD_ON level is normally set higher than the POWER_GOOD_OFF level. The 2 data bytes are in DIRECT format.

USER NOTE: There is a special test mode that forces a channel into and out of a power good state based on two unique values. If either of these settings is configured into POWER_GOOD_ON, the actual measured power-supply voltage is ignored and the logical state is forced.

- Force power-good deassert = POWER_GOOD_ON = 7FFFh
- Force power-good assert = POWER_GOOD_ON = 0000h

POWER_GOOD_OFF (5Fh)

The POWER_GOOD_OFF command sets the value of the output voltage that causes the PG output to deassert after it has been asserted. Any power supply that falls below the associated POWER_GOOD_OFF threshold causes the PG output to be deasserted. The POWER_GOOD_OFF level is normally set lower than the POWER_GOOD_ON level. The 2 data bytes are in DIRECT format.

When the V_{OUT} level of a power supply falls from greater than POWER_GOOD_ON to less than POWER_GOOD_OFF, the device does the following:

1) Sets the POWER_GOOD# bit in STATUS_WORD.
2) Sets the POWER_GOOD# bit in STATUS_MFR_SPECIFIC register (PAGE 0–11).

TON_DELAY (60h)

In the PMBus-sequencing configuration, TON_DELAY sets the time, in milliseconds, from when a START condition is received (a valid OPERATION command or through the CONTROL pin when enabled) until the PSENn output is asserted. In the timeslot-sequencing configuration, TON_DELAY sets the time, in milliseconds, from the beginning of a timeslot until the PSENn output is asserted. The undervoltage fault and warning are masked off during TON_DELAY. The 2 data bytes are in DIRECT format.

TOFF_DELAY (64h)

The TOFF_DELAY sets the time, in milliseconds, from when a STOP condition is received (a soft-off OPERATION command or through the CONTROL pin when enabled) until the PSENn output is deasserted. When commanded to turn off immediately (either through the OPERATION command or the CONTROL pin), the TOFF_DELAY value is ignored. The 2 data bytes are in DIRECT format.

Table 18. TON_MAX_FAULT_LIMIT Device Response

SEQUENCING CONFIGURATION (NOTE 2)	TON_MAX_ FAULT_LIMIT VALUE	DEVICE RESPONSE (FOR EACH ASSOCIATED PAGE) (NOTE 1)		
		SEQUENCING RESPONSE	VOLTAGE FAULT MONITORING (NOTE 3)	USE PSENn AS GPO (NOTE 4)
Standard	0001h to 7FFFh	Device asserts PSENn and monitors RSn to cross the undervoltage-fault limit in the time set by TON_MAX_FAULT_LIMIT.	Enabled	No
Blind	0000h	Device asserts PSENn and monitors RSn but does not wait for RS to cross the undervoltage-fault limit. In timeslot sequencing, this channel exceeding undervoltage-fault limit is not used to time the start of the next timeslot.	Enabled	No
Monitoring only	0000h	PSENn should be configured as GPO and RSn monitoring for faults and warnings is enabled. In timeslot sequencing, this channel should be assigned to timeslot 0 and TON_DELAY should be set to 0.	Enabled	Yes
Off	8000h to FFFFh	PSENn should be configured as GPO and RSn monitoring for faults and warnings is disabled.	Defeated	Yes

Note 1: There is one-to-one correspondence between the RSn input and the PSENn output for each page.
Note 2: See Figure 5 for example hardware configurations.
Note 3: Voltage monitoring includes overvoltage and undervoltage.
Note 4: The GPO configuration for PSENn is set with the MFR_PSEN_CONFIG command and can be configured to override the normal sequencing action of the PSENn output.

TON_MAX_FAULT_LIMIT (62h)

The TON_MAX_FAULT_LIMIT sets an upper time limit, in milliseconds, from when the PSENn output is asserted until the output voltage crosses the VOUT_UV_FAULT_LIMIT threshold. The 2 data bytes are in DIRECT format. If the value is less than zero, then the power supply is not sequenced by the device and the associated PSENn output remains deasserted and voltage faults are disabled. See Table 18 for more details. In response to the TON_MAX_FAULT_LIMIT being exceeded, the device does the following:

1) Sets the VOUT bit in STATUS_WORD.
2) Sets the TON_MAX_FAULT bit in STATUS_VOUT.
3) Responds as specified in the MFR_FAULT_RESPONSE.
4) Notifies the host using $\overline{\text{ALERT}}$ assertion (if enabled in MFR_MODE).

If an event is still present when the CLEAR_FAULTS command is issued, the bit is immediately asserted once again. When the $\overline{\text{ALERT}}$ latch is cleared, if any events are still present, they do not reassert the $\overline{\text{ALERT}}$ output.

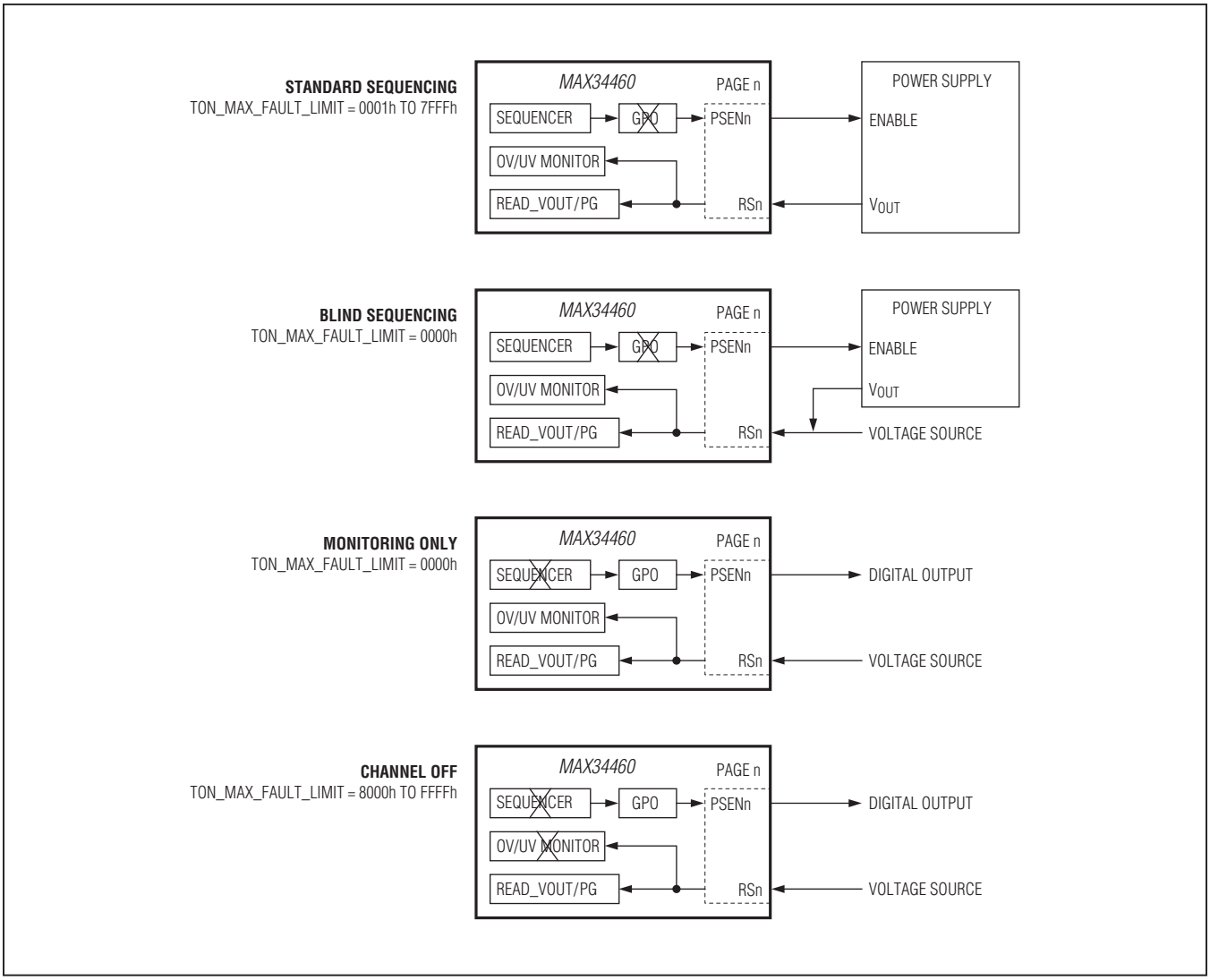


Figure 5. Sequencing Configurations

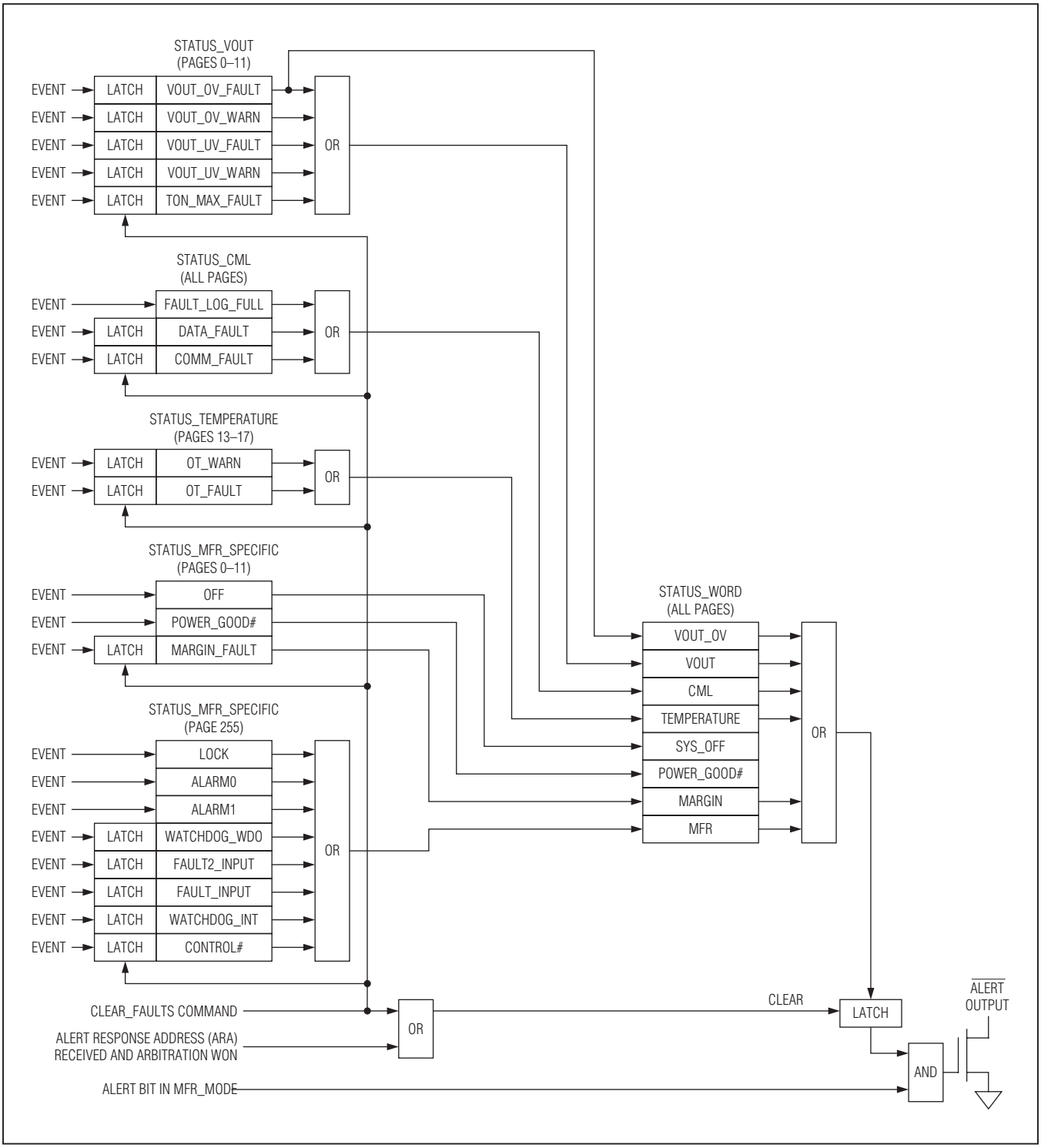


Figure 6. Status Register Organization

STATUS_WORD (79h)

The STATUS_WORD command returns 2 bytes of information with a summary of the reason for a fault. The STATUS_WORD message content is described in Table 19. See Figure 6 for status register organization.

STATUS_VOUT (7Ah)

The STATUS_VOUT command returns 1 byte of information with contents, as described in Table 20. All the bits in STATUS_VOUT are latched. When cleared, the bits are set again if the condition persists, or in the case of TON_MAX_FAULT, when the event occurs again.

Table 19. STATUS_WORD

BIT	NAME	MEANING
15	VOUT	An output voltage fault or warning or TON_MAX_FAULT has occurred.
14	0	This bit always returns a 0.
13	0	This bit always returns a 0.
12	MFR	A bit in STATUS_MFR_SPECIFIC (PAGE = 255) has been set.
11	POWER_GOOD#	Any power-supply voltage has fallen from POWER_GOOD_ON to less than POWER_GOOD_OFF (logical OR of all the POWER_GOOD# bits in STATUS_MFR_SPECIFC).
10	0	This bit always returns a 0.
9	0	This bit always returns a 0.
8	MARGIN	A margining fault has occurred.
7	0	This bit always returns a 0.
6	SYS_OFF	Set when any of the power supplies are sequenced off (logical OR of all the OFF bits in STATUS_MFR_SPECIFC).
5	VOUT_OV	An overvoltage fault has occurred.
4	0	This bit always returns a 0.
3	0	This bit always returns a 0.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communication, memory, or logic fault has occurred.
0	0	This bit always returns a 0.

Note: *The setting of the SYS_OFF and POWER_GOOD# bits do not assert the $\overline{ALERT}$ signal.*

Table 20. STATUS_VOUT

BIT	NAME	MEANING	LATCHED
7	VOUT_OV_FAULT	V_{OUT} overvoltage fault.	Yes
6	VOUT_OV_WARN	V_{OUT} overvoltage warning.	Yes
5	VOUT_UV_WARN	V_{OUT} undervoltage warning.	Yes
4	VOUT_UV_FAULT	V_{OUT} undervoltage fault.	Yes
3	0	This bit always returns a 0.	—
2	TON_MAX_FAULT	TON maximum fault.	Yes
1	0	This bit always returns a 0.	—
0	0	This bit always returns a 0.	—

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns 1 byte of information with contents, as described in Table 21. All the bits in STATUS_VOUT are latched. When cleared, the bits are set again if the condition persists.

STATUS_CML (7Eh)

The STATUS_CML command returns 1 byte of information with contents, as described in Table 22. The COMM_FAULT and DATA_FAULT bits are latched. When cleared, the bits are set again when the event occurs again. The FAULT_LOG_FULL bit reflects the current real-time state of the fault log.

Table 21. STATUS_TEMPERATURE

BIT	NAME	MEANING	LATCHED
7	OT_FAULT	Overtemperature fault.	Yes
6	OT_WARN	Overtemperature warning.	Yes
5	0	This bit always returns a 0.	—
4	0	This bit always returns a 0.	—
3	0	This bit always returns a 0.	—
2	0	This bit always returns a 0.	—
1	0	This bit always returns a 0.	—
0	0	This bit always returns a 0.	—

Table 22. STATUS_CML

BIT	NAME	MEANING	LATCHED
7	COMM_FAULT	An invalid or unsupported command has been received.	Yes
6	DATA_FAULT	An invalid or unsupported data has been received.	Yes
5	0	This bit always returns a 0.	—
4	0	This bit always returns a 0.	—
3	0	This bit always returns a 0.	—
2	0	This bit always returns a 0.	—
1	0	This bit always returns a 0.	—
0	FAULT_LOG_FULL	MFR_NV_FAULT_LOG is full and needs to be cleared.*	No

**When NV Fault Log Overwrite is enabled (NV_LOG_OVERWRITE = 1 in MFR_NV_LOG_CONFIG), FAULT_LOG_FULL will be set when the fault log is full but will clear when the fault log is overwritten since two fault logs are cleared before each overwrite.*

STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC message content varies based on the selected page, and is described in Table 23 and Table 24.

READ_VOUT (8Bh)

The READ_VOUT command returns the actual measured (not commanded) output voltage. READ_VOUT is measured and updated every 5ms. The 2 data bytes are in DIRECT format.

Table 23. STATUS_MFR_SPECIFIC (for PAGES 0–11)

BIT	NAME	MEANING	LATCHED
7	OFF	For enabled channels (TON_MAX_FAULT_LIMIT ≥ 0), this bit reflects the output state of the sequencer and is set when PSENn is not asserted due to either a sequencing delay or fault, or the power supply being turned off. This bit is always cleared when the channel is disabled (TON_MAX_FAULT_LIMIT < 0). If PSENn is reconfigured as a GPO, this bit does not reflect the state of the pin.	No
6	0	This bit always returns a 0.	—
5	0	This bit always returns a 0.	—
4	0	This bit always returns a 0.	—
3	MARGIN_FAULT	This bit is set if the device cannot properly close-loop margin the power supply.	Yes
2	POWER_GOOD#	This bit is set when the power-supply voltage has fallen from POWER_GOOD_ON to less than POWER_GOOD_OFF. In the PG test mode, this bit reflects the forced PG state. On device reset, this bit is set until the power supply is greater than POWER_GOOD_ON.	No
1	0	This bit always returns a 0.	—
0	0	This bit always returns a 0.	—

Note: *The setting of the OFF and POWER_GOOD# bits do not assert the $\overline{ALERT}$ signal.*

Table 24. STATUS_MFR_SPECIFIC (for PAGE 255)

BIT	NAME	MEANING	LATCHED
7	LOCK	Set when the device is password protected (Note 1).	No
6	FAULT_INPUT	Set each time the $\overline{FAULT}$ input is pulled low (Note 2).	Yes
5	FAULT2_INPUT	Set each time the $\overline{FAULT2}$ input is pulled low (Note 2).	Yes
4	WATCHDOG_INT	Set upon device reset when the internal watchdog has caused the device reset.	Yes
3	CONTROL#	Set each time the CONTROL input is deasserted (Note 3).	Yes
2	WDO	Set each time the external $\overline{WDO}$ pin is asserted.	Yes
1	ALARM1	Set when the $\overline{ALARM1}$ output is active.	No
0	ALARM0	Set when the $\overline{ALARM0}$ output is active.	No

Note 1: The setting of the LOCK bit does not assert the $\overline{ALERT}$ signal.

Note 2: The FAULTn status bits are set even if the $\overline{FAULTn}$ pins are configured in MFR_MODE to ignore the $\overline{FAULT}$ pin. The FAULT2_INPUT status bit only functions if the device is in dual-sequencing mode.

Note 3: In dual-sequencing mode, either CONTROL input sets this bit. ON_OFF_CONFIG must be set to use the CONTROL pin for this status bit to function.

READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE_1 command returns the temperature returned from the temperature sensor. READ_TEMPERATURE_1 returns 7FFFh if the sensor is faulty and 0000h if the sensor is disabled. READ_TEMPERATURE_1 is measured and updated once per second. The 2 data bytes are in DIRECT format.

PMBUS_REVISION (98h)

The PMBUS_REVISION command returns the revision of the PMBus specification to which the device is compliant. The command has 1 data byte. Bits [7:4] indicate the revision of PMBus specification Part I to which the device is compliant. Bits [3:0] indicate the revision of PMBus specification Part II to which the device is compliant. This command is read-only. The PMBUS_REVISION value returned is always 11h, which indicates that the device is compliant with Part I Rev 1.1 and Part II Rev 1.1.

MFR_ID (99h)

The MFR_ID command returns the text (ISO/IEC 8859-1) character of the manufacturer's (Maxim) identification. The default MFR_ID value is 4Dh (M). This command is read-only.

MFR_MODEL (9Ah)

The MFR_MODEL command returns the text (ISO/IEC 8859-1) character of the device model number. The default MFR_MODEL value is 57h (W). This command is read-only.

MFR_REVISION (9Bh)

The MFR_REVISION command returns two text (ISO/IEC 8859-1) characters that contain the device revision numbers for hardware (upper byte) and firmware (lower byte). This command is read-only.

MFR_LOCATION (9Ch)

The MFR_LOCATION command loads the device with text (ISO/IEC 8859-1) characters that identify the facility that manufactures the power supply. The maximum number of characters is 8. This data is written to internal flash using the STORE_DEFAULT_ALL command. The factory default text string value is 10101010.

MFR_DATE (9Dh)

The MFR_DATE command loads the device with text (ISO/IEC 8859-1) characters that identify the date of manufacture of the power supply. The maximum number of characters is 8. This data is written to internal flash using the STORE_DEFAULT_ALL command. The factory-default text string value is 10101010.

MFR_SERIAL (9Eh)

The MFR_SERIAL command loads the device with text (ISO/IEC 8859-1) characters that uniquely identify the device. The maximum number of characters is 8. This data is written to internal flash using the STORE_DEFAULT_ALL command. The factory-default text string value is 10101010. The upper 4 bytes of MFR_SERIAL are used to unlock a device that has been password protected. The lower 4 bytes of MFR_SERIAL are not used to unlock a device and can be set to any value.

MFR_MODE (D1h)

The MFR_MODE command is used to configure the device to support manufacturer-specific commands. The MFR_MODE command should not be changed while power supplies are operating. The MFR_MODE command is described in Table 25.

Table 25. MFR_MODE

<table>
<tr><th>BIT</th><th>NAME</th><th>MEANING</th></tr>
<tr><td>15:14</td><td>MULTI_SEQ[1:0]</td><td>These bits set the sequencing configuration for the primary sequencing group. The secondary sequencing group should not use cascaded sequencing if the group involves multiple devices.
00 = Single device or multiple devices with Common Control or Common OPERATION Command.
01 = Multiple devices with cascaded sequencing–slave device.
10 = Multiple devices with cascaded sequencing–master device with latchoff.
11 = Multiple devices with cascaded sequencing–master device with retry.</td></tr>
<tr><td>13</td><td>ALERT</td><td>0 = $\overline{\text{ALERT}}$ disabled (device does not respond to ARA).
1 = $\overline{\text{ALERT}}$ enabled (device does respond to ARA).</td></tr>
<tr><td>12</td><td>SEQ</td><td>0 = PMBus-defined time-based sequencing.
1 = Timeslot-defined event-based sequencing.</td></tr>
<tr><td>11</td><td>SOFT_RESET</td><td>This bit must be set, then cleared and set again within 8ms for a soft-reset to occur.</td></tr>
<tr><td>10</td><td>LOCK</td><td>This bit must be set, then cleared and set again within 8ms for the device to become password protected. This bit is cleared when the password is unlocked. The device should only be locked and then unlocked a maximum of 256 times before either a device reset is issued or a device power cycle occurs.</td></tr>
<tr><td>9:8</td><td>0</td><td>These bits always return a 0.</td></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">ADC_TIME[1:0]</td><td>These bits select the ADC conversion time.</td></tr>
<tr><td>ADC_TIME[1:0]</td><td>ADC CONVERSION TIME (µs)</td></tr>
<tr><td>00</td><td>1</td></tr>
<tr><td>01</td><td>2</td></tr>
<tr><td>10</td><td>4</td></tr>
<tr><td>11</td><td>8</td></tr>
<tr><td>5</td><td>DUAL_SEQ</td><td>0 = Single-sequence mode.
1 = Dual-sequence mode.</td></tr>
<tr><td>4</td><td>FAULT_IGNORE</td><td>0 = Shut down all GLOBAL primary channels when $\overline{\text{FAULT}}$ is pulled low.
1 = Ignore $\overline{\text{FAULT}}$ if pulled low ($\overline{\text{FAULT}}$ still asserted as configured in MFR_FAULT_RESPONSE).</td></tr>
<tr><td rowspan="6">3:2</td><td rowspan="6">ADC_AVERAGE[1:0]</td><td>These bits select the post ADC conversion averaging:</td></tr>
<tr><td>ADC_AVERAGE[1:0]</td><td>ADC AVERAGING</td></tr>
<tr><td>00</td><td>No averaging</td></tr>
<tr><td>01</td><td>Average 2 samples</td></tr>
<tr><td>10</td><td>Average 4 samples</td></tr>
<tr><td>11</td><td>Average 8 samples</td></tr>
<tr><td>1</td><td>FAULT2_IGNORE</td><td>0 = Shut down all GLOBAL secondary channels when $\overline{\text{FAULT2}}$ is pulled low.
1 = Ignore $\overline{\text{FAULT2}}$ if pulled low ($\overline{\text{FAULT2}}$ still asserted as configured in MFR_FAULT_RESPONSE).</td></tr>
<tr><td>0</td><td>ALARM_CLR</td><td>Setting this bit to a 1 clears $\overline{\text{ALARM0}}$ and $\overline{\text{ALARM1}}$ if they are asserted. Once set, the device clears this bit when the action is completed. The host must set again for subsequent action.</td></tr>
</table>

MFR_PSEN_CONFIG (D2h)

The MFR_PSEN_CONFIG command is used to configure the individual PSENn outputs. This command should not be changed while the power supplies are operating. The MFR_PSEN_CONFIG command is described in Table 26 and Table 27.

Table 26. PSENn Configuration

COMMAND BYTE	PSENn CONFIGURATION		
00	Normal power-supply enable/disable control action	Active low	Push-pull
40		Active high	
80		Active low	Open drain
C0		Active high	
01	Override action (GPO mode)	Force low	Push-pull
41		Force high	
81		Force low	Open drain
C1		Force high	

Table 27. MFR_PSEN_CONFIG

BIT	NAME	MEANING
7	PSEN_PP_OD	0 = PSENn push-pull output. 1 = PSENn open-drain output.
6	PSEN_HI_LO	0 = PSENn active-low. 1 = PSENn active-high.
5:1	0	These bits always return a 0.
0	OVERRIDE	When this bit is set to a 1, the associated PSENn output pin no longer responds as a normal enable/disable for the power supply, but rather is forced active either high or low as indicated by bit 6 and is configured as either open drain or push-pull as configured by bit 7.

MFR_SEQ_TIMESLOT (D3h)

The MFR_SEQ_TIMESLOT command is used in the timeslot-defined sequencing mode (SEQ bit in MFR_MODE is set) to determine which timeslot the PSENn output is associated with and the command is also used in the dual-sequencing mode (DUAL_SEQ bit in MFR_MODE is set) to assign channels to a group. In the timeslot-defined sequencing mode, multiple PSENn outputs can be assigned to the same timeslot. Not all timeslots must be used, but the ordering must be sequential. GLOBAL channels must start with timeslot 0. LOCAL channels can be assigned to any timeslot. The MFR_SEQ_TIMESLOT command is described in Table 28.

MFR_VOUT_PEAK (D4h)

The MFR_VOUT_PEAK command returns the maximum actual measured output voltage. To reset this value to 0, write to this command with a data value of 0. Any values written to this command are used as a comparison for future peak updates. The 2 data bytes are in DIRECT format.

MFR_TEMPERATURE_PEAK (D6h)

The MFR_TEMPERATURE_PEAK command returns the maximum measured temperature. To reset this value to its lowest value, write to this command with a data value of 8000h. Any other values written by this command are used as a comparison for future peak updates. The 2 data bytes are in DIRECT format.

MFR_VOUT_MIN (D7h)

The MFR_VOUT_MIN command returns the minimum actual measured output voltage. To reset this value, write to this command with a data value of 7FFFh. Any values written to this command are used as a comparison for future minimum updates. The 2 data bytes are in DIRECT format.

MFR_TEMPERATURE_AVG (E3h)

The MFR_TEMPERATURE_AVG command returns the calculated average temperature. To reset the average, write to this command with a data value of 0. Any other values written by this command are ignored. The 2 data bytes are in DIRECT format.

Table 28. MFR_SEQ_TIMESLOT

BIT	NAME	MEANING
7:6	0	These bits always return a 0.
5	GROUP (dual-sequence mode only)	This bit is used in dual-sequencing mode to determine the sequencing channel assignment. This bit is ignored if the dual-sequencing mode is disabled (DUAL_SEQ bit in MFR_MODE is cleared). 0 = Channel is assigned to the primary sequencing group. 1 = Channel is assigned to the secondary sequencing group.
4	0	These bits always return a 0.
3:0	TIMESLOT[3:0]	Timeslot assignment (ignored in PMBus sequence mode): 0000 Timeslot 0 — 1000 Timeslot 8 0001 Timeslot 1 — 1001 Timeslot 9 0010 Timeslot 2 — 1010 Timeslot 10 0011 Timeslot 3 — 1011 Timeslot 11 0100 Timeslot 4 — 1100 Reserved 0101 Timeslot 5 — 1101 Reserved 0110 Timeslot 6 — 1110 Reserved 0111 Timeslot 7 — 1111 Reserved

MFR_NV_LOG_CONFIG (D8h)

The MFR_NV_LOG_CONFIG command is used to configure the operation of the nonvolatile fault logging in the device. The MFR_NV_LOG_CONFIG command is described in Table 29.

Table 29. MFR_NV_LOG_CONFIG

BIT	NAME	MEANING
15	FORCE_NV_FAULT_LOG	Setting this bit to a 1 forces the device to log data into the nonvolatile fault log. Once set, the device clears this bit when the action is completed. The host must set again for subsequent action. If an error occurs during this action, the device sets the CML bit in STATUS_WORD; no bits are set in STATUS_CML.
14	CLEAR_NV_FAULT_LOG	Setting this bit to a 1 forces the device to clear the nonvolatile fault log by writing FFh to all byte locations. Once set, the device clears this bit when the action is completed. The host must set again for subsequent action. If an error occurs during this action, the device sets the CML bit in STATUS_WORD; no bits are set in STATUS_CML. While clearing the fault log, monitoring is stopped and commands should not be sent to the PMBus port.
13:11	0	These bits always return a 0.
10	NV_LOG_T0_CONFIG	This bit determines the source of the data written into the T0 location of each page when a nonvolatile fault log is written. 0 = Log the last regular collection interval ADC reading. 1 = Read the latest ADC value before logging.
9	NV_LOG_OVERWRITE	0 = Do not overwrite the NV fault log. 1 = Overwrite the NV fault log once it is full.*
8:7	NV_LOG_DEPTH[1:0]	These bits determine the depth of the NV fault log: **ADC RESULT COLLECTION NV FAULT LOG** **NV_LOG_DEPTH[1:0] / INTERVAL (ms) / DEPTH (ms)** 00 / 5 / 25 01 / 20 / 100 10 / 80 / 400 11 / 160 / 800
6	NV_LOG_FAULT	0 = Do not write NV fault log when $\overline{\text{FAULT}}$ or $\overline{\text{FAULT2}}$ is externally pulled low. 1 = Write NV fault log when $\overline{\text{FAULT}}$ or $\overline{\text{FAULT2}}$ is externally pulled low if the FAULT_IGNORE or FAULT_IGNORE2 bits are not set in MFR_MODE.
5:0	0	These bits always return a 0.

**The device clears two fault logs at a time when overwrite is enabled.*

MFR_FAULT_RESPONSE (D9h)

The MFR_FAULT_RESPONSE command specifies the response to each fault or warning condition supported by the device. In response to a fault/warning, the device always reports the fault/warning in the appropriate status register and asserts the $\overline{ALERT}$ output (if enabled in MFR_MODE). A CML fault cannot cause any device action other than setting the status bit and asserting the $\overline{ALERT}$ output. The MFR_FAULT_RESPONSE command is described in Table 30 and Figure 7.

LOCAL vs. GLOBAL Channels

With the MFR_FAULT_RESPONSE command (bit 14), each power-supply channel can be tagged as either being LOCAL or GLOBAL. When bit 14 is cleared, the channel is configured as a LOCAL channel, which means that a detected fault only affects this channel. With the RESPONSE bits in the MFR_FAULT_RESPONSE command, the device can be configured to respond differently to each possible fault. When bit 14 is set, the channel is configured as a GLOBAL channel, which means that a detected fault on this channel affects all other channels also tagged as GLOBAL channels within their respective sequencing group (i.e., either the primary or secondary sequencing group). Also, any GLOBAL channel can be configured to assert their associated hardware fault signal pins ($\overline{FAULT}$ for the primary sequencing group and $\overline{FAULT2}$ for the secondary sequencing group). Only GLOBAL channels respond to assertions of the fault pins; LOCAL channels do not respond to the fault pins. In the timeslot-defined sequencing mode, GLOBAL channels must start with timeslot 0. LOCAL channels can be assigned to any timeslot.

Fault Detection Before PSENn Assertion

Before any power-supply channel is enabled, the device checks for overvoltage and temperature faults. With GLOBAL channels, all channels must be clear of faults and the fault pins must be deasserted (if enabled) before the channels are allowed to be enabled.

Table 30. MFR_FAULT_RESPONSE (Note 1)

BIT	NAME	MEANING
15	NV_LOG	0 = Do not log the fault into MFR_NV_FAULT_LOG. 1 = Log the fault into MFR_NV_FAULT_LOG.
14	GLOBAL	0 = LOCAL (affects only the selected page power supply). 1 = GLOBAL (affects all supplies with GLOBAL = 1).
13:12	FILTER[1:0]	Excursion time before a fault or warning is declared and action is taken (Note 2). 00 = Immediate 01 = 2ms 10 = 3ms 11 = 4ms
11:8	ALARM_CONFIG[3:0]	See Table 31.
7:6	OT_FAULT_LIMIT_RESPONSE[1:0]	See Tables 32 and 33 (Notes 3 and 4).
5:4	TON_MAX_FAULT_LIMIT_RESPONSE[1:0]	See Tables 32 and 33.
3:2	VOUT_UV_FAULT_LIMIT_RESPONSE[1:0]	See Tables 32 and 33.
1:0	VOUT_OV_FAULT_LIMIT_RESPONSE[1:0]	See Tables 32 and 33.

Note 1: The fault response for power-supply faults is determined by the programmed MFR_FAULT_RESPONSE for the faulting channel. If this channel is part of a GLOBAL group, this fault response is performed for all of the GLOBAL channels.

Note 2: The FILTER selection does not apply to temperature or sequencing faults.

Note 3: All enabled temperature-sensor faults are logically ORed together.

Note 4: Temperature faults affect all enabled power supplies. Supplies that are designated as GLOBAL all respond in the same manner. This response is the worst-case response of the GLOBAL channels for the given fault. Supplies that are not GLOBAL respond to a temperature fault based upon the programmed response for the particular supply.

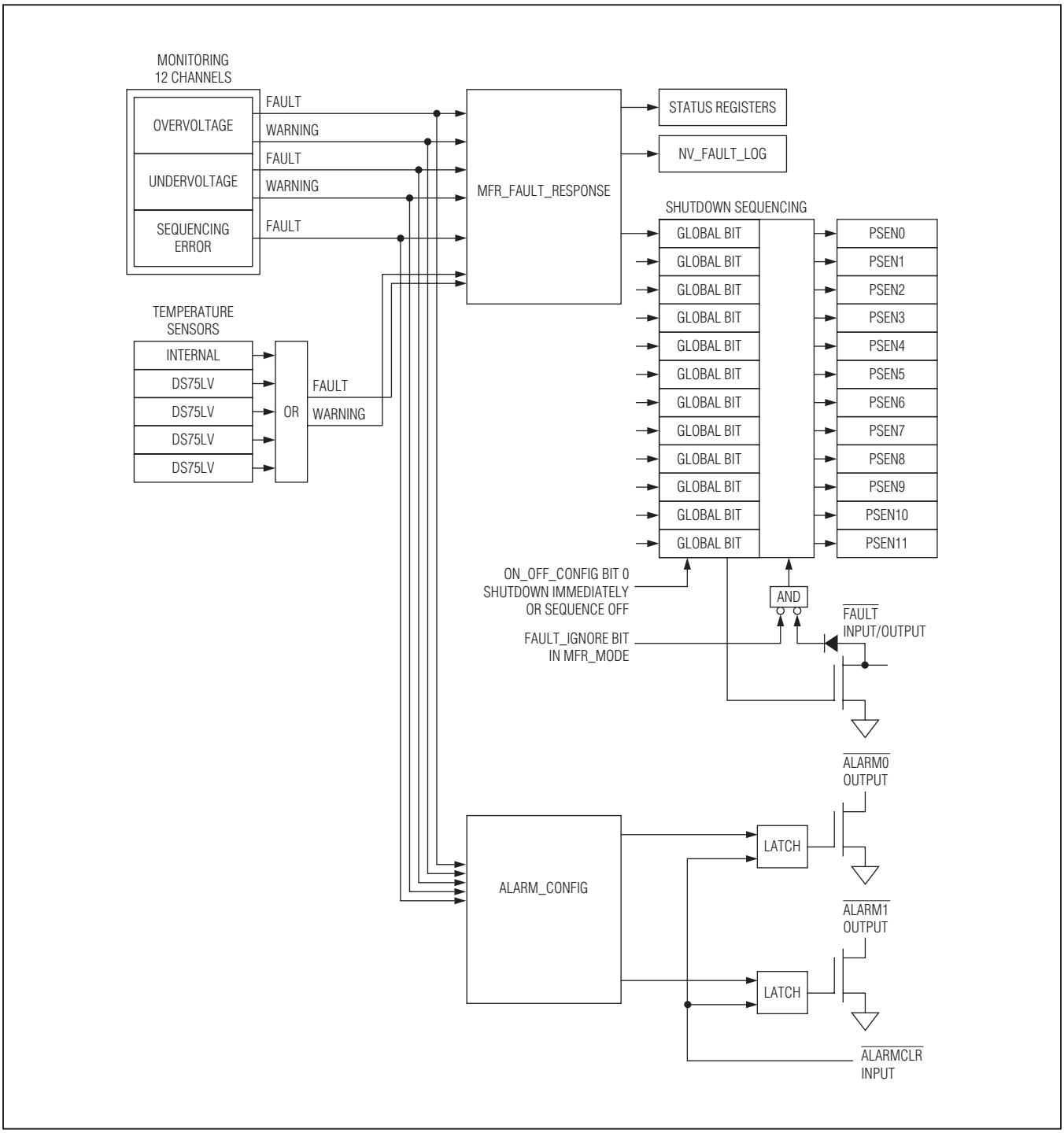


Figure 7. MFR_FAULT_RESPONSE Operation

Logging Faults into MFR_NV_FAULT_LOG

If bit 15 of MFR_FAULT_RESPONSE is set, faults are logged into the on-board nonvolatile fault log for this channel unless the response for the associated fault is configured to take no action (RESPONSE[1:0] = 00). To keep from needlessly filling the fault log with excessive data, the following rules are applied when subsequent faults occur. When overvoltage faults occur, subsequent overvoltage faults on this channel are not written to the fault log until either the CLEAR_FAULTS command is issued or the associated PSENn output has been deasserted for any reason. The same rule applies to undervoltage. When an overtemperature fault occurs, subsequent overtemperature faults on the faulting temperature sensor are not written to the fault log until a CLEAR_FAULTS command is written. All sequencing faults are written to the fault log.

Table 31. ALARM_CONFIG Codes

ALARM_CONFIG[3:0]	ALARM OUTPUT SELECTED	ALARM CONDITION	ALARM CRITERIA
0000	ALARM0	None	—
0001	ALARM0	Sequencing fault	Fault only
0010	ALARM0	Undervoltage only	Fault only
0011	ALARM0	Undervoltage only	Fault or warning
0100	ALARM0	Overvoltage only	Fault only
0101	ALARM0	Overvoltage only	Fault or warning
0110	ALARM0	Undervoltage or overvoltage	Fault only
0111	ALARM0	Undervoltage or overvoltage	Fault or warning
1000	ALARM1	None	—
1001	ALARM1	Sequencing fault	Fault only
1010	ALARM1	Undervoltage only	Fault only
1011	ALARM1	Undervoltage only	Fault or warning
1100	ALARM1	Overvoltage only	Fault only
1101	ALARM1	Overvoltage only	Fault or warning
1110	ALARM1	Undervoltage or overvoltage	Fault only
1111	ALARM1	Undervoltage or overvoltage	Fault or warning

Table 32. MFR_FAULT_RESPONSE Codes for GLOBAL Channels

RESPONSE[1:0]	FAULT RESPONSE
11	• Set the corresponding fault bit in the appropriate status register. • Log fault into MFR_NV_FAULT_LOG if NV_LOG = 1. • Continue operation.
10 (retry)	• Shut down the power supply by deasserting the PSENn output. All enabled GLOBAL power supplies are shut down in sequence as configured with TOFF_DELAY, or they are all shut DOWN immediately as configured by bit 0 in ON_OFF_CONFIG. Wait for the time configured in MFR_FAULT_RETRY and restart supplies in sequence as configured. • Assert the $\overline{\text{FAULT}}$ or $\overline{\text{FAULT2}}$ output until faults on all GLOBAL supplies clear and MFR_FAULT_RETRY expires. • Set the corresponding fault bit in the appropriate status register. • Log fault into MFR_NV_FAULT_LOG if NV_LOG = 1.
01 (latch off)	• Latch off the power supply by deasserting the PSENn output. All enabled GLOBAL power supplies are either shut down in sequence as configured with TOFF_DELAY, or they are shut down immediately as configured by bit 0 in ON_OFF_CONFIG. • Assert the $\overline{\text{FAULT}}$ or $\overline{\text{FAULT2}}$ outputs. • Set the corresponding fault bit in the appropriate status register. • Log fault into MFR_NV_FAULT_LOG if NV_LOG = 1.
00	• Set the corresponding fault bit in the appropriate status register. • Continue operation without any action.

Note: *$\overline{\text{ALERT}}$ is asserted, if enabled, when a new status bit is set. A status bit is latched when a particular fault occurs that causes a fault response.*

Table 33. MFR_FAULT_RESPONSE Codes for LOCAL Channels

RESPONSE [1:0]	FAULT RESPONSE
11	• Set the corresponding fault bit in the appropriate status register. • Log fault into MFR_NV_FAULT_LOG if NV_LOG = 1. • Continue operation.
10 (retry)	• Shut down the power supply by deasserting the PSENn output. All power supplies are shut down in sequence as configured with TOFF_DELAY or they are all shut down immediately as configured by bit 0 in ON_OFF_CONFIG. Wait for the time configured in MFR_FAULT_RETRY and restart the supply. • Set the corresponding fault bit in the appropriate status register. • Log fault into MFR_NV_FAULT_LOG if NV_LOG = 1.
01 (latchoff)	• Latch off the power supply by deasserting the PSENn output. All power supplies are shut down in sequence as configured with TOFF_DELAY or they are all shut down immediately as configured by bit 0 in ON_OFF_CONFIG. • Set the corresponding fault bit in the appropriate status register. • Log fault into MFR_NV_FAULT_LOG if NV_LOG = 1.
00	• Set the corresponding fault bit in the appropriate status register. • Continue operation without any action.

Note: *$\overline{\text{ALERT}}$ is asserted, if enabled, when a new status bit is set. A status bit is latched when a particular fault occurs that causes a fault response.*

Power-Supply Retry with Undervoltage Faults

If the power supply is configured to retry when an undervoltage fault occurs, the power supply is turned off for the fault retry time and then the power supply is turned back on by asserting the PSENn output. If the undervoltage fault still exists, the TON_MAX_FAULT_LIMIT is exceeded and the device takes fault action as configured.

MFR_FAULT_RETRY (DAh)

The MFR_FAULT_RETRY command sets the delay time between a power supply being shut down by a fault response and the power supply restarting. This command value is used for all fault responses that require delay retry. If global supplies are being sequenced off, the retry delay time does not begin until the last global channel is turned off. The 2 data bytes are in DIRECT format. When MFR_FAULT_RETRY = 0000h, the device restarts the power supply at the next available time period.

MFR_PG_DELAY (DBh)

The MFR_PG_DELAY command sets the delay time between when a power good is determined and the PG output is asserted. The 2 data bytes are in DIRECT format. When MFR_PG_DELAY = 0000h, the delay is disabled and the PG output is asserted immediately after power good is declared.

When the device is configured to operate in dual-sequencing mode (the DUAL_SEQ bit in MFR_MODE is set), the MFR_PG_DELAY command applies to both the primary and secondary sequences.

MFR_PG_DELAY is also used to set the external signal watchdog $\overline{WDO}$ active-low time. For the watchdog function, when MFR_PG_DELAY = 0000h, the $\overline{WDO}$ active-low time is set to 5ms.

MFR_NV_FAULT_LOG (DCh)

Each time the MFR_NV_FAULT_LOG command is executed, the device returns a block of 255 bytes containing one of the 15 nonvolatile fault logs. The MFR_NV_FAULT_LOG command must be executed 15 times to dump the complete nonvolatile fault log. If the returned fault log is all FFs (except bytes 0 and 1), this indicates that this fault log has not been written by the device. As the device is operating, it is reading the latest operating conditions for voltage and temperature and is updating the status registers. All this information is stored in on-board RAM. When a fault is detected (if so enabled in MFR_FAULT_RESPONSE), the device automatically logs this information to one of the 15 nonvolatile fault logs (Figure 8). After 15 faults have been written, bit 0 of STATUS_CML is set and the device can be configured (with the NV_LOG_OVERWRITE bit in MFR_NV_LOG_CONFIG) to either stop writing additional fault logs or to write over the oldest data. The host can clear the fault log by setting the CLEAR_NV_FAULT_LOG bit in MFR_NV_LOG_CONFIG. If a temperature sensor is disabled, the associated fault-log position returns 0000h.

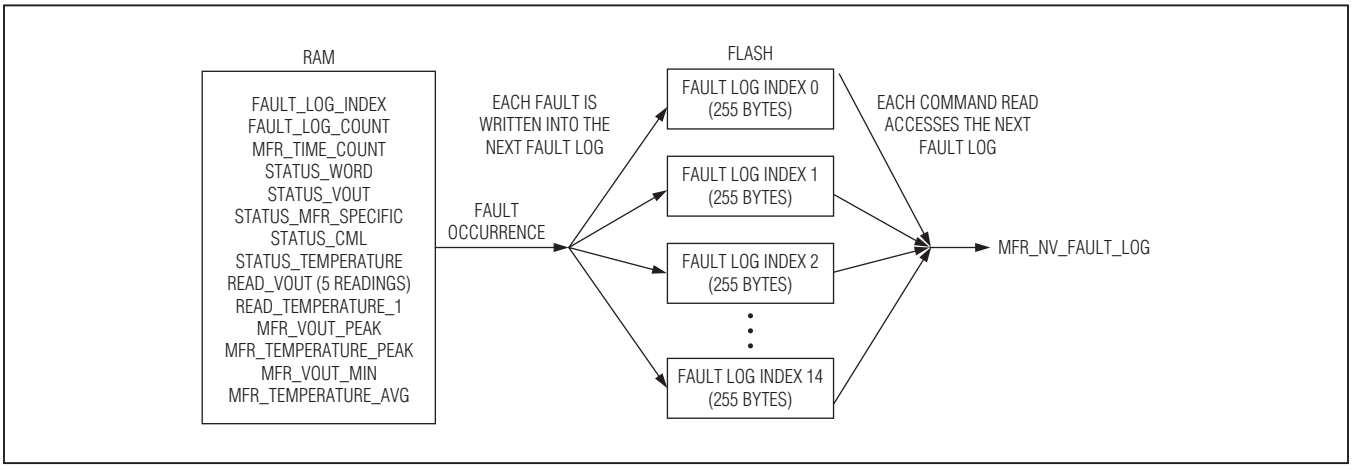


Figure 8. MFR_NV_FAULT_LOG

There is a FAULT_LOG_COUNT (16-bit counter) at the beginning of each fault log that indicates which fault log is the latest. This counter rolls over should more than 65,535 faults be logged. This counter is not cleared when the CLEAR_NV_FAULT_LOG bit in MFR_NV_LOG_CONFIG is toggled. The 255 bytes returned by the MFR_NV_FAULT_LOG command are described in Table 34.

If an error occurs while the device is attempting to write or clear the MFR_NV_FAULT_LOG, the device sets the CML bit in STATUS_WORD; no bits are set in STATUS_CML. $\overline{\text{ALERT}}$ is asserted (if enabled in MFR_MODE).

USER NOTE: V_{DD} must be above 2.9V for the device to clear or log data into MFR_NV_FAULT_LOG.

Table 34. MFR_NV_FAULT_LOG

BYTE	PARAMETER	BYTE	PARAMETER
0	00h/FAULT_LOG_INDEX	128	READ_VOUT T4 PAGE 7
2	FAULT_LOG_COUNT	130	READ_VOUT T0 PAGE 8
4	MFR_TIME_COUNT (LSW)	132	READ_VOUT T1 PAGE 8
6	MFR_TIME_COUNT (MSW)	134	READ_VOUT T2 PAGE 8
8	0000h	136	READ_VOUT T3 PAGE 8
10	STATUS_CML/00h	138	READ_VOUT T4 PAGE 8
12	STATUS_WORD	140	READ_VOUT T0 PAGE 9
14	STATUS_VOUT PAGEs 0/1	142	READ_VOUT T1 PAGE 9
16	STATUS_VOUT PAGEs 2/3	144	READ_VOUT T2 PAGE 9
18	STATUS_VOUT PAGEs 4/5	146	READ_VOUT T3 PAGE 9
20	STATUS_VOUT PAGEs 6/7	148	READ_VOUT T4 PAGE 9
22	STATUS_VOUT PAGEs 8/9	150	READ_VOUT T0 PAGE 10
24	STATUS_VOUT PAGEs 10/11	152	READ_VOUT T1 PAGE 10
26	STATUS_MFR_SPECIFIC PAGEs 0/1	154	READ_VOUT T2 PAGE 10
28	STATUS_MFR_SPECIFIC PAGEs 2/3	156	READ_VOUT T3 PAGE 10
30	STATUS_MFR_SPECIFIC PAGEs 4/5	158	READ_VOUT T4 PAGE 10
32	STATUS_MFR_SPECIFIC PAGEs 6/7	160	READ_VOUT T0 PAGE 11
34	STATUS_MFR_SPECIFIC PAGEs 8/9	162	READ_VOUT T1 PAGE 11
36	STATUS_MFR_SPECIFIC PAGEs 10/11	164	READ_VOUT T2 PAGE 11
38	STATUS_MFR_SPECIFIC PAGEs 255/00h	166	READ_VOUT T3 PAGE 11
40	STATUS_TEMPERATURE PAGEs 13/14	168	READ_VOUT T4 PAGE 11
42	STATUS_TEMPERATURE PAGEs 15/16	170	0000h
44	STATUS_TEMPERATURE PAGEs 17/00h	172	MFR_VOUT_PEAK PAGE 0
46	0000h	174	MFR_VOUT_PEAK PAGE 1
48	0000h	176	MFR_VOUT_PEAK PAGE 2
50	READ_VOUT T0 PAGE 0	178	MFR_VOUT_PEAK PAGE 3
52	READ_VOUT T1 PAGE 0	180	MFR_VOUT_PEAK PAGE 4
54	READ_VOUT T2 PAGE 0	182	MFR_VOUT_PEAK PAGE 5
56	READ_VOUT T3 PAGE 0	184	MFR_VOUT_PEAK PAGE 6
58	READ_VOUT T4 PAGE 0	186	MFR_VOUT_PEAK PAGE 7
60	READ_VOUT T0 PAGE 1	188	MFR_VOUT_PEAK PAGE 8
62	READ_VOUT T1 PAGE 1	190	MFR_VOUT_PEAK PAGE 9
64	READ_VOUT T2 PAGE 1	192	MFR_VOUT_PEAK PAGE 10
66	READ_VOUT T3 PAGE 1	194	MFR_VOUT_PEAK PAGE 11

Table 34. MFR_NV_FAULT_LOG (continued)

BYTE	PARAMETER	BYTE	PARAMETER
68	READ_VOUT T4 PAGE 1	196	MFR_VOUT_MIN PAGE 0
70	READ_VOUT T0 PAGE 2	198	MFR_VOUT_MIN PAGE 1
72	READ_VOUT T1 PAGE 2	200	MFR_VOUT_MIN PAGE 2
74	READ_VOUT T2 PAGE 2	202	MFR_VOUT_MIN PAGE 3
76	READ_VOUT T3 PAGE 2	204	MFR_VOUT_MIN PAGE 4
78	READ_VOUT T4 PAGE 2	206	MFR_VOUT_MIN PAGE 5
80	READ_VOUT T0 PAGE 3	208	MFR_VOUT_MIN PAGE 6
82	READ_VOUT T1 PAGE 3	210	MFR_VOUT_MIN PAGE 7
84	READ_VOUT T2 PAGE 3	212	MFR_VOUT_MIN PAGE 8
86	READ_VOUT T3 PAGE 3	214	MFR_VOUT_MIN PAGE 9
88	READ_VOUT T4 PAGE 3	216	MFR_VOUT_MIN PAGE 10
90	READ_VOUT T0 PAGE 4	218	MFR_VOUT_MIN PAGE 11
92	READ_VOUT T1 PAGE 4	220	0000h
94	READ_VOUT T2 PAGE 4	222	READ_TEMPERATURE_1 PAGE 13
96	READ_VOUT T3 PAGE 4	224	READ_TEMPERATURE_1 PAGE 14
98	READ_VOUT T4 PAGE 4	226	READ_TEMPERATURE_1 PAGE 15
100	READ_VOUT T0 PAGE 5	228	READ_TEMPERATURE_1 PAGE 16
102	READ_VOUT T1 PAGE 5	230	READ_TEMPERATURE_1 PAGE 17
104	READ_VOUT T2 PAGE 5	232	MFR_TEMPERATURE_PEAK PAGE 13
106	READ_VOUT T3 PAGE 5	234	MFR_TEMPERATURE_PEAK PAGE 14
108	READ_VOUT T4 PAGE 5	236	MFR_TEMPERATURE_PEAK PAGE 15
110	READ_VOUT T0 PAGE 6	238	MFR_TEMPERATURE_PEAK PAGE 16
112	READ_VOUT T1 PAGE 6	240	MFR_TEMPERATURE_PEAK PAGE 17
114	READ_VOUT T2 PAGE 6	242	MFR_TEMPERATURE_AVG PAGE 13
116	READ_VOUT T3 PAGE 6	244	MFR_TEMPERATURE_AVG PAGE 14
118	READ_VOUT T4 PAGE 6	246	MFR_TEMPERATURE_AVG PAGE 15
120	READ_VOUT T0 PAGE 7	248	MFR_TEMPERATURE_AVG PAGE 16
122	READ_VOUT T1 PAGE 7	250	MFR_TEMPERATURE_AVG PAGE 17
124	READ_VOUT T2 PAGE 7	252	0000h
126	READ_VOUT T3 PAGE 7	254	LOG_VALID

Note: *LOG_VALID is set to DDh if the fault log contains valid data. For READ_VOUT, T4 is the oldest reading and T0 is the newest reading.*

MFR_TIME_COUNT (DDh)

The MFR_TIME_COUNT command returns the current value of a real-time counter that increments every 5ms, 20ms, 80ms, or 160ms depending on the configuration of the NV_LOG_DEPTH bits in MFR_NV_LOG_CONFIG. This counter is useful in determining the time between multiple faults. The counter is a 32-bit value that rolls over. The count is reset to zero upon device power cycle or $\overline{RST}$ action, or a soft-reset. This count can also be reset to zero by writing a sequence of all zeros (00000000h), followed by all ones (FFFFFFFFh), followed by all zeros (00000000h) within 8ms.

MFR_MARGIN_CONFIG (DFh)

The MFR_MARGIN_CONFIG command configures the external DS4424 current DAC (if present) to margin the associated power supplies. The MFR_MARGIN_CONFIG command is described in Table 35.

For the power supplies connected to PSENn (PAGES 0–11), power-supply margining is implemented using the external DS4424 DAC outputs, according to Table 36. The device's closed loop controls the DAC output current setting to margin the power supply.

The device margins the power supplies when OPERATION is set to one of the margin states. Margining of the supplies does not begin until **ALL** power supplies have exceeded their programmed POWER_GOOD_ON levels. When this happens, the DAC output is enabled and margining is initiated. The device then averages four samples of V_{OUT} for a total time of 20ms. If the measured V_{OUT} and the target (set by either VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW) differ by more than 1%, the DAC setting is adjusted by one step that is 1/64 of full scale. The direction of the duty-cycle adjustment is determined by the SLOPE bit in MFR_MARGIN_CONFIG. All changes to the DAC setting are made after averaging four samples of V_{OUT} over a 20ms period.

Table 35. MFR_MARGIN_CONFIG

BIT	NAME	MEANING
15	SLOPE	DAC setting to resulting voltage relationship. 0 = Negative slope (DAC source current results in a lower voltage). 1 = Positive slope (DAC source current results in a higher voltage).
14	OPEN_LOOP	0 = Normal closed-loop margining. 1 = DAC setting constantly to the DAC_VALUE when margining invoked.
13:7	0	These bits always return a 0.
6:0	DAC_VALUE	When bit 14 is set, this 7-bit value is written to the external current DAC.

Table 36. Power-Supply Margining with DS4424 DAC outputs

PAGE	POWER SUPPLY	DS4424 DEVICE	DS4424 OUTPUT
0	PSEN0	Unit 0 I²C address 20h	OUT0
1	PSEN1		OUT1
2	PSEN2		OUT2
3	PSEN3		OUT3
4	PSEN4	Unit 1 I²C address 60h	OUT0
5	PSEN5		OUT1
6	PSEN6		OUT2
7	PSEN7		OUT3
8	PSEN8	Unit 2 I²C address A0h	OUT0
9	PSEN9		OUT1
10	PSEN10		OUT2
11	PSEN11		OUT3

Margining Faults

The device detects two possible margining faults. First, if the initial DAC step causes V_{OUT} to exceed the target value (either high or low depending on whether the device has been instructed to margin high or low, respectively), this creates a fault. Second, if the target value cannot be reached when the DAC reaches full scale, this also creates a fault. If either margining fault occurs, the device continues attempting to margin the power supply and does the following:

1) Sets the MARGIN bit in STATUS_WORD.
2) Sets the MARGIN_FAULT bit in STATUS_MFR_SPECIFIC (PAGES 0–11).
3) Notifies the host through $\overline{\text{ALERT}}$ assertion (if enabled in MFR_MODE).

If a communication error occurs between the device and the external DS4424, a fault occurs when the device attempts to set the DAC to full scale and the target margin value is not reached.

DAC Margining Component Selection

The external components needed to realize the margining circuitry for the current DAC outputs are shown in Figure 9 and described in the formulas below:

DAC “RFS” = (7.75)/(IFB x Margining Range)

where IFB is the feedback node current.

Example:

IFB = 500µA, margining range = ±15%

DAC “RFS” value = (7.75)/(500µA x 15%) = 103kΩ

Note: 40kΩ < RFS < 160kΩ

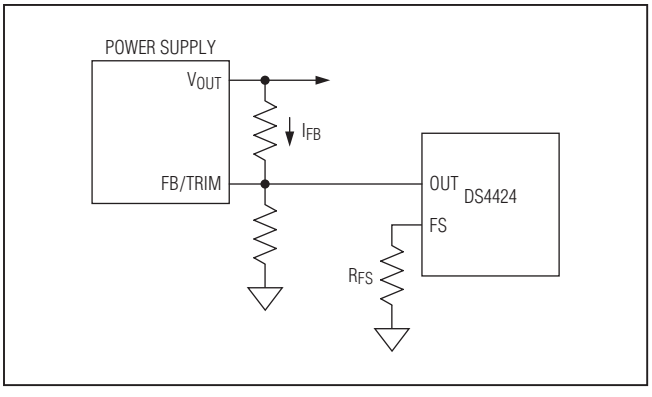


Figure 9. DAC Margining Circuit

Temperature-Sensor Operation

The device can monitor up to five different temperature sensors, four external sensors, plus its own internal temperature sensor. The external temperature sensors are all connected in parallel to the master I²C port (MSDA and MSCL pins). The device can support up to four DS75LV devices.

Each of the enabled temperature sensors are measured once per second. The internal temperature sensor is averaged four times to reduce the effect of noise. Each time the device attempts to read a temperature sensor, it checks for faults. For the internal temperature sensor, a fault is defined as reading greater than +130°C or less than -60°C. For the I²C temperature sensors, a fault is defined as a communication access failure. Temperature-sensor faults are reported by setting the temperature reading to 7FFFh. A temperature-sensor fault results in the setting of the TEMPERATURE bit in STATUS_WORD and $\overline{\text{ALERT}}$ is asserted (if enabled in MFR_MODE). No bits are set in STATUS_TEMPERATURE. On reset of the device, if it cannot initialize the external DS75LV device, the TEMPERATURE bit in STATUS_WORD is set and $\overline{\text{ALERT}}$ is asserted (if enabled in MFR_MODE), but the device does not attempt to reinitialize the DS75LV until 8000h is written to MFR_TEMP_SENSOR_CONFIG. Reading disabled temperature sensors returns a fixed value of 0000h.

Up to four DS75LV digital temperature sensors can be controlled by the device. The A0–A2 pins on the DS75LV should be configured as shown in Table 37. The thermostat function on the DS75LV is not used and hence the O.S. output should be left open circuit.

Table 37. DS75LV Address Pin Configuration

PAGE	MAX34460 TEMP SENSOR	DS75LV ADDRESS PIN CONFIGURATION		
		A2	A1	A0
13	MAX34460 internal	—	—	—
14	DS75LV (address 90h)	0	0	0
15	DS75LV (address 92h)	0	0	1
16	DS75LV (address 94h)	0	1	0
17	DS75LV (address 96h)	0	1	1

Table 38. MFR_TEMP_SENSOR_CONFIG

BIT	NAME	MEANING
15	ENABLE	0 = Temperature sensor disabled. 1 = Temperature sensor enabled.
14:0	0	These bits always return a 0.

MFR_TEMP_SENSOR_CONFIG (F0h)

The MFR_TEMP_SENSOR_CONFIG command is used to configure the temperature sensors. The MFR_TEMP_SENSOR_CONFIG command is described in Table 38.

MFR_GPO_CONFIG (FBh)

The MFR_GPO_CONFIG command is used to configure the individual GPO outputs. The MFR_GPO_CONFIG command is described in Table 39. The GPO pins can be found in Table 7.

Table 39. MFR_GPO_CONFIG

BIT	NAME	MEANING
15	GPO7_OVERRIDE	0 = Pin 41 acts as WDI. 1 = Force GPO7/pin 41 to an open-drain output.
14	GPO6_OVERRIDE	0 = Pin 40 acts as $\overline{WDO}$. 1 = Force GPO6/pin 40 to an open-drain output.
13	GPO5_OVERRIDE	0 = Pin 28 acts as PG2. 1 = Force GPO5/pin 28 to an open-drain output.*
12	GPO4_OVERRIDE	0 = Pin 29 acts as CONTROL2. 1 = Force GPO4/pin 29 to an open-drain output.*
11	GPO3_OVERRIDE	0 = Pin 17 acts as $\overline{FAULT2}$. 1 = Force GPO3/pin 17 to an open-drain output.*
10	GPO2_OVERRIDE	0 = Pin 12 acts as $\overline{ALARMCLR}$. 1 = Force GPO2/pin 12 to an open-drain output.
9	GPO1_OVERRIDE	0 = Pin 25 acts as $\overline{ALARM1}$. 1 = Force GPO1/pin 25 to an open-drain output.
8	GPO0_OVERRIDE	0 = Pin 24 acts as $\overline{ALARM0}$. 1 = Force GPO0/pin 24 to an open-drain output.
7	GPO7_HI_LO	0 = Force GPO7/pin 41 low if bit 15 is set. 1 = Force GPO7/pin 41 high impedance if bit 15 is set.
6	GPO6_HI_LO	0 = Force GPO6/pin 40 low if bit 14 is set. 1 = Force GPO6/pin 40 high impedance if bit 14 is set.
5	GPO5_HI_LO	0 = Force GPO5/pin 28 low if bit 13 is set. 1 = Force GPO5/pin 28 high impedance if bit 13 is set.
4	GPO4_HI_LO	0 = Force GPO4/pin 29 low if bit 12 is set. 1 = Force GPO4/pin 29 high impedance if bit 12 is set.
3	GPO3_HI_LO	0 = Force GPO3/pin 17 low if bit 11 is set. 1 = Force GPO3/pin 17 high impedance if bit 11 is set.
2	GPO2_HI_LO	0 = Force GPO2/pin 12 low if bit 10 is set. 1 = Force GPO2/pin 12 high impedance if bit 10 is set.
1	GPO1_HI_LO	0 = Force GPO1/pin 25 low if bit 9 is set. 1 = Force GPO1/pin 25 high impedance if bit 9 is set.
0	GPO0_HI_LO	0 = Force GPO0/pin 24 low if bit 8 is set. 1 = Force GPO0/pin 24 high impedance if bit 8 is set.

**In dual-sequencing mode, CONTROL2, PG2, and $\overline{FAULT2}$ cannot be configured as GPOs.*

MFR_WATCHDOG_CONFIG (FDh)

The MFR_WATCHDOG_CONFIG command is used to configure the external watchdog function. The MFR_WATCHDOG_CONFIG command is described in Table 40.

Applications Information

V_{DD}, V_{DDA}, and REG18 Decoupling

To achieve the best results when using the device, decouple V_{DD} and V_{DDA} power inputs each with a 0.1µF capacitor. If possible, use a high-quality, ceramic, surface-mount capacitor. Surface-mount components minimize lead inductance, which improves performance; ceramic capacitors tend to have adequate high-frequency response for decoupling applications. Decouple the REG18 regulator output using 1µF and 10nF capacitors with a maximum ESR of 500mΩ.

Open-Drain Pins

MSDA, MSCL, SCL, SDA, $\overline{FAULT}$, and $\overline{ALERT}$ are open-drain pins and require external pullup resistors connected to V_{DD} to realize high logic levels.

PSEN0–PSEN11 can be user-configured as either CMOS push-pull or open-drain outputs. When configured as open-drain (see MFR_PSEN_CONFIG), external pullup resistors connected to V_{DD} are required to realize high logic levels.

Keep-Alive Circuit

In systems where the power to the device may be not always be present, a keep-alive circuit consisting of a Schottky diode and a bulk capacitor can be added to allow the device time to orderly shut down the power supplies it is controlling before power is lost.

Table 40. MFR_WATCHDOG_CONFIG

BIT	NAME	MEANING
15:13	WD_STARTUP[2:0]	These bits define the watchdog startup time. 000 1s 100 16s 001 2s 101 32s 010 4s 110 64s 011 8s 111 128s
12	0	This bit always returns a 0.
11:8	WD_TIMEOUT[3:0]	These bits define the watchdog timeout time. 0000 5ms 1000 1s 0001 10ms 1001 2s 0010 20ms 1010 4s 0011 40ms 1011 8s 0100 80ms 1100 16s 0101 160ms 1101 32s 0110 320ms 1110 64s 0111 640ms 1111 128s
7:4	0	These bits always return a 0 when read.
3	WD_WDO_MR	0 = $\overline{WDO}$ pin is watchdog output only. 1 = $\overline{WDO}$ pin is watchdog output and manual-reset input.
2	WD_TOGGLE	When this bit is set to a 1, it resets the watchdog the same as a rising edge on WDI does. This bit always returns a 0 when read.
1	WD_MODE	0 = Independent mode. 1 = Dependent mode.*
0	WD_ENABLE	0 = Watchdog disabled ($\overline{WDO}$ is forced high impedance). 1 = Watchdog enabled.

**If dual sequencing is enabled, only the primary group is used to time the start of the watchdog.*

Configuration Port

Some applications require the ability to configure the device when it has been mounted on a PCB. In such applications, a 3- or 4-wire header can be added to allow access to the slave I²C pins.

Resistor-Dividers and Source Impedance for RSn Inputs

The maximum full-scale voltage on the ADC inputs is 2.048V (nominal). A resistor-divider must be used to measure voltages greater than 1.8V. The maximum source impedance to the RSn inputs is determined by the ADC_TIME bits in MFR_MODE. See the *Recommended Operating Conditions* table for more information. In applications where voltages up to 2V can be applied to the RSn inputs when V_{DD} or V_{DDA} is grounded, a series resistance of 100Ω is recommended to protect the device by limiting power dissipation.

Current Measurement on RSn Inputs

The RSn inputs normally measure voltages, but with the addition of an external current-sense amplifier the device can also be configured to measure current. Any of the RSn inputs can be configured to measure current. On channels that measure current, the sequencing for that channel should be disabled by setting TON_MAX_FAULT_LIMIT = 8000h to FFFFh. On these channels, the associated PSENn output is available to be configured as a GPO. Also, for these channels, POWER_GOOD_ON should be set to 0000h to force power-good assertion since this channel is not measuring voltage (Figure 10).

The current-sense amplifier must have a source impedance of less than the value as constrained by the selection of the ADC_TIME bits in MFR_MODE and the output from the amplifier must not exceed the maximum input-voltage limits of the device. The 100Ω series resistor is required to protect the device if the current-sense amplifier can be active when the system manager is powered off.

The VOUT_SCALE_MONITOR command can be used to properly scale the external sense element and current-sense amplifier gain so that the READ_VOUT command reports current instead of voltage. Normally VOUT_SCALE_MONITOR scales voltage from 0 to 32.767V in 1mV steps. For channels used to measure current instead of voltage, the VOUT_SCALE_MONITOR command can be configured to report current from 0A to 32.767A in 1mA steps by using the following formula. Table 41 provides some examples. Note that VOUT_SCALE_MONITOR cannot exceed a ratio of 1. System designs should avoid RG combinations with a value greater than 1.

VOUT_SCALE_MONITOR = R x G x 32,767

Exposed Pad Grounding

The device uses the exposed pad of the TQFN package as the common ground (V_{SS}) for the entire device. The exposed pad must be connected to the local ground plane.

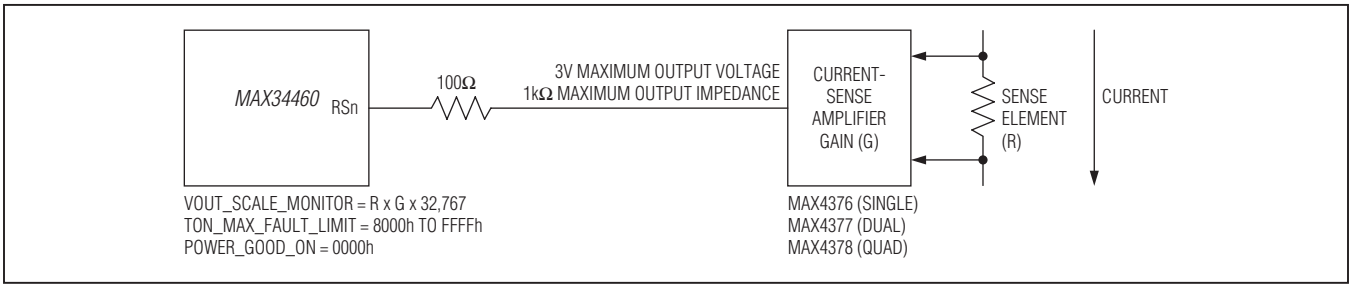


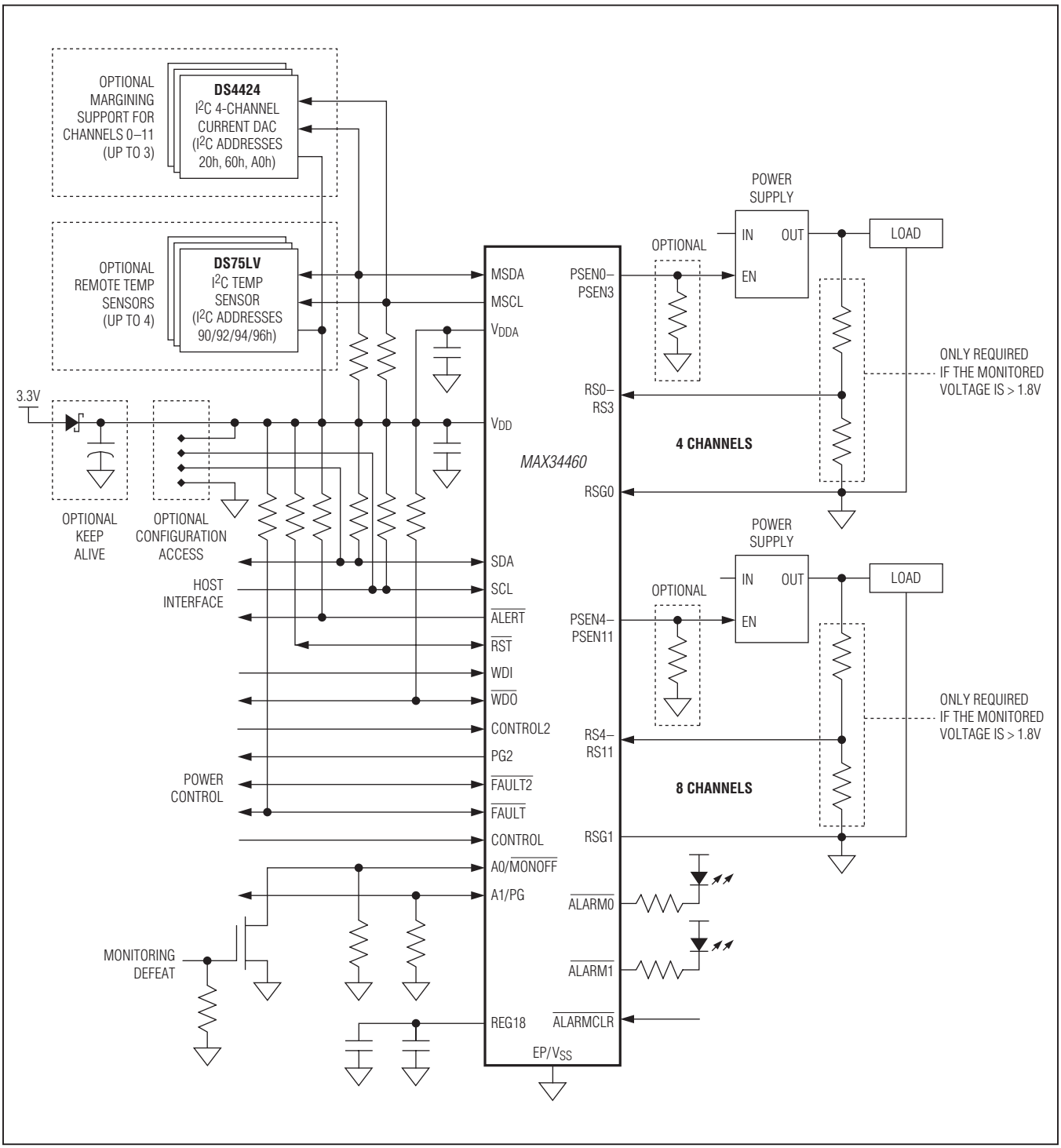
Figure 10. Current-Measuring Circuit

Table 41. Scale Current-Gain Example

R SENSE ELEMENT (mΩ)	G AMPLIFIER GAIN (V/V)	V/A RATIO R x G (Ω)	VOUT_SCALE_MONITOR VALUE	
			Dec	Hex
1	100	0.1	3276	0CCC
2	100	0.2	6553	1999
2	50	0.1	3276	0CCC
4	20	0.08	2621	0A3D
0.5	100	0.05	1638	0666

PMBus 12-Channel Voltage Monitor and Sequencer

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX34460ETM+	-40°C to +85°C	48 TQFN-EP*
MAX34460ETM+T	-40°C to +85°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4866+2	21-0141	90-0007

PMBus 12-Channel Voltage Monitor and Sequencer

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/12	Initial release	—

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