Si510/511

CRYSTAL OSCILLATOR (XO) 100 kHz TO 250 MHz

Features

- Supports any frequency from 100 kHz to 250 MHz
- Low jitter operation
- 2 to 4 week lead times
- Total stability includes 10-year aging
- Comprehensive production test coverage includes crystal ESR and DLD
- On-chip LDO regulator for power supply noise filtering
- 3.3, 2.5, or 1.8 V operation
- Differential (LVPECL, LVDS, HCSL) or CMOS output options
- Optional integrated 1:2 CMOS fanout buffer
- Runt suppression on OE and power on
- Industry standard 5 x 7 and 3.2 x 5 mm packages
- Pb-free, RoHS compliant
- –40 to 85 °C operation

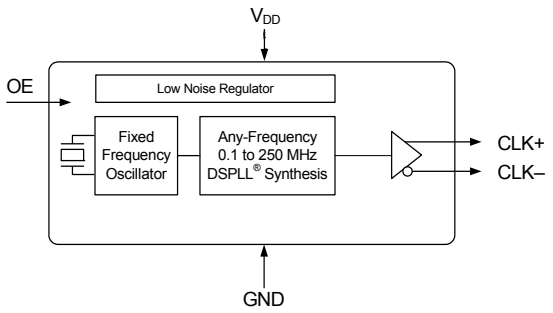
Applications

- SONET/SDH/OTN
- Gigabit Ethernet
- Fibre Channel/SAS/SATA
- PCI Express
- 3G-SDI/HD-SDI/SDI
- Telecom
- Switches/routers
- FPGA/ASIC clock generation

Description

The Si510/511 XO utilizes Silicon Laboratories' advanced DSPLL technology to provide any frequency from 100 kHz to 250 MHz. Unlike a traditional XO where a different crystal is required for each output frequency, the Si510/511 uses one fixed crystal and Silicon Labs' proprietary DSPLL synthesizer to generate any frequency across this range. This IC-based approach allows the crystal resonator to provide enhanced reliability, improved mechanical robustness, and excellent stability. In addition, this solution provides superior supply noise rejection, simplifying low jitter clock generation in noisy environments. Crystal ESR and DLD are individually production-tested to guarantee performance and enhance reliability. The Si510/511 is factory-configurable for a wide variety of user specifications, including frequency, supply voltage, output format, output enable polarity, and stability. Specific configurations are factory-programmed at time of shipment, eliminating long lead times and non-recurring engineering charges associated with custom frequency oscillators.

Functional Block Diagram



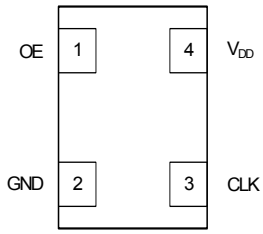


Ordering Information:

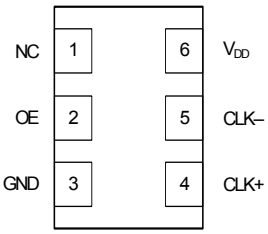
See page 14.

Pin Assignments:

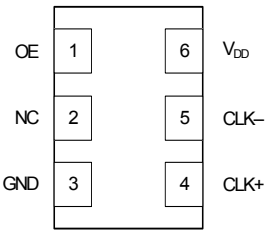
See page 12.



Si510 (CMOS)



Si510(LVDS/LVPECL/HCSL/ Dual CMOS)



Si511(LVDS/LVPECL/HCSL/ Dual CMOS)

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1. Electrical Specifications

Table 1. Operating Specifications

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	V
		1.8 V option	1.71	1.8	1.89	V
Supply Current	I_{DD}	CMOS, 100 MHz, single-ended	—	21	26	mA
		LVDS (output enabled)	—	19	23	mA
		LVPECL (output enabled)	—	39	43	mA
		HCSL (output enabled)	—	41	44	mA
		Tristate (output disabled)	—	—	18	mA
OE "1" Setting	V_{IH}	See Note	0.80 x V_{DD}	—	—	V
OE "0" Setting	V_{IL}	See Note	—	—	0.20 x V_{DD}	V
OE Internal Pull-Up/Pull-Down Resistor*	R_I		—	45	—	kΩ
Operating Temperature	T_A		–40	—	85	°C

***Note:** Active high and active low polarity OE options available. Active high option includes an internal pull-up. Active low option includes an internal pull-down. See ordering information on page 14.

Table 2. Output Clock Frequency Characteristics

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Frequency	F_O	CMOS, Dual CMOS	0.1	—	212.5	MHz
	F_O	LVDS/LVPECL/HCSL	0.1	—	250	MHz
Total Stability*		Frequency Stability Grade C	–30	—	+30	ppm
		Frequency Stability Grade B	–50	—	+50	ppm
		Frequency Stability Grade A	–100	—	+100	ppm
Temperature Stability		Frequency Stability Grade C	–20	—	+20	ppm
		Frequency Stability Grade B	–25	—	+25	ppm
		Frequency Stability Grade A	–50	—	+50	ppm
Startup Time	T_{SU}	Minimum V_{DD} until output frequency (F_O) within specification	—	—	10	ms
Disable Time	T_D	$F_O \geq 10$ MHz	—	—	5	µs
		$F_O < 10$ MHz	—	—	40	µs
Enable Time	T_E	$F_O \geq 10$ MHz	—	—	20	µs
		$F_O < 10$ MHz	—	—	60	µs

***Note:** Total stability includes initial accuracy, operating temperature, supply voltage change, load change, shock and vibration (not under operation), and 10 years aging at 40 °C.

Table 3. Output Clock Levels and Symmetry

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CMOS Output Logic High	V_{OH}		0.85 x V_{DD}	—	—	V
CMOS Output Logic Low	V_{OL}		—	—	0.15 x V_{DD}	V
CMOS Output Logic High Drive	I_{OH}	3.3 V	–8	—	—	mA
		2.5 V	–6	—	—	mA
		1.8 V	–4	—	—	mA
CMOS Output Logic Low Drive	I_{OL}	3.3 V	8	—	—	mA
		2.5 V	6	—	—	mA
		1.8 V	4	—	—	mA
CMOS Output Rise/Fall Time (20 to 80% V_{DD})	T_R/T_F	0.1 to 212.5 MHz, C_L = 15 pF	—	0.8	1.2	ns
		0.1 to 212.5 MHz, C_L = no load	—	0.6	0.9	ns
LVPECL/HCSL Output Rise/Fall Time (20 to 80% VDD)	T_R/T_F		—	—	565	ps
LVDS Output Rise/Fall Time (20 to 80% VDD)	T_R/T_F		—	—	800	ps
LVPECL Output Common Mode	V_{OC}	50 Ω to V_{DD} – 2 V, single-ended	—	V_{DD} – 1.4 V	—	V
LVPECL Output Swing	V_O	50 Ω to V_{DD} – 2 V, single-ended	0.55	0.8	0.90	V_{PPSE}
LVDS Output Common Mode	V_{OC}	100 Ω line-line V_{DD} = 3.3/2.5 V	1.13	1.23	1.33	V
		100 Ω line-line, V_{DD} = 1.8 V	0.83	0.92	1.00	V
LVDS Output Swing	V_O	Single-ended, 100 Ω differential termination	0.25	0.35	0.45	V_{PPSE}
HCSL Output Common Mode	V_{OC}	50 Ω to ground	0.35	0.38	0.42	V
HCSL Output Swing	V_O	Single-ended	0.58	0.73	0.85	V_{PPSE}
Duty Cycle	DC	All formats	48	50	52	%

Table 4. Output Clock Jitter and Phase Noise (LVPECL)

V_{DD} = 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C; Output Format = LVPECL

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Period Jitter (RMS)	JPRMS	10k samples[1]	—	—	1.3	ps
Period Jitter (Pk-Pk)	JPPKPK	10k samples[1]	—	—	11	ps
Phase Jitter (RMS)	φJ	1.875 MHz to 20 MHz integration bandwidth[2] (brickwall)	—	0.31	0.5	ps
		12 kHz to 20 MHz integration bandwidth[2] (brickwall)	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	φN	100 Hz	—	–86	—	dBc/Hz
		1 kHz	—	–109	—	dBc/Hz
		10 kHz	—	–116	—	dBc/Hz
		100 kHz	—	–123	—	dBc/Hz
		1 MHz	—	–136	—	dBc/Hz
Additive RMS Jitter Due to External Power Supply Noise[3]	JPSR	10 kHz sinusoidal noise	—	3.0	—	ps
		100 kHz sinusoidal noise	—	3.5	—	ps
		500 kHz sinusoidal noise	—	3.5	—	ps
		1 MHz sinusoidal noise	—	3.5	—	ps
Spurious	SPR	LVPECL output, 156.25 MHz, offset>10 kHz	—	–75	—	dBc

Notes:
1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5, 250 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 and 250 MHz.
3. 156.25 MHz. Increase in jitter on output clock due to sinewave noise added to VDD (2.5/3.3 V = 100 mVPP).

Table 5. Output Clock Jitter and Phase Noise (LVDS)

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C; Output Format = LVDS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Period Jitter (RMS)	JPRMS	10k samples[1]	—	—	2.1	ps
Period Jitter (Pk-Pk)	JPPKPK	10k samples[1]	—	—	18	ps
Phase Jitter (RMS)	φJ	1.875 MHz to 20 MHz integration bandwidth[2] (brickwall)	—	0.25	0.55	ps
		12 kHz to 20 MHz integration bandwidth[2] (brickwall)	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	φN	100 Hz	—	–86	—	dBc/Hz
		1 kHz	—	–109	—	dBc/Hz
		10 kHz	—	–116	—	dBc/Hz
		100 kHz	—	–123	—	dBc/Hz
		1 MHz	—	–136	—	dBc/Hz
Spurious	SPR	LVPECL output, 156.25 MHz, offset>10 kHz	—	–75	—	dBc

Notes:
1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5, 250 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 and 250 MHz.

Table 6. Output Clock Jitter and Phase Noise (HCSL)

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C; Output Format = HCSL

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Period Jitter (RMS)	JPRMS	10k samples*	—	—	1.2	ps
Period Jitter (Pk-Pk)	JPPKPK	10k samples*	—	—	11	ps
Phase Jitter (RMS)	φJ	1.875 MHz to 20 MHz integration bandwidth* (brickwall)	—	0.25	0.30	ps
		12 kHz to 20 MHz integration bandwidth* (brickwall)	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	φN	100 Hz	—	–90	—	dBc/Hz
		1 kHz	—	–112	—	dBc/Hz
		10 kHz	—	–120	—	dBc/Hz
		100 kHz	—	–127	—	dBc/Hz
		1 MHz	—	–140	—	dBc/Hz
Spurious	SPR	LVPECL output, 156.25 MHz, offset>10 kHz	—	–75	—	dBc

***Note:** Applies to an output frequency of 100 MHz.

Table 7. Output Clock Jitter and Phase Noise (CMOS, Dual CMOS)

V_{DD} = 1.8 V ±5%, 2.5 or 3.3 V ±10%, T_A = –40 to +85 °C; Output Format = CMOS, Dual CMOS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase Jitter (RMS)	φJ	1.875 MHz to 20 MHz integration bandwidth[2] (brickwall)	—	0.25	0.35	ps
		12 kHz to 20 MHz integration bandwidth[2] (brickwall)	—	0.8	1.0	ps
Phase Noise, 156.25 MHz	φN	100 Hz	—	–86	—	dBc/Hz
		1 kHz	—	–108	—	dBc/Hz
		10 kHz	—	–115	—	dBc/Hz
		100 kHz	—	–123	—	dBc/Hz
		1 MHz	—	–136	—	dBc/Hz
Spurious	SPR	LVPECL output, 156.25 MHz, offset>10 kHz	—	–75	—	dBc

Notes:
1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 MHz.

Table 8. Environmental Compliance and Package Information

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold over Nickel

Table 9. Thermal Characteristics

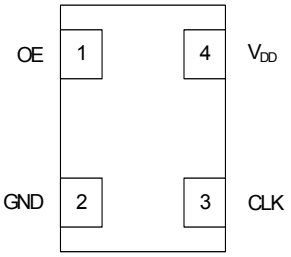
Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air	110	°C/W

Table 10. Absolute Maximum Ratings[1]

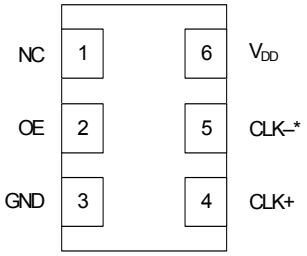
Parameter	Symbol	Rating	Unit
Maximum Operating Temperature	T_{AMAX}	85	°C
Storage Temperature	T_S	–55 to +125	°C
Supply Voltage	V_{DD}	–0.5 to +3.8	V
Input Voltage (any input pin)	V_I	–0.5 to V_{DD} + 0.3	V
ESD Sensitivity (HBM, per JESD22-A114)	HBM	2	kV
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[2]	T_P	20–40	sec

Notes:
1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

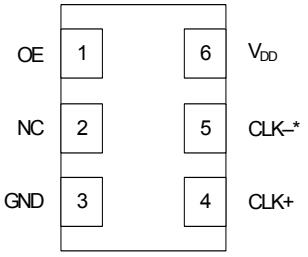
2. Pin Descriptions



Si510 (CMOS)



Si510 (LVDS/LVPECL/HCSL/Dual CMOS*)



Si511 (LVDS/LVPECL/HCSL/DualCMOS)*

*Supports integrated 1:2 CMOS buffer. See ordering information and section 2.1“Dual CMOS Buffer”.

Table 11. Si510 Pin Descriptions (CMOS)

Pin	Name	CMOS Function
1	OE	Output Enable. Includes internal pull-up for OE active high. Includes internal pull-down for OE active low. See ordering information.
2	GND	Electrical and Case Ground.
3	CLK	Clock Output.
4	V_{DD}	Power Supply Voltage.

Table 12. Si510 Pin Descriptions (LVPECL/LVDS/HCSL, Dual CMOS, OE Pin 2)

Pin	Name	LVPECL/LVDS/HCSL Function
1	NC	No connect. Make no external connection to this pin.
2	OE	Output Enable. Includes internal pull-up for OE active high. Includes internal pull-down for OE active low. See ordering information.
3	GND	Electrical and Case Ground.
4	CLK+	Clock Output.
5	CLK–	Complementary Clock Output.
6	V_{DD}	Power Supply Voltage.

Table 13. Si511 Pin Descriptions (LVPECL/LVDS/HCSL, Dual CMOS, OE Pin 1)

Pin	Name	LVPECL/LVDS/HCSL Function
1	OE	Output Enable. Includes internal pull-up for OE active high. Includes internal pull-down for OE active low. See ordering information.
2	NC	No connect. Make no external connection to this pin.
3	GND	Electrical and Case Ground.
4	CLK+	Clock Output.
5	CLK–	Complementary Clock Output.
6	V_{DD}	Power Supply Voltage.

2.1. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase output signals. This feature enables replacement of multiple XOs with a single Si510/11 device.

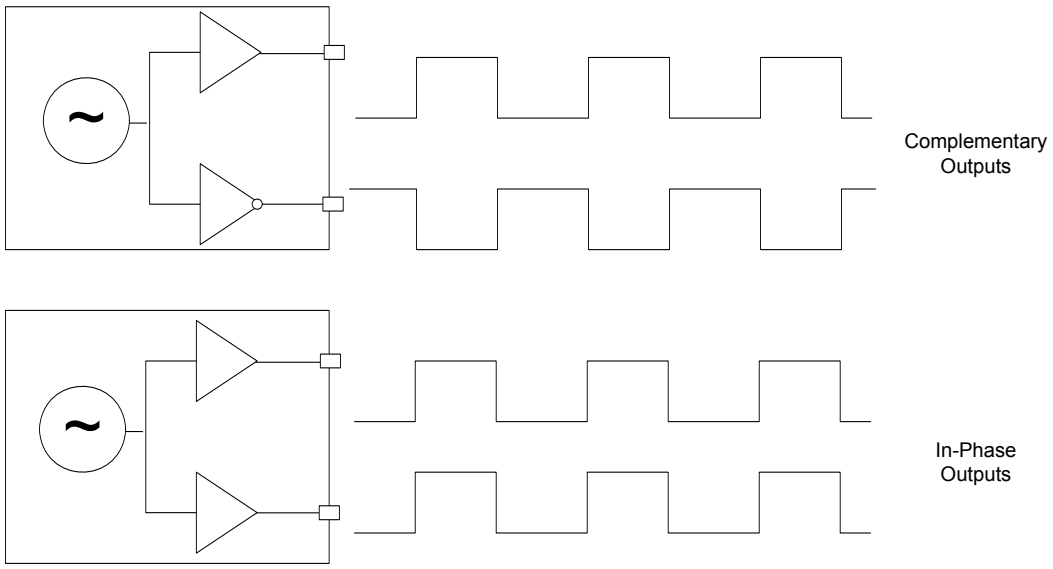


Figure 1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs

3. Ordering Information

The Si510/511 supports a wide variety of options including frequency, stability, output format, and V_{DD}. Specific device configurations are programmed into the Si510/511 at time of shipment. Configurations can be specified using the Part Number Configuration chart below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. Refer to www.silabs.com/VCXOpartnumber to access this tool. The Si510/511 XO series is supplied in industry-standard, RoHS compliant, lead-free, 3.2 x 5.0 mm and 5 x 7 mm packages. Tape and reel packaging is an ordering option.

Series	Output Format	OE Pin	Package
510	CMOS	OE on pin 1	4-pin
510	LVPECL, LVDS, HCSL, Dual CMOS	OE on pin 2	6-pin
511	LVPECL, LVDS, HCSL, Dual CMOS	OE on pin 1	6-pin

A = Revision: A
G = Temp Range: -40°C to 85°C
R = Tape & Reel; Blank = Trays.



1st Option Code: Output Format

	VDD	Output Format
A	3.3V	LVPECL
B	3.3V	LVDS
C	3.3V	CMOS
D	3.3V	HCSL
E	2.5V	LVPECL
F	2.5V	LVDS
G	2.5V	CMOS
H	2.5V	HCSL
J	1.8V	LVDS
K	1.8V	CMOS
L	1.8V	HCSL
M	3.3V	Dual CMOS (In-phase)
N	3.3V	Dual CMOS (Complementary)
P	2.5V	Dual CMOS (In-phase)
Q	2.5V	Dual CMOS (Complementary)
R	1.8V	Dual CMOS (In-phase)
S	1.8V	Dual CMOS (Complementary)

2nd Option Code: Frequency Stability

	Total	Temperature
A	±100ppm	±50ppm
B	±50ppm	±25ppm
C	±30ppm	±20ppm

3rd Option Code: Output Enable

	OE Polarity
A	OE Active High
B	OE Active Low

Package Option

	Dimensions
A	5 x 7 mm
B	3.2 x 5 mm

Frequency Code

Frequency	Description
Mxxxxxx	f_{OUT} < 1 MHz
xMxxxxx	1 MHz ≤ f_{OUT} < 10 MHz
xxMxxxx	10 MHz ≤ f_{OUT} < 100 MHz
xxxMxxx	100 MHz ≤ f_{OUT} < 250 MHz
xxxxxx	Code if frequency requires >6 digit resolution

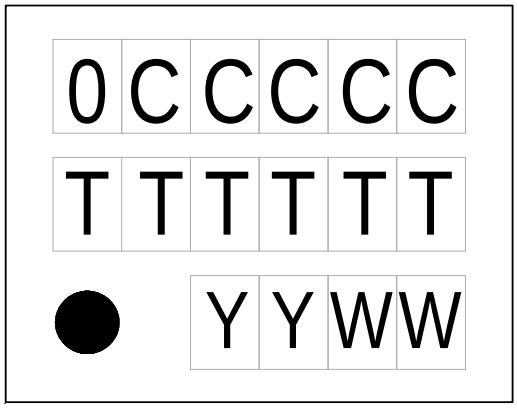
Figure 2. Part Number Syntax

Example orderable part number: 510ECB156M250AAG supports 2.5 V LVPECL, ±30 ppm total stability, OE active low in 5 x 7 mm package across –40°C to 85°C temperature range. The output frequency is 156.25 MHz.

Note: CMOS and Dual CMOS maximum frequency is 212.5 MHz.

4. Si510/511 Mark Specification

Figure 3 illustrates the mark specification for the Si510/511. Use the part number configuration utility located at: www.silabs.com/VCXOpartnumber to cross-reference the mark code to a specific device configuration.



0 = Si510, 1 = Si511
CCCCC = mark code
TTTTTT = assembly manufacturing code
YY = year
WW = work week

Figure 3. Top Mark

5. Package Outline Diagram: 5 x 7 mm, 4-pin

Figure 4 illustrates the package details for the 5 x 7 mm Si510/511. Table 14 lists the values for the dimensions shown in the illustration.

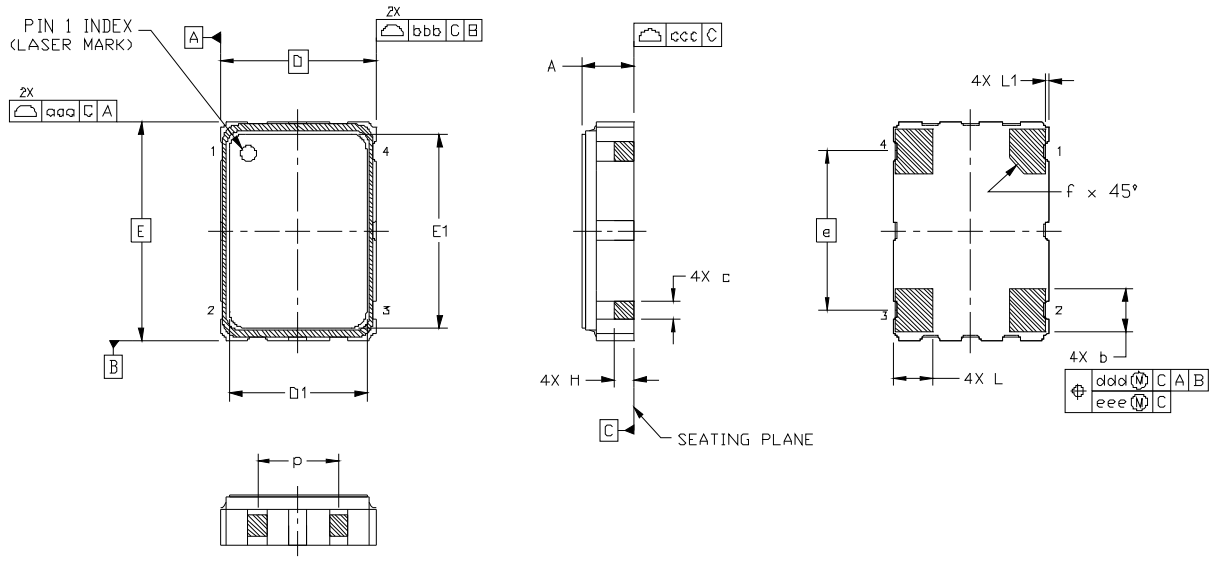


Figure 4. Si510/511 Outline Diagram

Table 14. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
c	0.50	0.60	0.70
D		5.00 BSC	
D1	4.30	4.40	4.50
e		5.08 BSC	
f		0.50 TYP	
E		7.00 BSC	
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	0.05	0.10	0.15
p	2.50	2.60	2.70
aaa		0.15	
bbb		0.15	
ccc		0.10	
ddd		0.10	
eee		0.05	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

6. PCB Land Pattern: 5 x 7 mm, 4-pin

Figure 5 illustrates the 5 x 7 mm PCB land pattern for the 5 x 7 mm Si510/511. Table 15 lists the values for the dimensions shown in the illustration.

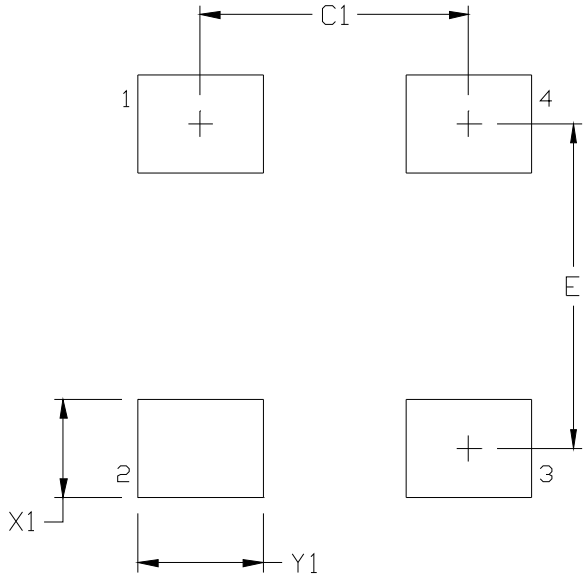


Figure 5. Si510/511 PCB Land Pattern

Table 15. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	4.20
E	5.08
X1	1.55
Y1	1.95

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

7. Package Outline Diagram: 5 x 7 mm, 6-pin

Figure 6 illustrates the package details for the Si510/511. Table 16 lists the values for the dimensions shown in the illustration.

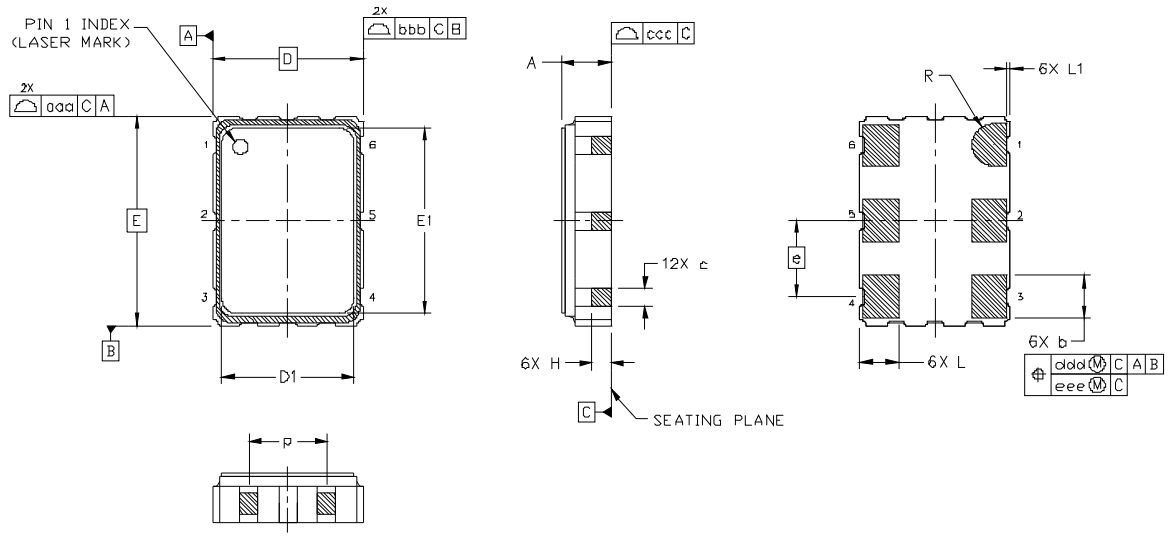


Figure 6. Si510/511 Outline Diagram

Table 16. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
c	0.50	0.60	0.70
D		5.00 BSC	
D1	4.30	4.40	4.50
e		2.54 BSC	
E		7.00 BSC	
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	0.05	0.10	0.15
p	1.80	—	2.60
R		0.70 REF	
aaa		0.15	
bbb		0.15	
ccc		0.10	
ddd		0.10	
eee		0.05	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

8. PCB Land Pattern: 5 x 7 mm, 6-pin

Figure 7 illustrates the 5 x 7 mm PCB land pattern for the Si510/511. Table 17 lists the values for the dimensions shown in the illustration.

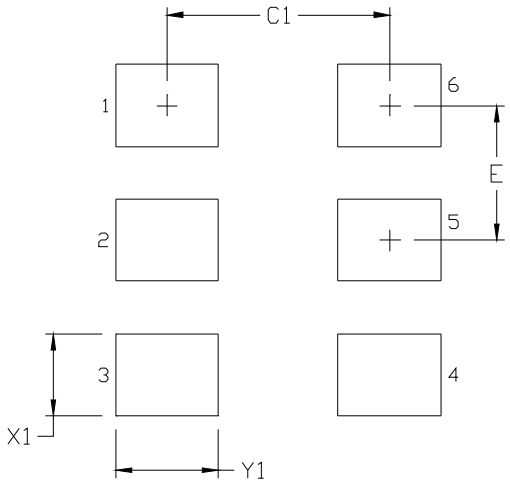


Figure 7. Si510/511 PCB Land Pattern

Table 17. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	4.20
E	2.54
X1	1.55
Y1	1.95

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Package Outline Diagram: 3.2 x 5 mm, 4-pin

Figure 8 illustrates the package details for the 3.2 x 5 mm Si510/511. Table 18 lists the values for the dimensions shown in the illustration.

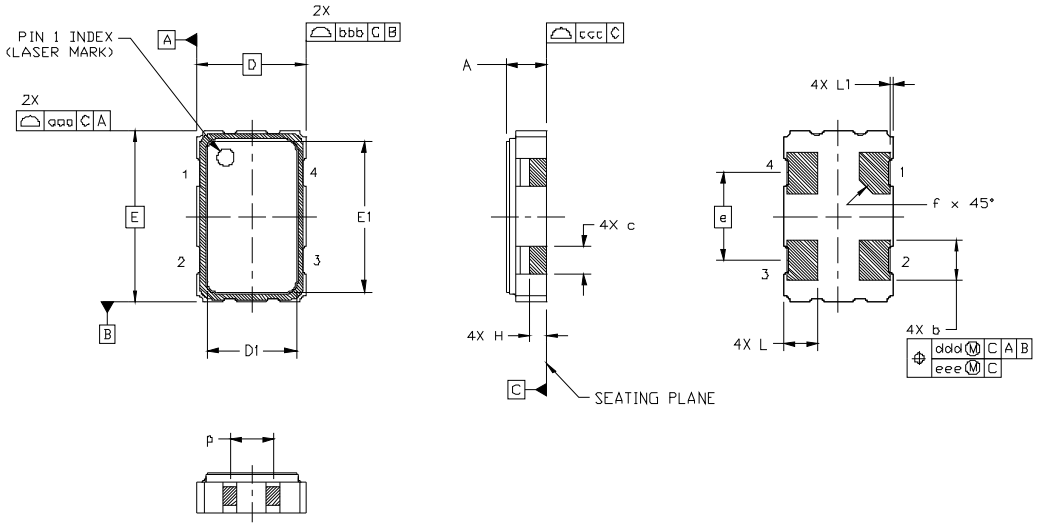


Figure 8. Si510/511 Outline Diagram

Table 18. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.06	1.17	1.28
b	1.10	1.20	1.30
c	0.70	0.80	0.90
D		3.20 BSC	
D1	2.55	2.60	2.65
e		2.54 BSC	
f		0.40 TYP	
E		5.00 BSC	
E1	4.35	4.40	4.45
H	0.40	0.50	0.60
L	0.90	1.00	1.10
L1	0.05	0.10	0.15
p	1.17	1.27	1.37
aaa		0.15	
bbb		0.15	
ccc		0.10	
ddd		0.10	
eee		0.05	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

10. PCB Land Pattern: 3.2 x 5 mm, 4-pin

Figure 9 illustrates the 3.2 x 5 mm PCB land pattern for the Si510/511. Table 19 lists the values for the dimensions shown in the illustration.

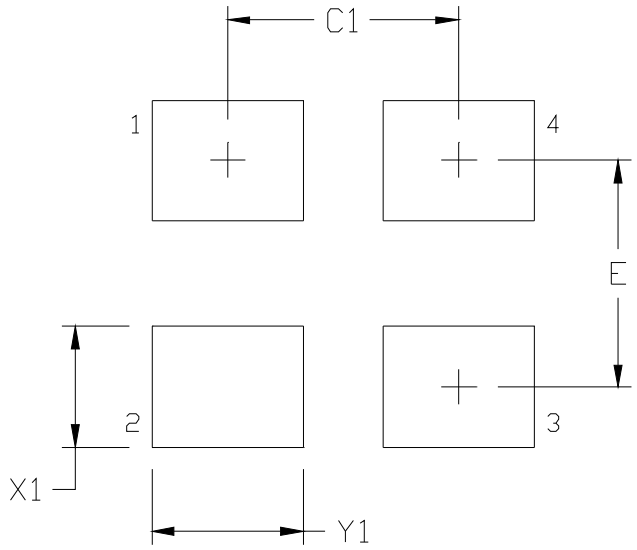


Figure 9. Si510/511 PCB Land Pattern

Table 19. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.60
E	2.54
X1	1.35
Y1	1.70

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Package Outline Diagram: 3.2 x 5 mm, 6-Pin

Figure 10 illustrates the package details for the 3.2 x 5 mm Si510/511. Table 20 lists the values for the dimensions shown in the illustration.

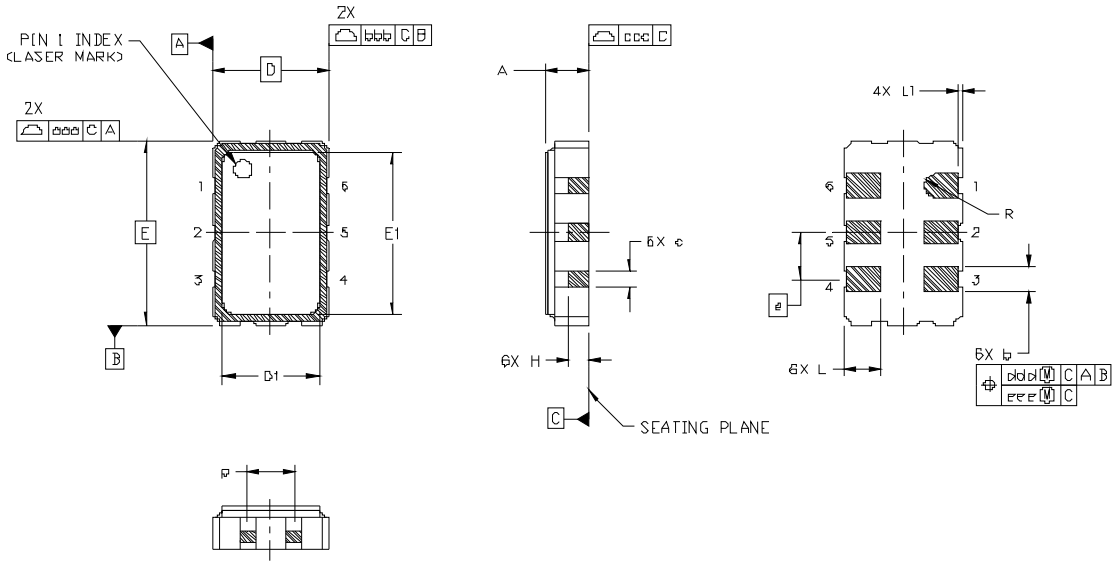


Figure 10. Si510/511 Outline Diagram

Table 20. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.06	1.17	1.28
b	0.54	0.64	0.74
c	0.35	0.45	0.55
D		3.20 BSC	
D1	2.55	2.60	2.65
e		1.27 BSC	
E		5.00 BSC	
E1	4.35	4.40	4.45
H	0.45	0.55	0.65
L	0.90	1.00	1.10
L1	0.05	0.10	0.15
p	1.17	1.27	1.37
R		0.32 REF	
aaa		0.15	
bbb		0.15	
ccc		0.10	
ddd		0.10	
eee		0.05	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

12. PCB Land Pattern: 3.2 x 5.0 mm, 6-pin

Figure 11 illustrates the 3.2 x 5.0 mm PCB land pattern for the Si510/511. Table 21 lists the values for the dimensions shown in the illustration.

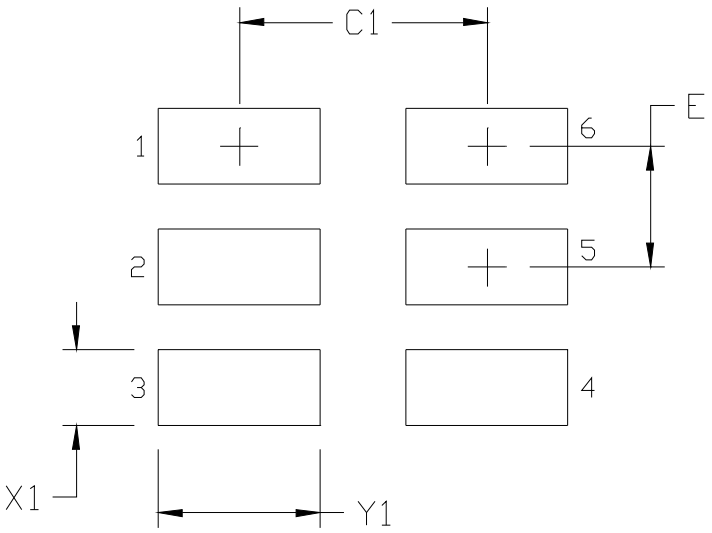


Figure 11. Si510/511 Recommended PCB Land Pattern

Table 21. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.60
E	1.27
X1	0.80
Y1	1.70

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.9 to Revision 1.0

- Updated Table 1 on page 4.
  - Updates to supply current typical and maximum values for CMOS, LVDS, LVPECL and HCSL.
  - CMOS frequency test condition corrected to 100 MHz.
  - Updates to OE VIH minimum and VIL maximum values.
- Updated Table 2 on page 5.
  - Dual CMOS nominal frequency maximum added.
  - Total stability footnotes clarified for 10 year aging at 40 °C.
  - Disable time maximum values updated.
  - Enable time parameter added.
- Updated Table 3 on page 6.
  - CMOS output rise / fall time typical and maximum values updated.
  - LVPECL/HCSL output rise / fall time maximum value updated.
  - LVPECL output swing maximum value updated.
  - LVDS output common mode typical and maximum values updated.
  - HCSL output swing maximum value updated.
  - Duty cycle minimum and maximum values tightened to 48/52%.
- Updated Table 4 on page 7.
  - Phase jitter test condition and maximum value updated.
  - Phase noise typical values updated.
  - Additive RMS jitter due to external power supply noise typical values updated.
  - Footnote 3 updated limiting the VDD to 2.5/3.3V
- Added Tables 5, 6, 7 for LVDS, HCSL, CMOS, and Dual CMOS operations.
- Moved Absolute Maximum Ratings table.
- Added note to Figure 2 clarifying CMOS and Dual CMOS maximum frequency.
- Updated Figure 10 outline diagram to correct pinout.

Revision 1.0 to Revision 1.1

- Updated Table 3.
  - CMOS Output Rise/Fall Time Test Condition updated.

NOTES:

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